(TSMC10, 2N22J / 64QFP) Electrical Distribution

TSMC11(0N22J) Baseline Data

TSMC10(2N22J) T0 and Post-HTOL Shift Analysis from Baseline

				Time0 (Pre-HTOL)			Post-HTOL			Baseline T0 Data			Baseline Post-HTOL Data			T0 Mean Shift toward LSL	T0 Mean Shift toward USL	Post Mean Shift toward LSL	Post Mean Shift toward USL
				Temp	105	C	Temp	105	C	Temp	105	C	Temp	105	C	Shift within +/-1 sigma or less than +/-15% to spec	Shift within +/-1 sigma or less than +/-15% to spec	Shift within +/-1 sigma or less than +/-15% to spec	Shift within +/-1 sigma or less than +/-15% to spec
Parameter Name, as in Datasheet	Units	Lower Spec Limit	Upper Spec Limit	Avg	Std	Cpk	Avg	Std	Cpk	Avg	Std	Cpk	Avg	Std	Cpk				
Leakage (to VSS)	nA	-1000.000	1000.000	-29.605	3.154	102.56	-31.042	3.155	102.37	-29.846	3.158	102.41	-31.041	3.119	103.54	PASS	PASS	PASS	PASS
Leakage (to VDD)	nA	-1000.000	1000.000	47.037	6.570	48.35	46.039	6.719	47.33	47.438	6.574	48.30	46.622	6.987	45.49	PASS	PASS	PASS	PASS
ICS trimmed	MHz	1.964	2.036	2.002	0.003	3.40	2.001	0.003	3.58	2.002	0.003	3.44	2.001	0.003	3.46	PASS	PASS	PASS	PASS
Bandgap trimmed	V	1.140	1.180	1.156	0.001	9.84	1.159	0.001	9.56	1.156	0.001	5.40	1.156	0.001	4.01	PASS	PASS	PASS	PASS
VOL high drive 5V	V	NA	0.800	0.435	0.012	10.46	0.439	0.014	8.47	0.433	0.005	25.09	0.447	0.006	19.10	NA	PASS	NA	PASS
VOH high drive 5V	V	4.200	5.000	4.503	0.017	6.08	4.510	0.013	7.75	4.521	0.010	11.10	4.538	0.020	5.78	PASS	PASS	PASS	PASS
VOL low drive 5V	V	NA	0.800	0.384	0.008	16.90	0.382	0.018	7.86	0.381	0.005	28.96	0.389	0.006	21.88	NA	PASS	NA	PASS
VOH low drive 5V	V	4.200	5.000	4.654	0.008	13.96	4.634	0.015	8.16	4.629	0.009	13.18	4.606	0.015	8.93	PASS	PASS	PASS	PASS
Run IDD all clock on 5V	mA	NA	14.800	6.744	0.040	66.66	6.754	0.056	47.65	6.862	0.086	30.66	6.923	0.100	26.17	NA	PASS	NA	PASS
Run IDD all clock off 5V	mA	NA	12.300	5.872	0.028	76.06	5.869	0.031	68.50	5.962	0.074	28.69	5.999	0.089	23.67	NA	PASS	NA	PASS
Wait IDD all clock on 5V	mA	NA	5.500	4.978	0.036	4.82	4.976	0.034	5.19	4.855	0.055	3.92	4.914	0.073	2.68	NA	PASS	NA	PASS
Stop IDD all clock off 5V	uA	NA	85.000	56.898	2.068	4.53	56.899	2.056	4.56	57.714	2.745	3.31	58.776	2.994	2.92	NA	PASS	NA	PASS
Run IDD all clock on 3V	mA	NA	11.800	6.709	0.045	37.65	6.731	0.054	31.26	6.826	0.085	19.52	6.888	0.097	16.86	NA	PASS	NA	PASS
Run IDD all clock off 3V	mA	NA	9.200	5.846	0.034	32.49	5.842	0.033	33.90	5.934	0.075	14.48	5.959	0.091	11.91	NA	PASS	NA	PASS
Wait IDD all clock on 3V	mA	NA	5.400	4.945	0.035	4.31	4.976	0.049	2.86	4.926	0.058	2.73	4.913	0.070	2.31	NA	PASS	NA	PASS
Stop IDD all clock off 3V	uA	NA	80.000	53.715	1.069	8.20	54.150	1.064	8.10	52.660	1.093	8.34	53.602	1.080	8.15	NA	PASS	NA	PASS

				Time0 (Pre-HTOL)			Post-HTOL			Baseline T0 Data			Baseline Post-HTOL Data			T0 Mean Shift toward LSL	T0 Mean Shift toward USL	Post Mean Shift toward LSL	Post Mean Shift toward USL
				Temp	25	C	Temp	25	C	Temp	25	C	Temp	25	C	Shift within +/-1 sigma or less than +/-15% to spec	Shift within +/-1 sigma or less than +/-15% to spec	Shift within +/-1 sigma or less than +/-15% to spec	Shift within +/-1 sigma or less than +/-15% to spec
Parameter Name, as in Datasheet	Units	Lower Spec Limit	Upper Spec Limit	Avg	Std	Cpk	Avg	Std	Cpk	Avg	Std	Cpk	Avg	Std	Cpk				
Leakage (to VSS)	nA	-1000.000	1000.000	-0.046	0.250	1333.32	-0.048	0.253	1319.32	-0.049	0.229	1452.72	-0.056	0.232	1436.64	PASS	PASS	PASS	PASS
Leakage (to VDD)	nA	-1000.000	1000.000	0.857	0.330	1008.68	0.852	0.327	1017.23	0.877	0.336	991.63	0.830	0.324	1027.37	PASS	PASS	PASS	PASS
ICS trimmed	MHz	1.964	2.036	2.000	0.005	2.22	2.000	0.005	2.34	1.999	0.005	2.57	1.999	0.005	2.54	PASS	PASS	PASS	PASS
Bandgap trimmed	V	1.140	1.180	1.162	0.001	5.61	1.161	0.001	6.16	1.161	0.001	4.78	1.160	0.001	6.53	PASS	PASS	PASS	PASS
VOL high drive 5V	V	NA	0.800	0.314	0.012	13.16	0.324	0.006	25.74	0.314	0.004	44.67	0.330	0.004	42.35	NA	PASS	NA	PASS
VOH high drive 5V	V	4.200	5.000	4.640	0.015	8.07	4.631	0.005	24.88	4.648	0.005	23.45	4.633	0.008	15.14	PASS	PASS	PASS	PASS
VOL low drive 5V	V	NA	0.800	0.264	0.004	49.43	0.269	0.004	48.17	0.269	0.003	58.72	0.274	0.005	34.01	NA	PASS	NA	PASS
VOH low drive 5V	V	4.200	5.000	4.690	0.004	26.04	4.686	0.004	29.82	4.698	0.002	52.19	4.695	0.003	30.89	PASS	PASS	PASS	PASS
Run IDD all clock on 5V	mA	NA	9.000	6.686	0.051	15.22	6.669	0.038	20.49	6.777	0.066	11.25	6.730	0.088	8.57	NA	PASS	NA	PASS
Run IDD all clock off 5V	mA	NA	8.000	5.834	0.033	21.96	5.821	0.034	21.24	5.925	0.056	12.43	5.886	0.084	8.37	NA	PASS	NA	PASS
Wait IDD all clock on 5V	mA	NA	5.500	4.743	0.020	12.72	4.725	0.028	9.12	4.803	0.036	6.44	4.769	0.066	3.72	NA	PASS	NA	PASS
Stop IDD all clock off 5V	uA	NA	75.000	1.499	0.054	453.71	1.411	0.061	403.91	1.553	0.041	595.52	1.496	0.065	375.61	NA	PASS	NA	PASS
Run IDD all clock on 3V	mA	NA	8.800	6.649	0.046	15.59	6.636	0.039	18.56	6.745	0.066	10.46	6.694	0.093	7.59	NA	PASS	NA	PASS
Run IDD all clock off 3V	mA	NA	7.800	5.806	0.028	23.33	5.792	0.022	30.10	5.899	0.064	9.93	5.860	0.083	7.81	NA	PASS	NA	PASS
Wait IDD all clock on 3V	mA	NA	5.400	4.721	0.030	7.56	4.697	0.031	7.59	4.765	0.046	4.60	4.741	0.056	3.90	NA	PASS	NA	PASS
Stop IDD all clock off 3V	uA	NA	60.000	1.343	0.063	310.35	1.260	0.055	354.59	1.317	0.045	434.90	1.242	0.039	504.51	NA	PASS	NA	PASS

				Time0 (Pre-HTOL)			Post-HTOL			Baseline T0 Data			Baseline Post-HTOL Data			T0 Mean Shift toward LSL	T0 Mean Shift toward USL	Post Mean Shift toward LSL	Post Mean Shift toward USL
				Temp	-40	C	Temp	-40	C	Temp	-40	C	Temp	-40	C	Shift within +/-1 sigma or less than +/-15% to spec	Shift within +/-1 sigma or less than +/-15% to spec	Shift within +/-1 sigma or less than +/-15% to spec	Shift within +/-1 sigma or less than +/-15% to spec
Parameter Name, as in Datasheet	Units	Lower Spec Limit	Upper Spec Limit	Avg	Std	Cpk	Avg	Std	Cpk	Avg	Std	Cpk	Avg	Std	Cpk				
Leakage (to VSS)	nA	-1000.000	1000.000	0.192	0.565	589.44	0.195	0.566	589.25	0.191	0.546	610.20	0.198	0.540	617.09	PASS	PASS	PASS	PASS
Leakage (to VDD)	nA	-1000.000	1000.000	0.564	0.492	676.89	0.671	0.492	677.73	0.583	0.484	687.95	0.571	0.478	696.89	PASS	PASS	PASS	PASS
ICS trimmed	MHz	1.964	2.036	1.980	0.002	2.15	1.980	0.002	2.19	1.980	0.002	2.76	1.981	0.002	2.61	PASS	PASS	PASS	PASS
Bandgap trimmed	V	1.140	1.180	1.161	0.001	7.38	1.160	0.001	7.60	1.160	0.003	2.29	1.159	0.002	2.56	PASS	PASS	PASS	PASS
VOL high drive 5V	V	NA	0.800	0.298	0.008	20.09	0.274	0.006	29.61	0.277	0.007	26.54	0.270	0.013	13.79	NA	PASS	NA	PASS
VOH high drive 5V	V	4.200	5.000	4.653	0.009	12.69	4.678	0.008	13.39	4.685	0.013	7.82	4.689	0.016	6.32	PASS	PASS	PASS	PASS
VOL low drive 5V	V	NA	0.800	0.225	0.005	39.55	0.225	0.005	37.57	0.220	0.004	46.00	0.221	0.005	36.22	NA	PASS	NA	PASS
VOH low drive 5V	V	4.200	5.000	4.702	0.007	13.71	4.727	0.005	20.19	4.731	0.012	7.18	4.745	0.011	8.02	PASS	PASS	PASS	PASS
Run IDD all clock on 5V	mA	NA	9.000	6.662	0.045	17.14	6.594	0.039	20.63	6.696	0.078	9.85	6.644	0.093	8.46	NA	PASS	NA	PASS
Run IDD all clock off 5V	mA	NA	8.000	5.818	0.026	28.12	5.781	0.021	35.58	5.862	0.071	10.00	5.813	0.085	8.60	NA	PASS	NA	PASS
Wait IDD all clock on 5V	mA	NA	5.500	4.728	0.032	8.11	4.677	0.037	7.40	4.745	0.072	3.49	4.713	0.073	3.60	NA	PASS	NA	PASS
Stop IDD all clock off 5V	uA	NA	75.000	1.342	0.129	190.37	1.368	0.126	194.75	1.346	0.113	217.53	1.223	0.082	301.27	NA	PASS	NA	PASS
Run IDD all clock on 3V	mA	NA	8.800	6.634	0.037	19.65	6.570	0.022	33.19	6.663	0.093	7.68	6.605	0.103	7.09	NA	PASS	NA	PASS
Run IDD all clock off 3V	mA	NA	7.800	5.794	0.037	17.84	5.734	0.030	23.32	5.828	0.076	8.70	5.743	0.197	3.48	NA	PASS	NA	PASS
Wait IDD all clock on 3V	mA	NA	5.400	4.707	0.032	7.14	4.650	0.044	5.64	4.728	0.059	3.78	4.680	0.075	3.19	NA	PASS	NA	PASS
Stop IDD all clock off 3V	uA	NA	60.000	1.013	0.069	283.21	1.012	0.041	481.56	1.016	0.037	528.18	0.947	0.056	353.36	NA	PASS	NA	PASS