AEC-Q100G Qualification Results

Objective: **SPC5646 ATMC Cu Wire Qualification In ASE-CL**								
Freescale PN: SPC5646 Part Name: Bolero3M			Customer Name(s): Varies PN(s): Varies				Plan or Results: Result Revision # & Date: See below revision history	
Technology / Tech Code: CMOS90FG / H009FXX6 Package / Code: LQFP 208 28*28*1.4P0.5 / 8268			Design Engr: Not Applicable				QUARTZ Tracking #: 225769	
Fab / Assembly / FSL-ATMC-FAB / ASECL / FSL-KLM-FM Final Test Sites:			Product Engr: Autar Singh Parvinder - B07153					(Signature/Date shown below may be electronic)
Maskset#: N32E Rev#: 0			GAO(Global Assembly Operation) Engr: Jasmine Lim-B18239				GAO Approval (for DIM/BOM results) Signature & Date: Jasmine Lim-B18239 25-June-2014	
Die Size (in mm) 6.699 x 6.538 mm W x L			NPI PRQE: Chew Kim Seong-B36347				NPI PRQE Approval Signature & Date: Chew Kim Seong-B36347 25-June-2014	
Part Operating Temp. Grade:	Grade 1	- 40°C to + 125°C	Trace/DateCode:	LOT A 8EXG402APT 00	LOT B NA	LOT C NA	CAB Approval 13100535M Signature & Date: 2-Oct-2014	
							Customer Approval NA Signature & Date:	

TESTS HIGHLIGHTED IN YELLOW WILL BE PERFORMED FOR THIS STUDY

This testing is performed by Freescale Reliability Lab (KLM) unless otherwise noted in the Comments.

GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
PC	JESD22-A113 J-STD-020	**Preconditioning (PC) :** PC required for SMDs only. MSL 3 @ 260°C, +5/-0°C	TEST @ RH	All surface mount devices prior to HAST, UHST, TC and as required per test conditions.			Lot A: 0/231	**Generic Data** Rainbow, (N29D), 208LQFP, ASECL-FM, Q223567: Lot A: 0/231 Lot B: 0/231
HAST	JESD22-A101 A110	**Highly Accelerated Stress Test (HAST):** PC before HAST (for SMDs only): Required HAST = 110°C/85%RH for 264 hrs. Bias = Max Vdd *Timed RO of 48hrs. MAX*	TEST @ RH	77	1	77	Lot A: 0/77	**Generic Data** Rainbow, (N29D), 208LQFP, ASECL-FM, Q223567: Lot A: 0/77 Lot B: 0/77
UHST	JESD22-A102 A118	**Unbiased HAST (UHST):** PC before UHST (for SMDs only): Required UHST = 110°C/85%RH for 264 hrs. *Timed RO of 2-48hrs. MAX*	TEST @ R	77	1	77	Lot A: 0/77	**Generic Data** Rainbow, (N29D), 208LQFP, ASECL-FM, Q223567: Lot A: 0/77 Lot B: 0/77
TC	JESD22-A104 AEC Q100-Appendix 3	**Temperature Cycle (TC):** PC before TC (for SMDs only): Required TC = -65°C to 150°C for 500 cycles. For AEC only: WBP after TC on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.	TEST @ H For AEC: WBP =/> 3 grams	77	1	77	Lot A: 0/77 WBP: 0/5; minimum > 3.0 grams	**Generic Data** Rainbow, (N29D), 208LQFP, ASECL-FM, Q223567: Lot A: 0/77 Lot B: 0/77
HTSL	JESD22-A103	**High Temperature Storage Life (HTSL):** 150°C for 1008 hrs. *Timed RO = 96hrs. MAX*	TEST @ RH	77	1	77	Lot A: 0/77	**Generic Data** Rainbow, (N29D), 208LQFP, ASECL-FM, Q223567: Lot A: 0/77

TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
HTOL	JESD22-A108	**High Temperature Operating Life (HTOL):** AEC Ta = 125°C for 1008 hrs Devices incorporating NVM shall receive 1X 'NVM endurance preconditioning'(W/E cycling). Test R, H, C after W/E cycling. *Timed RO of 96hrs. MAX*	TEST @ RHC	77	0	0	Not required	
ELFR	AEC Q100-008	**Early Life Failure Rate (ELFR):** AEC Ta = 125°C for 48 hrs *Timed RO of 48 hrs MAX*	TEST @ RH	800	0	0	Pass	**Generic Data** Rainbow, (N29D_ATMC), 208LQFP, ASECL-FM, Q223567: Lot A: 0/800
EDR	AEC Q100-005	**NVM Endurance, Data Retention, and Operational Life (EDR):** 150°C for 1008 hrs Devices incorporating NVM shall receive 'NVM endurance preconditioning'(W/E cycling). Test R, H, C after W/E cycling. *Timed RO of 96hrs. MAX*	TEST @ RHC	77	0	0	Not required	

TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
WBS	AEC Q100-001	**Wire Bond shear (WBS)**	Cpk = or > 1.67	30 bonds from minimum 5 units	1	5	Lot A: Cpk>1.67	
WBP	MilStd883-2011	**Wire Bond Pull (WBP):** Cond. C or D	Cpk = or > 1.67	30 bonds from minimum 5 units	1	5	Lot A: Cpk>1.67	
SD	JESD22-B102	**Solderability (SD):** 8hr.(1 hr. for Au-plated leads) Steam age prior to test. If production burn-in is done, samples must also undergo burn-in prior to SD.	>95% lead coverage of critical areas	15	1	15	Lot B: Pass	**Generic Data** Rainbow, (N29D), 208LQFP, ASECL-FM; Lot A: Pass Lot B: Pass
PD	JESD22-B100	**Physical Dimensions(PD):** PD per FSL 98A drawing	Cpk = or > 1.67	10	1	10	Lot B: Cpk>1.67	**Generic Data** Rainbow, (N29D), 208LQFP, ASECL-FM; Lot A: Cpk>1.67 Lot B: Cpk>1.67
DIM & BOM		**Dimensional (DIM):** GAO to verify PD results against valid 98A drawing. **BOM Verification (BOM):** GAO to verify qual lot ERF BOM is accurate.					DIM: Passed BOM: Approved	
SBS	AEC-Q100-010	**Solder Ball Shear (SBS):** Performed on all solder ball mounted packages e.g. PBGA, Chip Scale, Micro Lead Frame (but NOT Flip Chip). Two reflow cycles at MSL reflow temperature before shear.	Cpk = or >1.67	10 (5 balls from a min. of 10 devices)	0	0	Not required	For solder ball mounted packages only; NOT for Flip Chips.
LI	JESD22-B105	**Lead Integrity (LI):** Not required for surface mount devices; Only required for through-hole devices.	No lead breakage or cracks	5 (10 leads from each of 5 parts)	0	0	Not required	

TEST GROUP D - DIE FABRICATION RELIABILITY TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments
EM		**Electro Migration (EM)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
TDDB		**Time Dependent Dielectric Breakdown (TDDB)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
HCI		**Hot Carrier Injection (HCI)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
SM		**Stress Migration (SM)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
NBTI		**Negative Bias Temperature Instability (NBTI)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.

TEST GROUP E - ELECTRICAL VERIFICATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
TEST	Freescale 48A	**Pre- and Post Functional / Parametrics (TEST):** For AEC, test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device specification in temperature and limit value.	0 Fails	All	All	All	See Results Summary	This action refers to Final Testing of all qualification units.
HBM	AEC-Q100-002 / JESD22-A114E Jan 2007	**ElectroStatic Discharge/ Human Body Model Classification (HBM):** Test @ 500/1000/1500/2000 Volts For AEC, see AEC-Q100-002 for classification levels.	TEST @ RH 2KV min.	3 units per Voltage level	1	12	Lot A 500V: 0/3 1000V: 0/3 1500V: 0/3 2000V: 0/3	
MM	AEC-Q100-003 or JESD22	**ElectroStatic Discharge/ Machine Model Classification m(MM):** Test @ 50/100/200 Volts For AEC, see AEC-Q100-003 for classification levels.	TEST @ RH 200V min.	3 units per Voltage level	0	0	Not required	
CDM	AEC-Q100-011	**ElectroStatic Discharge/ Charged Device Model Classification (CDM):** Test @ 250/500/750 Volts For AEC, see AEC-Q100-011 for classification levels. ***Timed RO of 96hrs MAX.***	TEST @ RH All pins =/> 500V For AEC, Corner pins =/> 750V;	3 units per Voltage level	1	9	Lot A 250V: 0/3 500V: 0/3 750V: 0/3 (Corner pins)	
LU	JESD78 plus AEC-Q100-004 for AEC	**Latch-up (LU):** Test per JEDEC JESD78 with the AEC-Q100-004 requirements for AEC. Ta= Maximum operating temperature Vsupply = Maximum operating voltage	TEST @ RH	6	0	0	Not required	
ED	AEC-Q100-009, Freescale 48A spec	**Electrical Distribution (ED)**	TEST @ HC For AEC, Cpk target > 1.67	30	1	30	Pass; Cpk > 1.67	T0 comparison between Cu and Au wires
FG	For AEC, AEC-Q100-007	**Fault Grading (FG)**	FG shall be = or > 90% for qual units				FG%= No change	
CHAR	For AEC, AEC-Q003	**Characterization (CHAR):** Ony performed on new technologies and part families per AEC Q003.					Not required	
GL (for information only)	For AEC, AEC-Q100-006	**Electro-Thermally Induced Gate Leakage (GL):** 155°C, 2.0 min, +400/-400 V Per AEC Q100 Rev G, this test is performed for information only. *Timed RO of 96 hrs MAX. For all failures, perform unbiased bake (4hrs/125°C, or 2hrs/150°C) and retest; recovered units are GL failures.*	TEST @ R	6	0	0	Not required	Freescale does not plan Gate Leakage testing in alignment with the expected revision to AEC Q100 that will eliminate this "for information only" stress.
EMC	SAE J1752/3 - Radiated Emissions	**Electromagnetic Compatibility (EMC)** (see AEC Q100 Appendix 5 for test applicability; done on case-by-case basis per customer/Freescale agreement)	<40dBuV 150kHz - 1GHz	1	0	0	Not required	

Product Information

Quartz#	Fab/Mask Set/Tech	Product-Qual Description/Part Number (s)	Die Area (mm)	Assembly Site	Package (Code)	Die Attach	Mold Compound	Wire Description
225769	FSL-ATMC-FAB / N32E / H009FXX6	Bolero3M / SPC5646	6.699 x 6.538	ASECL	LQFP 208 28*28 (8268)	EN-4900G	EME-G631SH	20um Cu

Die Generic Data List:

Quartz#	Fab/Mask Set/Tech	Product-Qual Description/Part Number (s)	Die Area (mm)	Assembly Site	Package (Code)	Die Attach	Mold Compound	Wire Description
223567	FSL-ATMC-FAB / N29D / H009FXX6	Rainbow / SPC5645	7.469 x 8.850	ASECL	LQFP 208 28*28 (8268)	EN-4900G	EME-G631SH	20um Cu

Package Generic Data List:

Quartz#	Fab/Mask Set/Tech	Product-Qual Description/Part Number (s)	Die Area (mm)	Assembly Site	Package (Code)	Die Attach	Mold Compound	Wire Description
223567	FSL-ATMC-FAB / N29D / H009FXX6	Rainbow / SPC5645	7.469 x 8.850	ASECL	LQFP 208 28*28 (8268)	EN-4900G	EME-G631SH	20um Cu

Revision	Date	Comments	Author
Rev 1	25-Jun-14	Qualification Result Update	Chew Kim Seong

AEC-Q100G Qualification Results

Objective: **SPC5645 ATMC Cu Wire Qualification In ASE-CL**								
Freescale PN: SPC5645 Part Name: Rainbow			Customer Name(s): Varies PN(s): Varies				Plan or Results: Result Revision # & Date: See below revision history	
Technology / Tech Code: CMOS90FG / H009FXX6 Package / Code: LQFP 208 28*28*1.4P0.5 / 8268			Design Engr: Not Applicable				QUARTZ Tracking #: 223567	
Fab / Assembly / Final Test Sites: FSL-ATMC-FAB / ASECL / FSL-KLM-FM			Product Engr: Poon Win Yan-B02691					(Signature/Date shown below may be electronic)
Maskset#: N29D Rev#: 1			GAO(Global Assembly Operation) Engr: Jasmine Lim-B18239				GAO Approval (for DIM/BOM results) Signature & Date: Jasmine Lim-B18239 25-June-2014	
Die Size (in mm) W x L: 7.469 x 8.850 mm			NPI PRQE: Chew Kim Seong-B36347				NPI PRQE Approval Signature & Date: Chew Kim Seong-B36347 25-June-2014	
Part Operating Temp. Grade: Grade 2	- 40°C to + 105°C		Trace/DateCode:	LOT A 8EXG403BLR 00	LOT B 8EXG403BLS00	LOT C NA	CAB Approval 13100535M Signature & Date: 2-Oct-2014	
							Customer Approval NA Signature & Date:	

TESTS HIGHLIGHTED IN YELLOW WILL BE PERFORMED FOR THIS STUDY

This testing is performed by Freescale Reliability Lab (KLM) unless otherwise noted in the Comments.

GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
PC	JESD22-A113 J-STD-020	**Preconditioning (PC) :** PC required for SMDs only. MSL 3 @ 260°C, +5/-0°C	TEST @ RH	All surface mount devices prior to HAST, UHST, TC and as required per test conditions.			Lot A: 0/231 Lot B: 0/231	**Generic Data** Bolero3M, (N32E), 208LQFP, ASECL-FM, Q225769: Lot A: 0/231
HAST	JESD22-A101 A110	**Highly Accelerated Stress Test (HAST):** PC before HAST (for SMDs only): Required HAST = 110°C/85%RH for 264 hrs. Bias = Max Vdd *Timed RO of 48hrs. MAX*	TEST @ RH	77	2	154	Lot A: 0/77 Lot B: 0/77	**Generic Data** Bolero3M, (N32E), 208LQFP, ASECL-FM, Q225769: Lot A: 0/77
UHST	JESD22-A102 A118	**Unbiased HAST (UHST):** PC before UHST (for SMDs only): Required UHST = 110°C/85%RH for 264 hrs. *Timed RO of 2-48hrs. MAX*	TEST @ R	77	2	154	Lot A: 0/77 Lot B: 0/77	**Generic Data** Bolero3M, (N32E), 208LQFP, ASECL-FM, Q225769: Lot A: 0/77
TC	JESD22-A104 AEC Q100-Appendix 3	**Temperature Cycle (TC):** PC before TC (for SMDs only): Required TC = -65°C to 150°C for 500 cycles. For AEC only: WBP after TC on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.	TEST @ H For AEC: WBP =/> 3 grams	77	2	154	Lot A: 0/77 WBP: 0/5; minimum > 3.0grams Lot B: 0/77 WBP: 0/5; minimum > 3.0grams	**Generic Data** Bolero3M, (N32E), 208LQFP, ASECL-FM, Q225769: Lot A: 0/77
HTSL	JESD22-A103	**High Temperature Storage Life (HTSL):** 150°C for 1008 hrs. *Timed RO = 96hrs. MAX*	TEST @ RH	77	1	77	Lot B: 0/77	**Generic Data** Bolero3M, (N32E), 208LQFP, ASECL-FM, Q225769: Lot A: 0/77

TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
HTOL	JESD22-A108	**High Temperature Operating Life (HTOL):** AEC Ta = 125°C for 1008 hrs Devices incorporating NVM shall receive 1X 'NVM endurance preconditioning'(W/E cycling). Test R, H, C after W/E cycling. *Timed RO of 96hrs. MAX*	TEST @ RHC	77	0	0	Not required	
ELFR	AEC Q100-008	**Early Life Failure Rate (ELFR):** AEC Ta = 125°C for 48 hrs Bias = 1.6V *Timed RO of 48 hrs MAX*	TEST @ RH	800	1	800	Lot A: 0/800	
EDR	AEC Q100-005	**NVM Endurance, Data Retention, and Operational Life (EDR):** 150°C for 1008 hrs Devices incorporating NVM shall receive 'NVM endurance preconditioning'(W/E cycling). Test R, H, C after W/E cycling. *Timed RO of 96hrs. MAX*	TEST @ RHC	77	0	0	Not required	

TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
WBS	AEC Q100-001	**Wire Bond shear (WBS)**	Cpk = or > 1.67	30 bonds from minimum 5 units	2	10	Lot A: Cpk>1.67 Lot B: Cpk>1.67	
WBP	MilStd883-2011	**Wire Bond Pull (WBP):** Cond. C or D	Cpk = or > 1.67	30 bonds from minimum 5 units	2	10	Lot A: Cpk>1.67 Lot B: Cpk>1.67	
SD	JESD22-B102	**Solderability (SD):** 8hr.(1 hr. for Au-plated leads) Steam age prior to test. If production burn-in is done, samples must also undergo burn-in prior to SD.	>95% lead coverage of critical areas	15	2	30	Lot A: Pass Lot B: Pass	**Generic Data** Bolero3M, (N32E), 208LQFP, ASECL-FM; Lot A: Pass
PD	JESD22-B100	**Physical Dimensions(PD):** PD per FSL 98A drawing	Cpk = or > 1.67	10	2	20	Lot A: Cpk>1.67 Lot B: Cpk>1.67	**Generic Data** Bolero3M, (N32E), 208LQFP, ASECL-FM; Lot A: Cpk>1.67
DIM & BOM		**Dimensional (DIM):** GAO to verify PD results against valid 98A drawing. **BOM Verification (BOM):** GAO to verify qual lot ERF BOM is accurate.					DIM: Pass BOM: Approved	

SBS	AEC-Q100-010	**Solder Ball Shear (SBS):** Performed on all solder ball mounted packages e.g. PBGA, Chip Scale, Micro Lead Frame (but NOT Flip Chip). Two reflow cycles at MSL reflow temperature before shear.	Cpk = or >1.67	10 (5 balls from a min. of 10 devices)	0	0	Not required	For solder ball mounted packages only; NOT for Flip Chips.
LI	JESD22-B105	**Lead Integrity (LI):** Not required for surface mount devices; Only required for through-hole devices.	No lead breakage or cracks	5 (10 leads from each of 5 parts)	0	0	Not required	

TEST GROUP D - DIE FABRICATION RELIABILITY TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments
EM		**Electro Migration (EM)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
TDDB		**Time Dependent Dielectric Breakdown (TDDB)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
HCI		**Hot Carrier Injection (HCI)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
SM		**Stress Migration (SM)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
NBTI		**Negative Bias Temperature Instability (NBTI)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.

TEST GROUP E - ELECTRICAL VERIFICATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
TEST	Freescale 48A	**Pre- and Post Functional / Parametrics (TEST):** For AEC, test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device specification in temperature and limit value.	0 Fails	All	All	All	See Results Summary	This action refers to Final Testing of all qualification units.
HBM	AEC-Q100-002 / JESD22-A114E Jan 2007	**ElectroStatic Discharge/ Human Body Model Classification (HBM):** Test @ 500/1000/1500/2000 Volts For AEC, see AEC-Q100-002 for classification levels.	TEST @ RH 2KV min.	3 units per Voltage level	0	0	Not required	
MM	AEC-Q100-003 or JESD22	**ElectroStatic Discharge/ Machine Model Classification m(MM):** Test @ 50/100/200 Volts For AEC, see AEC-Q100-003 for classification levels.	TEST @ RH 200V min.	3 units per Voltage level	0	0	Not required	
CDM	AEC-Q100-011	**ElectroStatic Discharge/ Charged Device Model Classification (CDM):** Test @ 250/500/750 Volts For AEC, see AEC-Q100-011 for classification levels. ***Timed RO of 96hrs MAX.***	TEST @ RH All pins =/> 500V For AEC, Corner pins =/> 750V;	3 units per Voltage level	0	0	Not required	
LU	JESD78 plus AEC-Q100-004 for AEC	**Latch-up (LU):** Test per JEDEC JESD78 with the AEC-Q100-004 requirements for AEC. Ta= Maximum operating temperature Vsupply = Maximum operating voltage	TEST @ RH	6	0	0	Not required	
ED	AEC-Q100-009, Freescale 48A spec	**Electrical Distribution (ED)**	TEST @ HC For AEC, Cpk target > 1.67	30	1	30	Pass; Cpk > 1.67	T0 comparison between Cu and Au wires
FG	For AEC, AEC-Q100-007	**Fault Grading (FG)**	FG shall be = or > 90% for qual units				FG%= No change	
CHAR	For AEC, AEC-Q003	**Characterization (CHAR):** Ony performed on new technologies and part families per AEC Q003.					Not required	
GL (for information only)	For AEC, AEC-Q100-006	**Electro-Thermally Induced Gate Leakage (GL):** 155°C, 2.0 min, +400/-400 V Per AEC Q100 Rev G, this test is performed for information only. *Timed RO of 96 hrs MAX. For all failures, perform unbiased bake (4hrs/125°C, or 2hrs/150°C) and retest; recovered units are GL failures.*	TEST @ R	6	0	0	Not required	Freescale does not plan Gate Leakage testing in alignment with the expected revision to AEC Q100 that will eliminate this "for information only" stress.
EMC	SAE J1752/3 - Radiated Emissions	**Electromagnetic Compatibility (EMC)** (see AEC Q100 Appendix 5 for test applicability; done on case-by-case basis per customer/Freescale agreement)	<40dBuV 150kHz - 1GHz	1	0	0	Not required	

Product Information

Quartz#	Fab/Mask Set/Tech	Product-Qual Description/Part Number (s)	Die Area (mm)	Assembly Site	Package (Code)	Die Attach	Mold Compound	Wire Description
223567	FSL-ATMC-FAB / N29D / H009FXX6	Rainbow / SPC5645	7.469 x 8.850	ASECL	LQFP 208 28*28 (8268)	EN-4900G	EME-G631SH	20um Cu

Package Generic Data List:

Quartz#	Fab/Mask Set/Tech	Product-Qual Description/Part Number (s)	Die Area (mm)	Assembly Site	Package (Code)	Die Attach	Mold Compound	Wire Description
225769	FSL-ATMC-FAB / N32E / H009FXX6	Bolero3M / SPC5646	6.699 x 6.538	ASECL	LQFP 208 28*28 (8268)	EN-4900G	EME-G631SH	20um Cu

Revision	Date	Comments	Author
Rev 1	25-Jun-14	Qualification Result Update	Chew Kim Seong

AEC-Q100G Qualification Results

Objective: **SPC5644 176LQFP LeadFrame & Cu Wire Qualification In ASE-CL**			
Freescale PN: SPC5644 Part Name: Andorra 4M	Customer Name(s): Varies PN(s): Varies		Plan or Results: Result Revision # & Date: See below revision history
Technology / Tech Code: CMOS90FG / H009FHX6 Package / Code: LQFP 176 24*24*1.4P0.5 / 8271	Design Engr: Not Applicable		QUARTZ Tracking #: 225843
Fab / Assembly / FSL-ATMC-FAB / ASECL / FSL-KLM-FM Final Test Sites:	Product Engr: Jeremy Tee - B07476		(Signature/Date shown below may be electronic)
Maskset#: M14X Rev#: 0	GAO(Global Assembly Operation) Engr: Jasmine Lim - B18239		GAO Approval (for DIM/BOM results) Signature & Date: Jasmine Lim-B18239 25-June-2014
Die Size (in mm) 7.238 x 8.375 W x L	NPI PRQE: Chew Kim Seong - B36347		NPI PRQE Approval Signature & Date: Chew Kim Seong-B36347 25-June-2014
Part Operating Temp. Grade: Grade 1 - 40°C to + 125°C	Trace/DateCode: LOT A XG408A4R00 / LOT B NA / LOT C NA		CAB Approval 13100535M Signature & Date: 2-Oct-2014
			Customer Approval NA Signature & Date:

TESTS HIGHLIGHTED IN YELLOW WILL BE PERFORMED FOR THIS STUDY

This testing is performed by Freescale Reliability Lab (KLM) unless otherwise noted in the Comments.

GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
PC	JESD22-A113 J-STD-020	**Preconditioning (PC) :** PC required for SMDs only. MSL 3 @ 260°C, +5/-0°C	TEST @ RH	All surface mount devices prior to HAST, UHST, TC and as required per test conditions.			Lot A: 0/77	**Generic Data** Spectrum_SPC5606, (M25V), LQFP 176, ASECL, Q223504; Lot A: 0/231 Lot B: 0/231 Lot C: 0/231 **Spectrum uses the same leadframe as Andorra4M* Bolero3M_SPC5646, (N32E), 208LQFP, ASECL-FM, Q225769: Lot A: 0/231 Rainbow_SPC5645, (N29D), 208LQFP, ASECL-FM, Q223567: Lot A: 0/2321 Lot B: 0/231
HAST	JESD22-A101 A110	**Highly Accelerated Stress Test (HAST):** PC before HAST (for SMDs only): Required HAST = 110°C/85%RH for 264 hrs. Bias = Max Vdd *Timed RO of 48hrs. MAX*	TEST @ RH	77	0	0	Pass	**Generic Data** Spectrum_SPC5606, (M25V), LQFP 176, ASECL, Q223504; Lot A: 0/77 Lot B: 0/77 Lot C: 0/77 **Spectrum uses the same leadframe as Andorra4M* Bolero3M_SPC5646, (N32E), 208LQFP, ASECL-FM, Q225769: Lot A: 0/77 Rainbow_SPC5645, (N29D), 208LQFP, ASECL-FM, Q223567: Lot A: 0/77 Lot B: 0/77
UHST	JESD22-A102 A118	**Unbiased HAST (UHST):** PC before UHST (for SMDs only): Required UHST = 110°C/85%RH for 264hrs *Timed RO of 48hrs. MAX*	TEST @ R	77	0	0	Pass	**Generic Data** Spectrum_SPC5606, (M25V), LQFP 176, ASECL, Q223504; Lot A: 0/77 Lot B: 0/77 Lot C: 0/77 **Spectrum uses the same leadframe as Andorra4M* Bolero3M_SPC5646, (N32E), 208LQFP, ASECL-FM, Q225769: Lot A: 0/77 Rainbow_SPC5645, (N29D), 208LQFP, ASECL-FM, Q223567: Lot A: 0/77 Lot B: 0/77
TC	JESD22-A104 AEC Q100-Appendix 3	**Temperature Cycle (TC):** PC before TC (for SMDs only): Required TC = -65°C to 150°C for 500 cycles. For AEC only: WBP after TC on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.	TEST @ H For AEC: WBP =/> 3 grams	77	1	77	Lot A: 0/77 WBP: 0/5; minimum > 3.0grams	**Generic Data** Spectrum_SPC5606, (M25V), LQFP 176, ASECL, Q223504; Lot A: 0/77 Lot B: 0/77 Lot C: 0/77 **Spectrum uses the same leadframe as Andorra4M* Bolero3M_SPC5646, (N32E), 208LQFP, ASECL-FM, Q225769: Lot A: 0/77 Rainbow_SPC5645, (N29D), 208LQFP, ASECL-FM, Q223567: Lot A: 0/77 Lot B: 0/77
HTSL	JESD22-A103	**High Temperature Storage Life (HTSL):** 150°C for 1008 hrs. *Timed RO = 96hrs. MAX*	TEST @ RH	77	0	0	Pass	**Generic Data** Spectrum_SPC5606, (M25V), LQFP 176, ASECL, Q223504; Lot A: 0/77 **Spectrum uses the same leadframe as Andorra4M* Bolero3M_SPC5646, (N32E), 208LQFP, ASECL-FM, Q225769: Lot A: 0/77 Rainbow_SPC5645, (N29D), 208LQFP, ASECL-FM, Q223567: Lot A: 0/77

TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
HTOL	JESD22-A108	**High Temperature Operating Life (HTOL):** AEC Ta = 125°C for 1008 hrs Devices incorporating NVM shall receive 1X 'NVM endurance preconditioning'(W/E cycling). Test R, H, C after W/E cycling. *Timed RO of 96hrs. MAX*	TEST @ RHC	77	0	0	Not required	
ELFR	AEC Q100-008	**Early Life Failure Rate (ELFR):** AEC Ta = 125°C for 48 hrs *Timed RO of 48 hrs MAX*	TEST @ RH	800	0	0	Pass	**Generic Data** Rainbow, (N29D_ATMC), 208LQFP, ASECL-FM, Q223567: Lot A: 0/800
EDR	AEC Q100-005	**NVM Endurance, Data Retention, and Operational Life (EDR):** 150°C for 1008 hrs Devices incorporating NVM shall receive 1X 'NVM endurance preconditioning'(W/E cycling). Test R, H, C after W/E cycling. *Timed RO of 96hrs. MAX*	TEST @ RHC	77	0	0	Not required	

TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
WBS	AEC Q100-001	**Wire Bond shear (WBS)**	Cpk = or > 1.67	30 bonds from minimum 5 units	1	5	Lot A: Cpk>1.67	
WBP	MilStd883-2011	**Wire Bond Pull (WBP):** Cond. C or D	Cpk = or > 1.67	30 bonds from minimum 5 units	1	5	Lot A: Cpk>1.67	
SD	JESD22-B102	**Solderability (SD):** 8hr.(1 hr. for Au-plated leads) Steam age prior to test. If production burn-in is done, samples must also undergo burn-in prior to SD.	>95% lead coverage of critical areas	15	1	15	Lot A: Pass	**Generic Data** Spectrum_SPC5606, (2M25V), LQFP 176, ASECL: Lot A: Pass Lot B: Pass Lot C: Pass
PD	JESD22-B100	**Physical Dimensions(PD):** PD per FSL 98A drawing	Cpk = or > 1.67	10	1	10	Lot A: Cpk>1.67	**Generic Data** Faraday_SVR332R, (N02G), LQFP-EP 176, ASECL: Lot A: Cpk > 1.67 Lot B: Cpk > 1.67 Lot C: Cpk > 1.67
DIM & BOM		**Dimensional (DIM):** GAO to verify PD results against valid 98A drawing. **BOM Verification (BOM):** GAO to verify qual lot ERF BOM is accurate.					DIM: Pass BOM: Approved	
SBS	AEC-Q100-010	**Solder Ball Shear (SBS):** Performed on all solder ball mounted packages e.g. PBGA, Chip Scale, Micro Lead Frame (but NOT Flip Chip). Two reflow cycles at MSL reflow temperature before shear.	Cpk = or >1.67	10 (5 balls from a min. of 10 devices)	0	0	Not required	For solder ball mounted packages only; NOT for Flip Chips.
LI	JESD22-B105	**Lead Integrity (LI):** Not required for surface mount devices; Only required for through-hole devices.	No lead breakage or cracks	5 (10 leads from each of 5 parts)	0	0	Not required	

TEST GROUP D - DIE FABRICATION RELIABILITY TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments
EM		**Electro Migration (EM)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
TDDB		**Time Dependent Dielectric Breakdown (TDDB)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
HCI		**Hot Carrier Injection (HCI)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
SM		**Stress Migration (SM)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
NBTI		**Negative Bias Temperature Instability (NBTI)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.

TEST GROUP E - ELECTRICAL VERIFICATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
TEST	Freescale 48A	**Pre- and Post Functional / Parametrics (TEST):** For AEC, test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device specification in temperature and limit value.	0 Fails	All	All	All	See Results Summary	This action refers to Final Testing of all qualification units.
CCU	Freescale 12MYS-62419B	**Control/Correlation Units (CCU):** Units shall be marked to distinguish them from the qual units and must be marked in such a way as to retain marking over the test temperature.	NA	60 30 units as primary units, 30 units as back-up units	0	0	Not required	
HBM	AEC-Q100-002 / JESD22-A114E Jan 2007	**ElectroStatic Discharge/ Human Body Model Classification (HBM):** Test @ 500/1000/1500/2000 Volts For AEC, see AEC-Q100-002 for classification levels.	TEST @ RH 2KV min.	3 units per Voltage level	0	0	Not required	
MM	AEC-Q100-003 or JESD22	**ElectroStatic Discharge/ Machine Model Classification m(MM):** Test @ 50/100/200 Volts For AEC, see AEC-Q100-003 for classification levels.	TEST @ RH 200V only	3 units per Voltage level	0	0	Not required	

CDM	AEC-Q100-011	**ElectroStatic Discharge/ Charged Device Model Classification (CDM):** Test @ 250/500/750 Volts For AEC, see AEC-Q100-011 for classification levels. ***Timed RO of 96hrs MAX.***	TEST @ RH All pins =/> 500V For AEC, Corner pins =/> 750V;	3 units per Voltage level	0	0	Not required	
LU	JESD78 plus AEC-Q100-004 for AEC	**Latch-up (LU):** Test per JEDEC JESD78 with the AEC-Q100-004 requirements for AEC. Ta= Maximum operating temperature Vsupply = Maximum operating voltage	TEST @ RH	6	0	0	Not required	
ED	AEC-Q100-009, Freescale 48A spec	**Electrical Distribution (ED)**	TEST @ RHC For AEC, Cpk target > 1.67	30	0	0	Not required	
FG	For AEC, AEC-Q100-007	**Fault Grading (FG)**	FG shall be = or > 90% for qual units				FG%= No change	
CHAR	For AEC, AEC-Q003	**Characterization (CHAR):** Ony performed on new technologies and part families per AEC Q003.					Not required	
GL (for information only)	For AEC, AEC-Q100-006	**Electro-Thermally Induced Gate Leakage (GL):** 155°C, 2.0 min, +400/-400 V Per AEC Q100 Rev G, this test is performed for information only. *Timed RO of 96 hrs MAX.* *For all failures, perform unbiased bake (4hrs/125°C, or 2hrs/150°C) and retest; recovered units are GL failures.*	TEST @ R	6	0	0	Not required	Freescale does not plan Gate Leakage testing in alignment with the expected revision to AEC Q100 that will eliminate this "for information only" stress.
EMC	SAE J1752/3 - Radiated Emissions	**Electromagnetic Compatibility (EMC)** (see AEC Q100 Appendix 5 for test applicability; done on case-by-case basis per customer/Freescale agreement)	<40dBuV 150kHz - 1GHz	1	0	0	Not required	

Product Information

Quartz#	Fab/Mask Set/Tech	Product-Qual Description/Part Number (s)	Die Area (mm)	Assembly Site	Package (Code)	Die Attach	Mold Compound	Wire Description
225843	FSL-ATMC-FAB / M14X / H009FHX6	Andorra4M / SPC5644	7.238 x 8.375	ASECL	LQFP 176 24*24 (8271)	EN-4900G	EME G631SH	20um Cu

Die Generic Data List:

Quartz#	Fab/Mask Set/Tech	Product-Qual Description/Part Number (s)	Die Area (mm)	Assembly Site	Package (Code)	Die Attach	Mold Compound	Wire Description
223567	FSL-ATMC-FAB / N29D / H009FHX6	Rainbow / SPC5645	7.469 x 8.850	ASECL	LQFP 208 28*28 (8268)	EN-4900G	EME-G631SH	20um Cu

Package Generic Data List

Quartz#	Fab/Mask Set/Tech	Product-Qual Description/Part Number (s)	Die Area (mm)	Assembly Site	Package (Code)	Die Attach	Mold Compound	Wire Description
223504	FSL-ATMC-FAB / M25V / H009FXXQ	Spectrum / SPC5606	5.495 x 5.460	ASECL	LQFP 176 24*24 (8271)	EN-4900G	CEL9240HF10AK	20 um Cu
223567	FSL-ATMC-FAB / N29D / H009FXX6	Rainbow / SPC5645	7.469 x 8.850	ASECL	LQFP 208 28*28 (8268)	EN-4900G	EME-G631SH	20um Cu
225769	FSL-ATMC-FAB / N32E / H009FXX6	Bolero3M / SPC5646	6.699 x 6.538	ASECL	LQFP 208 28*28 (8268)	EN-4900G	EME-G631SH	20um Cu
NA	TSMC14 / N02G / EN40LXX7	Faraday / SVF332R	5.919 x 4.929	ASECL	LQFP-EP 176 24*24 (00C2)	EN-4900G	EME G631SH	23um Cu

Devices Qualify By Similarity

Quartz#	Fab/Mask Set/Tech	Product-Qual Description/Part Number (s)	Die Area (mm)	Assembly Site	Package (Code)	Die Attach	Mold Compound	Wire Description
NA	FSL-ATMC-FAB / N60C / H009FXX6	Andorra2M / SPC5642	6.154 x 6.915	ASECL	LQFP 176 24*24 (8271)	EN-4900G	EME-G631SH	20um Cu
NA	FSL-ATMC-FAB / N32E / H009FXX6	Bolero3M / SPC5646	6.699 x 6.538	ASECL	LQFP 176 24*24 (8271)	EN-4900G	EME-G631SH	20um Cu
NA	FSL-ATMC-FAB / M35Y / H009FHX6	Monaco1.5M / SPC5634	4.877 x 5.937	ASECL	LQFP 176 24*24 (8271)	EN-4900G	EME-G631SH	20um Cu

Revision	Date	Comments	Author
Rev 1	25-Jun-14	Qualification Result Update	Chew Kim Seong

AEC-Q100G Qualification Results

Objective: **SPC5645 ATMC Cu Wire Qualification In ASE-CL**				
Freescale PN: SPC5645 Part Name: Rainbow	Customer Name(s): Varies PN(s): Varies			Plan or Results: Result Revision # & Date: See below revision history
Technology / Tech Code: CMOS90FG / H009FHX6 Package / Code: LQFP 176 24*24*1.4P0.5 / 8271	Design Engr: Not Applicable			QUARTZ Tracking #: 223758
Fab / Assembly / FSL-ATMC-FAB / ASECL / FSL-KLM-FM Final Test Sites:	Product Engr: Poon Win Yan-B02691			(Signature/Date shown below may be electronic)
Maskset#: N29D Rev#: 1	GAO(Global Assembly Operation) Engr: Jasmine Lim - B18239			GAO Approval (for DIM/BOM results) Jasmine Lim-B18239 25-June-2014 Signature & Date:
Die Size (in mm) 7.469 x 8.850 mm W x L	NPI PRQE: Chew Kim Seong - B36347			NPI PRQE Approval Signature & Date: Chew Kim Seong-B36347 25-June-2014
Part Operating Temp. Grade: Grade 2 - 40°C to + 105°C	Trace/DateCode:	LOT A 8EXG403BLQ 00	LOT B / LOT C	CAB Approval 13100535M Signature & Date: 2-Oct-2014
				Customer Approval NA Signature & Date:

TESTS HIGHLIGHTED IN YELLOW WILL BE PERFORMED FOR THIS STUDY

This testing is performed by Freescale Reliability Lab (KLM) unless otherwise noted in the Comments.

GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
PC	JESD22-A113 J-STD-020	**Preconditioning (PC) :** PC required for SMDs only. MSL 3 @ 260°C, +5/-0°C	TEST @ RH	All surface mount devices prior to HAST, UHST, TC and as required per test conditions.			Lot A: 0/77	**Generic Data** Bolero3M_SPC5646, (N32E), 208LQFP, ASECL-FM, Q225769: Lot A: 0/231 Rainbow_SPC5645, (N29D), 208LQFP, ASECL-FM, Q223567: Lot A: 0/2321 Lot B: 0/231
HAST	JESD22-A101 A110	**Highly Accelerated Stress Test (HAST):** PC before HAST (for SMDs only): Required HAST = 110°C/85%RH for 264 hrs. Bias = Max Vdd *Timed RO of 48hrs. MAX*	TEST @ RH	77	0	0	Pass	**Generic Data** Bolero3M_SPC5646, (N32E), 208LQFP, ASECL-FM, Q225769: Lot A: 0/77 Rainbow_SPC5645, (N29D), 208LQFP, ASECL-FM, Q223567: Lot A: 0/77 Lot B: 0/77
UHST	JESD22-A102 A118	**Unbiased HAST (UHST):** PC before UHST (for SMDs only): Required UHST = 110°C/85%RH for 264 hrs. *Timed RO of 2-48hrs. MAX*	TEST @ R	77	0	0	Pass	**Generic Data** Bolero3M_SPC5646, (N32E), 208LQFP, ASECL-FM, Q225769: Lot A: 0/77 Rainbow_SPC5645, (N29D), 208LQFP, ASECL-FM, Q223567: Lot A: 0/77 Lot B: 0/77
TC	JESD22-A104 AEC Q100-Appendix 3	**Temperature Cycle (TC):** PC before TC (for SMDs only): Required TC = -65°C to 150°C for 500 cycles. For AEC only: WBP after TC on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.	TEST @ H For AEC: WBP =/> 3 grams	77	1	77	Lot A: 0/77 WBP: 0/5; minimum>3.0 grams	**Generic Data** Bolero3M_SPC5646, (N32E), 208LQFP, ASECL-FM, Q225769: Lot A: 0/77 Rainbow_SPC5645, (N29D), 208LQFP, ASECL-FM, Q223567: Lot A: 0/77 Lot B: 0/77
HTSL	JESD22-A103	**High Temperature Storage Life (HTSL):** 150°C for 1008 hrs. *Timed RO = 96hrs. MAX*	TEST @ RH	77	0	0	Pass	**Generic Data** Bolero3M_SPC5646, (N32E), 208LQFP, ASECL-FM, Q225769: Lot A: 0/77 Rainbow_SPC5645, (N29D), 208LQFP, ASECL-FM, Q223567: Lot A: 0/77

TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
HTOL	JESD22-A108	**High Temperature Operating Life (HTOL):** AEC Ta = 125°C for 1008 hrs Devices incorporating NVM shall receive 1X 'NVM endurance preconditioning'(W/E cycling). Test R, H, C after W/E cycling. *Timed RO of 96hrs. MAX*	TEST @ RHC	77	0	0	Not required	
ELFR	AEC Q100-008	**Early Life Failure Rate (ELFR):** AEC Ta = 125°C for 48 hrs *Timed RO of 48 hrs MAX*	TEST @ RH	800	0	0	Pass	**Generic Data** Rainbow, (N29D_ATMC), 208LQFP, ASECL-FM, Q223567: Lot A: 0/800
EDR	AEC Q100-005	**NVM Endurance, Data Retention, and Operational Life (EDR):** 150°C for 1008 hrs Devices incorporating NVM shall receive 'NVM endurance preconditioning'(W/E cycling). Test R, H, C after W/E cycling. *Timed RO of 96hrs. MAX*	TEST @ RHC	77	0	0	Not required	

TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS								
Stress Test	**Reference**	**Test Conditions**	**End Point Requirements**	**Minimum Sample Size**	**# of Lots**	**Total Units including spares**	**Results** Lot ID-(#Rej/SS) NA=Not Applicable	**Comments or Generic Data**
WBS	AEC Q100-001	**Wire Bond shear (WBS)**	Cpk = or > 1.67	30 bonds from minimum 5 units	1	5	Lot A: Cpk>1.67	
WBP	MilStd883-2011	**Wire Bond Pull (WBP):** Cond. C or D	Cpk = or > 1.67	30 bonds from minimum 5 units	1	5	Lot A: Cpk>1.67	
SD	JESD22-B102	**Solderability (SD):** 8hr.(1 hr. for Au-plated leads) Steam age prior to test. If production burn-in is done, samples must also undergo burn-in prior to SD.	>95% lead coverage of critical areas	15	0	0	Pass	**Generic Data** Spectrum_SPC5606, (M25V), LQFP 176, ASECL: Lot A: Pass Lot B: Pass Lot C: Pass Andorra4M_SPC5644, (M14X), LQFP 176, ASECL: Lot A: Pass
PD	JESD22-B100	**Physical Dimensions(PD):** PD per FSL 98A drawing	Cpk = or > 1.67	10	0	0	Pass	**Generic Data** Faraday_SVR332R, (N02G), LQFP-EP 176, ASECL: Lot A: Cpk > 1.67 Lot B: Cpk > 1.67 Lot C: Cpk > 1.67 Andorra4M_SPC5644, (M14X), LQFP 176, ASECL: Lot A: Cpk>1,67
DIM & BOM		**Dimensional (DIM):** GAO to verify PD results against valid 98A drawing. **BOM Verification (BOM):** GAO to verify qual lot ERF BOM is accurate.					DIM: Pass BOM: Approved	
SBS	AEC-Q100-010	**Solder Ball Shear (SBS):** Performed on all solder ball mounted packages e.g. PBGA, Chip Scale, Micro Lead Frame (but NOT Flip Chip). Two reflow cycles at MSL reflow temperature before shear.	Cpk = or >1.67	10 (5 balls from a min. of 10 devices)	0	0	Not required	For solder ball mounted packages only; NOT for Flip Chips.
LI	JESD22-B105	**Lead Integrity (LI):** Not required for surface mount devices; Only required for through-hole devices.	No lead breakage or cracks	5 (10 leads from each of 5 parts)	0	0	Not required	

TEST GROUP D - DIE FABRICATION RELIABILITY TESTS								
Stress Test	**Reference**	**Test Conditions**	**End Point Requirements**	**Minimum Sample Size**	**# of Lots**	**Total Units including spares**	**Results** Lot ID-(#Rej/SS) NA=Not Applicable	**Comments**
EM		**Electro Migration (EM)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
TDDB		**Time Dependent Dielectric Breakdown (TDDB)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
HCI		**Hot Carrier Injection (HCI)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
SM		**Stress Migration (SM)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
NBTI		**Negative Bias Temperature Instability (NBTI)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.

TEST GROUP E - ELECTRICAL VERIFICATION TESTS								
Stress Test	**Reference**	**Test Conditions**	**End Point Requirements**	**Minimum Sample Size**	**# of Lots**	**Total Units including spares**	**Results** Lot ID-(#Rej/SS) NA=Not Applicable	**Comments or Generic Data**
TEST	Freescale 48A	**Pre- and Post Functional / Parametrics (TEST):** For AEC, test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device specification in temperature and limit value.	0 Fails	All	All	All	See Results Summary	This action refers to Final Testing of all qualification units.
CCU	Freescale 12MYS-62419B	**Control/Correlation Units (CCU):** Units shall be marked to distinguish them from the qual units and must be marked in such a way as to retain marking over the test temperature.	NA	60 30 units as primary units, 30 units as back-up units	0	0	Not required	
HBM	AEC-Q100-002 / JESD22-A114E Jan 2007	**ElectroStatic Discharge/ Human Body Model Classification (HBM):** Test @ 500/1000/1500/2000 Volts For AEC, see AEC-Q100-002 for classification levels.	TEST @ RH 2KV min.	3 units per Voltage level	0	0	Not required	
MM	AEC-Q100-003 or JESD22	**ElectroStatic Discharge/ Machine Model Classification m(MM):** Test @ 50/100/200 Volts For AEC, see AEC-Q100-003 for classification levels.	TEST @ RH 200V min.	3 units per Voltage level	0	0	Not required	
CDM	AEC-Q100-011	**ElectroStatic Discharge/ Charged Device Model Classification (CDM):** Test @ 250/500/750 Volts For AEC, see AEC-Q100-011 for classification levels. ***Timed RO of 96hrs MAX.***	TEST @ RH All pins =/> 500V For AEC, Corner pins =/> 750V;	3 units per Voltage level	0	0	Not required	
LU	JESD78 plus AEC-Q100-004 for AEC	**Latch-up (LU):** Test per JEDEC JESD78 with the AEC-Q100-004 requirements for AEC. Ta= Maximum operating temperature Vsupply = Maximum operating voltage	TEST @ RH	6	0	0	Not required	
ED	AEC-Q100-009, Freescale 48A spec	**Electrical Distribution (ED)**	TEST @ HC For AEC, Cpk target > 1.67	30	0	0	Pass	**Generic Data** Rainbow_SPC5645, (N29D), 208LQFP, ASECL-FM: Cpk>1.67 T0 comparison between Cu and Au wire
FG	For AEC, AEC-Q100-007	**Fault Grading (FG)**	FG shall be = or > 90% for qual units				FG%= No change	

CHAR	For AEC, AEC-Q003	**Characterization (CHAR):** Ony performed on new technologies and part families per AEC Q003.					Not required	
GL (for information only)	For AEC, AEC-Q100-006	**Electro-Thermally Induced Gate Leakage (GL):** 155°C, 2.0 min, +400/-400 V Per AEC Q100 Rev G, this test is performed for information only. *Timed RO of 96 hrs MAX. For all failures, perform unbiased bake (4hrs/125°C, or 2hrs/150°C) and retest; recovered units are GL failures.*	TEST @ R	6	0	0	Not required	Freescale does not plan Gate Leakage testing in alignment with the expected revision to AEC Q100 that will eliminate this "for information only" stress.
EMC	SAE J1752/3 - Radiated Emissions	**Electromagnetic Compatibility (EMC)** (see AEC Q100 Appendix 5 for test applicability; done on case-by-case basis per customer/Freescale agreement)	<40dBuV 150kHz - 1GHz	1	0	0	Not required	

Product Information

Quartz#	Fab/Mask Set/Tech	Product-Qual Description/Part Number (s)	Die Area (mm)	Assembly Site	Package (Code)	Die Attach	Mold Compound	Wire Description
223758	FSL-ATMC-FAB / N29D / H009FHX6	Rainbow / SPC5645	7.469 x 8.850	ASECL	LQFP 176 24*24 (8271)	EN-4900G	EME G631SH	20um Cu

Die Generic Data List:

Quartz#	Fab/Mask Set/Tech	Product-Qual Description/Part Number (s)	Die Area (mm)	Assembly Site	Package (Code)	Die Attach	Mold Compound	Wire Description
223567	FSL-ATMC-FAB / N29D / H009FXX6	Rainbow / SPC5645	7.469 x 8.850	ASECL	LQFP 208 28*28 (8268)	EN-4900G	EME-G631SH	20um Cu

Package Generic Data List

Quartz#	Fab/Mask Set/Tech	Product-Qual Description/Part Number (s)	Die Area (mm)	Assembly Site	Package (Code)	Die Attach	Mold Compound	Wire Description
223567	FSL-ATMC-FAB / N29D / H009FXX6	Rainbow / SPC5645	7.469 x 8.850	ASECL	LQFP 208 28*28 (8268)	EN-4900G	EME-G631SH	20um Cu
225769	FSL-ATMC-FAB / N32E / H009FXX6	Bolero3M / SPC5646	6.699 x 6.538	ASECL	LQFP 208 28*28 (8268)	EN-4900G	EME-G631SH	20um Cu
223504	FSL-ATMC-FAB / M25V / H009FXXQ	Spectrum / SPC5606	5.495 x 5.460	ASECL	LQFP 176 24*24 (8271)	EN-4900G	CEL9240HF10AK	20 um Cu
225843	FSL-ATMC-FAB / M14X / H009FHX6	Andorra4M / SPC5644	7.238 x 8.375	ASECL	LQFP 176 24*24 (8271)	EN-4900G	EME G631SH	20um Cu
NA	TSMC14 / N02G / EN40LXX7	Faraday / SVF332R	5.919 x 4.929	ASECL	LQFP-EP 176 24*24 (00C2)	EN-4900G	EME G631SH	23um Cu

Revision	Date	Comments	Author
Rev 1	25-Jun-14	Qualification Result Update	Chew Kim Seong