

APPLICATION NOTE

PCI - DVB Tuner Boards and
Windows Drivers

AN00084

Abstract

This paper describes a set of PC boards and the related Windows drivers to feature the digital transmission standards of DVB for a PC system.

After sketching the system components the SW drivers are explained in detail, as well as constraints of the installation and operation.

Certain details of the HW approach are focussed to point out the possibilities with the DVB system and future expansions.

As also other parties are involved, their home page links are listed in a separate chapter.

Support tools are listed in the appendix, as well as the schematics of the board.

Please notice, that this app-note might be subject of updates.

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APPLICATION NOTE

PCI - DVB Tuner Boards and Windows Drivers

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I. INTRODUCTION

Philips Semiconductors developed a set of DVB compliant systems for the PC environment. The distinctions are the different transmission standards. A common HW platform has been established, which can feature the different transmission standards by simply exchanging the related tuner front-end. To operate the DVB systems in an appropriate manner, the advanced Microsoft Windows driver technology of BDA has been used. Microsoft introduces the BDA architecture within DirectX 8.0. The Philips Semiconductor driver set consists of a generic tuner driver and a capture driver.

For complete DVB system operation components from other vendors have been employed as described later. At the moment there are front-ends available for:

DVB-S	Sylt board
DVB-T	Tenerife board
DVB-C	Crete board

I.1 Purpose

Purpose of this document is to describe how to install the drivers and how to use the board in a DirectShow environment.

I.2 Glossary

A/V-Streaming	Means to transfer continuously audio and video data, e.g. in a PC
BIOS	Basic Input Output System
BDA	Broadcast Diver Architecture, latest driver architecture of Microsoft supporting A/V Streaming. It is on top of WDM architecture.
CA	Conditional Access, copy protection systems
CI	Common Interface, standard related to PCMCIA cards
DEBI-port	specific data port of the SAA7146A
DirectShow	Part of the Windows architecture
DiSEqC	Digital Satellite Equipment Control
DVB-C	Digital Video Broadcast – Cable, digital transmission standard
DVB-S	Digital Video Broadcast – Satellite, digital transmission standard
DVB-T	Digital Video Broadcast – Terrestrial, digital transmission standard
EEPROM	Electrically Erasable PROM
LNB	Low Noise Block converter
OS	Operating System
PCI	Peripheral Component Interconnect, bus system in a PC
PROM	Programmable Read-Only Memory
WDM	Windows Driver Model, Microsoft driver architecture supporting A/V Streaming

2. SYSTEM ENVIRONMENT

2.1 Hardware Relationship

Additional to the standard PC system the SAA7146A connects the DVB compliant front-ends to the PC internal PCI bus. The implemented CI interface allows the connectivity to an external CA module.

The tuner receives the HF signal either from a satellite, terrestrial, or cable source, depending on the specific system. The tuner front-end internally demodulates the HF signals into the digital transport stream, which is then fed into the video port of the SAA7146A.

The SAA7146A bus-masters this data-stream via the PCI bus into the system memory of the PC by means of the provided SW drivers.

An external CA module can be accessed via the CI interface from the I2C-bus and/or the DEBI-port of the SAA7146A.

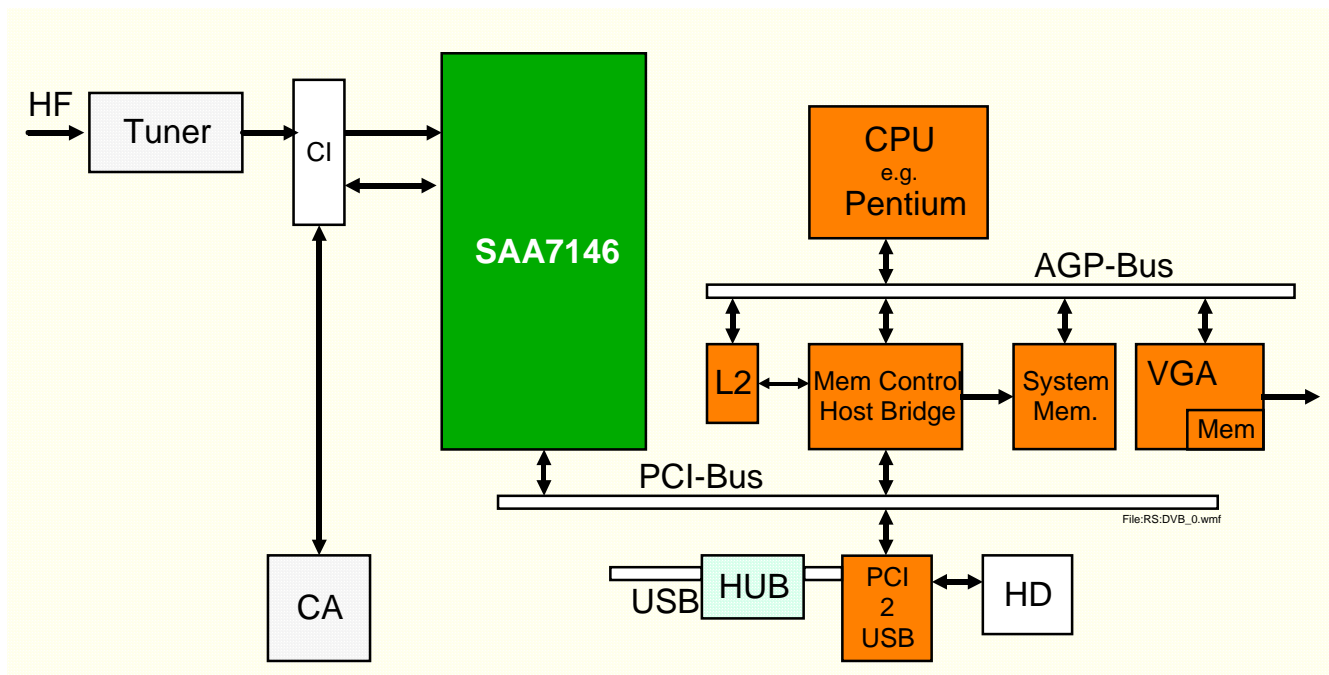


Figure 1: PC System with SAA7146A, DVB tuner front-end, and CA module

2.2 Software Relationship

The figure below describes the general hardware/software relationship in a PC environment. It consists of one of the DVB PCI Tuner-Board and the BDA AV-Streaming driver providing a common Direct Show interface to the application.

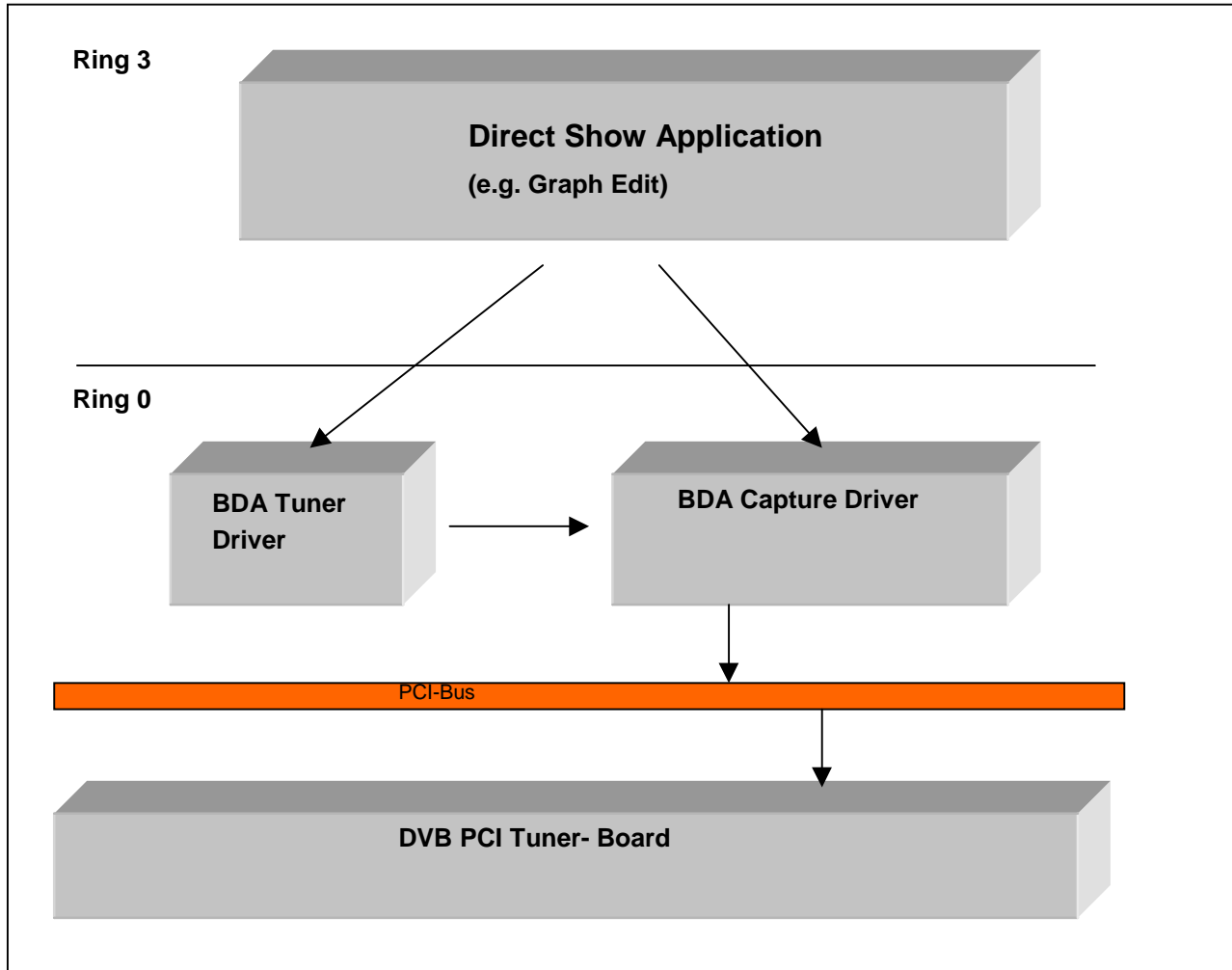


Figure 2: Software Relationship

2.3 Hardware Resources

At least

- Pentium II PC (> 400 MHz)
- PCI Graphics Adapter (e.g. ATI Rage 128 Pro)
- 64 MB RAM
- one of the DVB PCI Tuner Boards
- DVB video source (e.g. Astra Digital Satellite system)

2.4 Software Resources

- Windows 2000 Professional
- DirectX 8.0¹
- Graph Edit (part of DirectX 8.0 SDK)
- Philips DVB/BDA Capture Driver and Philips BDA/DVB Tuner Driver (Version 2.5)
- MPEG2 Transport Splitter e.g. Ravisent¹ or Microsoft (part of DX8.0 SDK)
- MPEG2 Decoder e.g. *Ravisent Cinemaster*, *XingDVD Player*¹ or other DirectX compliant decoder

¹The URLs for the different components are listed below

3. HARDWARE AND SOFTWARE INSTALLATION

Note: Before installing the driver be sure DirectX8.0 is already installed.

1. Insert the DVB board into a free PCI slot.
2. After starting the PC new hardware will be found.
To install the drivers, direct the hardware wizard to the driver disk of the PCI-DVB Tuner board or to another location where the INF files and the driver binaries can be found.
3. After finishing the installation of the capture driver, again new hardware will be found. Install the drivers for the tuner driver in the same way.

3.1 Registry Settings

The following registry entries have been made for the tuner driver during driver installation.

They can be found *somewhere* under

HKEY_LOCAL_MACHINE\SYSTEM\CurrentControlSet\Control\Class

To find the correct location, simply search the registry path for *Philips DVB/BDA*. As a reference an example is shown in the following figure.

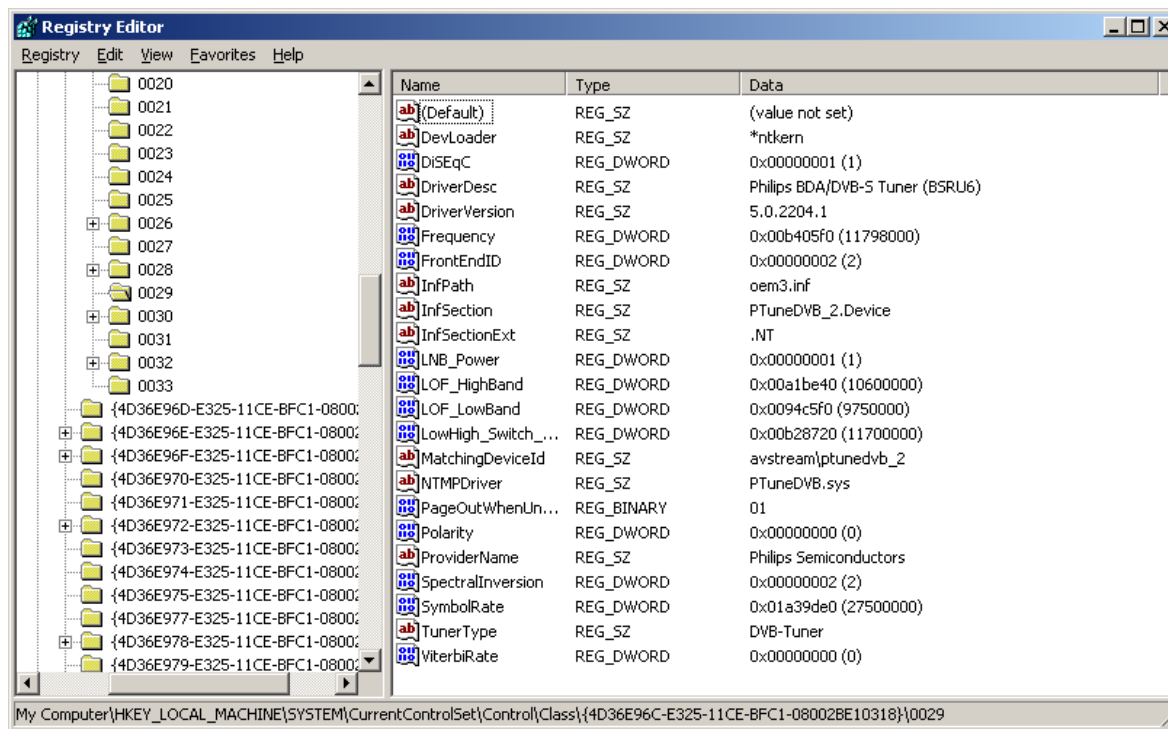


Figure 3: Register Setting: Example Philips BDA/DVB-S Tuner BSRU6

In our example the key DriverDesc holds the value 'Philips BDA/DVB-S Tuner (BSRU6)'. The other values can be seen in the table above.

The important registry entries that have to be changed or checked for the local DVB environment / broadcast¹ are:

- Frequency
Transponder frequency in kHz
- SymbolRate
Symbolrate in Hz
- ViterbiRate
inner FEC
0: automatic (default)
1: 1/2; 2: 2/3; 3: 3/4; 4: 4/5;
5: 5/6; 6: 6/7; 7: 7/8
- Polarity
0: Horizontal or left rotation → LNB Power 18V (default)
1: Vertical or right rotation → LNB Power 13V
- DiSEqC
0: disabled
>0: see details on next page
- LNB_Power
0: LNB Power disabled
1: LNB Power enabled (default)
- LOF_HighBand
Local oscillator frequency for frequency high band in kHz
- LOF_LowBand
Local oscillator frequency for frequency low band in kHz
- LowHigh_Switch_Frequency
Boundary between high and low frequency in kHz

The change of one of the last 4 entries requires a re-boot of the system. All other settings listed above are valid when re-inserting the tuner filter into the filter graph.

¹ Frequency tables for the different DVB-S broadcasters can be found in the internet.

DISEqC Details:

The DISEqC is a command bus similar to the I2C bus. The DISEqC command sequence consists of 3 or 4 bytes. An example command sequence is: 0xE0, 0x10, 0x38, 0xF3.

1. The first byte is the start byte with the value 0xE0.
2. The second byte holds the address. The value 0x10 means all switches.
3. The third byte means command: 0x38.
4. The fourth and last byte contains the command. The upper nibble 0xF means reset all previous settings. The lower nibble holds the bits (from high to low): option, position, polarisation, and band. The example value of 0x3 means vertical position, and high band.

For more details check the web-page link in the web-link chapter.

3.2 How to build a Graph Edit Application

The following steps have to be taken to build a test application with Graph Edit.

Note: Check the registry for the correct settings, otherwise no data can be received.

1. Open *Graph Edit* and insert the following filters.
 - BDA Receiver component -> Philips BDA/DVB-S Capture (xxxx)
 - BDA Receiver component -> Philips BDA/DVB-S Tuner (xxxx)
 - DirectShow Filters -> RAVISENT MPEG Splitter (or equivalent components)
 - DirectShow Filters -> RAVISENT MPEG Decoder (or equivalent components)
2. Connect the output pin of the first inserted filter with the input pin of the next inserted filter. Do that with all filters so that a chain of filters is built up. Finally render the output of the decoder filter automatically.
The picture below shows a correctly rendered filter graph.

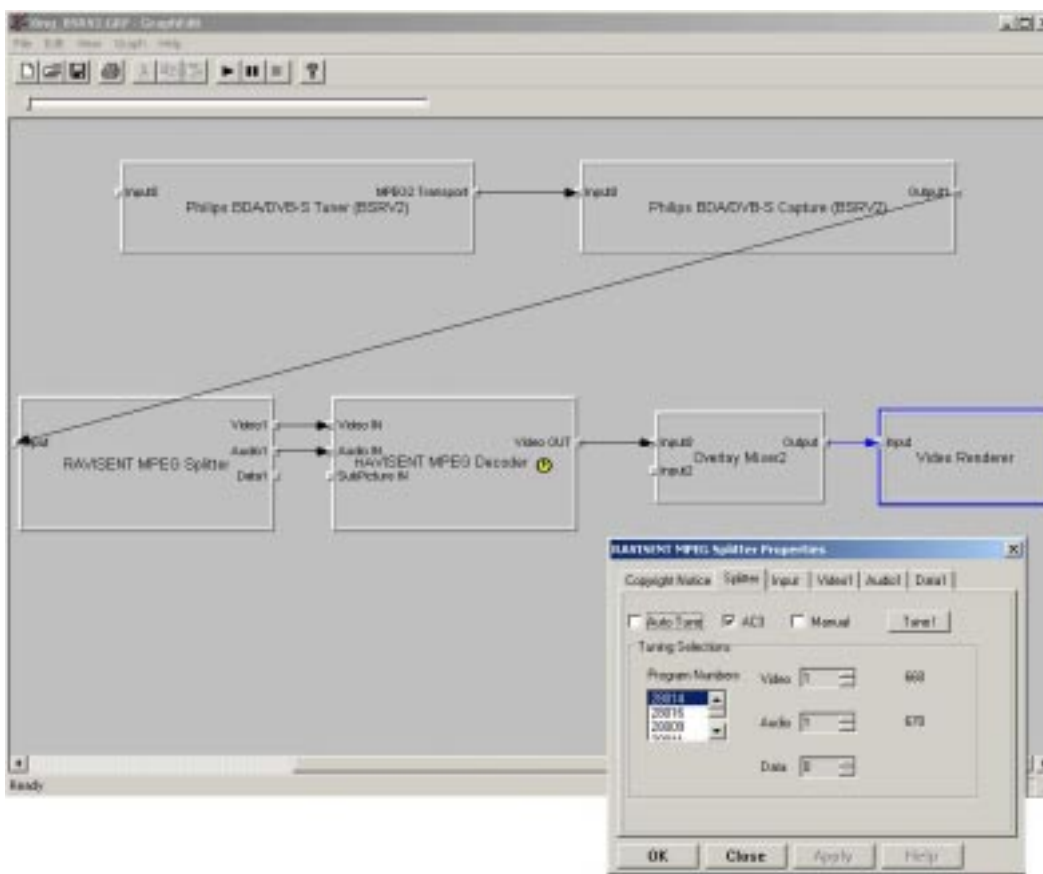


Figure 4: Direct Show Filter Graph

4. BOARD DESCRIPTION

4.1 Tuner

The board provides footprints for different types of digital tuners. Depending on the supported standard the board is called Sylt (DVB-S), Tenerife (DVB-T), and Crete (DVB-C). The layout supports the Philips DVB-S solution of SU1200. As the tuner is adapted to this application area, the can is small. This provides a form factor to a production board. The solutions for terrestrial and cable tuner will follow.

As the ALPS brand provides digital tuners for DVB-S, DVB-T, and DVB-C application areas with the same footprint, all those tuners will be supported. For the time being only the DVB-S solution is available. The tuner types are BSRU6, and BSRV2. These types have been tested.

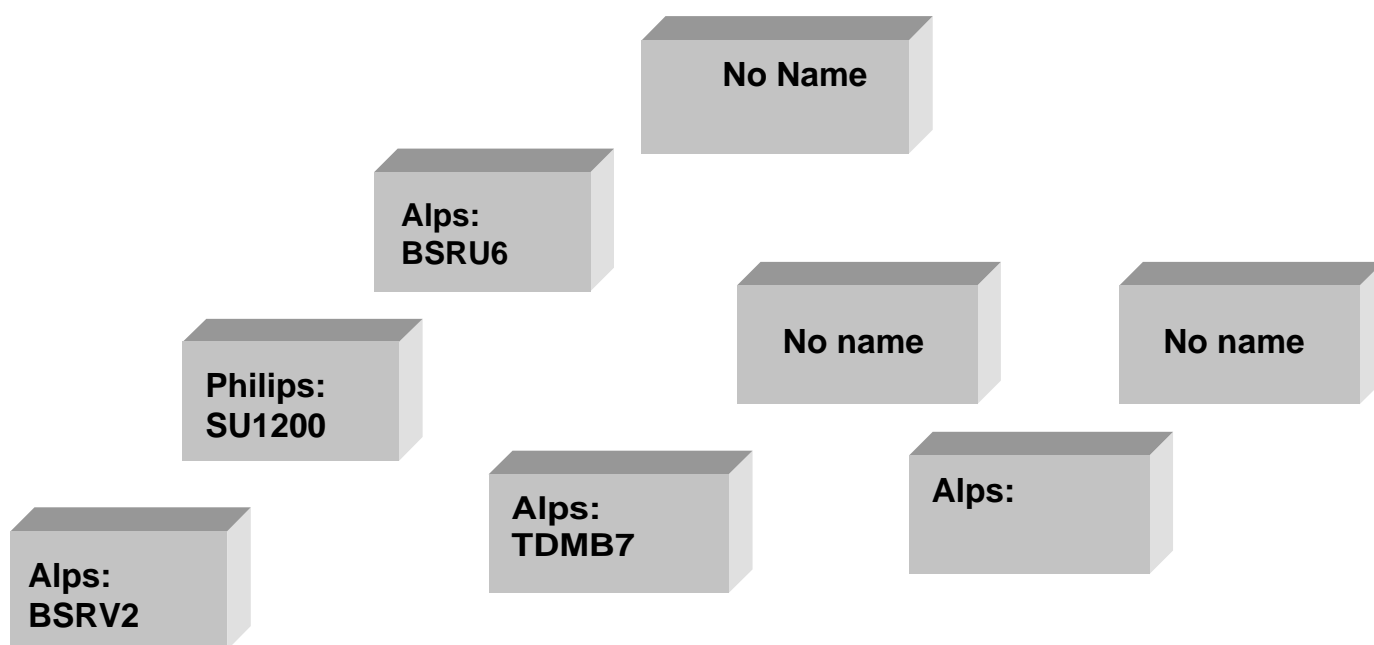


Figure 5: Supported Tuners: Actual State and Future

Other brands of tuners will be supported on a case-by-case basis.

The power supply of the existing platform will support a wide variety of tuner front-ends. Due to the variety of tuner type areas (DVB-T, DVB-C), some parts of the power supply might be obsolete.

4.2 SAA7146A

The PCI bridge SAA7146A provides versatile interconnects to the PC. The video ports with their internal buffers enable the streaming of transport data to the buffer in the main memory. The I2C bus interface provides control to the different components on the board, such as tuner including its channel decoding facilities, the EEPROM for storing the board setting, and the CA module via the CI interface. The DEBI bus provides fast interfacing to the CA module. The audio interface is currently not used in the application.

As only one of the video ports is used, the other one could provide access for analogue video input (with an additional video decoder). However this is not foreseen on this board.

4.3 Common Interface (CI) for Conditional Access (CA)

A Common Interface is provided on the board for communication to a Conditional Access module. The CI interface is set up as two 50-pin connectors for ribbon cables. While one row holds the signals, the other one is (mostly) grounded to shield the signals.

The 8 bit transport streams (outbound and inbound) including their control signals are on these connectors. For controlling the CA module the I2C bus is provided as well as the DEBI bus with its control signals. Furthermore also GPIO signals are available.

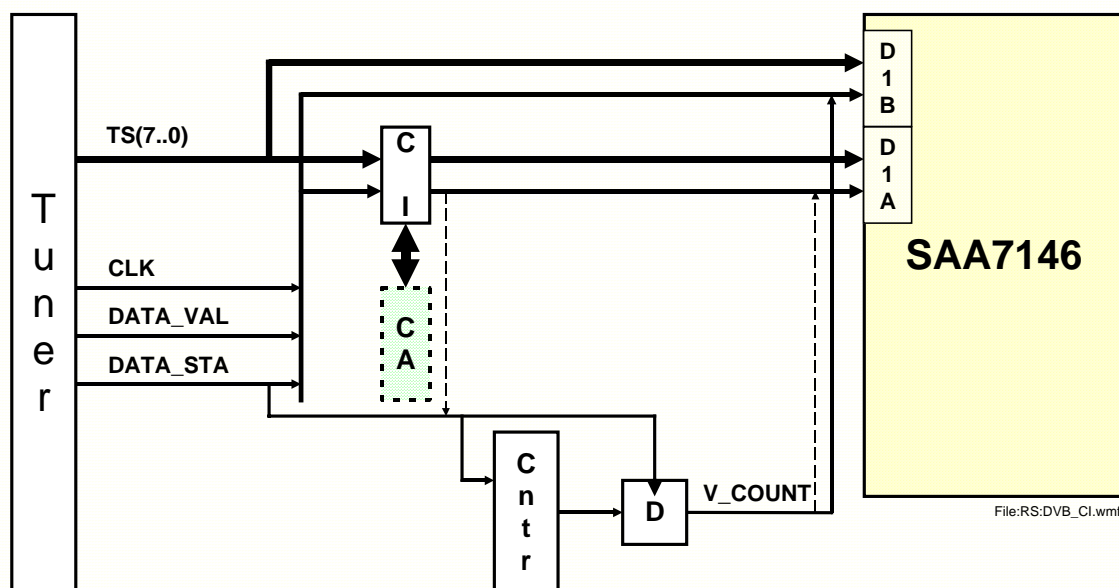


Figure 6: Transport Stream Path between Tuner and SAA7146A

A counter structure for generating V_COUNT is implemented only for the direct path into the D1B port. It is expected that a similar structure is built on the CA sub board. If not, an optional hard-wired solution is possible (indicated by the dotted lines).

4.4 Control Signals for Transport Stream

The tuner outputs the transport stream on an 8-bit data bus accompanied by a set of control signals. All tuner output signals are de-coupled by means of serial 33 Ohm resistors. The transport stream data bus is then called VDB (VDB7..VDB0). The control signals to the tuner have to be adapted to the video interface of the SAA7146A. This adaptation includes a small circuitry for generating a block count signal, which emulates a vertical sync of an artificial video signal. The circuitry consists of an asynchronous counter of type 74LV4040 (74LV4020 or 74LV4060) followed by a D-latch. The count length is set to

512, but also other values might be used. The count length determines the distance of the vertical sync pulses, driving the internal buffer handling.

The general structure is shown in picture Figure 6: Transport Stream Path between Tuner and SAA7146A. The signal description is given in the following table.

Tuner / Counter	Bus	D1 B @ SAA7146A	Comments
CLK	CTR_B0	LLC_B	Clock
DATA_VAL	CTR_B1	PXQ_B	Data Valid
DATA_STA	CTR_B2	HS_B	Pack Start Sync
V_COUNT	CTR_B3	VS_B	Packet Count

Table 1: Transport Stream Control Signals

4.5 LED Control

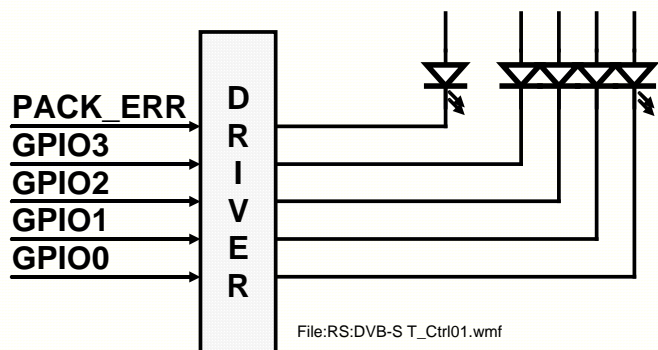


Figure 7: LED Controls

The LED set allows visualising specific system information. A red LED signals a packet error condition of the tuner (PACK_ERR). The GPIO lines can be individually used.

4.6 LNB Control

The supply and control of the remote LNB is provided from a single IC. A single voltage up-converter feeds both voltage inputs. The control signals for external modulation (DISEqC), vertical selection (VSEL), enabling (EN), and locking (ENT) are provided from the tuner front-end. Inside the tuner these output signals are controlled via I2C bus.

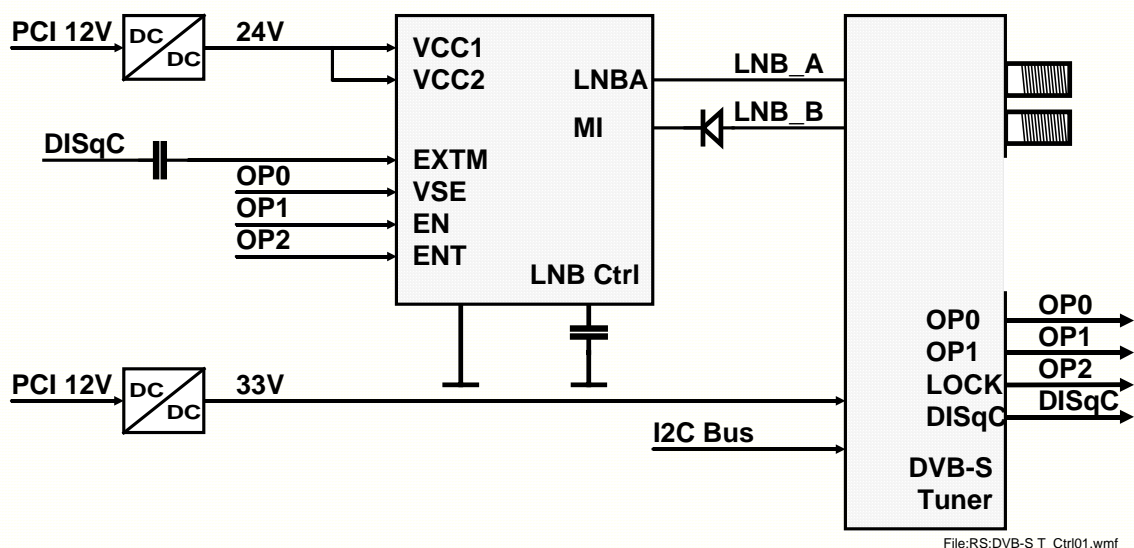


Figure 8: LNB Control for Satellite Tuner

The output of the LNB power supply chip is fed as LNB_A and LNB_B signals to the satellite tuner for supplying and controlling the remote LNB via the coax cable.

4.7 EEPROM

The EEPROM PCF8582C-2T provides the means to identify the board on the PCI bus and its supported type of DVB-S tuner. Further values can be stored in the remaining space. A content map and the different settings are provided in chapter 6. The first 6 lower byte addresses are reserved according to the PCI bus spec. They are reflected in the PCI bus device address space.

The EEPROM type used, provides 256 bytes of storage and its address has to be set to 0xA0. The PCI bus BIOS in combination with the SAA7146A expects this address.

4.8 Power Supply

The components on the board need a set of different power supply voltages. To ease this approach for the demonstration board, ready-off-the-shelf solutions are used. For a production there might be more cost-effective solutions available on the market.

Input Voltage	Converter	Output Voltage	Comment
PCI 5V	LF25A	VDD2.5	Standard voltage regulator 2.5 V tuner front-end Device dependent
PCI 5V	LF33A	VDD3D	Standard voltage regulator 3.3 V of tuner device and SAA7146A
P5VD	5V/33V Converter	V30TUN	Up-converter to 33V as tuner voltage
PCI 12V	78M05	VDD5A	Standard 5V voltage regulator Std 5V voltage regulator
PCI 12V	TEN 5 _ 1222	VDD24	Up-converter to 24V to LNB P13P Satellite specific

Table 2: Power Supplies

The VDD24 power supply generation is for satellite application only, it is obsolete for the terrestrial and the cable solution.

5. OPERATION

Before starting the application for the first time, please modify the settings of your local transponder by changing the register settings inside the key mentioned in chapter Registry Settings.

After any registry modification, the tuner filter has to be re-inserted into the graph. The power settings (LNB_Power, LOF_HighBand, LOF_LowBand, LowHigh_Switch) are valid after re-boot only.

1. Start the filter graph application which is included in the DirectX package.
2. Build up the filter tree including the Philips tuner filter and the Philips capture filter.
3. For operation start the graph. A video window will pop up.
4. Open the properties menu (right mouse click) of the splitter filter, and select a **proper** channel
5. Then press the TUNE button! Reference is the small window in Figure 4: Direct Show Filter Graph.
6. The selected video content of the transport stream will then be streamed to the video window. As the OS buffers are large, it can take a few seconds until video appears.

6. BOARD SELECTION BY THE DRIVER

6.1 EEPROM Content

The lower Addresses of the EEPROM are reserved for specific PCI bus related data. The Subsystem ID is used for keying a specific type of tuner in a specific environment.

Address	Data	PCI Configuration Space	Comment
0x00	0x4F	Sub System ID	Sub System ID: This is subject to change for different tuners and application fields Example: Sylt-board (DVB-S, BSRU6) := 0x4F52
0x01	0x51	Sub System ID	
0x02	0x11	Sub Vendor ID	This ID is used for the tuner identification of the BDA driver. The Sub Vendor ID is set to the Philips Vendor ID value as default. This might be subject of change in case of customized drivers.
0x03	0x31	Sub Vendor ID	
0x04	0x26	Max_Latency	Default value 0x26
0x05	0x0F	Min_Grant	Default value 0x0F

Table 3: PCI Configuration Space

6.2 Subsystem ID System

There is a specific system for identifying the board and tuner type out of the Sub System ID.

Data	Selection of (additional) analogue Video Decoder
0xy1yy	SAA7111
0xy2yy	SAA7112
0xy3yy	SAA7113
0xy4yy	SAA7114
0xy8yy	SAA7118

Table 4: Subsystem ID: Selection of analogue Video Decoder

Reference Board	Transmission System	Tuner Vendor: Tuner Type	Sub System ID
MAUI	ATSC	Philips: TDA1536/FH44	0x7A42
RUEGEN	ATSC / NTSC	Philips: FCV1236	0x7844
SYLT	DVB-S	Philips :SU1200	0x4F50
		Alps: BSRV2	0x4F51
		Alps: BSRU6	0x4F52
		LG:	0x4F53
TENERIFE	DVB_T	Philips:	0x5F50
		Alps:	0x5F51
		LG:	0x5F52
		Sharp:	0x5F53
CRETE	DVB-C	Philips:	0x6F50
		Alps:	0x6F51
		LG:	0x6F52
		Sharp:	0x6F53

Table 5: Subsystem ID: Reference Boards with related digital Tuner Types

At the moment of printing this document, only the drivers for tuner types BRSV2 and BSRU6 from Alps are in operation. The driver for Philips SU1200 is under test.

The boards MAUI and RUEGEN support the ATSC standard and are mentioned for completeness purposes only.

6.3 Support Tool: PCITEST.EXE

With the DOS-based tool PCITEST.exe and a related supplied batch and INI file it is easily possible to program the EEPROM on the board with the appropriate setting. The listing of a sample batch and INI file is provided in the annex.

7. WEB LINKS

7.1 Philips Semiconductors

Addresses:

Philips Semiconductors internal Demo-Board Shop:

<http://pww-cs.hamburg.sc.philips.com/MarCom/OF/index.htm>

Go to the Philips Semiconductors Homepage:

<http://www.semiconductors.philips.com>

Select: Computing -> PC Products -> Digital Video Encoders & Decoders
to come to the following web page:

http://www.semiconductors.philips.com/pc/systems/eval_board/sylt/

7.2 Selection of Links to 3rd Party Vendors

This table is a selection and will be updated by adequate means. Inputs from other 3rd parties are welcome.

Intervideo:

<http://www.intervideo.com>

Microsoft: Homepage

<http://www.microsoft.com>

Microsoft: DirectX Homepage

<http://www.microsoft.com/directx/>

<http://www.microsoft.com/directx/homeuser/downloads/default.asp>

Microsoft: Beta Homepage

<http://www.betaplace.com>

Ravisent

<http://www.ravisent.com>

Viona:

<http://www.viona.de/>

Xing Labs:

<http://www.xinglabs.com>

7.3 Frequency Tables

Here are satellite stations listed with their respective frequencies.

<http://www.astra.la>

<http://www.euteldat.com>

<http://www.euteldat.de>

<http://www.lyngsat.com>

7.4 Miscellaneous

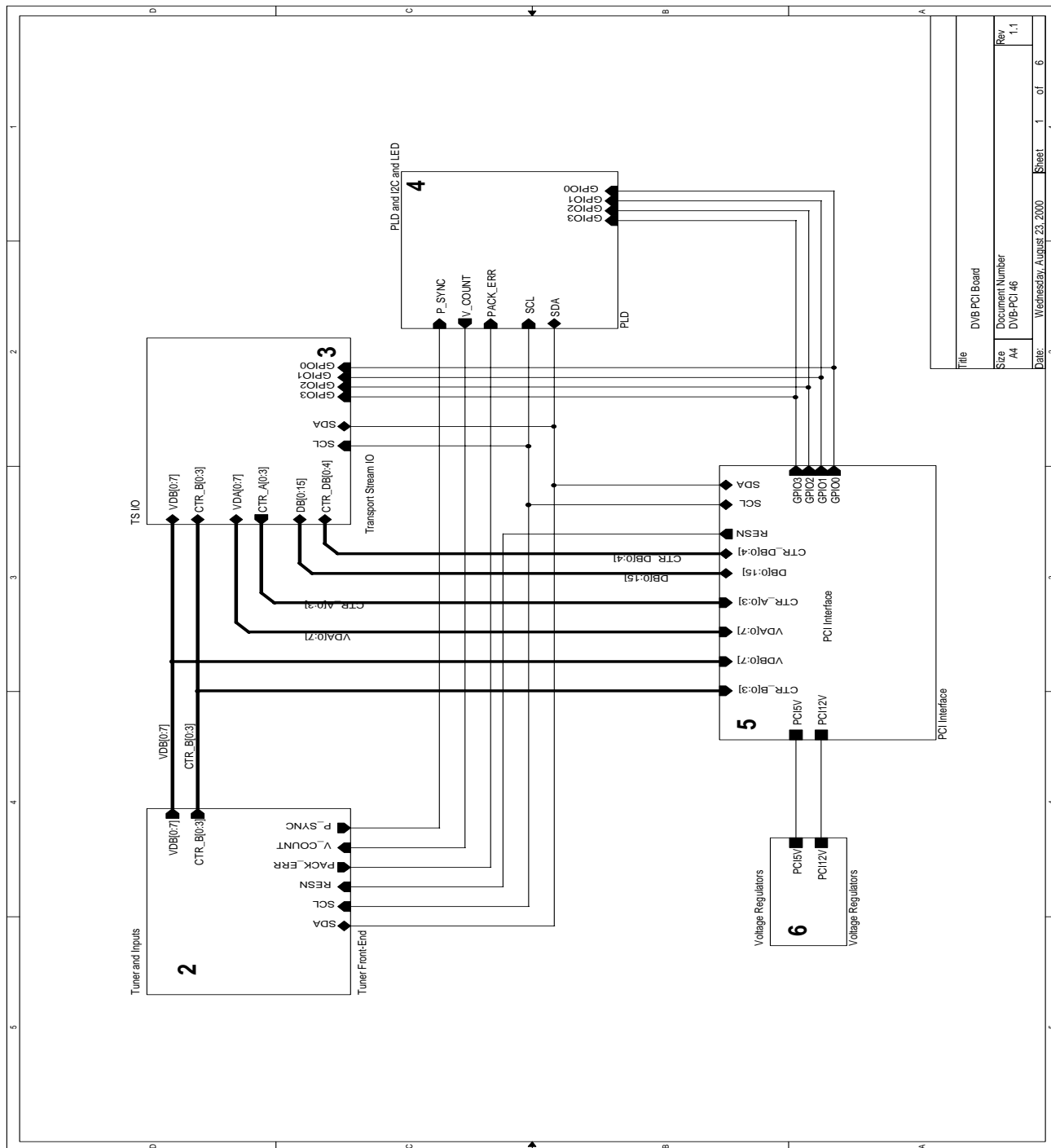
On this link more information on the control of satellite dishes are listed.

<http://www.satshop.com/diseqc.htm>

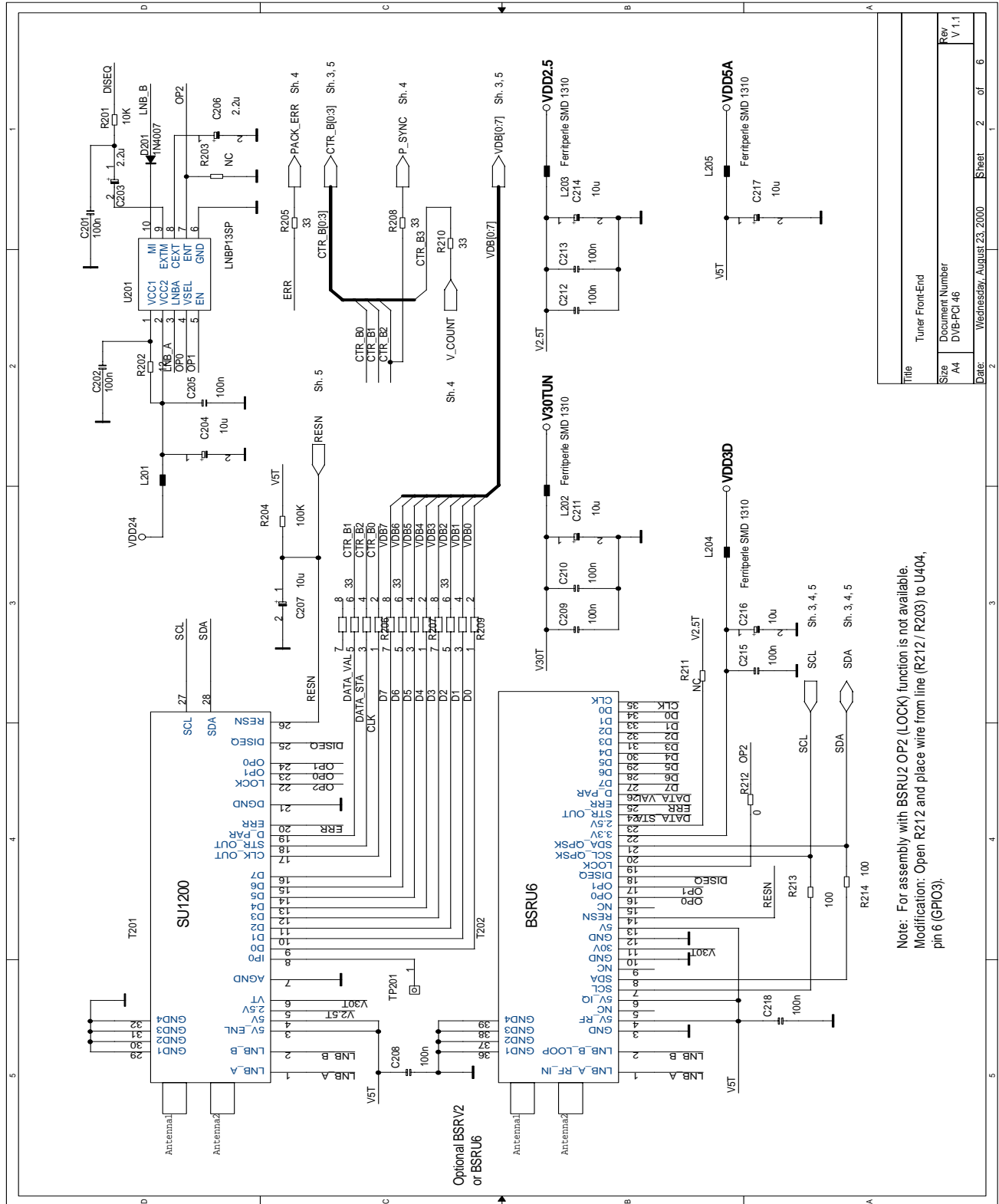
8. APPENDIX

8.1 Schematics

8.1.1 Overview

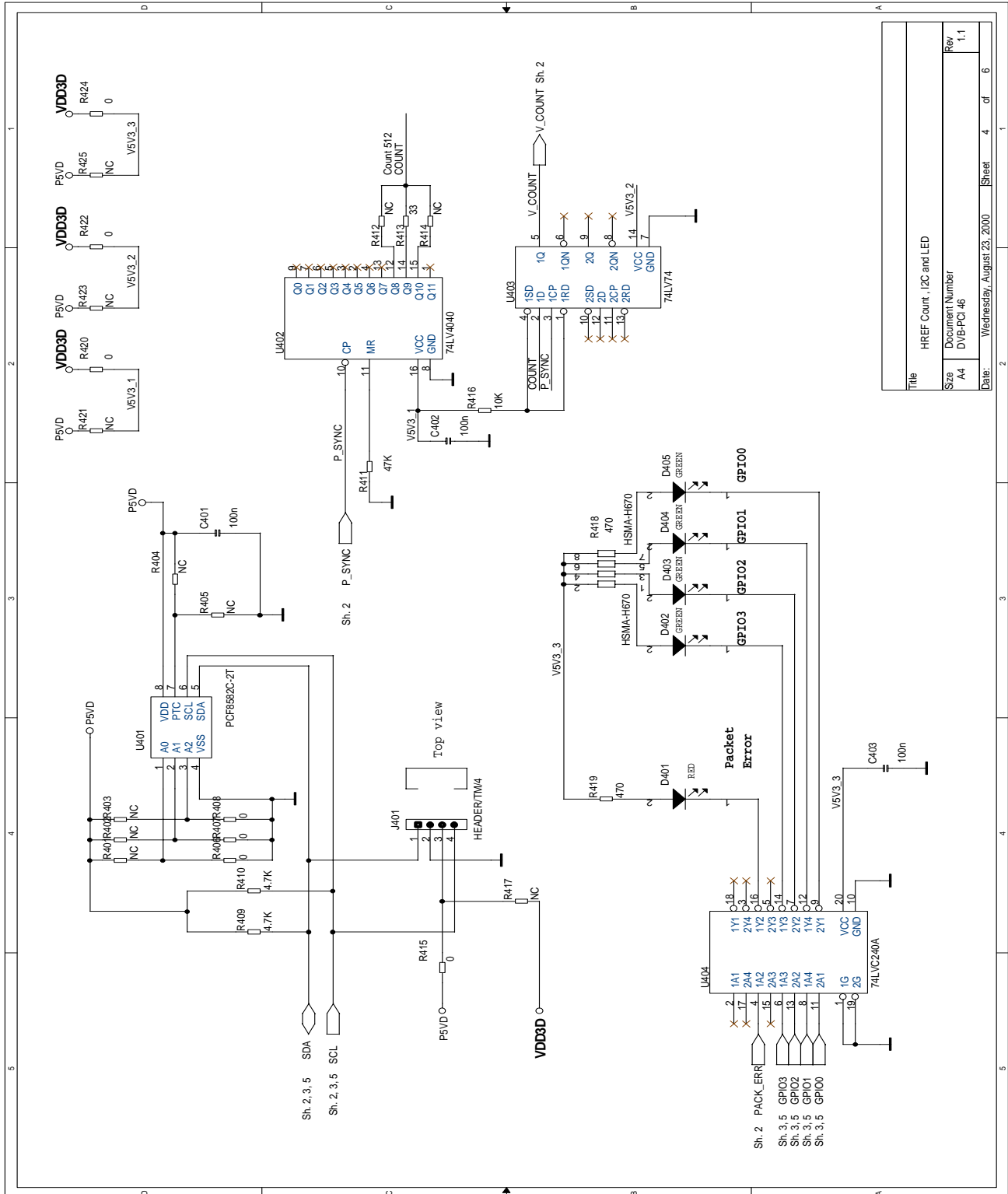


8.1.2 Tuner Front-End



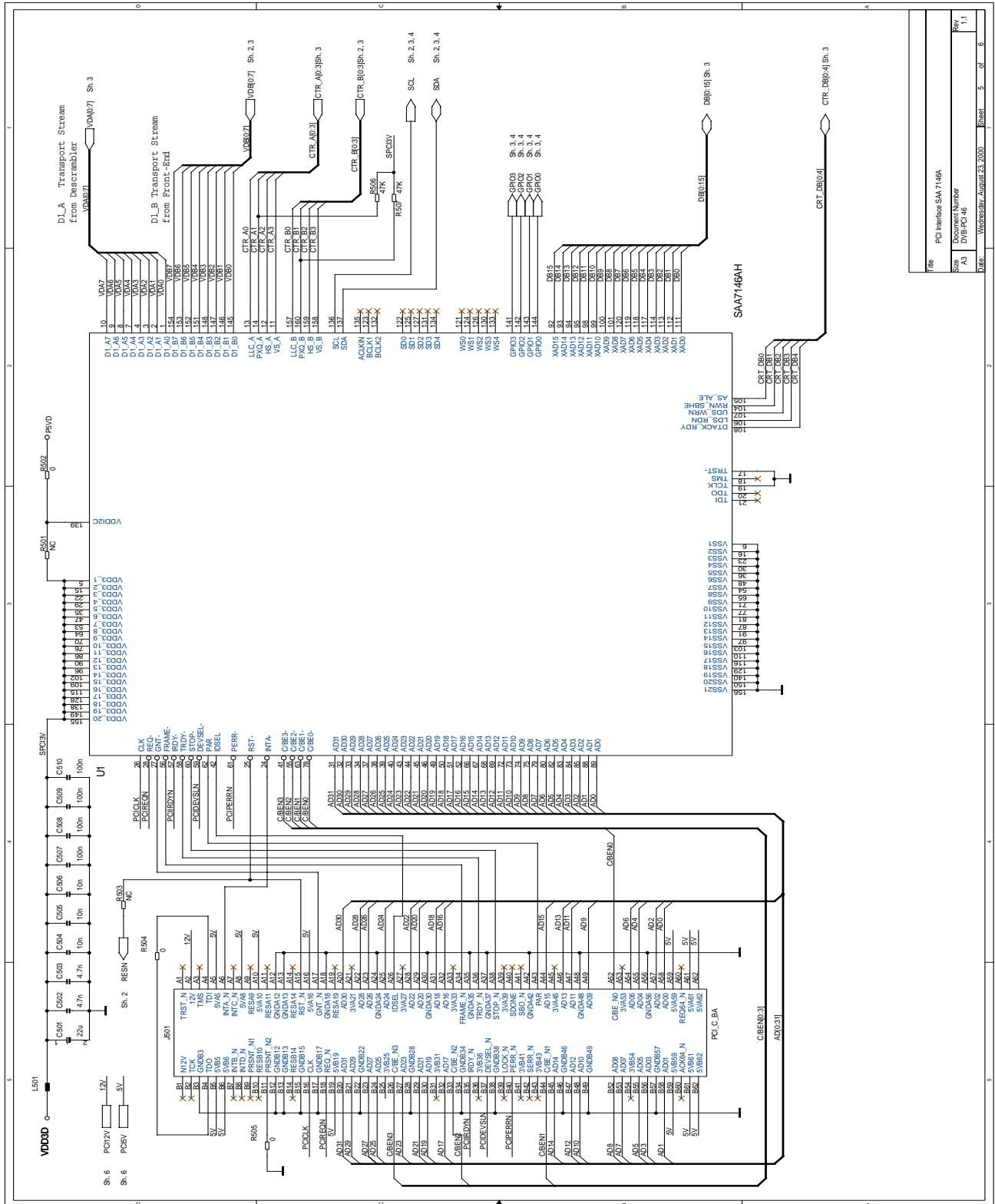
Title		Tuner Front-End
Size	Document Number	DVB-PCI 46
A4	Rev	V 1.1
Date:	Wednesday, August 23, 2000	Sheet 2 of 6

8.1.4 HREF Count, I2C and LED

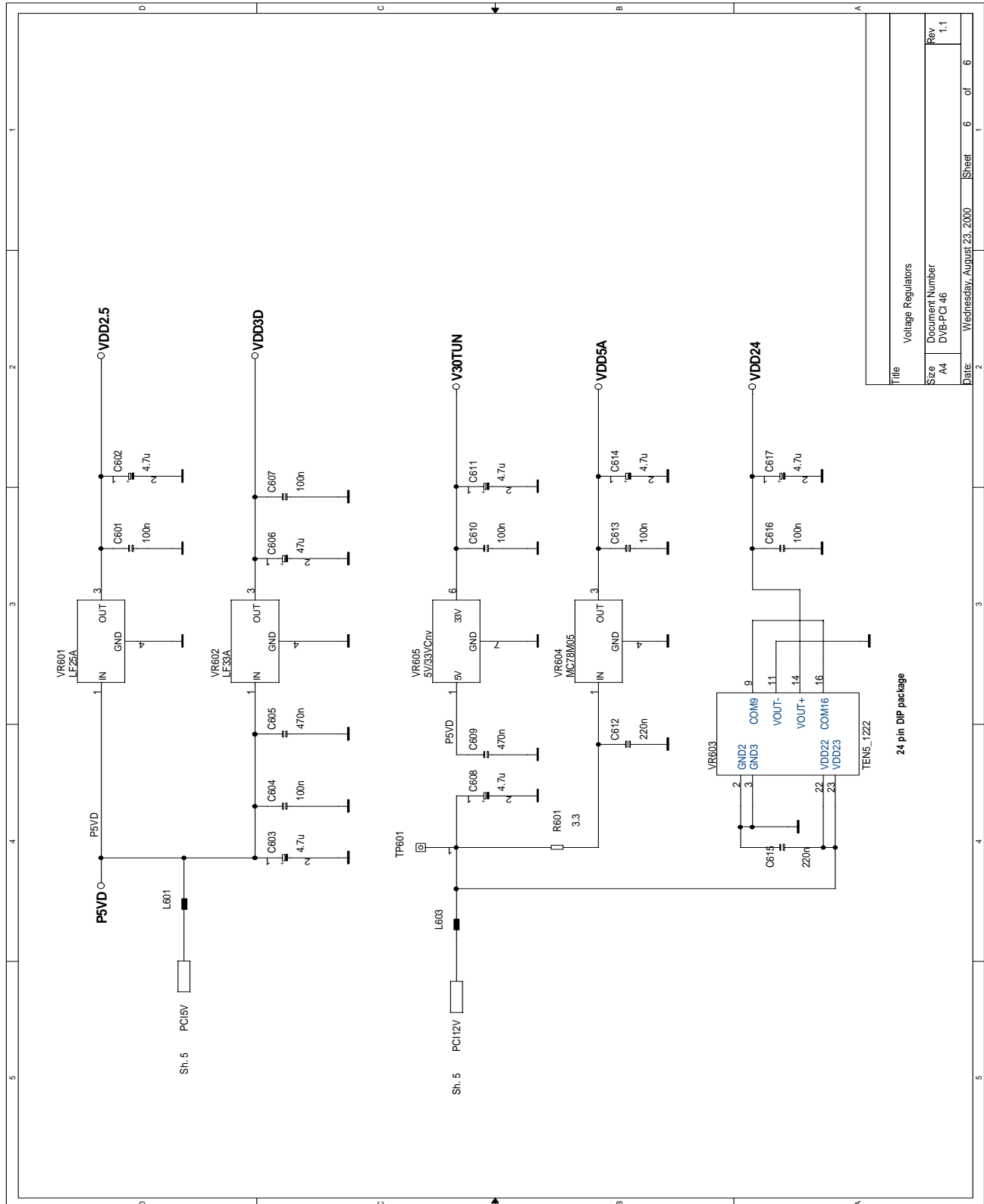


Title	HREF Count, I2C and LED
Size	Document Number
A4	DVB-PCI 46
Date:	Wednesday, August 23, 2000
Sheet	4 of 6
Rev	1.1

8.1.5 PCI Interface SAA7146A



8.1.6 Voltage Regulators



Title		Voltage Regulators	
Size	A4	Document Number	DVB-PCI 46
Rev	1.1	Date:	Wednesday, August 23, 2000
Sheet		6 of 6	

8.2 Checked Configurations

The following configurations are checked.

Input Voltage	Converter	Output Voltage	Comment
1	Intervideo Win DVD 2000 V.2.1	MS: DX8 Splitter	under test
2	Ravisent Decoder Cinemaster 2000	Ravisent Splitter Filter N.143	working
3	Ravisent Decoder Cinemaster 2000	Ravisent Splitter Filter N.143	working
4	Xing DVD Player V.2.05	MS: DX8 Splitter	working

Table 6: Checked Configurations

This list will be updated and also posted on the home page of the board.

8.3 EEPROM Settings

```

; -----
;           (C) Philips Semiconductors 2000
; All rights are reserved.  Reproduction in whole or in part is prohibited
; without the written consent of the copyright owner.
;
; Philips reserves the right to make changes without notice at any time.
; Philips makes no warranty, expressed, implied or statutory, including but
; not limited to any implied warranty of merchantability of fitness for any
; particular purpose, or that the use will not infringe any third party
; patent, copyright or trademark.  Philips must not be liable for any loss
; or damage arising from its use.
; -----
; -----
;           The EEPROM address is 0xA0 fixed
;           The first six byte are related to PCI settings
;           They point to the Subvendor ID's
;           The Customer Codes are implemented
[EEPROM]
LastEntry=05
Entry000=0x00 0x4F           ;Sub System ID: DVB-PCI46 (DVB-S, BSRU6)
Entry001=0x01 0x52
Entry002=0x02 0x11           ;Sub System Vendor ID : Philips
Entry003=0x03 0x31
Entry004=0x04 0x26           ;Max_Latency: Default 0x26
Entry005=0x05 0x0F           ;Min_Grant: Default 0x0F
; -----

```

8.4 Sample PCITEST Batch File for Programming the EEPROM

The content of the batch file *Set_eepr.bat* consists of the following line:

```
pcitest e_set
```

It will transfer the data of the INI file section into the EEPROM on board of the reference boards.