

# AN10753

## ESD protection for USB 2.0 interfaces

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Application note

### Document information

Info	Content
<b>Keywords</b>	ESD, USB, PESD5V0X1BL, PESD12VS1UL
<b>Abstract</b>	This application note describes how to protect USB 2.0 ports with NXP general-application discretes parts, i.e. low-capacitance ElectroStatic Discharge (ESD) protection diode PESD5V0X1BL.

## Revision history

Rev	Date	Description
01	20090115	Initial version

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## 1. Introduction

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An Integrated Circuit (IC) connected to external ports can be damaged by ElectroStatic Discharge (ESD) from the operating environment.

The result of ever-shrinking IC process technology is the decrease of ESD robustness because of the smaller geometry of the silicon die.

Traditional methods to prevent ICs from ESD damage are the implementation of additional devices such as:

- Zener diodes
- Varistors
- Transient Voltage Suppressor (TVS) diodes
- Bipolar clamp diodes

However, at much higher data rates, the parasitic characteristics can distort or deteriorate signal integrity. This application note examines the general parameters the hardware designer should look at to increase the ESD robustness of the application, e.g. USB interfaces.

## 2. ElectroStatic Discharge (ESD) basics

ESD issues are one of the most challenging issues in the semiconductor industry these days.



Fig 1. Typical attention sign

This is the result of ever-shrinking IC process technology. Due to the smaller geometry of the silicon die, the ICs are more ESD sensitive.

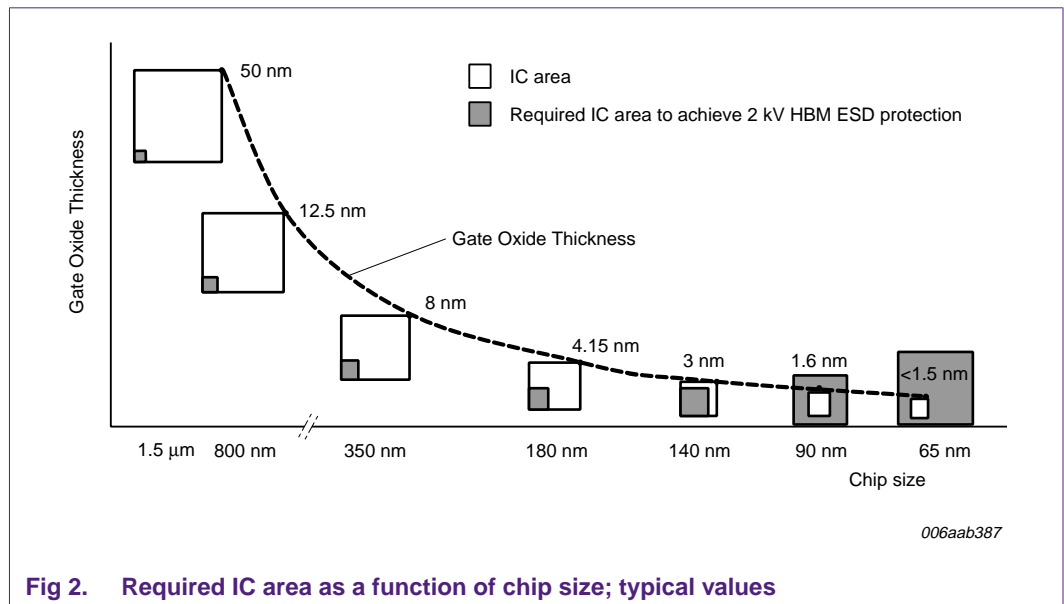


Fig 2. Required IC area as a function of chip size; typical values

An ESD event is the transfer of energy between two bodies of different electrostatic potential.

ElectroStatic Discharge can happen by contact, or via an ionized ambient discharge.

There are several models known:

- Human Body Model (HBM) - A human body is discharged to an electronic component.
- Machine Model (MM) - A machine or tool is discharged to an electronic component.
- Charged Device Model (CDM) - An electronic component is discharged to the ambient.
- System Level (IEC) - A human body is discharged to a powered system.

This application note covers the differences between the Human Body and the System Level Models which are both Human Body Models, but the System Level Model is relevant for a complete solution, e.g. a portable multimedia device.

### 2.1 Human Body Model (HBM) - Standards IEC/EN 61340-3-1 or MIL-STD 883

This standard covers the manual handling of none-powered electronic components. The handling can be picking up a device for testing or mounting the device on a Printed-Circuit Board (PCB)!

A capacitor of 100 pF is charged and then discharged via a 1.5 kΩ resistor to the Device Under Test (DUT).

The waveform of IEC 61340-3-1 is shown in [Figure 3](#), the rise time is defined up to 10 ns.

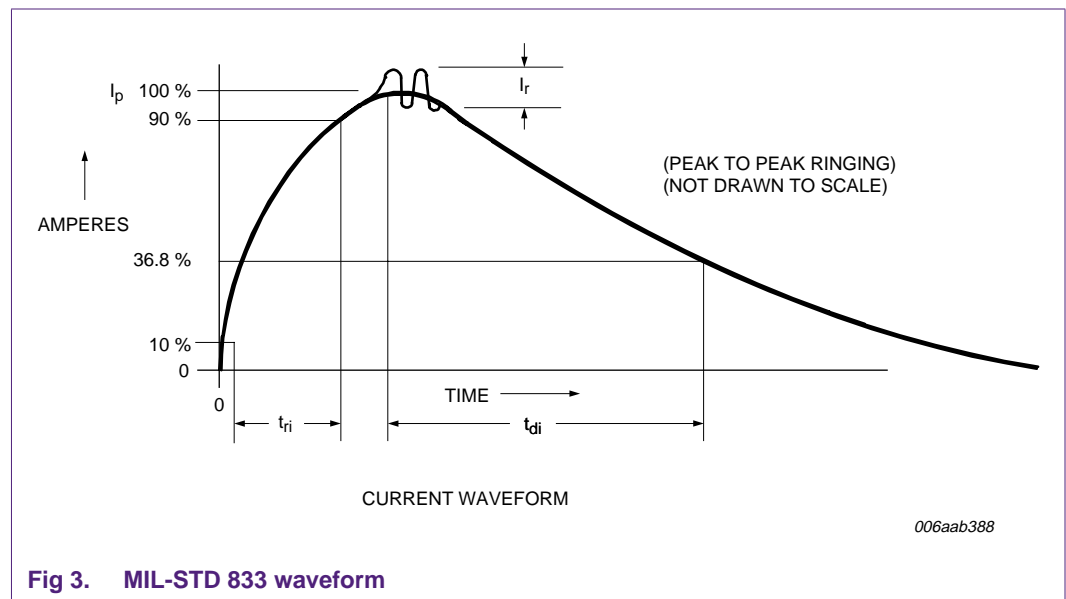


Fig 3. MIL-STD 833 waveform

Table 1. Waveform parameters according to MIL-STD 833

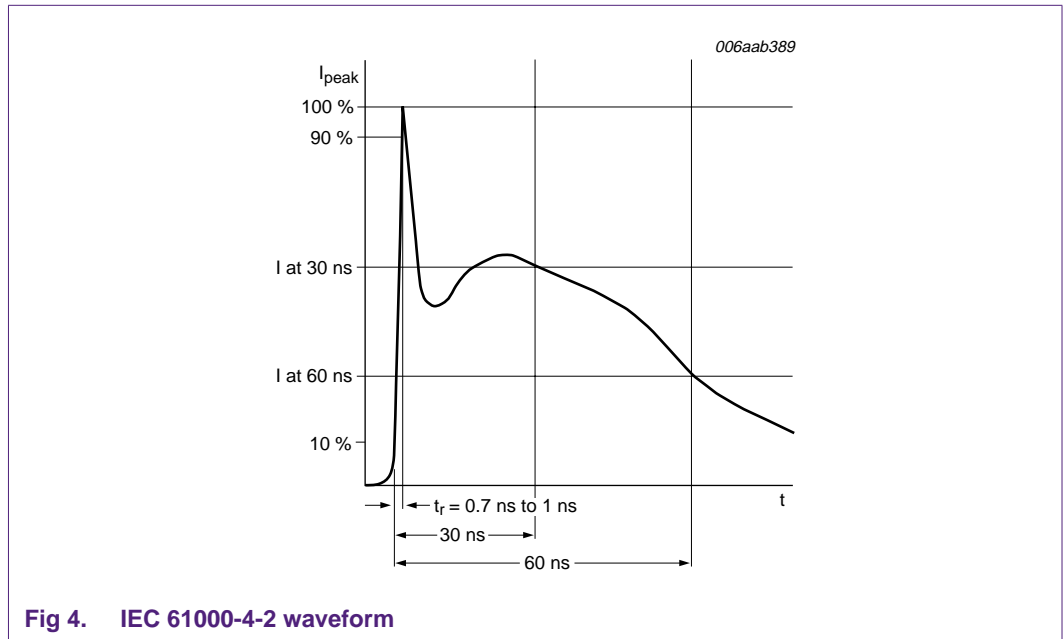
Step	Test voltage (kV)	Peak current (A)
1	0.5	0.33
2	1	0.67
3	2	1.33
4	4	2.67

**2.2 System Level (IEC) - Standard IEC 61000-4-2**

This standard covers the manual handling of a powered electronic system, e.g. touching an interface connector.

A capacitor of 150 pF is charged and then discharged via a 330 Ω resistor to the DUT.

The waveform of IEC 61000-4-2 is shown in [Figure 4](#), the rise time is defined between 0.7 ns and 1 ns.



There are different levels for test proposals mentioned.

For contact or air discharge test, they differ in the voltage value (see [Table 2](#)).

**Table 2. Waveform parameters according to IEC 61000-4-2**

Level	Test voltage (kV)		Current (A)		
	Contact	Air	Peak current	After 30 ns	After 60 ns
1	2	2	7.5	4	2
2	4	4	15	8	4
3	6	8	22.5	12	6
4	8	15	30	16	8

### 2.3 Standard comparison

Both models differentiate concerning the test voltages.

One can see that a 2 kV discharge voltage refers to different discharger currents.

Therefore, NXP recommends external ESD protection to be compliant with the IEC 61000-4-2 standard.

### 3. USB interface protection

The USB 2.0 standard covers several data transmission rates. It is also compliant to the former specification USB 1.1.

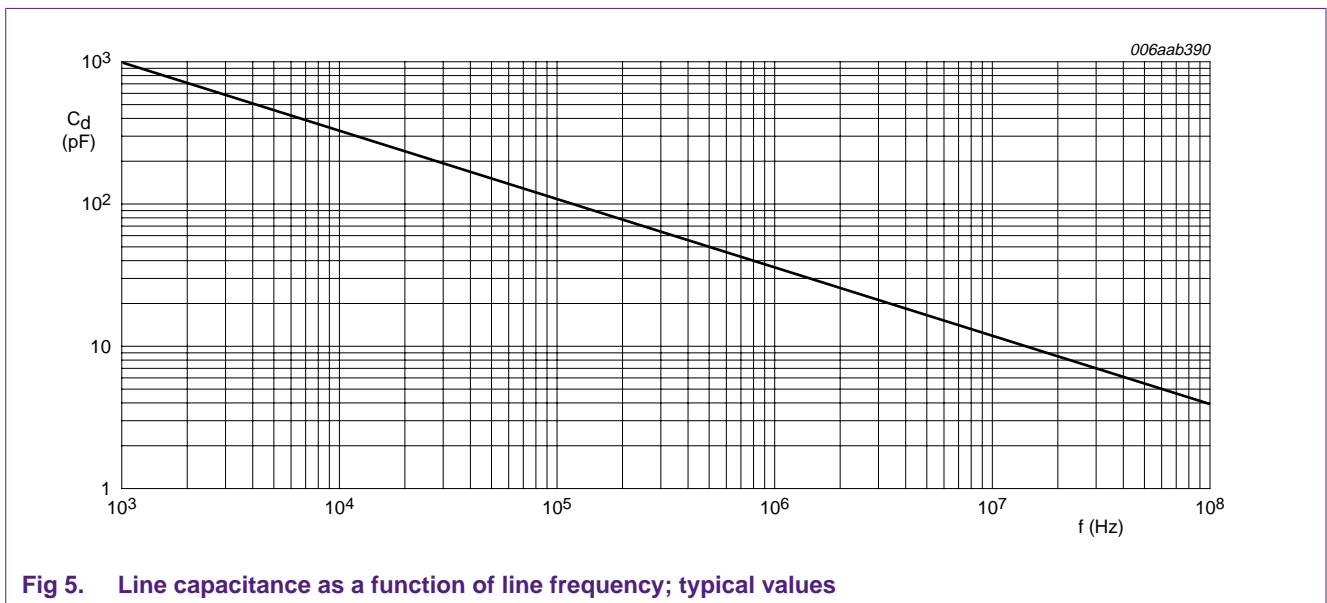
Following data transmission rates are covered:

- 1.5 MBit/s (low speed)
- 12.0 MBit/s (full speed)
- 480 MBit/s (hi-speed)

For the hi-speed mode, the maximum allowed capacitance according to the USB 2.0 specification is 10 pF overall.

These 10 pF are shared by a maximum of 5 pF for the transceiver itself, and the other 5 pF for the connector, PCB traces, and additional components.

[Figure 5](#) shows the maximum allowed line capacitance at different data speeds.



**Fig 5. Line capacitance as a function of line frequency; typical values**

To expose any issue in USB data lines, the measurement method “eye pattern”, also known as “eye diagram”, is used.

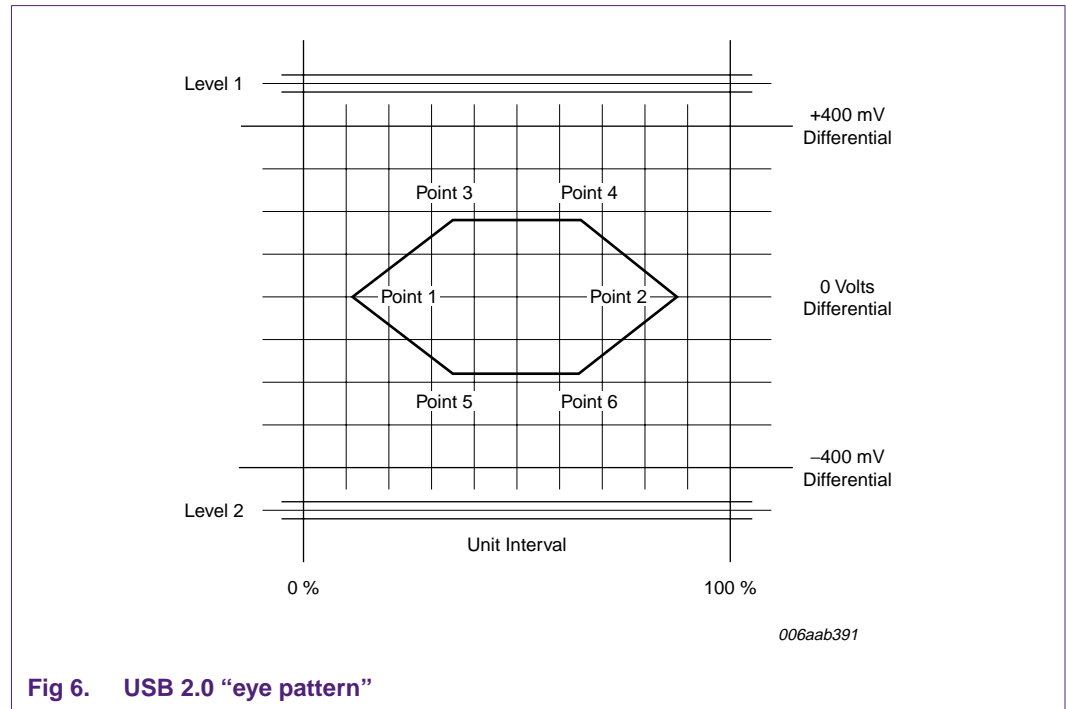
It represents a digital signal that provides minimum and maximum voltage levels and signal jitter.

One can also measure the signal rise time and the fall time, as well as overshoot and undershoot.

Line capacitance and bandwidth effects of the USB data transmission can be evaluated!

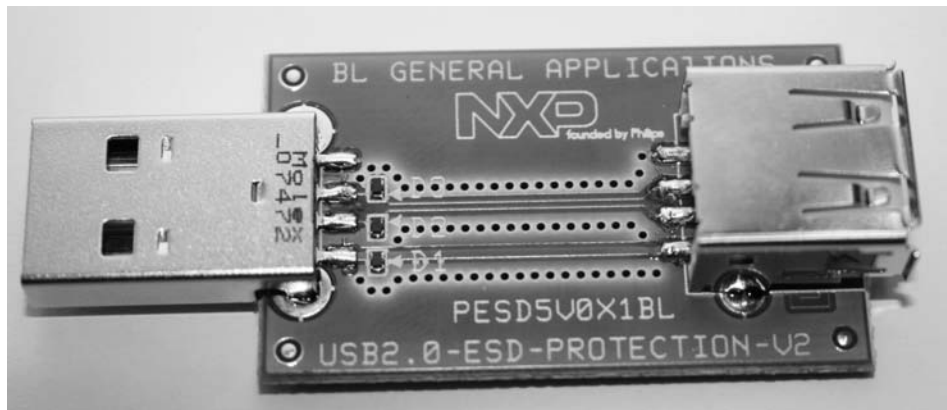
USB 2.0 signal mask specifications are provided by the USB Implementers Forum.

Figure 6 shows an “eye pattern” with the critical issues of a USB 2.0 data signal.



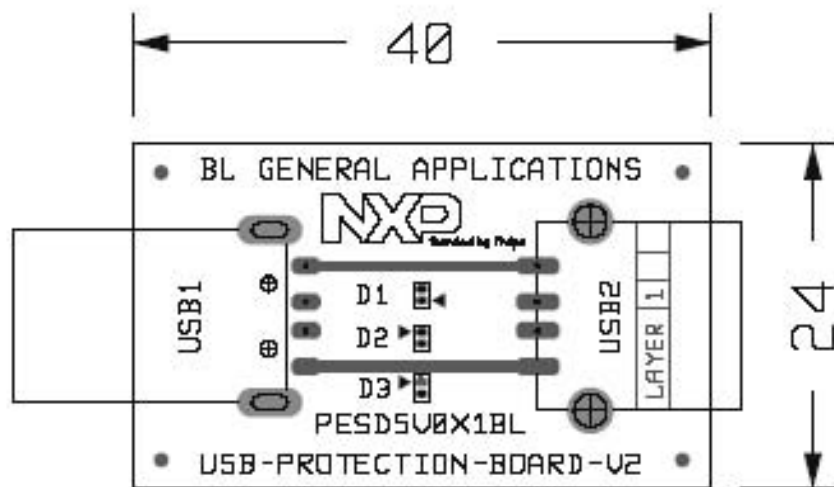
### 4. Measurement methods

To evaluate the PESD5V0X1BL behavior in USB 2.0 applications, a reference board (see [Figure 7](#)) was designed.



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Fig 7. USB 2.0-ESD-Protection-V2-board

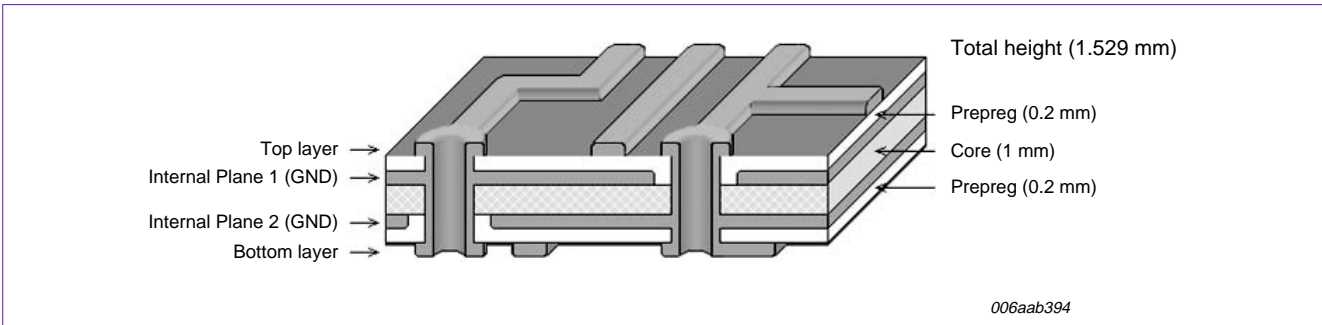


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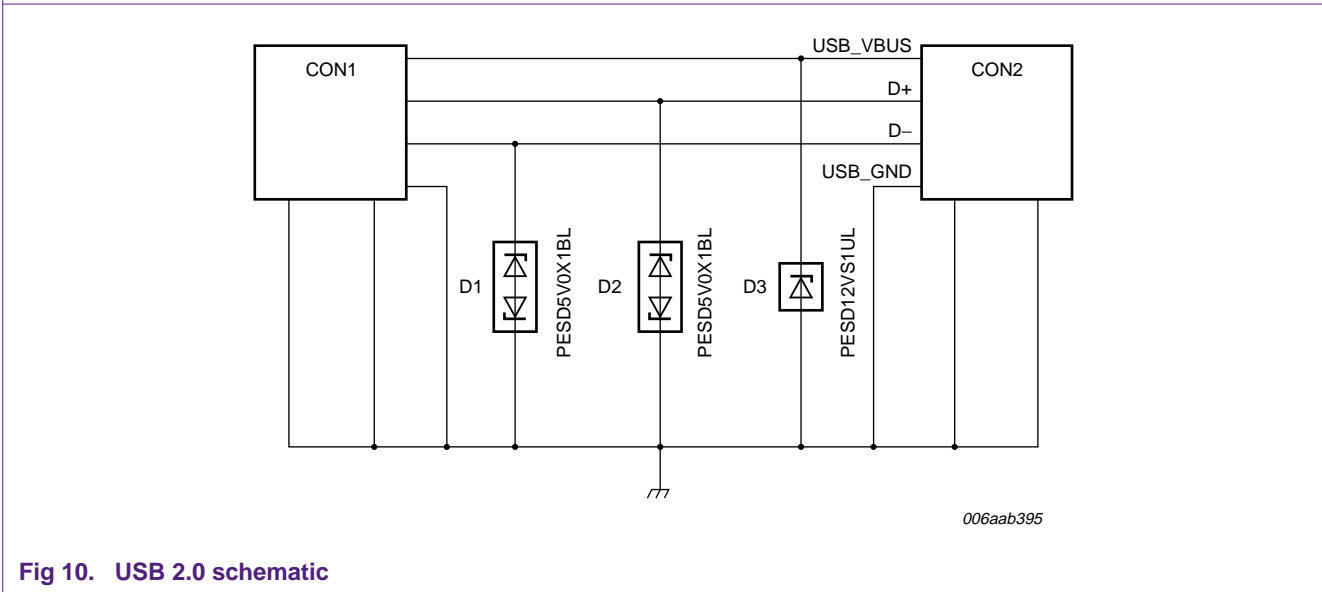
Fig 8. USB 2.0-ESD-Protection-V2-assembly diagram

An image of the PCB layer structure having two controlled impedance lines is shown in [Figure 9](#).

[Figure 10](#) provides the schematic of the demo board using PESD5V0X1BL for D1 and D2 each. In order to meet the USB charging requirements of even more than 5 V, there was a PESD12VS1UL chosen for D3.



**Fig 9. USB 2.0 PCB layer structure**



**Fig 10. USB 2.0 schematic**

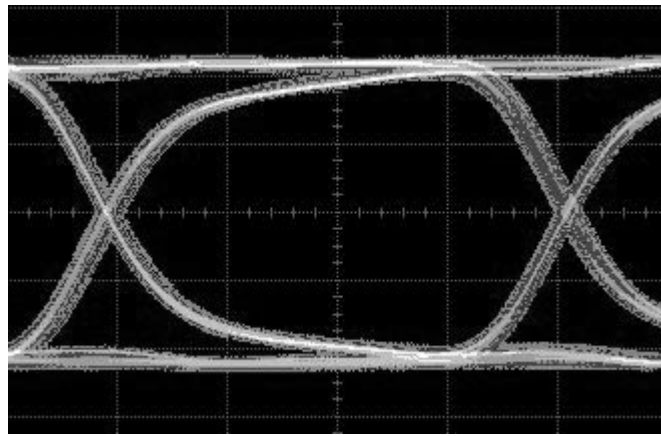
#### 4.1 Reference measurement

To evaluate the influence of different ESD protection components, the measurements were done in several steps.

A board without a device was evaluated as reference.

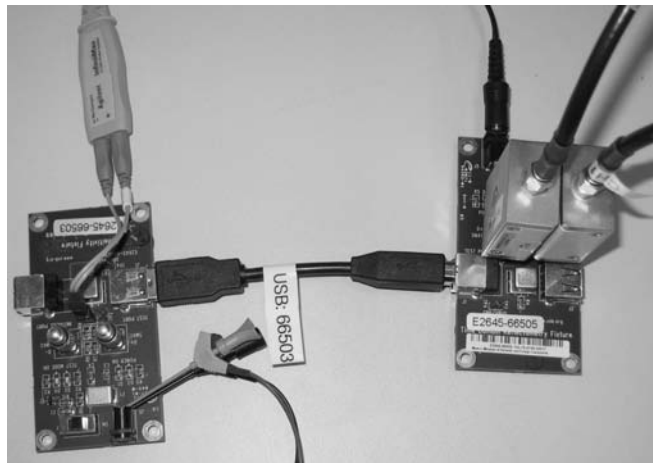
Comparing all “eye patterns” demonstrates the degradation caused by the ESD protection devices.

The first test was done without any protection diode (see [Figure 11](#)), the result pattern is shown in [Figure 13](#).



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Fig 11. USB 2.0 “eye pattern” without DUT

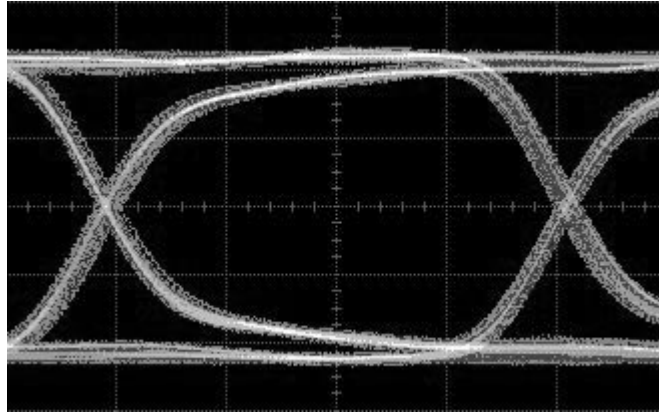


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Fig 12. Test setup for USB 2.0 “eye pattern” without DUT

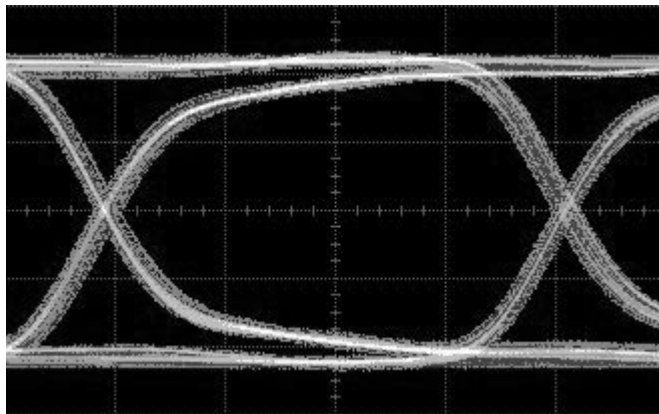
**4.2 DUT measurement**

The DUT measurements were done on three different PCBs using two different PESD5V0X1BL diodes each.



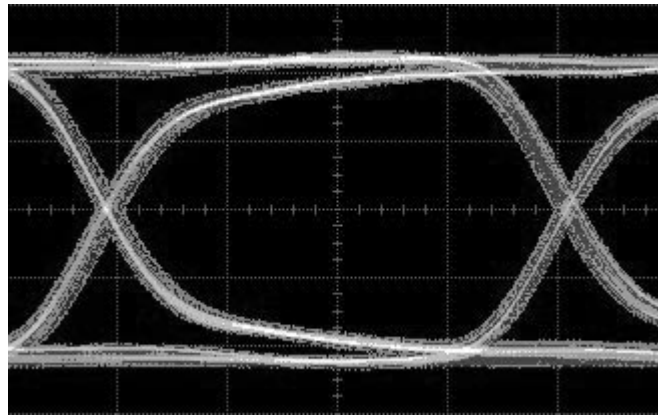
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**Fig 13. USB 2.0 “eye pattern” with a 0.9 pF PESD5V0X1BL ESD protection diode; PCB1**



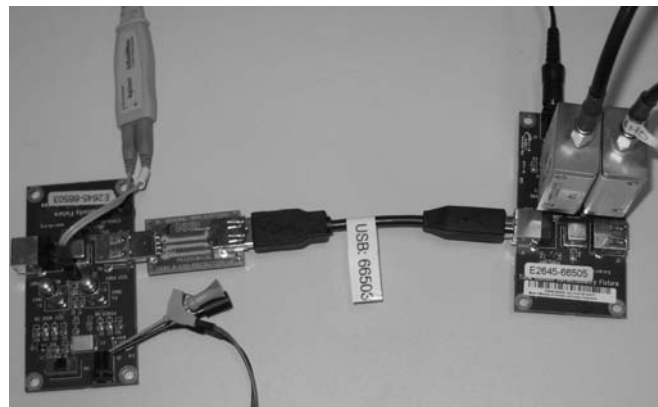
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**Fig 14. USB 2.0 “eye pattern” with a 0.9 pF PESD5V0X1BL ESD protection diode; PCB2**



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Fig 15. USB 2.0 “eye pattern” with a 0.9 pF PESD5V0X1BL ESD protection diode; PCB3



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Fig 16. Test setup for USB 2.0 “eye pattern” with a 0.9 pF PESD5V0X1BL ESD protection diode

## 5. Summary

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The NXP low-capacitance ESD protection devices offer best results for USB 2.0 hi-speed applications.

The “eye pattern” evaluations show that NXP’s low-capacitance ESD protection devices have an extremely low impact on the USB 2.0 data signals.

This option gives the hardware designer some space for additional capacitance on the USB 2.0 signal lines!

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