

# AN10790

## Greenchip TEA1742T PFC controller

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Application note

### Document information

Info	Content
<b>Keywords</b>	GreenChip, TEA1742T, PFC, high efficiency, dual boost, PC Power
<b>Abstract</b>	<p>The TEA1742T is a GreenChip PFC controller IC. Its quasi-resonant operation and dual boost option enable the design of a highly efficient PFC controller stage.</p> <p>The device can be used in all applications that require an efficient and cost-effective PFC solution up to 500 W. PC power supplies, in particular, can benefit from the high level of integration and high efficiency.</p>

## Revision history

Rev	Date	Description
01	20090209	First release

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## 1. Introduction

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The TEA1742T is a controller for Power Factor Correction (PFC). Its high level of integration allows the design of a cost-effective power supply with very few external components.

The built-in green functions provide high efficiency at all power levels. This applies to quasi-resonant operation at high power levels and quasi-resonant operation with valley skipping.

The TEA1742T makes it possible to design highly efficient and reliable supplies with power requirements up to 500 W and with the minimum number of external components.

The PFC output power is on-time controlled for simplicity. It is not necessary to sense the phase of the mains voltage.

The voltage and current levels listed in this application note are typical values. A detailed description of the pin level spreading can be found in the TEA1742T data sheet.

### 1.1 Scope of this application note

This application note describes the control functions of the TEA1742T and the adjustments needed within the power converter application.

### 1.2 The TEA1742T GreenChip PFC controller

The key features of the GreenChip PFC are summarized below. These features enable the power supply engineer to design a reliable switched mode power supply with highly efficient PFC control.

#### 1.2.1 Distinctive features

- Universal mains supply operation (70 V (AC) to 276 V (AC))
- Dual boost PFC with accurate output voltage (NXP patented)
- High level of integration, resulting in a very low external component count and a cost-effective design
- Low start-up supply voltage

#### 1.2.2 System features

- Safe restart mode for system fault conditions
- High ohmic resistive dividers possible to minimize losses
- Continuous mode protection by means of demagnetization detection (NXP patented)
- Wide  $V_{CC}$  range (38 V)
- MOSFET driver voltage limited
- Internal IC OverTemperature Protection (OTP)
- Open pin protection at pins VINSENSE and VOSENSE

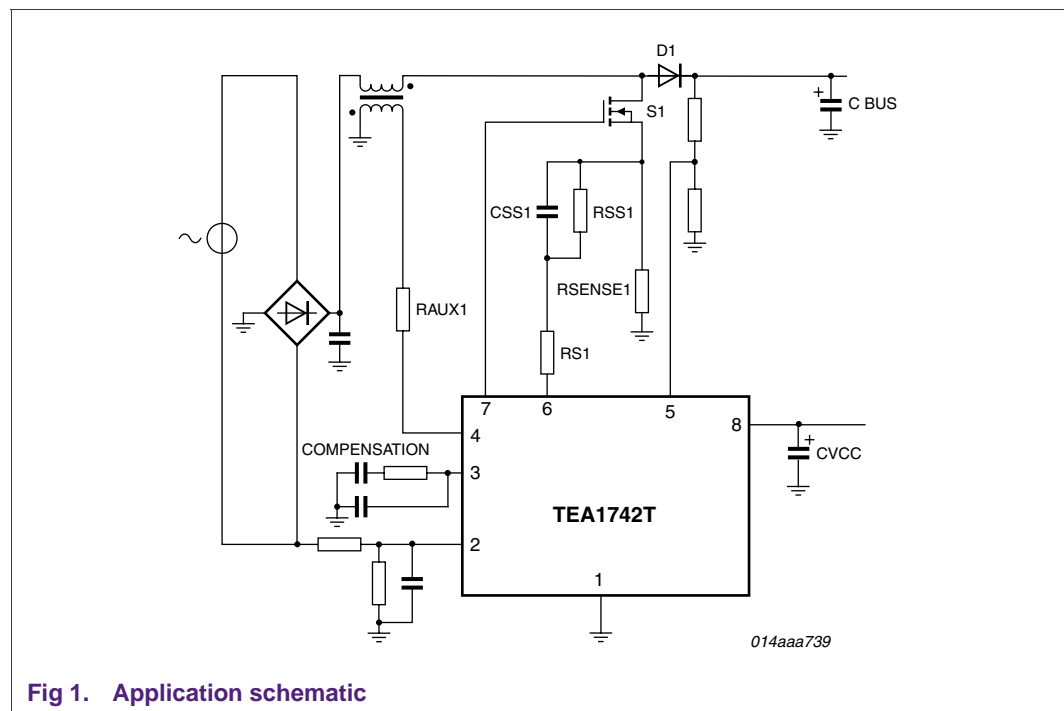
#### 1.2.3 PFC features

- Dual output voltage boost converter

- Quasi Resonant (QR)/ Discontinuous Conduction Mode (DCM) operation with valley switching
- Frequency limitation (125 kHz) to reduce switching losses and EMI
- T-on controlled
- Mains input voltage compensation for control loop for good transient response
- OverCurrent Protection (OCP)
- Soft start
- Open / short detection for PFC feedback loop; no external OverVoltage Protection (OVP) circuit necessary

### 1.3 Application schematic

[Figure 1](#) is a complete functional schematic of the TEA1742T application.



**Fig 1. Application schematic**

## 2. Pinning information

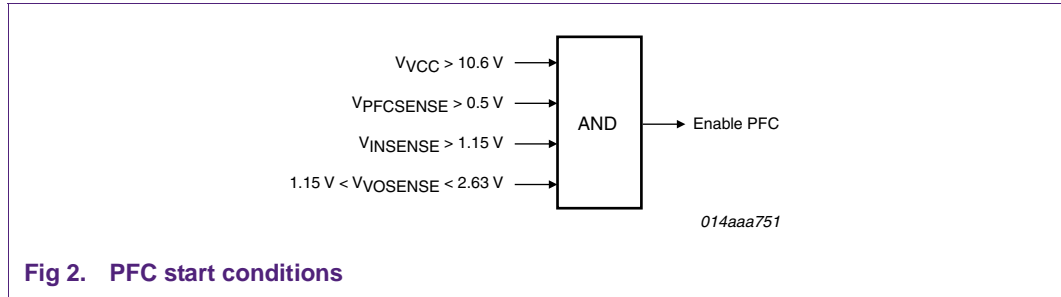
Table 1. Pin description

Pin	Name	Functional description
1	GND	Ground connection
2	VINSENSE	<p>Sense input for mains voltage</p> <p>This pin has 3 functions:</p> <ul style="list-style-type: none"> <li>• mains enable level: <math>V_{\text{start(VINSENSE)}} = 1.15 \text{ V}</math></li> <li>• mains stop level (brownout): <math>V_{\text{stop(VINSENSE)}} = 0.9 \text{ V}</math></li> <li>• mains-voltage compensation for the PFC control-loop gain bandwidth.</li> </ul> <p>The mains enable and mains stop levels will enable and disable the PFC. The voltage at the VINSENSE pin must be an averaged DC value, representing the AC line voltage. This pin is not used for sensing the phase of the mains voltage.</p>
3	PFCCOMP	Frequency compensation pin for the PFC control loop
4	PFC AUX	Input from an auxiliary winding of the PFC coil for demagnetization timing and valley detection to control PFC switching. The auxiliary winding needs to be connected via a 5 k $\Omega$ series resistor to prevent damage of the input due to lightning surges.
5	VOSENSE	<p>Sense input for PFC output voltage</p> <p>This pin has 3 functions:</p> <ul style="list-style-type: none"> <li>• pin VOSENSE short detection: <math>V_{\text{th(ol)(VOSENSE)}} = 1.15 \text{ V}</math></li> <li>• regulation of PFC output-voltage: <math>V_{\text{reg(VOSENSE)}} = 2.5 \text{ V}</math></li> <li>• PFC soft-OVP (cycle by cycle): <math>V_{\text{ovp(VOSENSE)}} = 2.63 \text{ V}</math></li> </ul>
6	PFCSENSE	<p>Overcurrent protection input for PFC</p> <p>This input is used to limit the maximum peak current in the PFC core. This is a cycle-by-cycle protection; at 0.5 V the PFC MOSFET is switched off.</p> <p>Internally, a 60 <math>\mu\text{A}</math> current source connected to the pin is controlled by the internal logic. This current source is used to implement soft-start and soft-stop functions for the PF to prevent audible noise in PFC burst mode. The pin is also used for enabling the PFC. The PFC will only start up when the internal current source is able to charge the soft-start capacitor to a voltage greater than 0.5 V; therefore a minimum soft start resistor of 12 k<math>\Omega</math> is required to guarantee enabling of the PFC.</p>
7	PFC DRIVER	Gate driver output for PFC MOSFET
8	V <sub>CC</sub>	<p>Supply voltage: <math>V_{\text{startup}} = 10.6 \text{ V}</math>, <math>V_{\text{th(UVLO)}} = 10.3 \text{ V}</math></p> <p>When the voltage on this pin exceeds the <math>V_{\text{startup}}</math> threshold, the control logic activates charging of the soft-start capacitor on the PFCSENSE pin. When this capacitor is charged to 0.5 V, the PFC circuit is activated. See <a href="#">Section 3.1</a> for a detailed description of the start-up sequence</p>

## 3. System description and calculations

### 3.1 PFC start conditions

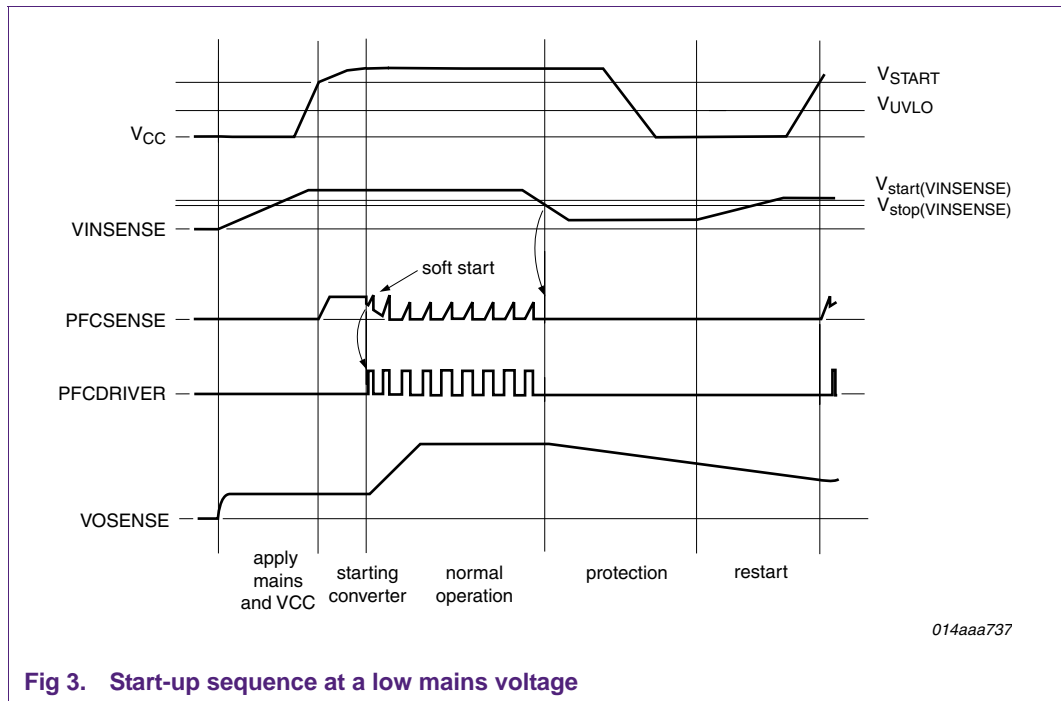
The conditions for enabling the PFC are detailed in [Figure 2](#). The supply for pin V<sub>CC</sub> should be provided by the main supply. In the event of start-up problems, these conditions can be checked to determine the cause of the problem. Some of the conditions are dynamic signals (see [Figure 3](#)) and should be checked using an oscilloscope.



### 3.2 Start-up sequence

When the mains voltage is applied, the TEA1742T power supply initiates the following start-up sequence (see [Figure 3](#)):

1. When the voltage on pin  $V_{CC}$  reaches 10.6 V ( $V_{startup}$ ), the soft start function at pin PFCSENSE is activated. An internal current source charges the external capacitor to 0.5 V ( $V_{start(soft)PFC}$ ).
2. When the voltage on pin VINSENSE reaches 1.15 V ( $V_{start(VINSENSE)}$ ), the PFC can start switching.
3. The voltage on pin VOSENSE must be between 1.15 V ( $V_{th(ol)(VOSENSE)}$ ) and 2.63 V ( $V_{ovp(VOSENSE)}$ ).  $V_{VOSENSE} < 1.5$  V indicates a short circuit;  $V_{VOSENSE} > 2.63$  V indicates either an overvoltage condition or the pin is open.



### 3.3 Mains voltage sensing and brownout

The mains input voltage is measured through pin VINSENSE. When pin VINSENSE has reached the  $V_{start(VINSENSE)}$  threshold of 1.15 V, the PFC can start switching, but only if the other start conditions have also been met (see [Section 3.1](#)). As soon as the voltage on pin VINSENSE drops below the  $V_{stop(VINSENSE)}$  threshold of 0.89 V, the PFC stops switching.

The voltage on pin VINSENSE must be an average DC value, representing the mains input voltage. Optimal performance is achieved with a time constant of approximately 150 ms at pin VINSENSE.

The long time constant at pin VINSENSE would prevent a fast restart of the PFC after a mains drop-out. To avoid this, the voltage on pin VINSENSE is clamped at 100 mV below the  $V_{start(VINSENSE)}$  threshold. This guarantees a fast PFC restart once the mains input voltage has recovered.

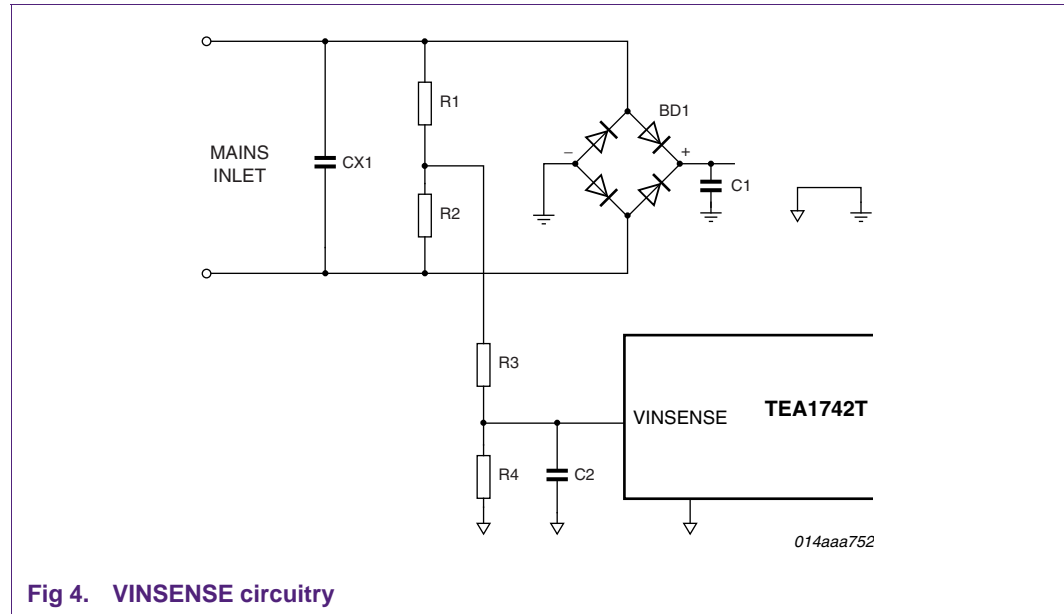


Fig 4. VINSENSE circuitry

### 3.3.1 Discharging the mains input capacitor

For safety, according to IEC-60950 chapter 2.1.1.7 "discharge of capacitors in equipment", the X-capacitors in the EMC input filtering must be discharged with a time constant  $\tau < 1$  s.

The R to discharge the X-cap in the input filtering is determined by the replacement value of  $R1 + R2$ .

In a typical 90 W adapter application with  $CX1 = 220$  nF, the replacement value of  $R1 + R2$  must be smaller than or equal to:

$$R_v \leq \frac{\tau}{C} = \frac{1}{220 \text{ nF}} = 4.55 \text{ M}\Omega \tag{1}$$

### 3.3.2 Brownout voltage adjustment

The rectified AC input voltage is measured via R1 and R2. The resistors alternately sense half the sine cycle, so they must be of the same value.

The average voltage sensed at the junction of R1 and R2 is:

$$V_{avg} = \frac{2 \times \sqrt{2}}{\pi} \times V_{acrms} \tag{2}$$

The brownout RMS AC voltage level is calculated as follows:

$$V_{brownout(AC)} = \frac{\pi}{2 \times \sqrt{2}} \times V_{stop(VINSENSE)} \times 2 \times \left( \frac{R1 \times R2}{R1 + R2} + R3 \right) \div I \tag{3}$$

where  $V_{stop(VINSENSE)} = 0.89 \text{ V}$ .

Example values for a brownout threshold of 68 V AC, and compliance with IEC-60950 are given in [Table 2](#).

**Table 2. VINSENSE component values**

Component values for R1, R2, R3 and R4 as a function of the value of CX1

CX1	R1	R2	R3	R4
220 nF	2 MΩ	2 MΩ	560 kΩ	47 kΩ
330 nF	1.5 MΩ	1.5 MΩ	820 kΩ	47 kΩ
470 nF	1 MΩ	1 MΩ	1.1 MΩ	47 kΩ

A value of 3.3 μF for capacitor C21 with R4 = 47 kΩ satisfies the recommended time constant requirement of  $\geq 150\text{ms}$  at pin VINSENSE.

### 3.4 Internal OTP

The IC employs internal temperature protection to protect the IC from overheating due to overloading at the V<sub>CC</sub> pin. When the junction temperature exceeds the thermal shutdown temperature, the IC will stop switching. OTP is a latched protection. It will be reset when the voltage on pin V<sub>CC</sub> is removed.

## 4. PFC description and calculation

The PFC operates in Quasi Resonant (QR) or Discontinuous Conduction Mode (DCM) with valley detection to minimize switch-on losses. The maximum switching frequency of the PFC is limited to 125 kHz to reduce switching losses. One or more valleys are skipped, when necessary, to keep the frequency below 125 kHz.

The PFC is designed as a dual boost converter with two output voltage levels that are dependent on the mains input voltage range. The advantage of such a dual boost is that overall system efficiency at low mains can be improved due to reduced PFC switching losses.

The dual output voltage is controlled through an internal 8 μA current source at pin VOSENSE (see [Figure 5](#)). The mains input voltage measured at pin VINSENSE is used to control the internal current source. This current source, in combination with the resistors at pin VOSENSE, sets the lower PFC output voltage. At high mains, the current source is switched off. Therefore, the maximum PFC output voltage is not affected by the accuracy of the current source. In a typical application with a PFC output voltage of 350 V (DC) at high mains, the PFC output voltage will be 270 V (DC) at low mains. A voltage of 2.2 V at pin VINSENSE corresponds with a mains input voltage of approximately 180 V (AC). The steep slope in the transfer function will ensure stable switch-over of the PFC output voltage without hiccups.

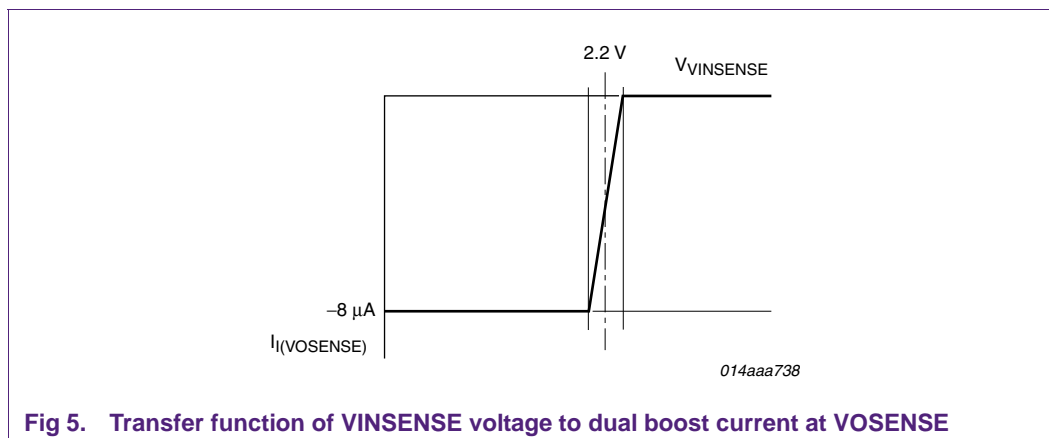


Fig 5. Transfer function of V\_INSENSE voltage to dual boost current at VOSENSE

#### 4.1 PFC output power and voltage control

The PFC is on-time controlled. Therefore, it is not necessary to measure the mains phase angle. The on time is held constant during the half sine wave to obtain a good power factor (PF), and class-D Mains Harmonics Reduction (MHR) according IEC61000-3-2.

The PFC output voltage is controlled through pin VOSENSE. At pin VOSENSE there is a trans-conductance error amplifier with a reference voltage of 2.5 V. The error at pin VOSENSE is converted with  $80 \mu\text{A} / \text{V}$  into a current at pin PFCCOMP. The voltage at PFCCOMP, in combination with the voltage at pin V\_INSENSE, determines the PFC on time.

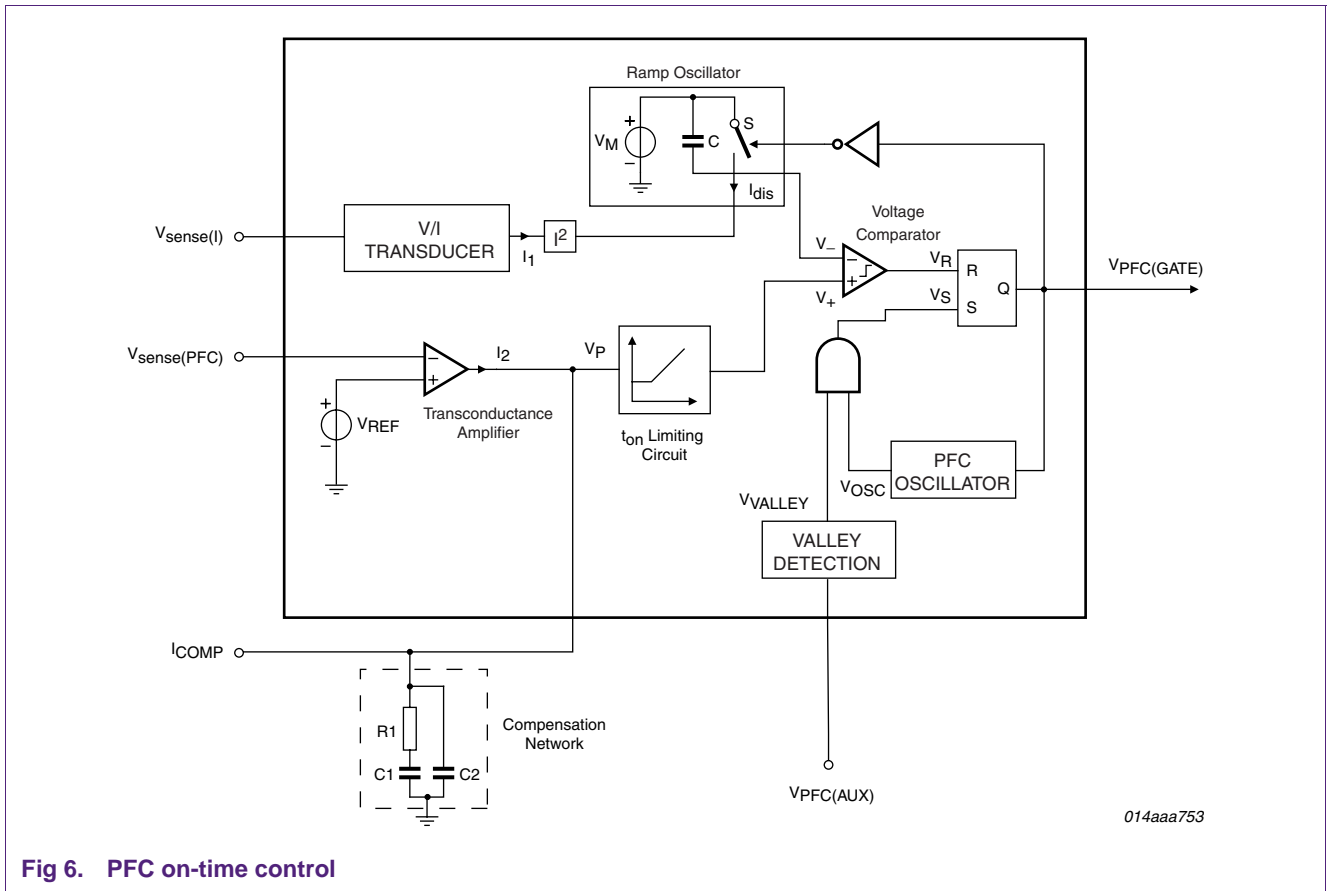


Fig 6. PFC on-time control

A compensation network consisting of a resistor and two capacitors is connected to pin PFCCOMP to stabilize the PFC control loop. The mathematical equation for the transfer function of a boost converter contains the square of the mains input voltage. In a typical application, this results in a low regulation bandwidth at low mains input voltages and a high regulation bandwidth at high mains input voltages. At high mains input voltages it can be difficult to meet class-D MHR requirements. The TEA1742T uses the mains input voltage measured at pin VINSENSE to compensate the control loop gain as a function of the mains input voltage. As a result, the gain will be constant over the entire mains input voltage range.

The voltage on pin VINSENSE must be an average DC value, representing the mains input voltage. Optimal performance is achieved with a time constant of approximately 150 ms at pin VINSENSE.

#### 4.1.1 Setting the PFC output voltage

A resistive divider connected between the PFC output and pin VOSENSE is used to set the PFC output voltage. In PFC normal mode, the PFC output voltage is regulated such that the voltage on the VOSENSE pin is equal to  $V_{reg(VOSENSE)} = 2.5 \text{ V}$ .

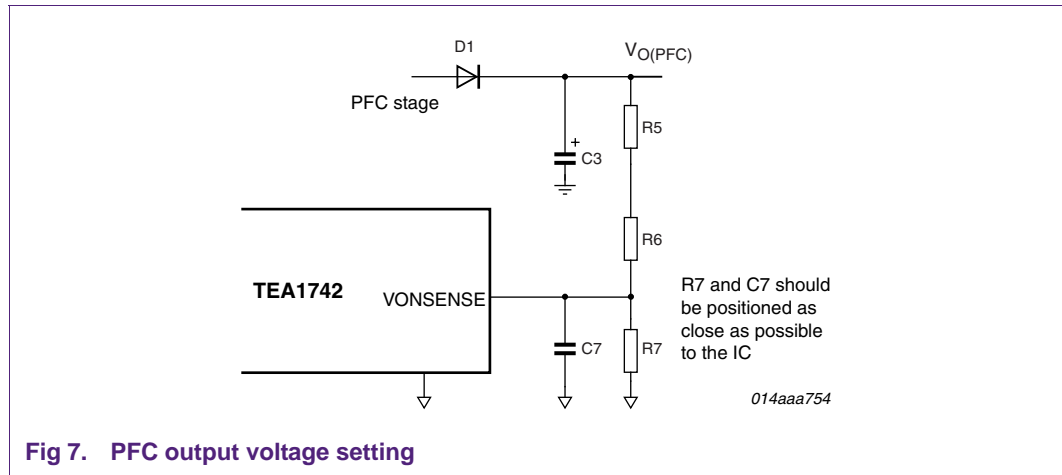


Fig 7. PFC output voltage setting

For low no-load input power, two 4.7 MΩ (1%) resistors can be connected between the bulk elcap and pin VOSENSE. The dimensioning of the  $I_{bst(dual)}$  current source ( $-8 \mu A$ ) has been adapted to these resistor values. With  $R5 = R6 = 4.7 M\Omega$  and  $R7 = 68 k\Omega$ , a typical supply application will have a PFC output voltage of approximately 345 V to 350 V at high mains and 270 V to 275 V at low mains.

The value of resistor R7 (1%), connected between pin VOSENSE and ground, can be calculated as follows:

$$R7 = \frac{(R5 + R6) \times V_{reg(VOSENSE)}}{V_{O(PFC)} - V_{reg(VOSENSE)}} \tag{4}$$

Suppose the regulated PFC output voltage is 348 V, then:

$$R7 = \frac{(4.7 M\Omega + 4.7 M\Omega) \times 2.5 V}{348 V - 2.5 V} = 68 k\Omega (1\%) \tag{5}$$

At low mains, the 8 μA current source  $I_{bst(dual)}$  is active. The lower PFC output voltage can be calculated as follows:

$$\left( V_{O(PFCLOW)} = \frac{R5 + R6 + R7}{R7} \right) \times (V_{reg(VOSENSE)} - I_{bst(dual)} \times R7) \tag{6}$$

With  $R5 = R6 = 4.7 M\Omega$  and  $R7 = 68 k\Omega$ , the lower PFC output voltage is:

$$V_{O(PFCLOW)} = \frac{4.7 M\Omega + 4.7 M\Omega + 68 k\Omega}{68 k\Omega} \times (2.5 V - 8 \mu A \times 68 k\Omega) = 272 V \tag{7}$$

The function of the capacitor (C7) at pin VOSENSE is to filter noise and to prevent false triggering of the protections due to MOSFET switching noise, mains-surge events or ESD events. False triggering of the  $V_{OVP(VOSENSE)}$  protection can cause audible noise and disturbance of the AC mains input current. False triggering of the  $V_{th(ol)(VOSENSE)}$  protection will initiate a safe restart cycle. A time constant of between 500 ns and 1 ms at pin VOSENSE should be sufficient, so a value of 10 nF for C7 would be appropriate.

R7 and C7 should be placed as close as possible to the IC between pin VOSENSE and the IC ground pin.

#### 4.1.2 Voltage control loop compensation network

A compensation network consisting of a resistor and two capacitors is connected to pin PFCCOMP to stabilize the PFC control loop.

#### 4.1.3 Calculating the PFC soft start component values

The soft start is implemented through the RC network at pin PFCSENSE.

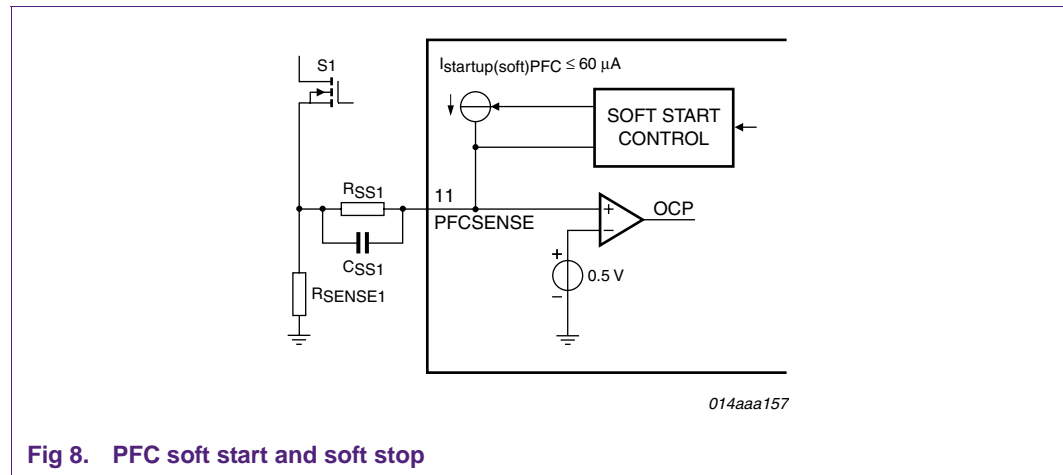


Fig 8. PFC soft start and soft stop

RSS1 must have a minimum value of 12 kΩ as specified ( $R_{\text{start(soft)PFC}}$ ). This is to ensure that the  $V_{\text{start(soft)PFC}}$  threshold of 0.5 V is reached to enable start-up of the PFC (see [Section 3.1](#)).

The total soft-start or soft-stop time is equal to:  $t_{\text{softstart}} = 3 \times RSS1 \times CSS1$ .

It is advisable to keep the PFC soft-start time within the range 2 ms to 5 ms.

With  $CSS1 = 100$  nF and  $RSS1 = 12$  kΩ, the total soft-start time will be 3.6 ms.

## 4.2 PFC demag and valley detection

The PFC MOSFET is switched on after the transformer has been demagnetized. Internal circuitry connected to the PFCAUX pin detects the end of the secondary stroke. It also detects the voltage across the PFC MOSFET. The next stroke is started if the voltage across the PFC MOSFET is at its minimum in order to reduce switching losses and ElectroMagnetic Interference (EMI) (valley switching).

The maximum switching frequency of the PFC is limited to 125 kHz ( $f_{\text{sw(PFC)max}}$ ) to minimize switching losses. One or more valleys are skipped, when necessary, to keep the frequency below 125 kHz.

If no demagnetization signal is detected on the PFCAUX pin, the controller generates a Zero Current Signal (ZCS) 50 ms after the last PFC gate signal.

If no valley signal is detected on the PFCAUX pin, the controller generates a valley signal 4 ms after demagnetization was detected.

To protect pin PFCAUX against electrical overstress, for example during lighting surge events, it is advisable to connect a 5 kΩ resistor (RAUX1; see [Figure 1](#)) between the PFC auxiliary winding and the pin. The resistor should be located close to the IC to avoid spurious PFC valley switching due to external disturbances.

For applications with high transformer ringing frequencies (after the secondary stroke), the PFCAUX pin should be connected to the auxiliary winding via a capacitor and a resistor to prevent incorrect skipping of valleys. In such cases, a diode, with a 1 MΩ resistor in parallel, must be connected between pin PFCAUX and ground.

#### 4.2.1 Designing the PFCAUX winding and circuit

To guarantee valley detection at low ringing amplitudes, the voltage at the PFCAUX pin should be set as high as possible, taking into account its absolute maximum rating of ±25 V.

The number of turns in the PFCAUX winding can be calculated using the following equation:

$$N_{a\_max} = \frac{V_{PFCaux}}{V_{Lmax}} \times N_p = \frac{25 \text{ V}}{V_{Lmax}} \times N_p \quad (8)$$

where:

$V_{PCFaux}$  = absolute maximum rating of the PFCAUX pin

$V_{Lmax}$  = the maximum voltage across the PFC primary winding

The PFC output voltage at the PFC OVP level determines the maximum voltage across the primary winding and can be calculated using the following equation:

$$V_{Lmax} = \frac{V_{ovp(VOSENSE)}}{V_{reg(VOSENSE)}} \times V_{O(PFC)} = \frac{2.63 \text{ V}}{2.5 \text{ V}} \times V_{O(PFC)} \quad (9)$$

When a PFC coil with a higher number of auxiliary turns is used, then a resistive voltage divider can be placed between the auxiliary winding and pin PFCAUX. The total resistance of the divider should be less than 10 kΩ to avoid delaying valley detection due to parasitic capacitance.

The polarity of the signal at the PFCAUX pin must be reversed compared to the PFC MOSFET drain signal.

To protect pin PFCAUX against electrical overstress, for example during lighting surge events, it is advised to connect a 5 kΩ resistor (RAUX1; see [Figure 1](#)) between the PFC auxiliary winding and the pin. The resistor should be located close to the IC to avoid spurious PFC valley switching due to external disturbances.

### 4.3 PFC protection

#### 4.3.1 VOSENSE OverVoltage Protection (OVP)

At start-up, a voltage overshoot can occur at the boost elcap. This overshoot is caused by the relatively slow response of the PFC control loop. The PFC control loop response must be relatively slow to guarantee a good power factor and to satisfy MHR requirements. The OVP at pin VOSENSE will limit the overshoot. The PFC MOSFET will be switched off as

soon as the  $V_{ovp(VOSENSE)}$  threshold of 2.63 V is reached, regardless of the on time setting. Switching of the MOSFET remains blocked until the voltage on pin VOSENSE drops below 2.63 V again.

OVP will also be triggered in the event of an open circuit between pin VOSENSE and ground.

The peak voltage at the boost elcap, generated by the PFC due to an overshoot and limited by the PFC OVP, can be calculated using the following equation:

$$V_{O(PFC\_PEAK)} = \frac{V_{ovp(VOSENSE)}}{V_{reg(VOSENSE)}} \times V_{O(PFC\_NOMINAL)} = \frac{2.63 \text{ V}}{2.5 \text{ V}} \times V_{O(PFC\_NOMINAL)} \quad (10)$$

### 4.3.2 VOSENSE open and short circuit detection

The VOSENSE pin, which senses the PFC output voltage, contains integrated protection circuitry designed to detect open and short circuits on the pin. The pin can also sense if one of the resistors in the voltage divider is open. Therefore the VOSENSE pin is completely fail-safe. It is not necessary to add an external OVP circuit for the PFC. An internal current source will pull the pin down below the  $V_{th(ol)(VOSENSE)}$  detection threshold of 1.15 V when the pin is open.

### 4.3.3 VINSENSE open circuit detection

The VINSENSE pin, which senses the mains input voltage, contains integrated protection circuitry designed to detect an open circuit on the pin. An internal current source will pull the pin down below the  $V_{stop(VINSENSE)}$  detection threshold of 0.9 V when the pin is open.

### 4.3.4 OverCurrent Protection (OCP)

OCP limits the maximum current through the PFC MOSFET and PFC coil. The current is measured via a current sense resistor in series with the MOSFET source. The MOSFET is switched off as soon as the voltage on pin PFCSENSE exceeds the  $V_{sense(PFC)max}$  threshold of 0.52 V. The OCP is a switching-cycle-by-switching-cycle protection.

To avoid false triggering of the PFC OCP by switching of the flyback, it is advised to allow a margin of 0.1 V. False triggering of the  $V_{ovp(VOSENSE)}$  protection can cause disturbance of the AC mains input current. Furthermore, it is advised to connect a small capacitor of between 100 pF and 220 pF direct to pin PFCSENSE to suppress external disturbances.

The value of the current sense resistor can be calculated using the following equation:

$$R_{OCP(PFC)} = \frac{V_{sense(PFC)max} - V_{margin}}{I_{M(PFC)max}} = \frac{0.52 \text{ V} - 0.1 \text{ V}}{I_{M(PFC)max}} \quad (11)$$

where:

$I_{M(PFC)max}$  = the maximum PFC peak current at high load and low mains.

For the PFC operating in Quasi Resonant mode the maximum peak current can be calculated using the following equation:

$$I_{QRM(PFC)max} = \frac{2\sqrt{2} \times P_{i(max)} \times 1.1}{V_{min(AC)}} = \frac{2\sqrt{2} \times \frac{P_{o(max)}}{\eta} \times 1.1}{V_{min(AC)}} \quad (12)$$

where:

$P_{o(max)}$  = is the maximum output power of the flyback

1.1 = a factor to compensate for the dead time between zero current in the PFC inductor at the end of the secondary stroke and the detection of the first valley in QR mode

$\eta$  = is the expected efficiency of the total converter at maximum output power

$V_{min(AC)}$  = minimum mains voltage (AC).

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

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