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JESD204A: New serialization technique for high speed data converters

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Document information

Info	Content
Keywords	JESD204A, Data Converters, Data rate, EMC, EMI

Abstract	This document gives a high level description of the JESD204A serialization standard for data converters and the various advantages which are associated to it.

founded by Philips

Revision history

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1. Introduction

For years the sample rates of data converters have been rising progressively to make room for applications using increased bandwidths, like telecommunication products, medical products, instrumentation, and industrial products. Moreover, integration capabilities of advanced CMOS technologies have made digitization affordable. Therefore digitizing as early as possible in the signal chain and thus benefitting from complex digital signal processing techniques does have many advantages. This has motivated the development of high speed data converters with data rates, which are higher than 100 Msps and with resolutions ranging from 10 bits to 16 bits.

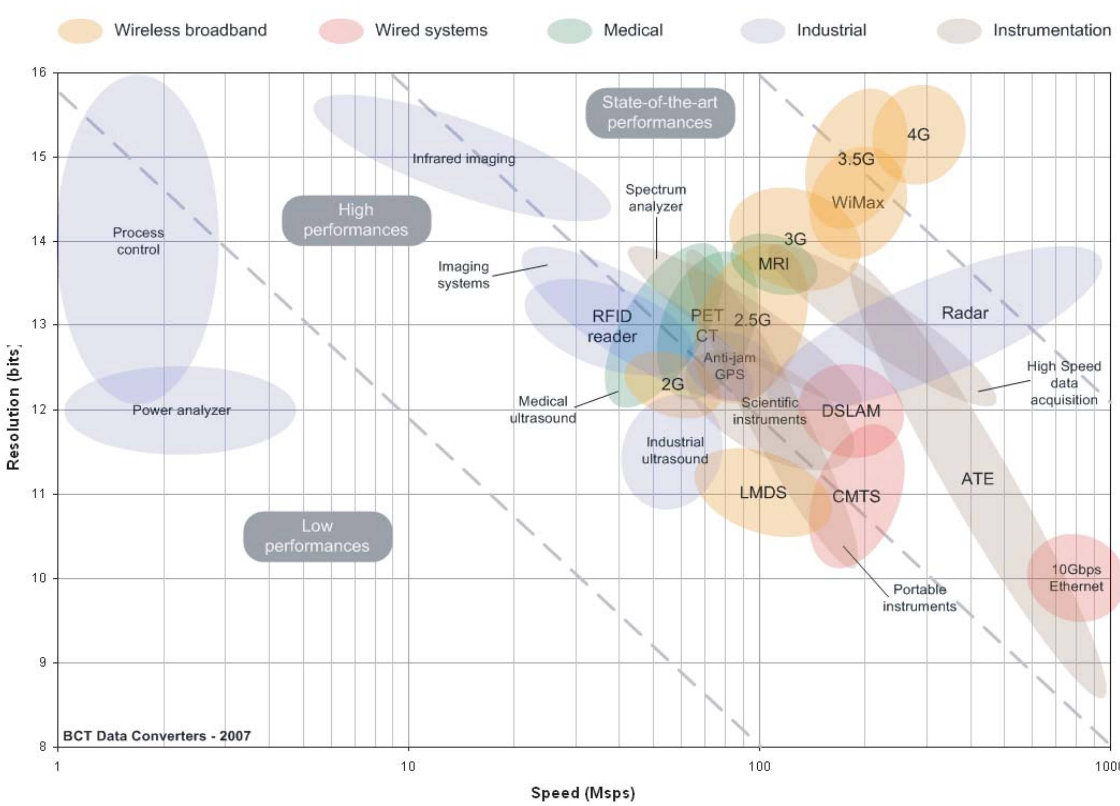

Fig 1. Distribution of applications with respect to resolution and speed

Another trend that can be seen is the complexity of the applications, which integrate Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC). Base-stations as wireless communication systems are a good example. The stringent demands related to the quality of the transceiver, the non-linearity specifications, the adjacent channels rejection capabilities, and the increasing demand in bandwidth has led to transceiver architectures integrating at least three ADCs and DACs, with a high data rate, high bandwidth and state of the art dynamic performances.

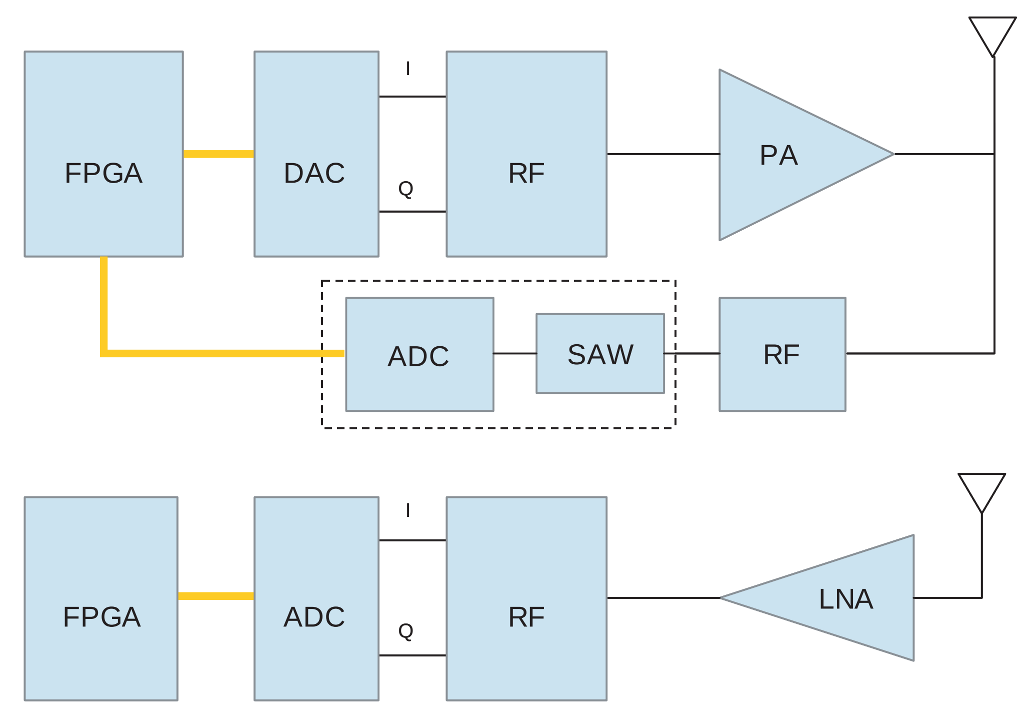

Fig 2. Transceiver system with 3 data converter devices with pre-distortion return path

System integrators have long had issues with e.g. signal integrity, Printed Circuit Board (PCB) layout, ElectroMagnetic Compatibility (EMC) and ElectroMagnetic Interference (EMI). These issues come with fast switching signals which, in their most basic form, are the signals that one can find on the input side of a DAC and the output side of an ADC. Communication and interfacing standards between various devices on the same PCB have been established to guarantee, first and foremost, signal integrity.

2. JESD204A: Serial interface

The JESD204A is a serial interface standard dedicated to data converters. It has been built by all the major stakeholders in the industry, involving System integrators, IC suppliers (including NXP Semiconductors) and Field Programmable Gate Array (FPGA) makers. This ecosystem is very useful as it allows easy interoperability between IC providers and FPGA makers.

Its main purpose is to simplify PCB design and allow for long distance transmissions.

The added value of the JESD204A over the JESD204 is that it is now possible to have multiple devices connected through multiple lanes, which is highly beneficial for achieving high data rates.

The JESD204A has the major advantage of capitalizing on previous serialization techniques and standards. For example, it consists of well known blocks, such as an 8B/10B coding, which is widely used in the industry and has a proven robustness.

The signaling defined in the JESD204A specification is low swing, differential, and suitable for low-voltage IC technologies. Current Mode Logic (CML) is typically used for the serial interface as it has the benefit of working at very high frequencies (from DC to > 3 Gbps). CML provides an 800 mV swing in certain implementations with the possibility to control the level of the output swing. The 800 mV may be adjustable down to a few hundred millivolts to minimize crosstalk. CML is for point-to-point links only and provides matched source and load terminations. This greatly simplifies the interconnections and stub lengths (termination to RX input) are minimized, optimizing the signal quality. Because one side is pulled to the rail, both the driver and the receiver should be powered from the same supply potential for DC coupled applications. This is one of the reasons that AC coupling is popular with CML interfaces. It provides common-mode tolerance, fault protection, and also supply independency.

2.1 Easy PCB design and flexibility

Complex systems require intricate PCB design with multiple metal layers. Figure 2 shows a telecommunication system that contains three data converter components. If each of these has a 12-bit resolution, a total of 36 traces are required for the data routing.

With the JESD204A, given a certain maximum speed, only one pair of differential lanes is required per data converter, which means a grand total of 6 traces when we have three data converters. This reduces the complexity of the PCB routing. A smaller board size can be used, which reduces the overall cost.

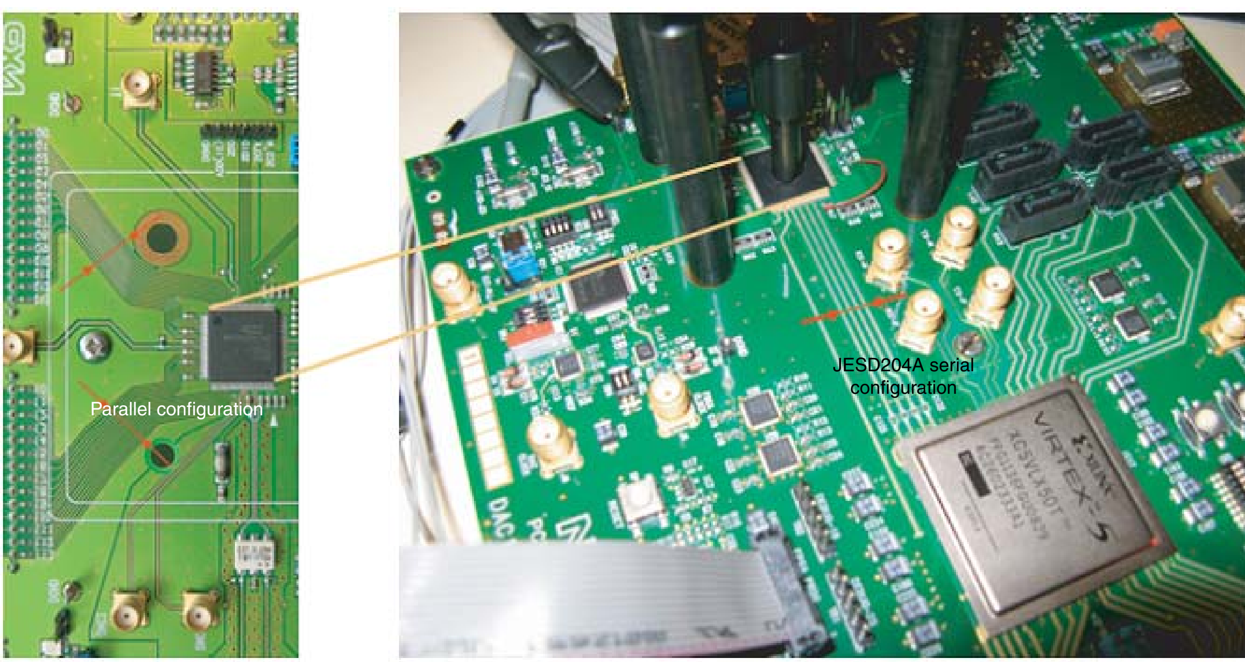

Fig 3. PCB optimization with the JESD204A

Moreover, an FPGA can be directly linked to multiple devices and occupying only a few I/Os on the logic device. This in it itself is extremely helpful because a change of device, for example, from a 12b to a 14b ADC, only needs a new reconfiguration file to reprogram the FPGA and not a total redesign of the board. For this reason there is a drastic reduction in costs and a lot of flexibility for the designers.

2.2 Electromagnetic interference, electromagnetic compatibility and speed

When a current flows in a conductor it results in a magnetic field at a certain distance, which is proportional to the intensity of the current and inversely proportional to the distance. When data is sent in parallel on the PCB, it creates large magnetic fields depending on the geographical situation. This can cause problems for the other blocks on the circuit board. A differential signal can help in reducing this effect. Indeed, if we consider the simplest differential signal, a current flowing from a supply route to a ground route, one can easily see that in the ground route, the current is in the opposite direction to the supply route. Both currents will result in a magnetic field, but as the currents are flowing in opposite directions, at a distance r, the magnetic field is cancelled. The same reasoning is valid for a switching current. As long as the signals are differential and routed closely, the magnetic field is extremely low.

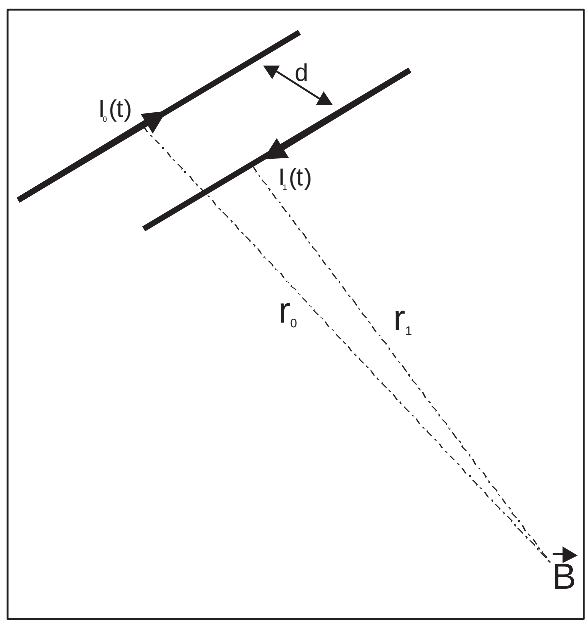

Fig 4. Far field electromagnetic coupling at one point in space

$$\vec{B} = \left(\frac{\mu_0 I_0(t)}{2\pi r_0} + \frac{\mu_0 I_1(t)}{2\pi r_1}\right)\vec{e_\varphi} \quad (1)$$

Remark: For a differential signal: $I_0(t) = -I_1(t)$.

If r_0 and r_1 >> d, then $r_0 = r_1 = r$ and:

$$\vec{B} = \left(\frac{\mu_0 I_0(t)}{2\pi r} - \frac{\mu_0 I_1(t)}{2\pi r}\right)\vec{e_\varphi} = 0 \quad (2)$$

JESD204A uses differential signals for the data. Therefore the Electromagnetic coupling and problems to other blocks are greatly decreased. In the same way, a differential signal is highly immune to EM coupling from other blocks.

Remark: The same thing applies to the supply routing. Due to its differential nature, the current flow in the supply routes of the IO drivers is nearly constant. In this way there are fewer problems.

To further decrease the chance of creating spurious, spur mitigation techniques are used in the digital processing. Considering an ADC, a highly sequential series of '0' and '1' is present at the output, creating a high frequency signal. This can result in spurs in the wanted domain through coupling mechanisms, which will degrade the overall performance of the ADC. To avoid this, a 'scrambler' is implemented in the JESD204A system.

The scrambler is a randomizing mechanism that is used to eliminate strings of consecutive identical transmitted symbols and to avoid the presence of tones in the signal spectrum without changing the signaling rate.

2.3 Synchronization, clock recovery and error detection

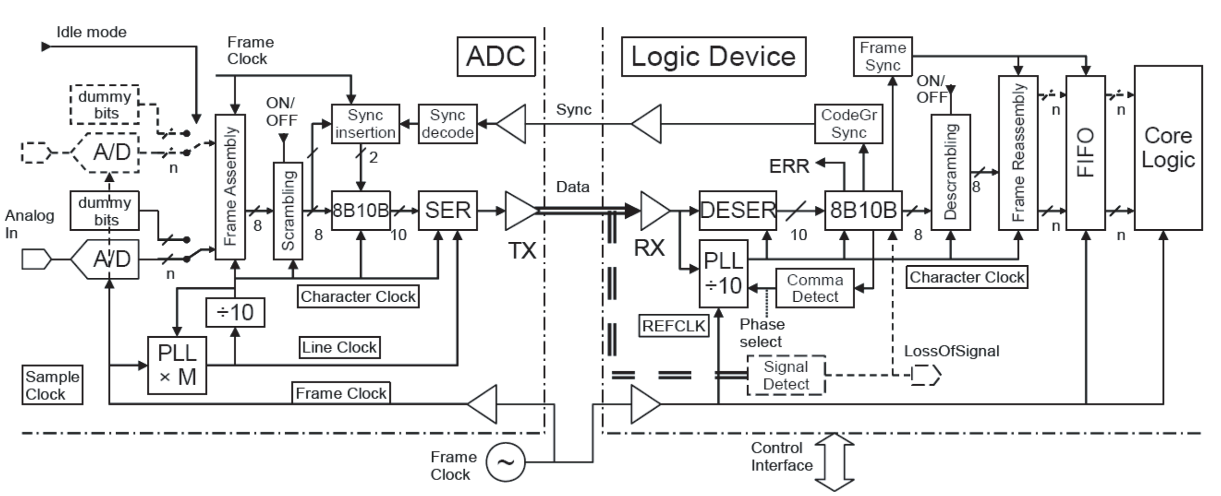

Fig 5. System description of the JESD204A with clock distribution

All clocks are based on the frame clock, which is the absolute timing reference in the JESD204A system. It is a relatively low frequency clock which is also the sampling clock of the ADC or the DAC. It is therefore distributed as a separate signal and supplied to all transmitter and receiver devices in the pipe.

In the JESD204A the transmitter and the receiver first have to synchronize through the SYNC interface. This interface is used as a time-critical return path from the receiver(s) to the transmitter(s). It is synchronous with the frame clock input of the devices.

The JESD204A data interface guarantees the synchronization between different devices. This allows for good matching between data lanes, which is very benificial for the interoperability between FPGA vendors.

As mentioned in Section 2 an 8b/10b coding is used to encode data before transmission. The 8B/10B codes have the following properties:

- Sufficient bit transition density (3 to 8 transitions per 10-bit symbol) to allow clock recovery by the receiver.
- Control symbols that are used:
  - To establish receiver synchronization to the symbol boundaries
  - To mark the start and end of frames or other sequences of data without impacting the bandwidth of the signal
  - To enable alignment between serial lanes
- Detection of errors

3. Conclusion

The JESD204A standard has many improvements and advantages:

- Reduced system cost
- Reduced system size; easy PCB design
- Synchronization of multiple lanes
- Capability to connect multiple converter devices to a single logic device
- Long distance transmission
- High flexibility and scalability
- High signal integrity and error detection
- No clock propagation

Table 1 gives a comparison of the JESD204A with its main competitors and the benefits that come along with this standard.

Table 1. Comparative table summarizing the advantages of JESD204A

Data rate	Parallel 200 Msps	Serial LVDS 150 Msps	JESD204A 320 Msps
PCB area saving	-	+	++
Customer PCB design effort	-- Managing inter traces skew and timing requirement versus clock required.	+ Complying to timing requirement versus clock required.	++ No need to manage inter lanes skew Multiple converters can be transmitted over a small number of lanes.
EMI/EMC (signal integrity)	--	-	++
Distance between ADC/DAC and FPGA	-- No guarantee (less than 4 cm)	-- No guarantee (less than 4 cm)	++ Guaranteed up to 20 cm
Multiple converter synchronization	-	-	++
Error detection	- No	- No	++ Yes
Radio system cost	-- Costly	+ (reduced number of FPGAs - cheaper)	+ (reduced number of FPGAs - cheaper)
Flexible/scalable configuration	-- No (new PCB design required)	++ 10/12/14/16 bits	++ 10/12/14/16 bits

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5. Contents

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