

AN10830

Interconnection between JESD204A compliant devices

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Application note

Document information

| Info | Content |
|-----------------|--|
| Keywords | JESD204A, Data Converters, CML, LVDS, Jitter, coupling |
| Abstract | This document relates to the interconnections that are required between the data converter device and the logic device for a JESD204A standard compliant system. It also depicts the types of interface that are necessary for the various signals |

Revision history

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1. Introduction

The JESD204A is a serial interface standard dedicated to data converters. It has been defined by all the major stakeholders in the industry, involving System integrators, IC suppliers (including NXP Semiconductors) and Field Programmable Gate Array (FPGA) makers. This ecosystem is very useful as it allows easy inter-operability between IC providers and FPGA makers.

Its main purpose is to simplify PCB design and allow for longer transmissions with guaranteed integrity.

NXP semiconductors offer the following parts, which are JESD204A compliant, as part of its portfolio:

- DAC1408D650 14-bit DAC, JESD204A compliant, 650 Msp/s maximum output rate (see for more information the data sheet for this product)
- ADC1413D 14-bit ADC, JESD204A compliant, $f_s = 125$ Msp/s, 105 Msp/s, 80 Msp/s and 65 Msp/s (see for more information the data sheet for this product)
- ADC1213D 12-bit ADC, JESD204A compliant, $f_s = 125$ Msp/s, 105 Msp/s, 80 Msp/s and 65 Msp/s (see for more information the data sheet for this product)

Xilinx Virtex5 documentation is available from: <http://www.xilinx.com/>. Documents of interest are ug196 (*Virtex-5 FPGA RocketIO GTP Transceiver*) and ds202 (*Virtex-5 FPGA Data Sheet: DC and Switching Characteristics*). This application note does not intend to replace these.

JESD204A has been issued by the JEDEC committee. This specification can be downloaded from <http://www.jedec.org/> website. NXP also provides an application note (*AN10812_1, JESD204A: New serialization technique for high speed data converters*) to give customer sufficient background on that standard.

2. Efficiently connecting NXP JESD204A DAC to Xilinx FPGA

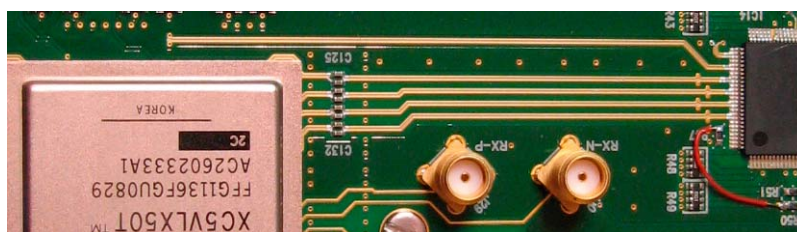


Fig 1. Lane interconnect example

JESD204A is a point to point protocol. There are three categories of connections:

- **Lanes:** those signals carry the data
- **SYNC:** This is a synchronization signal used at the beginning of the transmission. Later, it is used by the receiver to trigger loss of synchronization and requests re-initialization.
- **Frame clock:** this is the system clock

2.1 Virtex5 FPGA

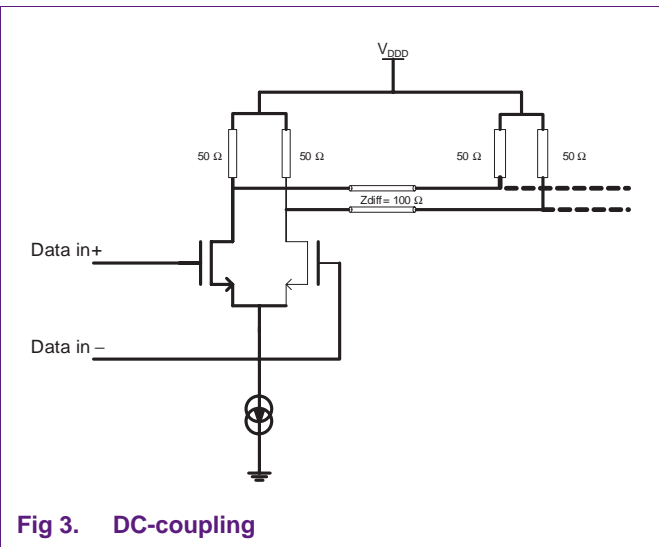
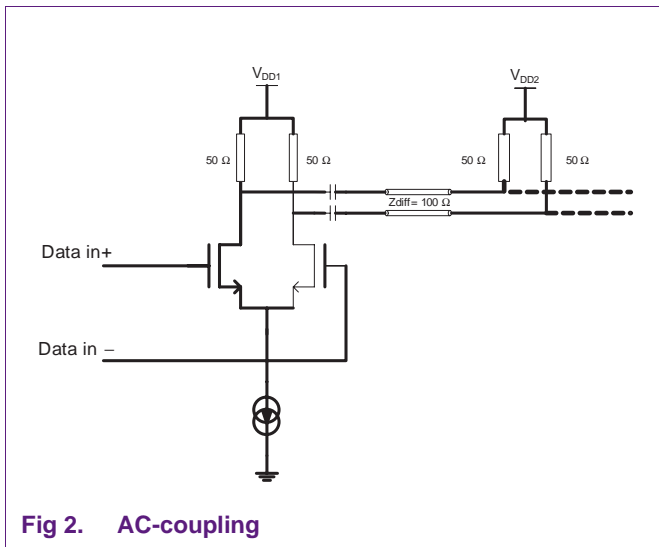
The key feature that these devices must have is a SerDes macro. It ensures the proper serialization/de-serialization of the data at very high speed. Moreover, they have extra features like Phase Locked Loops (PLL) running at very high frequencies (> Ghz) and hard wired 8b/10b coding/decoding.

In Xilinx terminology, these highly specialized macros are named GTP or GTX depending on their characteristics. The commercial name used is RocketIO. All Virtex5 devices which part number ends with a "T" have such transceivers (eg XC5VLX50T, XC5VFX70, etc.). GTP/GTX have a fixed location inside the FPGA. This is an important point for board design strategy.

2.2 Lanes

JESD204A specifies that the data link should be CML compliant. This implies current switching with positive supply, V_{DD} as reference. This also means that each lane is made up of a differential pair. Termination on both sides of the link is defined as being 50 Ω .

As V_{DD} is the reference, special care should be taken when the transmitter (FPGA here) and receiver (NXP DAC) have different supply voltages. This can lead to different common-mode voltages at each side, thus creating a potential difference. A situation like that must be avoided to prevent static current flowing from one device to the other. JESD204A has therefore introduced the concept of AC or DC coupling.



The AC coupling capacitor and the load resistors create a high pass filter. The value of the capacitor will determine the lower cut-off frequency of this first order filter. A 10 nF capacitor is sufficient to ensure correct AC coupling, as the cut-off frequency is at 0.3 MHz and is therefore not seen by the high frequency signals.

An example is: The NXP DAC1408D650 demo board. It features a DAC1408D650 and an XC5VLX50T. DAC1408D has a default common mode voltage of 800 mV. Virtex5 GTP has a common mode of 800 mV. So no capacitor is needed in that case. In any case, DAC1408D650 has a configurable common voltage and can cover a range from 700 mV to 1400 mV, if another device is used.

2.3 Frame clock

This clock has to be provided to the FPGA and to the data converter device. They must have the same frequency but the phase relationship can have any value (e.g. 180 °).

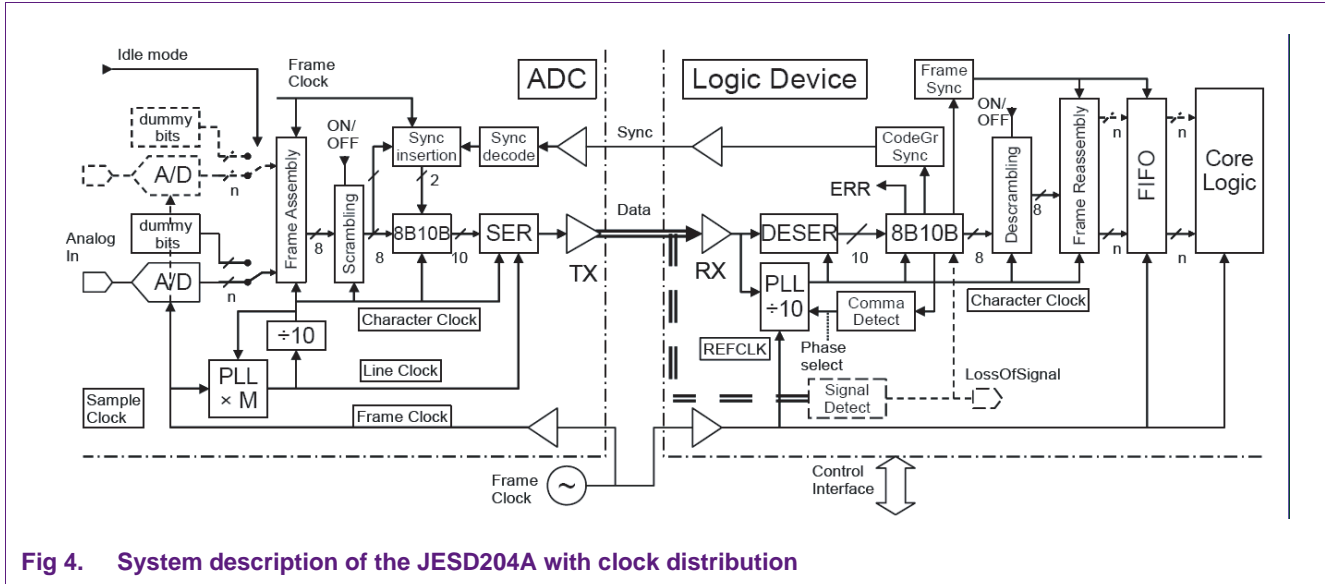


Fig 4. System description of the JESD204A with clock distribution

Remark: The ADC is a TX device as it does the serialization and then sends the data to the FPGA device which, when connected to an ADC, is an RX device. The DAC is an RX device and therefore the FPGA is the TX in this configuration. Therefore the FPGA can be both RX and TX, depending on whether it is connected to a DAC or an ADC.

2.3.1 RX clock input

The RX clock inputs should be driven with Low Voltage Differential Swing (LVDS) signals. A 100 Ω termination has to be implemented on the board close to the data converter device or the FPGA, to reduce parasitics. Good signal integrity is very important for this clock as a good data recovery can be achieved only if this clock is clean.

NXP DACs complies with IEEE1596.3-1996 specifications.

Table 1. IEEE1596.3-1996 receiver specifications

| Parameter | Description | Min | Max | Unit |
|--------------|--------------------------------------|------|------|------|
| V_i | input voltage | 825 | 1575 | mV |
| V_{idth} | input differential threshold voltage | -100 | +100 | mV |
| ΔZ_i | differential input impedance | 80 | 120 | Ω |

2.3.2 TX clock input

There are two ways to provide the clocks to a RocketIO macro:

- The global clock network
- The dedicated macro input

Xilinx recommends to use the latter for best jitter performances.

This dedicated input is differential. It is very similar to CML and is terminated by $50\ \Omega$ to a common-mode voltage. Therefore, driving these pins directly is only possible with a driver that has the same common-mode voltage. Else, bypass capacitors must be set up on the nets.

When a clock is provided to the ADC device, it should be in a suitable differential interface, LVDS, LVPECL, SINE or LVCMOS. It is the sampling clock and it will influence the quality of the ADC.

2.4 Layout

Two types of buses are required to interconnect your NXP JESD204A data converter device and a Virtex5:

- LVDS
- CML

2.4.1 LVDS routing

LVDS signaling has very fast edges. Therefore you should use differential routing with controlled impedance. Impedance discontinuities should be avoided as it creates high frequency spurs which can be coupled to the rest of the circuit, thus creating noise.

Target impedance is $100\ \Omega$ differential.

2.4.2 CML routing

The same layout constraints as for LVDS apply here. Target impedance is also $100\ \Omega$ differential.

To ease PCB routing, both the NXP JESD204A DAC and the Virtex5 FPGA have lane polarity swapping capability. Because of this the differential pairs can be routed in the most direct way possible, while the polarity issue can be dealt with very easily.

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