AN11066

SDARS active antenna 1st stage LNA with BFU730F, 2.33 GHz

Rev. 1 — 25 October 2011 Application note

Document information

Info	Content
Keywords	LNA, 2.33 GHz, BFU730F, SDARS.
Abstract	This document provides circuit, layout, BOM and performance information for 2.33 GHz LNA equipped with NXP Semiconductors BFU730F wide-band transistor.

Revision history

Rev	Date	Description
v.1	20111025	Initial version

Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

1. Introduction

The BFU730F is a wideband Silicon Germanium Amplifier transistor for high speed, low noise applications. It is used for LNA applications such as GPS, satellite radio, cordless phone and wireless LAN. The BFU730F comes in a SOT343F package that contains two emitter pins for improved grounding.

The BFU730F is ideal in all kinds of application where cost matters. It also provides the designer with increased flexibility.

BFU730F SiGeC low noise transistor is shown in Figure 1 in a Satellite Digital Audio Radio Service (SDARS) active antenna LNA application. It is intended for use as the first stage in a three stage SIRIUS LNA chain.

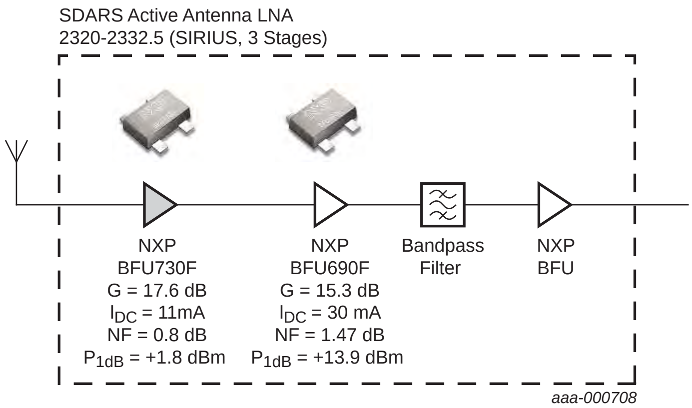
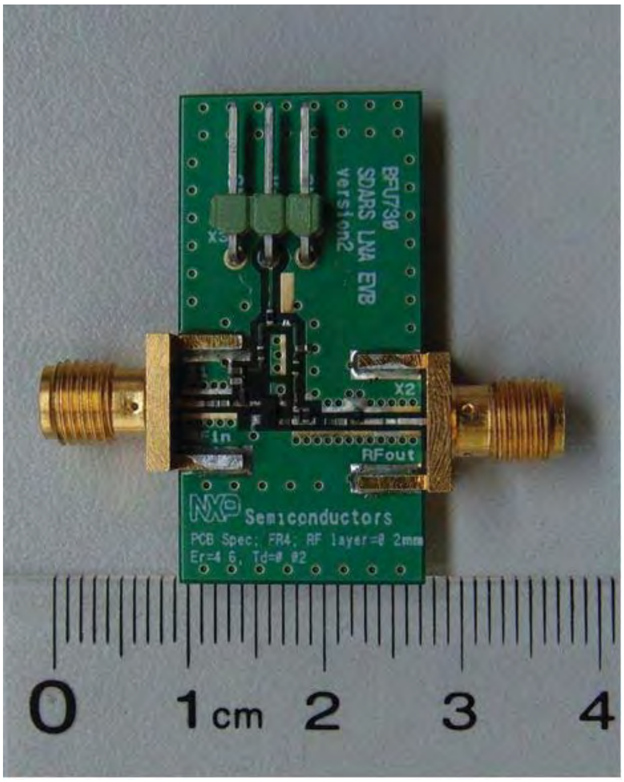


Fig 1. Overview of SDARS active antenna LNA

The 2.33 GHz LNA evaluation board (EVB) is designed to evaluate the performance of the BFU730F transistor applied as the first stage in a three stage SIRIUS LNA chain. This document provides an application diagram, board layout, bill of material, and some typical results.

Figure 2 depicts the evaluation board.



aaa-000709

Fig 2. BFU730F 2.33 GHz LNA evaluation board

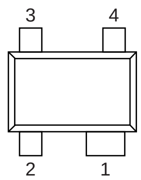
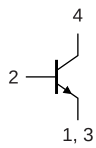
2. General description

The BFU730F is a discrete HBT produced in NXP Semiconductors SiGeC QuBIC4x BiCmos process. SiGeC is in principle a normal silicon germanium process with the addition of Carbon in the base layer of the NPN transistor. The presence of carbon in the base layer suppresses the boron diffusion during wafer processing. This process allows steeper and narrower SiGe HBT base and a heavier doped base. This results in lower base resistance, lower noise and higher cut-off frequency (higher gain). Table 1 provides a summary of the transistor performance in terms of noise and gain is shown.

Table 1. BFU730F values, measured at, 2 V, V_{ce} and 5 mA IC

Frequency (GHz)	Noise (dB)	Associated gain (dB)
1.5	0.50	25
1.8	0.50	23.5
2.4	0.55	21.5
5.8	0.80	15.0
12	1.30	11.0

Table 2. Pinning information

Pin	Description	Simplified outline	Graphic symbol
1	emitter		 mbb159
2	base		
3	emitter		
4	collector		

3. Application Board

The BFU730F 2.33 GHz EVB simplifies the evaluation of the BFU730F wideband transistor, for this frequency range. The EVB enables testing of the device performance and requires no additional support circuitry. The board is fully assembled with BFU730F, including input and output matching, to optimize the performance. The input match was a compromise between the best noise figure and a low input return loss. The board is mounted with signal input and output SMA connectors for connection to RF test equipment.

3.1 Application Circuit

Figure 3 provides the application diagram as supplied on the evaluation board.

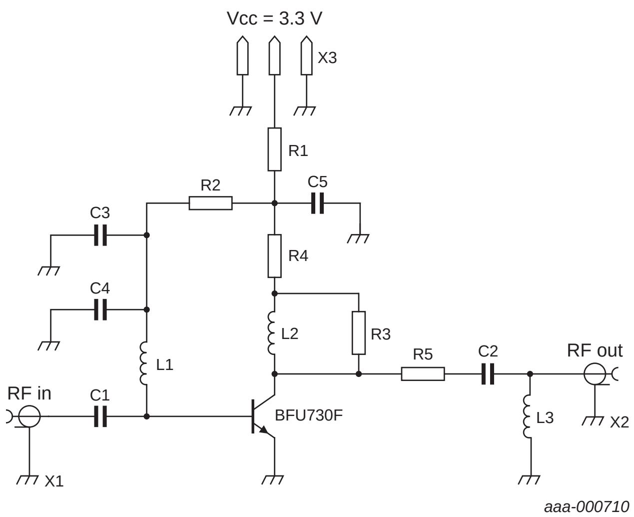


Fig 3. Circuit diagram of the evaluation board

3.2 Board Layout

Figure 3 shows the board layout including components.

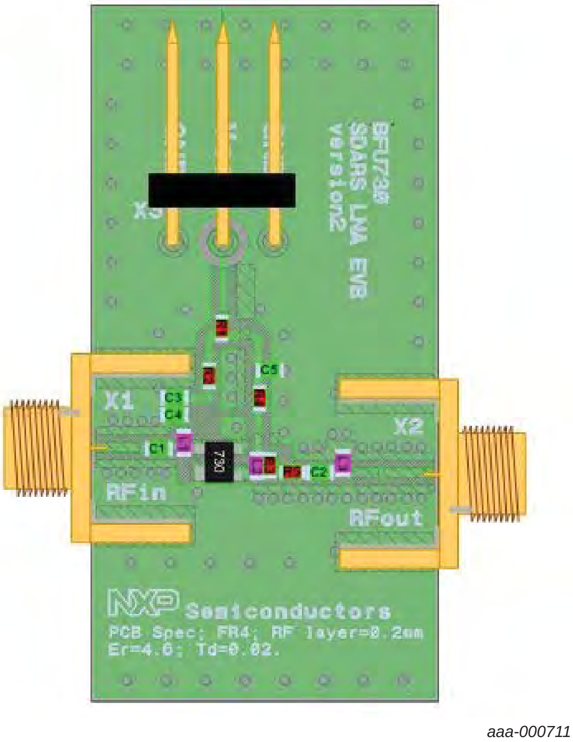


Fig 4. Printed circuit board of the BUF730F 2.33 GHz evaluation board

3.3 PCB layout

A good PCB Layout is an essential part of an RF circuit design. The EVB of the BFU730F serves as a guideline for laying out a board using the BFU730F. Use controlled impedance lines for all high frequency inputs and outputs. Bypass V_{CC} with decoupling capacitors, preferable located as close as possible to the device. For long bias lines, it may be necessary to add decoupling capacitors in the line further away from the device. Correct grounding of the GND pin is also essential for performance. Either connect the GND pin directly to the ground plane or through vias, or do both.

The EVB is made of FR4 material using the stack shown in Figure 5.

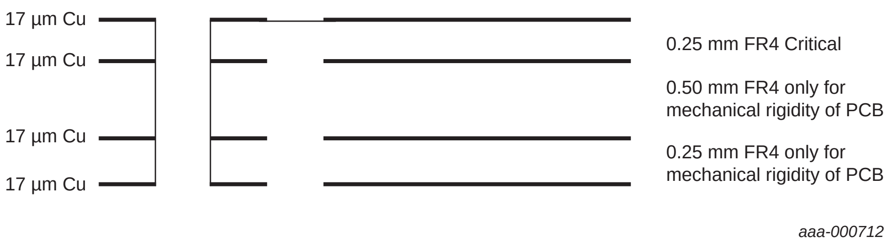


Fig 5. Stack of the PCB material

Material supplier is Isola Duraver; ε_r = 4.6 to 4.9: Tδ = 0.02.

3.4 Bill of materials

Table 3. Bill of materials

Designator	Description	Footprint	Value	Supplier name/type	Comment
C1	capacitor	0402	12 pF	Murata GRM1555	input matching/DC blocking
C2	capacitor	0402	3.3 pF	Murata GRM1555	input matching/DC blocking
C3	capacitor	0402	8.2 pF	Murata GRM1555	LF decoupling
C4	capacitor	0402	10 pF	Murata GRM1555	LF decoupling
C5	capacitor	0402	10 pF	Murata GRM1555	LF decoupling
L1	inductor	0402	15 nH	Murata/LQW15A high Q low Rs	input matching/DC bias
L2	inductor	0402	100 nH	Murata/LQW15A	DC bias
L3	inductor	0402	5.8 nH	Murata/LQW15A high Q low Rs	output matching
R1	resistor	0402	130 Ω	various	bias setting temperature stability
R2	resistor	0402	30 Ω	various	bias setting
R3	resistor	0402	100 Ω	various	stability
R4, R5	resistor	0402	0 Ω	various	backup tune pads
X1, X2	SMA RF connector	-	-	Johnson, end launch SMA 142-0701-841	RF input/RF output
X3	DC header	-	-	Molex, PCB header, right angle, 1 row, 3-way 90121-0763	bias connector

4. Equipment required

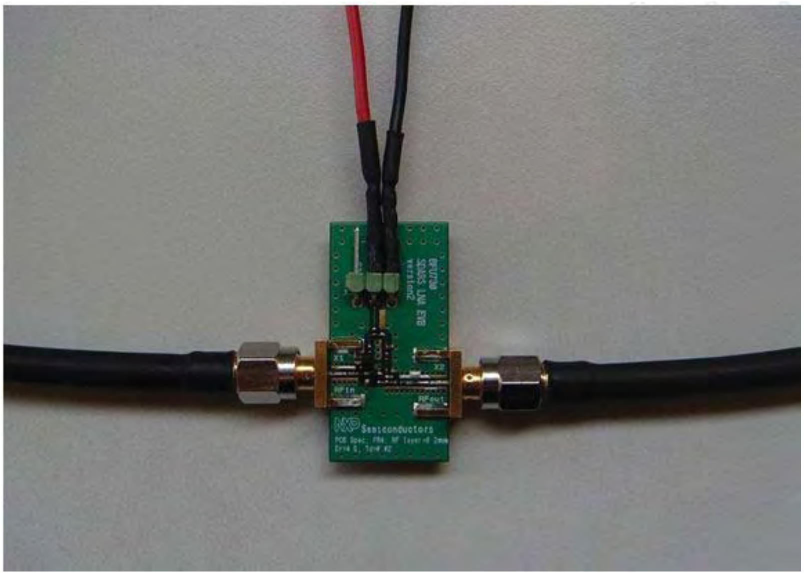
In order to measure the evaluation board the following is required:

- DC power supply up to 30 mA at 3.3 V (up to 15 V for bias control)
- RF signal generator capable of generating an RF signal at the operating frequency of 2.33 GHz.
- RF spectrum analyzer that covers at least the operating frequency of 2.33 GHz as well as a few of the harmonics. A spectrum analyzer that has a noise figure test function which measures up to 8 GHz, is sufficient. This is useful as it eliminates the necessity of having an expensive noise figure analyzer.
- Ammeter to measure the supply current (optional).
- Network analyzer for measuring gain, return loss and reverse Isolation.
- Noise figure analyzer.

5. Connections and setup

The BFU730F, 2.33 GHz EVB is fully assembled and tested. The following procedure is a step-by-step guide to operate the EVB and test the device functions.

1. Set the DC power supply to 3.3 V and connect it to the VCC and GND terminals.
2. Connect the RF signal generator and spectrum analyzer to the RF input and the RF output of the EVB, respectively. Do not turn on the RF output of the signal generator yet but set it to –30 dBm output power at 2.33 GHz. Set the spectrum analyzer to 2.33 GHz center frequency with a reference level of 0 dBm.
3. Turn on the DC power supply and it reads approximately 11 mA.
4. Enable the RF output of the generator; the Spectrum analyzer displays a tone of 2.33 GHz at around –13 dBm.
5. A network analyzer (NWA) can be used, instead of a signal generator and spectrum analyzer, to measure gain for input and output return loss
6. To evaluate the noise figure, use either a noise figure analyzer or a spectrum analyzer with noise option. The use of a 15 dB noise source, such as the Agilent 364B, is recommended. When measuring the noise figure of the evaluation board, minimize the use of any kind of adaptors or cables between the noise source and the EVB. Cables and adaptors significantly affect the noise performance.



aaa-000713

Fig 6. Printed circuit board of the BUF730F 2.33 GHz evaluation board

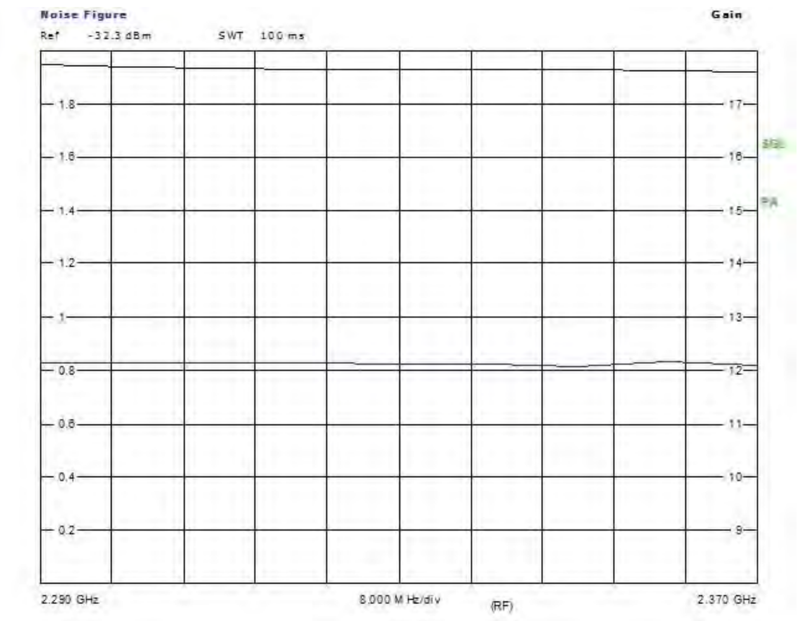
6. Typical EVB Results

Table 4. Typical measurement results measured on the evaluation board[1]

Symbol	Parameter	value	Unit
NF	noise figure	0.8	dB
G_p	power gain	17.6	dB
RL_{in}	input return loss	9.4	dB
RL_{out}	output return loss	22.5	dB
$\alpha_{isol(r)}$	reverse isolation	29.4	dB
$P_{i(1dB)}$	input 1 dB Gain Compression	–15	dBm
$P_{L(1dB)}$	output 1 dB Gain Compression	1.7	dBm
$IP3_I$	Input third order intercept point	4.7	dBm
$IP3_O$	output third order intercept point	22.6	dBm

[1] The NF and gain figures are measured at the SMA connectors of the EVB, so the connectors and PCB losses are not subtracted. When they are subtracted, the NF improves by approximately 0.1 dB.

6.1 Noise figure



aaa-000714

2290 MHz to 2370 MHz, center of plot (x-axis) is 2330 MHz

Fig 7. Plot of noise figure

6.1.1 Noise figure tabular data

Table 5. Frequency list results[1]

RF (GHz)	NF (dB)	Noise temperature (K)	Gain (dB)
2.290	0.825	60.701	17.736
2.300	0.827	60.840	17.694
2.310	0.825	60.650	17.662
2.320	0.832	61.259	17.639
2.330	0.822	60.425	17.644
2.340	0.821	60.378	17.641
2.350	0.812	59.642	17.643
2.360	0.834	61.426	17.632
2.370	0.819	60.216	17.609

[1] From Rohde and Schwarz FSU

6.2 Power gain compression test

V_{CC} = 3.3 V network analyzer is set to CW mode - for example, set to a single frequency, with power sweep. Input power is swept from –25 dBm to –5 dBm at 2332.5 MHz. Amplifier reaches input 1 dB compression point ($P_{i(1dB)}$) at –15.02 dBm input power. Output $P_{L(1dB)}$ = –15.02 dBm + 16.77 dB gain at $P_{L(1dB)}$ point ≥ +1.75 dBm, or 1.5 mW.

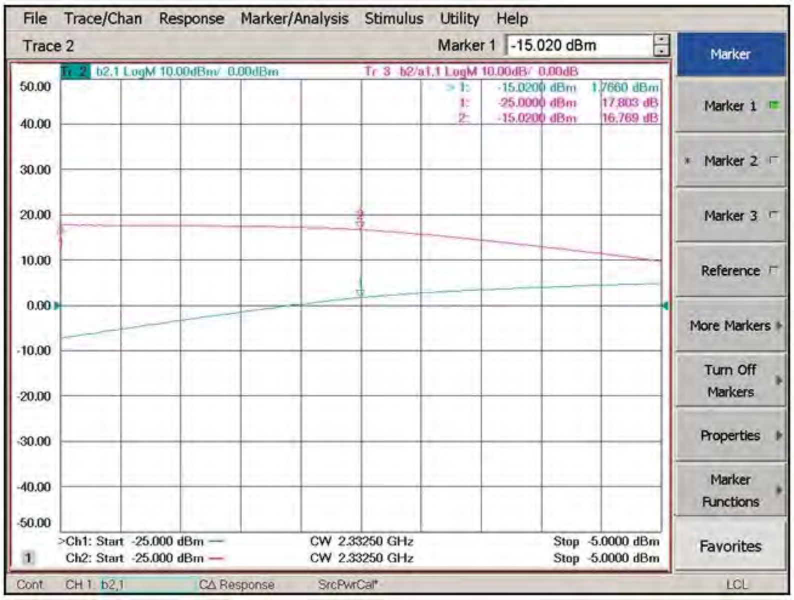


Fig 8. Plot of gain compression test

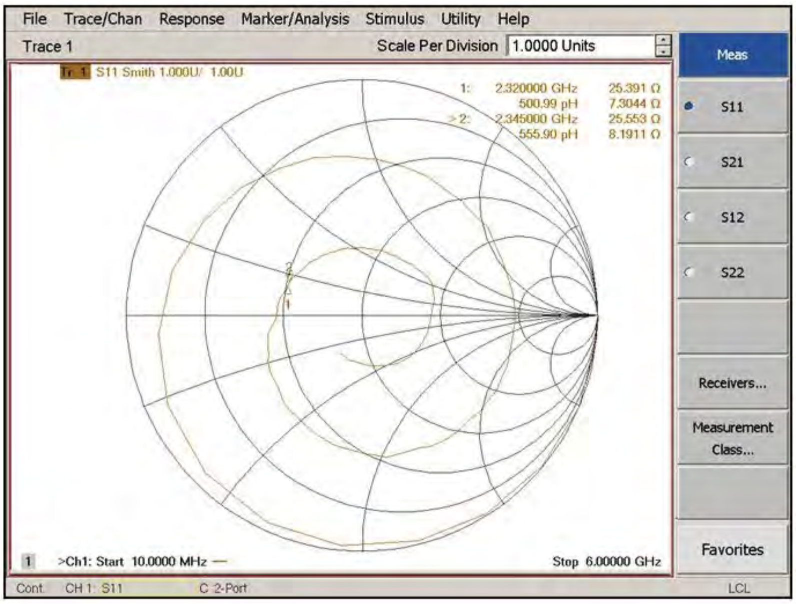
6.3 Input return losses (10 MHz to 6 GHz)

6.3.1 Log Mag

aaa-000716

Fig 9. Plot of input return losses

6.3.2 Smith chart



aaa-000717

Reference plain = input SMA connector on PCB

Fig 10. Smith chart of input return losses

6.3.3 Forward gain - wide sweep

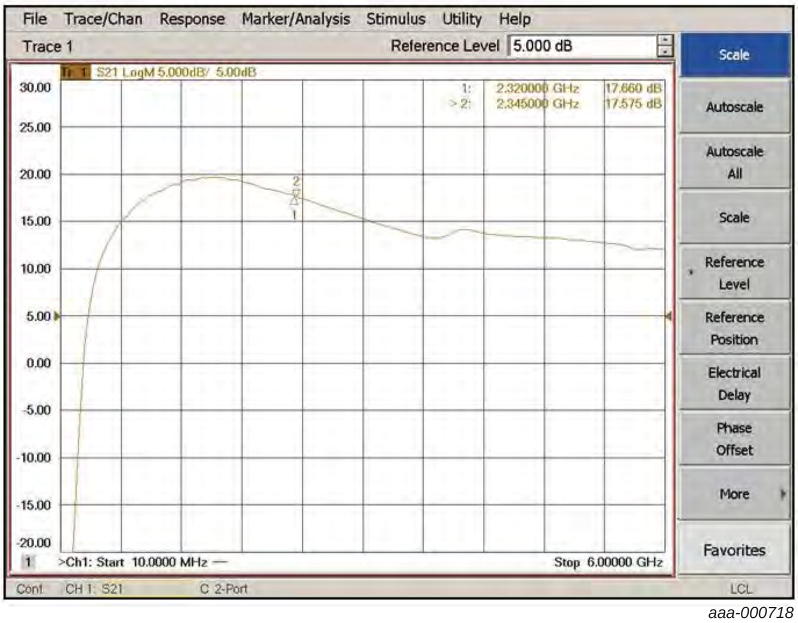


Fig 11. Plot of forward gain

6.4 Reverse isolation

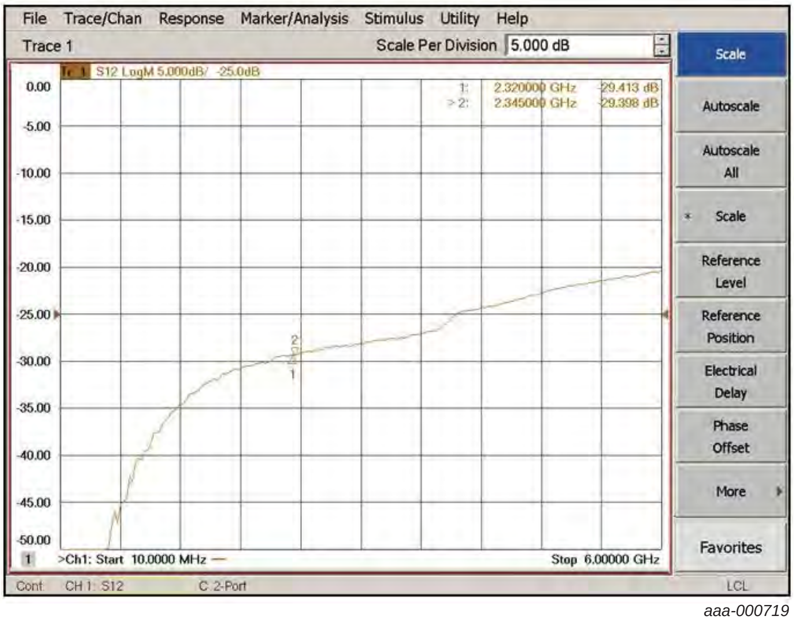


Fig 12. Plot of reverse isolation

6.5 Output return losses (10 MHz to 6 GHz)

6.5.1 Log Mag

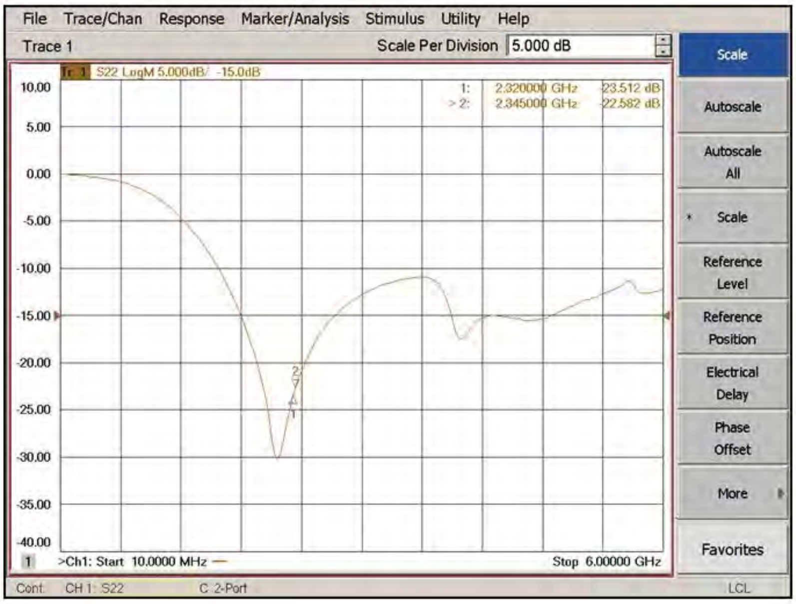
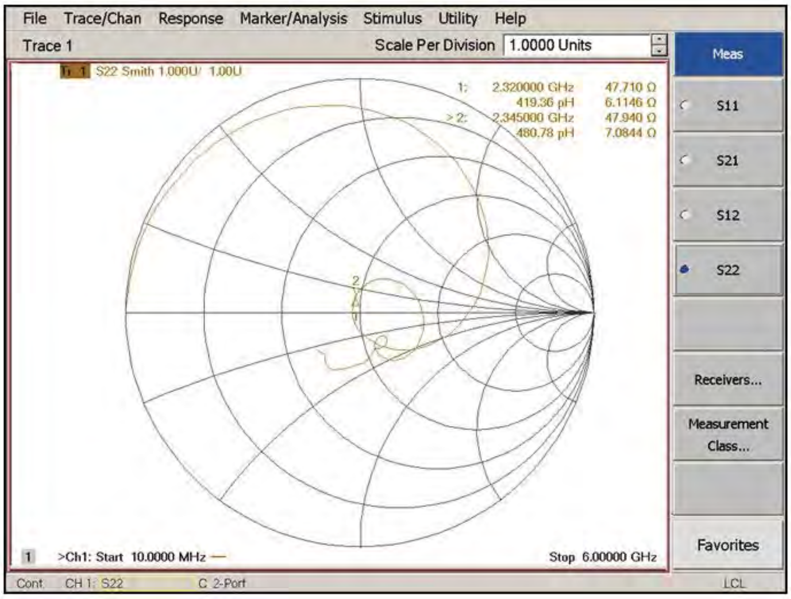


Fig 13. Plot of output return losses

6.5.2 Smith chart



Reference plain = input SMA connector on PCB

Fig 14. Smith chart of output return losses

6.6 Two-tone test (2332 MHz)

6.6.1 Input stimulus for amplifier two-tone test

- f_1 = 2332 MHz
- f_2 = 2333 MHz
- −24.37 dBm for each tone

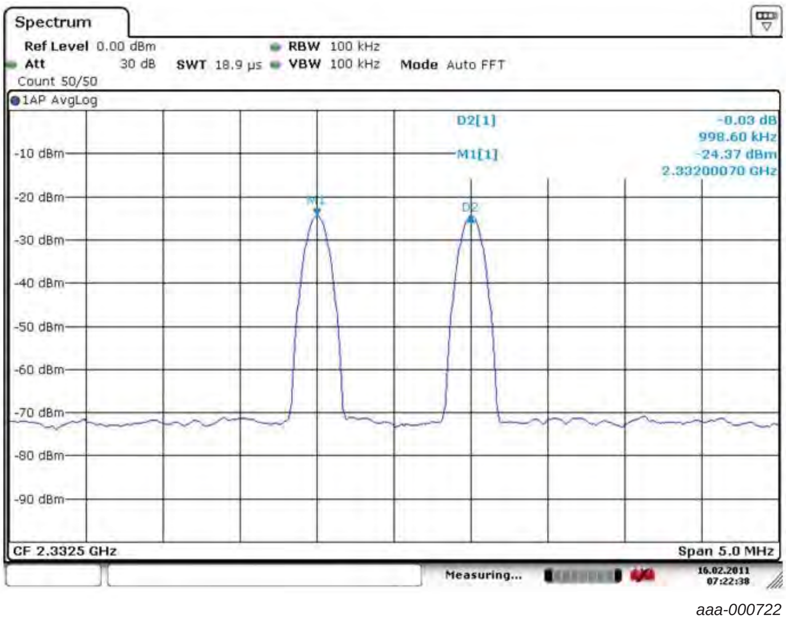
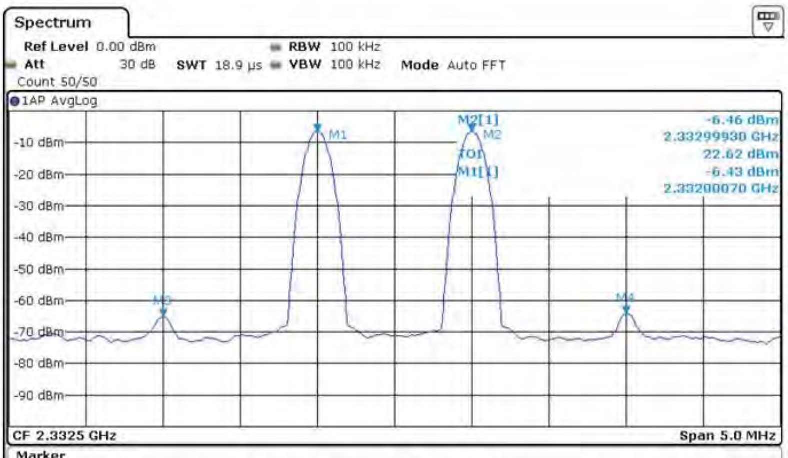


Fig 15. Plot of amplifier two-tone test at 2332 MHz

6.6.2 LNA response to two-tone test

- Output IP3 = 22.625 dBm
- Input IP3 = 22.625 dBm – (24.37 – 6.46) dBm = 4.7 dBm



No	Type	Trc	Stimulus	Response	Function	Function Result
1	1N	1	2.3320007 GHz	-6.43 dBm		
2	2N	1	2.3329993 GHz	-6.46 dBm	TOI	22.625 dBm
3	3N	1	2.3310022 GHz	-65.01 dBm		
4	4N	1	2.3339978 GHz	-64.19 dBm		

aaa-000723

Fig 16. Plot of LNA response to two-tone test

7. Legal information

7.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

7.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

7.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

8. Tables

9. Figures

10. Contents

Date of release: 25 October 2011
Document identifier: AN11066_1