### Document information

<table>
<thead>
<tr>
<th>Info</th>
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<tbody>
<tr>
<td><strong>Keywords</strong></td>
<td>SSL21101T, LED, flexible LED driver, LED lighting, LED lamp, SMPS, internal power switch, flyback, buck boost, natural PFC capability</td>
</tr>
<tr>
<td><strong>Abstract</strong></td>
<td>This application note describes how to design a mains LED driver using the NXP SSL21101T LED Driver IC in flyback mode. The focus is on Low Total Harmonic Distortion (LTHD) or Low LED current ripple (LR).</td>
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SSL21101T flexible focus flyback LED driver application

Revision history

<table>
<thead>
<tr>
<th>Rev</th>
<th>Date</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>v.1.1</td>
<td>20120521</td>
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</tr>
</tbody>
</table>

Modifications:
- Equation 4 in Section 5.3.1 “Phase 1” has been updated.
- Section 5.6 “VCC generation” has been updated.

Contact information

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1. Introduction

Light Emitting Diodes (LEDs) have been used in electronic systems for many years, primarily as indicator lights on electronic devices. Recent developments in terms of brightness and available colors have made it possible to use LEDs in a wide range of applications. These include lighting in cell phones, media players and replacing conventional light sources in commercial and domestic lighting applications.

The key enablers driving the expansion of LED lighting are the availability of high brightness LEDs and intelligent LED controllers. Product designers who incorporate high brightness LEDs face many challenges, like thermal management, driver scheme/topology and existing Lamp shape and regulation compliancy. The optimized lamp shape ensures that a minimum application BOM is required for building the IC.

The SSL21101T offers Smart Digital Control (SDC) to build either a low Form Factor (FF) application or a Low Total Harmonic Distortion (LTHD) (< 30 %) application.

The SSL21101T enables the lamp/module designer to produce an LED driver that:

- Does not require an external HV switch and works as Discontinuous Conduction Mode (DCM) flyback converter
- Can drive the power of retrofit lamps up to 11 W or retail displays up to 15 W
- Has a true current source behavior with High LED current accuracy (±3 % typical versus a mains variation of +10 %/−15 %)
- Enables the building of a high efficiency flyback application, 80 % to 85 % depending on the configuration
- Has an external LED OverTemperature Detection (OTD) and LED current regulation using a Negative Temperature Coefficient (NTC) connection.

2. LED properties

LEDs require a different type of driver than the type used with incandescent or halogen lamps. Incandescent lamps act as resistive loads with self-stabilizing properties whereas LEDs must have a current source. The amount of light an LED generates, is approximately proportional to the current flowing through the device. The voltage drop across the device increases with current but decreases with temperature. In this respect, LEDs behave like diodes. However, the voltage drop during operation (the forward voltage or $V_F$) is greater (see Figure 1). It is related to the amount of energy (eV) generated when an electron is converted to a photon. The amount of energy generated is directly related to the color of the light. Additionally, $V_F$ can vary greatly between batches due to production spread.
2.1 Serial/parallel configuration

In most applications where LEDs replace existing lamps, multiple units are connected to the driver, since a single LED would not generate enough light. The LEDs can be connected in either series or parallel.

If the LEDs are connected in series, the total voltage across the LED chain equals the sum of the forward voltages (the current is the same in all LEDs).

If LEDs are connected in parallel, the current is distributed among the branches. However, because the forward voltage of an LED tends to drop as the temperature rises, this configuration is intrinsically unstable. As the temperature rises, more of the current generated flows through the branches with the lower forward voltages. These branches become brighter while the branches with the higher forward voltages become darker.

A parallel configuration (or a combination of serial and parallel connections) is preferable because many LEDs can be combined on a safe supply voltage. An unacceptably high voltage is required to achieve the same degree of brightness with a series configuration.

The parallel configuration also offers the advantage of redundancy. If a single LED or connection in a serially connected LED chain fails, resulting in an open circuit, the light extinguishes in all LEDs in the chain. If the LEDs are connected in parallel this does not happen. In a parallel configuration, add current regulation at each additional branch to prevent thermal runaway and the unequal distribution of current and light.

In general, power converters operate at optimal efficiency when the difference between output and input voltages is minimized. The optimized functional point of the mains LED driver application is obtained at high output voltage, so more LEDs can be connected in series.
3. Flyback converter basics

In many applications, isolation from the mains is necessary for safety reasons. The flyback converter provides this isolation. It is cheaper and simpler to implement than a push-pull or a forward converter, since it only requires a single inductive element and a switch.

Figure 2 is a simplified application diagram of an isolated flyback converter, connected to a supply and a load. The polarities of some relevant voltages and currents are included in this diagram. \(V_I\) and \(V_O\) are DC voltages. In a practical application, a MOSFET or bipolar transistor replaces switch S1 and a diode replaces S2.

The state of the switches determines the operation of the circuit. Two switches allow four possible operating states (see Table 1):

- States 1 and 2
  Alternating primary and secondary conduction states
- State 3
  No primary or secondary conduction
- State 4
  Both switches closed (must be avoided)

The repeatability of the cycles (states 1, 2 and 3) gives the period switching \(t_{sw}\)

Initially, switch S1 is closed (for \(\delta t_{1sw}\)) and a current starts to flow in the primary winding of the transformer (state 1), rising linearly. Then S1 is opened and S2 is closed (for \(\delta t_{2sw}\)). The energy stored in the secondary winding of the transformer causes a current to flow in the load (state 2), which drops linearly as the energy is dissipated. The peak value of the load current equals the transformer primary-to-secondary turns ratio \((n = N_p/N_s)\) multiplied by the primary peak current when S1 is opened. While S2 is conducting, the output

<table>
<thead>
<tr>
<th>State</th>
<th>S1</th>
<th>S2</th>
<th>Duration</th>
<th>Naming</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>closed</td>
<td>open</td>
<td>(\delta t_{1sw})</td>
<td>primary stroke switching time</td>
</tr>
<tr>
<td>2</td>
<td>open</td>
<td>closed</td>
<td>(\delta t_{2sw})</td>
<td>secondary stroke switching time</td>
</tr>
<tr>
<td>3</td>
<td>open</td>
<td>open</td>
<td>(\delta t_{3sw})</td>
<td>free running</td>
</tr>
<tr>
<td>4</td>
<td>closed</td>
<td>closed</td>
<td>not applicable</td>
<td>not applicable</td>
</tr>
</tbody>
</table>
voltage is reflected in the primary side of the transformer. State 3 occurs when the secondary current falls to zero while S1 remains open (for $\delta t_{\text{sw}}$). The primary and secondary currents are both zero.

In Discontinuous Conduction Mode (DCM), the primary conducts for $\delta t_{\text{sw}}$ (primary stroke switching time), the secondary conducts for $\delta t_{\text{sw}}$ (the secondary stroke switching time) and then the conduction is halted for $\delta t_{\text{sw}}$. If a new cycle begins when the secondary current drops to zero ($\delta t_{\text{sw}} = 0$), the converter is operating in Boundary Conduction Mode (BCM). The switching period $t_{\text{sw}}$ in DCM mode is defined as $\delta t_{\text{sw}} + \delta t_{\text{sw}} + \delta t_{\text{sw}}$.

Figure 3 shows the equivalent circuit diagrams for the three valid states when a converter is operating in DCM mode. Simplified waveforms for one complete switching cycle are also shown.

Refer to various electronic engineering reference books for more detailed information on the operation of flyback converters.
Fig 3. Flyback equivalent circuits and waveforms (DCM mode)
4. Functional description

The SSL21101T is a Switched Mode Power Supply (SMPS) controller IC that operates directly from the rectified mains. It is designed to drive LED devices. The device includes a high-voltage power switch and a circuit enabling start-up directly from the rectified mains voltage. It has accurate control of the output current. The SSL21101T is part of the SSL21XX product family.

4.1 Features and benefits

- Smart Digital Control (SDC) deals with two kinds of applications:
  - High Power Factor (PF) (> 0.95) and Low Total Harmonic Distortion (LTHD) (< 30 %)
  - Low form factor (low LED current ripple with small electrolytic capacitors) - compatible with exception clause IEC61000-3-2
- Valley detection
  This feature reduces converter losses because the switch is closed at the optimal time.
- Primary side sensing enabling application building without using an optocoupler.
- True current source behavior:
  - LED current independent of mains voltage, LED voltage, temperature and coil variation
  - High LED current accuracy (±3 % typical)
- External (Negative Temperature Coefficient (NTC)) overtemperature detection for LED current regulation
- Internal supply voltage generation enabling start-up from the rectified mains voltage
- Enhanced thermal lead frame
  Enhanced thermal lead frame can increase the lifetime of the IC and enable it to operate at higher ambient temperatures. The lifetime of electronics at elevated temperatures can be a critical parameter for retrofit solutions.
- Built-in protections that ensure reliable operation of the IC and minimum defects:
  - Short winding detection
  - Internal OverTemperature Protection (OTP)
  - LED short protection via maximum control secondary stroke switching time
  - LED open protection via VCC OverVoltage LockOut (OVLO)
  - UnderVoltage LockOut (UVLO)
  - OverCurrent Protection (OCP) via maximum control primary stroke switching time

See the data sheet SSL21101T “Greenchip driver for LED lighting” for more detailed information and full specifications.
4.2 Block diagram

**Fig 4. SSL21101T block diagram**
5. Step-by-step design procedure

5.1 Basic electronic configuration

The mains voltage is rectified, buffered and filtered in the input section and connected to the primary winding of the transformer. Figure 5 gives an overview of the SSL21101T and the blocks around the device.

In the output section, the transferred energy is stored and filtered in a capacitor before it is available on the output pins. A clamp is added across the primary winding of the transformer. This clamp prevents high-voltage overshoot on the drain pin of the SSL21101T when the internal power MOSFET transistor is switched off. This new IC generation of 700 V MOSFET (SSL21101T) capability allows the building of snubberless applications.
5.2 Mode definition

Using the SLL21101T device applications focusing on Low Total Harmonic Distortion (LTHD) (PF > 0.95) or Low Ripple (LR) on LED current can be built. There are two modes of switching frequency which depend on the mains frequency and the chosen mode (see Table 2): 50 kHz or 60 kHz, or 100 kHz or 120 kHz.

The voltage applied on the Mode pin is different for each of the four mode configurations (see Table 2).

<table>
<thead>
<tr>
<th>Mode voltage range</th>
<th>Mains frequency</th>
<th>Behavior</th>
<th>Maximum switching frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DD(INTREGD)} \geq V_{MODE} &gt; 5 \times V_{DD(INTREGD)} / 6 )</td>
<td>50 Hz</td>
<td>low THD 100</td>
<td>100 kHz</td>
</tr>
<tr>
<td></td>
<td>60 Hz</td>
<td>low THD 100</td>
<td>120 kHz</td>
</tr>
<tr>
<td>( 5 \times V_{DD(INTREGD)} / 6 \geq V_{MODE} &gt; 4 \times V_{DD(INTREGD)} / 6 )</td>
<td>50 Hz</td>
<td>low THD 50</td>
<td>50 kHz</td>
</tr>
<tr>
<td></td>
<td>60 Hz</td>
<td>low THD 50</td>
<td>60 kHz</td>
</tr>
<tr>
<td>( 4 \times V_{DD(INTREGD)} / 6 \geq V_{MODE} &gt; 2 \times V_{DD(INTREGD)} / 6 )</td>
<td>not applicable</td>
<td>not functional</td>
<td>not applicable</td>
</tr>
<tr>
<td>( 2 \times V_{DD(INTREGD)} / 6 \geq V_{MODE} &gt; 1 \times V_{DD(INTREGD)} / 6 )</td>
<td>50 Hz</td>
<td>low ripple 50</td>
<td>50 kHz</td>
</tr>
<tr>
<td></td>
<td>60 Hz</td>
<td>low ripple 50</td>
<td>60 kHz</td>
</tr>
<tr>
<td>( 1 \times V_{DD(INTREGD)} / 6 \geq V_{MODE} &gt; 0 )</td>
<td>50 Hz</td>
<td>low ripple 100</td>
<td>100 kHz</td>
</tr>
<tr>
<td></td>
<td>60 Hz</td>
<td>low ripple 100</td>
<td>120 kHz</td>
</tr>
</tbody>
</table>

The voltage on the application is obtained with a resistor divider \([R9/(R9 + R8)]\). Apply the divider between pin \(V_{DD(INTREGD)}\) and the GND pins of the IC. The total resistor value \((R8 + R9)\) must be around 1 MΩ to reduce the current consumption on \(V_{DD(INTREGD)}\).

Example 1:

An application in LTHD 100 mode does not require a divider resistor. Pin MODE can be connected to \(V_{DD(INTREGD)}\).

Example 2:

An application in LR 100 mode does not require a divider resistor. Pin MODE can be connected to GND.

Example 3:

An application in LTHD mode with a 50 kHz switching frequency requires a 4.5 to 6 ratio. This ratio can be obtained with \(R9 = 1 \text{ MΩ}\) and \(R8 = 330 \text{ kΩ}\), respecting the constraint \(R8 + R9 \geq 1 \text{ MΩ}\).

The modulation controller takes into account the information of the Boundary Conduction Mode (BCM) detection. The chip has optimized performances in Discontinuous Conduction Mode (DCM). The IC prevents that the application enters Continuous Conduction Mode (CCM) and forces it to enter Boundary Conduction Mode (BCM).

Remark: Select specific values for external components, such as transformers and resistor \(R_{SOURCE}\) to avoid forced BCM. Otherwise, THD and the LED current ripple performances are directly impacted.
Example:

An application with PF > 0.7 can be built, using the IC in the 100 kHz Low Ripple (LR) mode, $\delta t_{\text{sw}}$ = around 10 $\mu$s, and keeping $\delta t_{\text{on}}$ as much as possible below $t_{\text{on(high)}}$. For example, $\delta t_{\text{sw}} = 2 \mu$s at $V_{\text{main(max)}}$. The application runs in BCM mode as the frequency switching is less than 100 kHz.

In that case, the accuracy in the range ±10 % of $V_{\text{main(nom)}}$ is around ±3 % for a 230 V (RMS) application and worse for a 120 V (RMS) application.

5.3 Current control

In this section, the maximum inductance value $L_{\text{max}}$ (primary inductor of T1; see Equation 4) and the values of the application components that control the LED current are calculated.

The maximum primary inductance value depends on the power application and the efficiency.

The full design is done in four phases:

1. Calculate and apply the maximum inductor ($L_{\text{max}}$) and the related peak current ($I_{\text{M}}$) values.
2. Calculate $R_{\text{source}}$ resistor $R_{12}$ (see Figure 5).
3. Calculate the values of resistors $R_{10}$, $R_{11}$ (divider resistor bridge)
4. Calculate the value of capacitor $C_{7}$ (see Figure 5). The capacitor is used as a filter function.

5.3.1 Phase 1

The input parameters required to calculate the values of the application components, the maximum primary inductor ($L_{\text{max}}$) and the peak current ($I_{\text{M}}$) are:

- Application mode and associated maximum switching frequency (see Table 4)
- Current on the LEDs ($I_{\text{LED}}$) and LED voltage ($V_{\text{LED}}$)
- Estimated input power ($P_{\text{in}} = \frac{I_{\text{LED}} \times V_{\text{LED}}}{\text{efficiency}}$)
- Select a transformer ratio:
  Select a primary-to-secondary transformer to obtain an optimized reflected $N \times V_{\text{LED}}$. The best compromise between efficiency and functionality can be achieved in the following way:
  - In LTHD mode the reflected voltage must be close to 100 V for a 230 V application and slightly below 100 V for a 110 V application.
  - In LR mode, where the buffer capacitor is higher, the reflected voltage can be increased to up to 150 V for a 230 V application and slightly over 100 V for a 110 V application. Keep the secondary stroke switching time ($\delta t_{\text{sw}}$) above the blanking time ($t_{\text{blank}}$).

A transformer ratio of approximately 3.3 is selected to obtain an $N \times V_{\text{LED}}$ of about 100 V.
• The minimum mains peak voltage \( V_{\text{main(M)(min)}} \) equals the mains peak voltage at the minimum level of the mains range (typically the nominal mains minus 15 %).

• Use the estimated primary inductor value \( L_{\text{estimated}} \) and the estimation of the DRAIN parasitic capacitor \( C_{\text{parasitic}} \) to evaluate the free running frequency and the associated \( \Delta \text{valley} \) (see Equation 6).

The input power can be calculated with Equation 1:

\[
p_{\text{in}} = \frac{1}{2} \times L_{\text{max}} \times I_{\text{M}}^2 \times f_{\text{sw(avg)}}
\]

Equation 2 and Equation 3 give the constraint that must be respected to remain in DCM mode:

\[
\delta t_{\text{sw}} + \Delta t_{\text{sw}} + \Delta \text{valley} \leq \frac{1}{f_{\text{sw(max)}}}
\]

\[
\frac{L_{\text{max}} \times I_{\text{M}}}{V_{\text{main(M)(min)}}} + \frac{L_{\text{max}} \times I_{\text{M}}}{N \times V_{\text{LED}}} + \Delta \text{valley} \leq \frac{1}{f_{\text{sw(max)}}}
\]

The maximum inductor value \( L_{\text{max}} \) is calculated with Equation 4:

\[
L_{\text{max}} = 2 \times \frac{P_{\text{in}}}{\left(2 \times P_{\text{in}} \times \frac{1}{V_{\text{main(M)(min)}}} + \frac{1}{N \times V_{\text{LED}}} \right)^2 \times f_{\text{sw(avg)}}}
\]

The peak current \( I_{\text{p}} \) can be calculated with Equation 5:

\[
I_{\text{M}} = \sqrt{\frac{2 \times P_{\text{in}}}{L_{\text{max}} \times f_{\text{sw(avg)}}}}
\]

Table 3 shows the value of the average switching frequency \( f_{\text{sw(avg)}} \) versus the application mode.

<table>
<thead>
<tr>
<th>Mode</th>
<th>( f_{\text{sw(avg)}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>low total harmonic distortion</td>
<td>( f_{\text{sw(max)}} )</td>
</tr>
<tr>
<td>low ripple</td>
<td>( f_{\text{sw(max)}} )</td>
</tr>
</tbody>
</table>

Table 2 shows the maximum switching frequency \( f_{\text{sw(max)}} \).

\( \Delta \text{valley} \) can be calculated with Equation 6:

\[
\Delta \text{valley} = \pi \times \sqrt{L_{\text{estimated}} \times C_{\text{parasitic}}}
\]
Where:
- \( L_{\text{estimated}} \) is the estimated primary inductor
- \( C_{\text{parasitic}} \) is the parasitic capacitance on pin DRAIN

Example:
- Mains power = 230 V (AC)
- LTHD mode: \( f_{\text{sw(max)}} = 100 \text{ kHz} \) and \( f_{\text{sw(avg)}} = 45.6 \text{ kHz} \)
- \( V_{\text{LED}} = 30 \text{ V} \) and \( N = 3.24; N \times V_{\text{LED}} = 97 \text{ V} \)
- \( P_{\text{in}} = 8 \text{ W} \)
- \( I_{\text{LED}} = 230 \text{ mA} \) with an efficiency of 86 %
- Estimated \( \Delta \text{valley} \) (\( L = 1 \text{ mH} \) and \( C_{\text{parasitic}} = 100 \text{ pF} \)) = 993 ns
- \( V_{\text{main(M)(min)}} = 282 \text{ V} \)

Results in:
- \( L_{\text{max}} = 1.21 \text{ mH} \)
- \( I_{\text{M}} = 538 \text{ mA} \)

The selected inductor (L) value is 1.22 mH and the related peak current \( (I_{\text{M}}) \) is 536 mA (see Equation 5).

### 5.3.2 Phase 2

The threshold voltage \( V_{\text{SOURCE}} = R_{12} \times I_{\text{M}} \) must be within the limits as given in Equation 7:

\[
V_{\text{th(det)SOURCE(min)}} \leq R_{12} \times I_{\text{M}} \leq V_{\text{th(det)SOURCE(max)}}
\]  

Choose resistor \( R_{12} \) using Equation 8:

\[
R_{12} = \frac{V_{\text{th(det)SOURCE(min)}} + V_{\text{th(det)SOURCE(max)}}}{2} \times \frac{0.75}{I_{pk}}
\]  

Example:
- Mains power = 230 V (AC); \( V_{I(\text{min})} = 282 \text{ V} \)
- LTHD mode: \( f_{\text{sw(max)}} = 100 \text{ kHz} \) and \( f_{\text{sw(avg)}} = 45.6 \text{ kHz} \)
- \( V_{\text{LED}} = 30 \text{ V}; N = 3.24 \)
- \( P_{\text{in}} = 8 \text{ W}; I_{\text{LED}} = 230 \text{ mA} \)
- \( \Delta \text{valley} = 993 \text{ ns}; L = 1.22 \text{ mH}; I_{\text{M}} = 536 \text{ mA} \)

Result: \( R_{12} = 1.39 \Omega \)

\( R_{12} \) can be obtained with two resistors in parallel: 1.5 \( \Omega \) in parallel with 10 \( \Omega \). In this case \( R_{12} = 1.3 \Omega \) and \( V_{\text{SOURCE}} = 0.69 \text{ V} \). Both are within the limits set in Equation 7.
5.3.3 Phase 3

Connecting resistors R10 and R11 between VDD(INTREGD) and the IC ground results in a ratio \( \frac{V_{(ILEDREF)}}{V_{DD(INTREGD)}} = \frac{R11}{(R11 + R10)} \).

Select resistors R10 and R11, which gives the ratio \( \frac{V_{(ILEDREF)}}{V_{DD(INTREGD)}} \) as calculated in Equation 9:

\[
\frac{V_{(ILEDREF)}}{V_{DD(INTREGD)}} = \frac{R12}{0.45} \times \frac{I_{LED}}{N} \tag{9}
\]

Choose values for resistors R10 and R11 that have a total resistor value (R10 + R11) of over 1 MΩ to reduce current consumption on VDD(INTREGD).

Where:

- \( N \) is the transformer ratio chosen: 3.24
- \( I_{LED} \) is the current in the output LEDs

Example:

- Mains voltage = 230 V (AC)
- LTHD mode: \( f_{sw(\text{max})} = 100 \text{kHz} \)
- \( V_{LED} = 30 \text{V} \)
- \( P_{in} = 8 \text{W} \)

The input power and the LED voltage give an LED current (\( I_{LED} \)) of approximately 230 mA.

The result: \( \frac{V_{(ILEDREF)}}{V_{DD(INTREGD)}} = 0.205 \), which equals \( \frac{R11}{(R11 + R10)} \).

A closed ratio value of 0.209 can be obtained when resistor R11 = 180 kΩ and resistor R10 = 680 kΩ. In this case: \( I_{LED} = \frac{0.45 \times 3.24 \times 0.209}{1.3} = 234 \text{mA} \).

5.3.4 Phase 4

The value of capacitor C7 is calculated with Equation 10. A first order filter is built with resistor R10 and capacitor C11. The cutting frequency (\( f_{cutting} \)) chosen must be below 100 Hz.

\[
C7 = \frac{I}{2 \times \pi \times f_{cutting} \times \frac{R10 \times R11}{R10 + R11}} \tag{10}
\]

A cutting frequency of 50 Hz for an application with R10 = 680 kΩ and R11 = 180 kΩ gives a capacitor of 22.3 nF. The result is a standard value of 22 nF.
5.4 NTC connection

Connecting a resistor divider, including an NTC, to pin NTC enables the external overtemperature detection. Resistors R6 and R7 are selected to use an NTC with an ambient value of 100 kΩ. The threshold voltages, \( V_{\text{det(H)(NTC)}} \) and \( V_{\text{det(L)(NTC)}} \) are optimized to have a maximum current consumption on \( V_{\text{DD(INTREGD)}} \) of 100 \( \mu \)A.

The values of resistors R6 and R7 can be calculated with Equation 11 and Equation 12:

\[
R_6 = \frac{(V_{\text{DD(INTREGD)}} - V_{\text{det(H)(NTC)}}) \times (R_{\text{NTC(125)}} - R_{\text{NTC(80)}}) \times (V_{\text{DD(INTREGD)}} - V_{\text{det(L)(NTC)}})}{V_{\text{det(L)(NTC)}} \times (V_{\text{DD(INTREGD)}} - V_{\text{det(H)(NTC)}}) - V_{\text{det(H)(NTC)}} \times (V_{\text{DD(INTREGD)}} - V_{\text{det(L)(NTC)}})}
\]

\[
R_7 = R_6 \times \frac{V_{\text{det(L)(NTC)}}}{(V_{\text{DD(INTREGD)}} - V_{\text{det(L)(NTC)}}) - R_{\text{NTC(125)}}}
\]

Example \((R_{\text{NTC(25)}} = 100 \text{ k}\Omega \text{ with a temperature coefficient beta of 4630)}:\)

- \( V_{\text{DD(INTREGD)}} = 5 \text{ V} \)
- \( V_{\text{det(H)(NTC)}} = 1.25 \text{ V} \)
- \( V_{\text{det(L)(NTC)}} = 0.625 \text{ V} \)
- Resistor value at 125 °C \((R_{\text{NTC(125)}}) = 2024 \text{ Ω} \)
- Resistor value at 80 °C \((R_{\text{NTC(80)}}) = 8905 \text{ Ω} \)

This results in:

- \( R_6 = 36 \text{ k}\Omega \)
- \( R_7 = 3.1 \text{ k}\Omega \)

The NTC resistor value for each temperature can be calculated with Equation 13:

\[
R_{\text{NTC(T)}} = 25 \text{ °C} \times \exp\left(\beta \times \left(\frac{I}{T + 273.15} - \frac{I}{25 + 273.15}\right)\right)
\]

5.5 \( V_{\text{DD(INTREGD)}} \) decoupling

Decouple the regulated voltage with a total capacitor \((C6)\) value of 2.2 \( \mu \)F for optimal regulation.

5.6 \( V_{\text{CC}} \) generation

A circuit, consisting of a capacitor, a rectifier diode and a peak current limiting resistor, is used to generate an external \( V_{\text{CC}} \) supply for the IC (see block 5 in Figure 5). The choice of component values involves a delicate trade-off between IC consumption, \( V_{\text{prot(VCC)}} \) and operation. The \( V_{\text{CC}} \) capacitor value depends on the time required to load the output capacitor until the reflected auxiliary voltage exceeds \( V_{\text{CC(UVLO)}} \) (see Figure 6). During this time, the capacitor is used to supply the IC when the JFET is not conducting.
When the VCC capacitor value is too low there is an oscillation on VCC between $V_{prot(VCC)}$ and $V_{CC(UVLO)}$. The device never starts-up.

The output voltage, the transformer auxiliary-to-secondary turns ratio, and the lowest converter frequency determine the values. They keep VCC between the maximum undervoltage lockout ($V_{CC(UVLO)(max)}$) and the minimum supply voltage protection voltage ($V_{prot(VCC)(min)}$).

The auxiliary-to-secondary turns ratio ($Na/Ns$) can be calculated using Equation 14:

$$\frac{Na}{Ns} = \frac{V_{aux(min)}}{V_{LED} + V_{D4}}$$

Where:

- $Na$ is the number of turns in the auxiliary winding
- $Ns$ is the number of turns in the secondary winding
- $V_{aux(min)}$ is the minimum voltage generated across the auxiliary winding
- $V_{D4}$ is the voltage across diode D4 when it is conducting (normally between 0.3 V and 0.8 V)
- $V_{LED}$ is the voltage across the LED chain

When selecting a value of about 22 V as minimum auxiliary voltage ($V_{aux(min)}$) (for $V_{CC(min)} > 22$ V), 30 V for the LED voltage ($V_{LED}$), and 0.8 V for the voltage on diode D4, the ratio $N_a/N_s = 0.714$.

The value of resistor $R5$ can be calculated with Equation 15:

$$R5 = \left( V_{LED(max)} \times \frac{Na}{Ns} - V_{prot(VCC)(min)} + \frac{Na}{N_p} \times V_{Li(prim)(max)} + \frac{V_{D4}}{2} \times \frac{Na}{Ns} \right) \times \frac{\delta 2t_{sw}}{t_{sw(avg)}} \times \frac{l}{I_{CC}}$$

---

**Fig 6. VCC start-up phase**

Phase 1: $V_{CC}$ capacitor charging at a current equaling $I_{start(sw)(DRAIN)}$
Phase 2: Switching start-up phase: IC supply current = $I_{CC(startup)}$ without auxiliary winding supply
Phase 3: Auxiliary winding supply: IC supply current = $I_{CC}$
Where:

- $V_{\text{LED(max)}}$ is the maximum voltage required on the output when open LED occurs
- $N_a$ is the number of turns in the auxiliary winding
- $N_s$ is the number of turns in the secondary winding
- $V_{\text{prot(VCC)}(\text{min})}$ is the protection voltage on pin VCC that stops the switching (shutdown mode)
- $N_p$ is the number of turns in the primary winding
- $V_{L(\text{prim})(\text{max})}$ is the maximum voltage on the primary inductor at the beginning of the secondary stroke time; is equal to the clamp voltage
- $\delta t_{\text{sw}}$ is the secondary stroke time
- $t_{\text{osc}}$ is the time to charge the transformer leakage inductance at the beginning of the secondary stroke time (first clamp voltage oscillation)
- $V_{D4}$ is the voltage on the output diode when conducting
- $t_{\text{sw(avg)}}$ is the average switching period
- $I_{\text{CC}}$ is the current consumption of the IC

Example:

- $V_{\text{aux}} = 22 \text{ V}$
- $V_{\text{LED}} = 30 \text{ V}$
- $V_{D4} = 0.8 \text{ V}$
- $N_a/N_s = 0.714$
- $NV_{\text{LED}} = 100 \text{ V}$

This results in $N_p/N_s = 3.3$. So, The $N_a/N_p$ ratio is:

$$N_a/N_p = (N_a/N_s) \times (N_s/N_p) = 0.214 \quad (16)$$

The typical $V_{\text{prot(VCC)}}$ of the SSL21101T equals 28 V. A maximum primary inductor voltage ($V_{L(\text{prim})(\text{max})}$) of close to 250 V can be selected, because the internal MOSFET has a 700 V capability.

When building a 100 kHz maximum switching frequency application, select an inductor value that obtains a $\delta t_{\text{sw}}$ of around 4 $\mu$s. The average switching period is 10 $\mu$s in LR mode and 21.9 $\mu$s in LTHD mode (see Table 4).

So $\Delta t = \delta t_{\text{sw}}/t_{\text{osc}}$ can be around 20, assuming $\delta t_{\text{sw}} \approx 4 \mu$s and $t_{\text{osc}} \approx 0.2 \mu$s. An IC consumption ($I_{\text{CC}}$) of 1.5 mA, a $V_{\text{prot(VCC)}}$ of 28 V, and a $V_{\text{LED(max)}}$ of 37 V (LR mode) and 39 V (LTHD mode) to protect the output capacitor, give a resistor $R_5$ value of 367 $\Omega$ in LR mode and 342 $\Omega$ in LTHD mode.

The maximum power dissipation in serial resistor $R_5$ is calculated with Equation 17:

$$P_{R5} = \left( \frac{V_{\text{LED(max)}}}{N_s} + \frac{N_a}{N_p} \times \frac{V_{L(\text{prim})(\text{max})}}{\delta t_{\text{sw}}} + \frac{V_{D4}}{2} \times \frac{N_a}{N_s} - V_{\text{prot(VCC)}} \right)^2 \times \frac{\delta t_{\text{sw}}}{t_{\text{sw(avg)}}} \times \frac{I}{R_5} \quad (17)$$
Using the values of the example of Equation 15, the power result of Equation 17 is 2.2 mW for both LR mode and LTHD mode.

The resulting VCC can be calculated with Equation 18:

\[ V_{CC} = \left( V_{LED} + \frac{V_{D4}}{2} \right) \times \frac{N_d}{N_s} \times \frac{N_s}{N_p} \times \frac{V_{I(prim)(max)}}{\delta_2 t_{sw}} \times \frac{t_{sw(avg)}}{\delta_2 t_{sw}} \times R5 \times I_{CC} \]  

(18)

Using the values of the example of Equation 15, the supply voltage result of Equation 18 is 23 V in LR mode and 21.6 V in LTHD mode.

Select diode D3 to withstand the peak current and reverse voltage Equation 19 calculates. The switching speed must be sufficient to operate at the converter working frequency.

The reverse voltage (V_{D3(reverse)}) depends on the primary-to-auxiliary turns ratio, the maximum buffer voltage and the maximum VCC voltage (= V_{prot(VCC)(max)}).

\[ V_{D3(reverse)} = \frac{N_d}{N_p} \times V_{buf(max)} + V_{prot(VCC)(max)} \]  

(19)

Where:

- \( V_{buf} \approx 400 \text{ V for a 230 V application} \)
- \( \frac{N_d}{N_p} = 0.216 \) (as explained when R5 was calculated (see Equation 16)

This results in a diode reverse voltage capability of 118 V. \( V_{prot(VCC)(max)} = 31 \text{ V} \).

The VCC buffer capacitor (C5) depends on the output capacitor loading time. The output capacitor loading time is the time required to reach the minimum output voltage for generating enough auxiliary voltage and I_{CC} supply current. So the minimum output LED voltage (V_{LED(min)}) can be calculated using Equation 20:

\[ V_{LED(min)} = \frac{N_s}{N_d} \times \left( V_{CC(UVLO)} + R5 \times I_{CC} \times \frac{t_{sw(avg)}}{\delta_2 t_{sw}} - \frac{N_d}{N_p} \times \frac{V_{I(prim)}}{\delta_2 t_{sw}} \right) - \frac{V_{D4}}{2} \]  

(20)

The value of resistor R5 is 342 \( \Omega \) for LTHD mode (see Equation 15). Using a \( V_{CC(UVLO)} \) value of 11 V, the minimum LED voltage result of Equation 20 is 15.2 V.

The time (\( \Delta t \)) it takes to charge the output capacitor can be calculated with Equation 21:

\[ t_{start(sw)} = \frac{10 \times C4 \times (V_{LED(min)} - 1)^2}{L \times I_{pk}^2 \times f_{sw(avg)} \times \ln(V'_{LED(min)} - 1)} \]  

(21)

Example (in LTHD mode):

- \( L = 1.22 \text{ mH} \)
- \( I_{pk} = 536 \text{ mA (see Section 5.3)} \)
- \( V_{LED(min)} = 15.2 \text{ V} \)
• C4 (output capacitor) = 1000 μF

The time \( t_{\text{start}(\text{sw})} \) it takes to charge the output capacitor is 47.5 ms.

The VCC capacitor (C5) can now be calculated with Equation 22:

\[
C_5 = \frac{I_{CC} \times t_{\text{start}(\text{sw})} \times (V_{CC(\text{start})} + V_{CC(\text{UVLO})})}{(V_{CC(\text{start})}^2 - V_{CC(\text{UVLO})}^2)}
\]  

(22)

Where:

• \( I_{CC} \) = current consumption of the IC
• \( t_{\text{start}(\text{sw})} \) = the time it takes to charge the output capacitor
• \( V_{CC(\text{UVLO})} \) = the maximum voltage to launch the VCC undervoltage protection = 11 V
• \( V_{CC(\text{start})} \) = the minimum start-up voltage of the IC = 17 V

Example (in LTHD mode):

• \( t_{\text{start}(\text{sw})} = 47.5 \text{ ms} \)
• \( (V_{CC(\text{start})} - V_{CC(\text{UVLO})}) = 6 \text{ V} \)

This results in \( C_5 = 4.4 \mu F \).

The minimum value of \( V_{CC(\text{start})} - V_{CC(\text{UVLO})} \) is 5.4 V. Do the worse case calculation of C5 using this minimum value. If the minimum value of \( V_{CC(\text{UVLO})} \) is 9.5 V, then \( C_5 = 5.9 \mu F \).

5.7 Snubber

The snubber circuit (block 6 in Figure 5) uses a combination of a blocking diode (D2), a clamp capacitor (C3) and a dissipative resistor (R4). An RCD snubber is selected because of a requirement to stop drain oscillations within 2 μs after switching off the MOSFET. Some Zener snubbers and snubberless options can also be compliant for several cases.

In the applied power range (see Table 2), this approach is more efficient (lower losses) than alternative designs.

<table>
<thead>
<tr>
<th>Method</th>
<th>Power range (W)</th>
<th>Efficiency average (mains range 190 V to 260 V) measurement results (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>no snubber</td>
<td>8</td>
<td>87.1</td>
</tr>
<tr>
<td>RCD snubber</td>
<td>8</td>
<td>86.4</td>
</tr>
<tr>
<td>Zener snubber 180 V</td>
<td>8</td>
<td>86.5</td>
</tr>
<tr>
<td>Zener snubber 270 V</td>
<td>8</td>
<td>87</td>
</tr>
</tbody>
</table>

5.8 Input circuit

The input circuit rectifies the mains voltage and provides overcurrent and overvoltage protection. It has to be overdimensioned to cope with overvoltage and overcurrent conditions on the input.
The primary protection consists of a fuse or fusistor that breaks down when an overcurrent event occurs and exceeds the nominal value of the protection. If a fuse is used, select a breakdown value that can handle inrush currents while still providing overcurrent protection. In practice, a value of between 1 A and 1.5 A is sufficient. If a fusistor is selected, the minimum value for this resistor (R1) can be calculated using Equation 23. For most diode bridge rectifiers, the I_{FSM} parameter is around 20 A. The diode D1 must have the same or a better I_{FSM} value.

\[ R_L = \frac{\sqrt{2} \times V_{\text{max}} (AC)}{I_{FSM}} \]  

(23)

Example:

- \( V_{\text{main}} = 230 \text{ V (AC) } \pm 20 \% \)
- \( V_{\text{max}} = 276 \text{ V (AC)} \)

The result: \( R_1 = 19.5 \Omega \). The nearest series standard value is 20 \( \Omega \).

In addition to its ohmic value, the continuous power dissipation in R1 is an important characteristic. This value can be calculated with Equation 24:

\[ P_{R1} = \text{crest factor} \times R_1 \times \frac{P_{\text{tot}}^2}{V_{\text{main}}^2 (AC)} \]  

(24)

The crest factor is the ratio of the peak current and the RMS current (5.4 typical in LR mode and 1.41 in LTHD mode).

Example:

- \( V_{\text{main}} = 230 \text{ V (AC)} \)
- \( P_{\text{tot}} = 8.5 \text{ W} \)
- \( R_1 = 20 \Omega \)
- \( \text{crest factor} = 5.4 \) (LR mode)

The resulting power dissipated in R1 is 147 mW.

Dimension resistor R1 so it can handle the peak power in the circuit, the combination of peak current and maximum mains voltage \( V_{\text{max}} (AC) \). The peak power can be calculated with Equation 25:

\[ P_M = I_{FSM} \times \sqrt{2} \times V_{\text{max}} (AC) \]  

(25)

The time of the peak depends on capacitor values. This time can be calculated with Equation 26:

\[ \Delta t = \frac{C_1 \times \sqrt{2} \times V_{\text{max}} (AC)}{I_{FSM}} \]  

(26)
Equation 27 calculates the added dissipation in resistor R1.

\[ P_{\text{additional}} = f_M \times \Delta t \times I_{\text{FSM}} \times \sqrt{2} \times V_{\text{max (AC)}} \]  

(27)

Where:

• \( f_M \) is the frequency of the peak
• \( \Delta t \) is the time of the peak from Equation 26

Example:

• \( C_i = 1 \ \mu \text{F} \)
• \( I_{\text{FSM}} = 20 \ \text{A} \)
• \( V_{\text{max}} = 260 \ \text{V (AC)} \)
• \( P_M = 7353 \ \text{W} \)
• \( \Delta t = 18.4 \ \mu\text{s} \)
• \( f_M = 1 \ \text{Hz} \)

Result: \( P_{\text{additional}} = 135 \ \text{mW}. \)

5.9 Mains buffer

The buffer circuit comprises two capacitors and an inductor. The circuit has dual functionality:

• Store energy
  For LR mode, ensuring the converter can transfer power continuously to the LED chain. LED operation becomes independent of mains power. Fluctuations are filtered out.
  For LTHD mode, minimize the total capacitor value to maintain a good input current waveform.
  The voltage across the converter must not drop below the minimum working voltage within a single mains cycle.
• Filter the current from the mains
  Filtering the ripple current the converter generates to ensure compliance with legal requirements on mains conducted emissions.

The total capacitance \((C_1 + C_2)\) can be estimated as follows:

First, calculate the minimum voltage at which the converter still delivers full power. The capacitor value is linked to the \( \delta 2t_{\text{sw(nom)}} \) value, which is used to retain DCM mode at maximum switching frequency (see Equation 28).

\[ V_{\text{buf(min)}} = \frac{L \times I_{pk}}{\delta 2t_{\text{sw(nom)}}} \]  

(28)

Next, calculate the time between the peak voltage and the mains voltage reaching this minimum voltage (see Equation 29).
Where:

- \( f_{\text{net}} \) = mains voltage frequency
- \( V_{\text{min}} \) (AC) = minimum RMS mains voltage.

Now take the transformer input power and add application losses. Use Equation 30 to calculate the total buffer capacitance:

\[
C1 + C2 = \frac{2 \times P_{\text{tot}} \times t_{\text{dis}}}{(\sqrt{2} \times V_{\text{min}} \text{ (AC)})^2 - (V_{\text{buf(min)}})^2}
\]

(30)

Where:

- \( P_{\text{tot}} = P_{\text{in}} + \text{losses} \)

The combination of \( L2, C1 \) and \( C2 \) forms a \( \pi \)-filter which helps to filter out the high frequency currents the converter action generates. Although a single filter stage is not enough to satisfy legal requirements concerning mains conducted emissions, it does go a long way to achieve these goals. The cut-off frequency \( (f_{\text{co}}) \) of this filter can be calculated with Equation 31:

\[
f_{\text{co}} = \frac{1}{2 \times \pi \times \sqrt{L1 \times \frac{C1 \times C2}{C1 + C2}}}
\]

(31)

Remark: \( C1 = C2 \)

In LR mode, the cut-off frequency must be below the working frequency divided by 36. Equation 32 (from Equation 31) calculates \( L1 \):

\[
L1 = \frac{648}{C_s \times \pi^2 \times f_{\text{conv}}^2}
\]

(32)

Remark: \( C_s = C1 = C2 \)

In LTHD mode, the cut-off frequency must be below the working frequency divided by 10. Equation 33 (from Equation 31) calculates for \( L1 \):

\[
L1 = \frac{20}{C_s \times \pi^2 \times f_{\text{conv}}^2}
\]

(33)

Remark: \( C_s = C1 = C2 \)

Example of an 8 W LR mode application (see Section 5.3.3):

- \( V_{\text{main}} \) (AC) = 230 V
- \( V_{\text{min}} \) (AC) = 190 V (RMS)
- \( f_{\text{net}} \) (mains frequency) = 50 Hz
• $P_{\text{tot}} = 8$ W
• $L_{\text{prim}}$ (transformer primary inductor) = 1.22 mH
• $I_M = 373$ mA (from Equation 6 in Section 5.3.2)
• $\delta t_{\text{sw(nom)}} = 3.5 \mu s$ (required to retain DCM mode at $f_{\text{sw}} = 100$ kHz)

Results:

$V_{\text{buf(min)}} = 159$ V (Equation 28)
$t_{\text{dis}} = 7.16$ ms (Equation 29)
$C_1 + C_2 = 3.07 \mu F$; this results in: $C_s = 1.5 \mu F$ (Equation 30)
$L_1 = 4.4$ mH (Equation 32)

Example of an 8 W LTHD mode application (see Section 5.3.3):

• $V_{\text{main (AC)}} = 230$ V
• $V_{\text{min (AC)}} = 190$ V (RMS)
• $f_{\text{net}}$ (mains frequency) = 50 Hz
• $P_{\text{tot}} = 8$ W
• $L_{\text{prim}}$ (transformer primary inductor) = 1.22 mH
• $I_M = 373$ mA (from Equation 6 in Section 5.3.2)
• Select a value for the maximum capacitance ($C_1 + C_2$) that keeps $\text{PF} > 0.95$ and $\text{THD} < 0.3 \%$. A good example is $C_1 = C_2 = 100$ nF.
• $f_{\text{conv}} = 100000 / 2.19 = 45660$ Hz).

Result: $L_1 = 9$ mH (Equation 33).

5.10 Output circuit

The values of components in the output circuit depend on the number of LEDs in the chain, the voltage across the chain and current the voltage flowing through the chain.

Depending on the converter mode, the current can have ripple from the primary side conversion at the rectified mains frequency and at the converter switching frequency. The size of the $I_{\text{LED}}$ ripple determines the size of input and output buffer capacitor $C_4$.

5.10.1 Low ripple

In LR mode, the rectified mains frequency has no effect on the LED current. The primary buffer capacitor enables the maintaining of a constant switching frequency. The LED current is maintained at a constant average value. The output capacitor is only used to filter the current ripple at the converter switching frequency. The size of the output capacitor ($C_4$) can be calculated with Equation 34.

$$C_4 = \frac{I_{\text{LED}}}{\Delta I_{\text{LED}}} \times \frac{1}{f_{\text{conv(nom)}} \times R}$$  \hspace{1cm} (34)

Where:
- $I_{\text{LED}}$ = LED current
- $\Delta I_{\text{LED}}$ = LED current variation
• \( f_{\text{conv(nom)}} \) = nominal converter frequency
• \( R \) = series resistance of LED chain

Example with 10 LEDs series application:
• \( I_{\text{LED}} = 220 \text{ mA} \)
• \( V_F = 3.5 \text{ V} \)
• current ripple = 10 %; \( \Delta I_{\text{LED}} = 22 \text{ mA} \)
• nominal converter frequency = 100 kHz

The voltage across the LED chain is \( 10 \times 3.5 \text{ V} = 35 \text{ V} \). Assuming that each LED has a dynamic resistance of 0.5 \( \Omega \) at 220 mA, the resistance of the LED chain is \( 10 \times 0.5 = 5 \Omega \). This results in a buffer capacitor (C4) value of 20 \( \mu \text{F} \).

**5.10.2 Low total harmonic distortion mode**

In LTHD mode, the rectified mains frequency has a major impact on the LED current. The primary buffer capacitor has a minimum value. The LED current is changing over the rectified mains to obtain a sine input current wave-form and to maintain a high Power Factor (PF). The output capacitor is used to filter the current ripple at the mains rectified frequency. The size of the output capacitor (C4) can be calculated with Equation 35:

\[
C4 = \frac{I}{f_{\text{net}} \times 5.2 \times \pi \times R} \times \sqrt{4 \times \left(\frac{I_{\text{LED}}}{\Delta I}\right)^2 - 1}
\]

(35)

Where:
• \( I_{\text{LED}} \) = LED current
• \( \Delta I_{\text{LED}} \) = LED current variation
• \( f_{\text{net}} \) = mains frequency
• \( R \) = series resistance of LED chain

Example with a 10 LEDs series application:
• \( I_{\text{LED}} = 220 \text{ mA} \)
• \( \Delta I_{\text{LED}} = 60 \text{ mA} \) (ripple = 30 %)
• \( R = 5 \Omega \)
• \( f_{\text{net}} = 50 \text{ Hz} \)

This results in an output buffer capacitor (C4) value of 1610 \( \mu \text{F} \).
5.11 Package thermal resistance

The package thermal resistance can be used for application calculation (see Table 5).

### Table 5. Thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{th(j-a)}$</td>
<td>thermal resistance from junction to ambient</td>
<td>in free air</td>
<td>70</td>
<td>K/W</td>
</tr>
<tr>
<td>$R_{th(j-c)}$</td>
<td>thermal resistance from junction to case</td>
<td>package covered with epoxy resin</td>
<td>42</td>
<td>K/W</td>
</tr>
</tbody>
</table>

[1] $R_{th(j,a)}$ can be lower when the GND pins are connected to an area with sufficient copper on the printed-circuit board.

The protection temperature is 10 K/W lower than the maximum temperature in the chip.

Example:

- 8 W application
- Dissipation inside the circuit is 0.5 W

The maximum junction temperature ($T_{j(max)}$) equals: $T_{amb} + 0.5 \times 70 \text{ K/W}$

The protection temperature ($T_{prot}$) equals: $T_{amb} + 0.5 \times 60 \text{ K/W}$

5.12 Wall switch compatibility

The 110 V application works with wall switches that have an impedance of higher than 800 kΩ. Compatibility with other wall switches and mains voltage ranges is achieved by adding a resistor, consuming only a few mW of power, in parallel to capacitor C4.
### 6. Abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCM</td>
<td>Boundary Conduction Mode</td>
</tr>
<tr>
<td>DCM</td>
<td>Discontinuous Conduction Mode</td>
</tr>
<tr>
<td>LED</td>
<td>Light-Emitting Diode</td>
</tr>
<tr>
<td>LR</td>
<td>Low Ripple</td>
</tr>
<tr>
<td>LTHD</td>
<td>Low Total Harmonic Distortion</td>
</tr>
<tr>
<td>NTC</td>
<td>Negative Temperature Coefficient</td>
</tr>
<tr>
<td>NV(_{LED})</td>
<td>Reflected LED voltage</td>
</tr>
<tr>
<td>OCP</td>
<td>OverCurrent Protection</td>
</tr>
<tr>
<td>OTP</td>
<td>OverTemperature Protection</td>
</tr>
<tr>
<td>PF</td>
<td>Power Factor</td>
</tr>
<tr>
<td>SDC</td>
<td>Smart Digital Control</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
</tr>
</tbody>
</table>
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