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TEA1716 resonant power supply control IC with PFC

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Document information

Info	Content
Keywords	TEA1716, Power Factor Corrector (PFC), LLC, burst mode operation, resonant, power converter
Abstract	The TEA1716 integrates a power factor corrector controller and a controller for a Half-Bridge resonant Converter (HBC) in a multi-chip IC. It provides the drive function for the discrete MOSFET in an upconverter and for the two discrete power MOSFETs in a resonant half-bridge configuration. The TEA1716 provides fully integrated burst mode operation functions for the PFC and HBC to reduce converter power consumption at low-power output. In burst mode operation, the power consumption of the IC is also minimized for further reduction of the power consumption in a standby state. The PFC circuit and resonant converter topology controlled using the TEA1716 is very flexible which enables it to be used in a broad range of applications across a wide mains voltage range. Combining PFC and HBC controllers in a single IC makes the TEA1716 ideal for controlling power supplies in high-power adapter topologies. Highly efficient and reliable power supplies can be designed with the TEA1716 using the minimum of external components.

Revision history

Rev	Date	Description
v. 1	20130109	first issue

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1. Introduction

This application note discusses the TEA1716 functions for applications in general. As the TEA1716 provides extensive functionality, many subjects are discussed.

In this application note, each section/paragraph can be read as a standalone explanation with few cross-references to other parts of the application note or data sheet. This leads to some repetition between this application note and the *TEA1716 data sheet*. In most cases, typical values are given to enhance the readability.

Table 1. Overview section application note

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Section 1	Introduction
Section 2	TEA1716 highlights and features
Section 3	Pin overview with functional description An overview of the TEA1716 pins with a summary of the functionality.
Section 4	Application diagram
Section 5	Block diagram
Section 6	Supply functions In this section and Section 7 to Section 10 the main functions of the TEA1716 are described. The functions are described from an application point of view.
Section 7	MOSFET drivers GATEPFC, GATELS and GATEHS See Section 6.1 “Basic supply system overview”
Section 8	PFC functions See Section 6.1 “Basic supply system overview”
Section 9	HBC functions See Section 6.1 “Basic supply system overview”
Section 10	Burst mode operation See Section 6.1 “Basic supply system overview”.
Section 11	Practical burst mode implementation Practical methods are given for optimizing the burst mode system.
Section 12	Protection functions An overview of the protection functions of the TEA1716.These functions are described from an application point of view.
Section 13	Recommendations Topics related to PCB design and debugging. Recommendations on the way of working.
Section 14	Application examples

1.1 Related documents

Additional information and tools:

- *TEA1716T data sheet*: “Resonant power supply control IC with PFC”
- *User manual: “TEA1716 resonant power supply control IC demo board” (UM10557)*
- *Calculation sheet*
- *Online design tool*

1.2 Related products

NXP products similar to the TEA1716 are:

- TEA1713:

  More suitable for applications that do not have severe requirements on burst mode operation and do not require a very low standby power consumption. The TEA1713 provides some extra design flexibility.
- SSL4120:

  More suitable for (lighting) applications that require a strong performance on low-mains distortions like (Total) Harmonic Distortions or Power Factor.

2. TEA1716 highlights and features

2.1 Resonant conversion

Today's market demands high-quality, reliable, small, lightweight and efficient power supplies.

The higher the operating frequency, the smaller and lighter the transformers, filter inductors and capacitors can be. On the other hand, the core, switching and winding losses of the transformer increase at higher frequencies and become dominant. This effect reduces the efficiency at high frequencies limiting the minimum size of the transformer.

The corner frequency of the output filter determines the bandwidth of the control loop. A well-chosen corner frequency allows high operating frequencies to achieve a fast and dynamic response.

Pulse Width Modulated (PWM) power converters, such as flyback, upconverters and downconverters, are widely used in low and medium power applications. A disadvantage of these converters is that the PWM rectangular voltage and current waveforms cause turn-on and turn-off losses which limit the operating frequency. The rectangular waveforms also generate broadband electromagnetic energy that can produce ElectroMagnetic Interference (EMI).

A resonant DC-to-DC converter produces sinusoidal waveforms and reduces the switching losses enabling operation at higher frequencies.

Recent environmental considerations have resulted in a need for high-efficiency performance at low loads. Burst mode operation of the resonant converter can provide this performance when the converter is required to remain active.

Resonant conversion is chosen when there is a requirement for:

- High power
- High efficiency
- EMI friendly
- Compact size

2.2 Power factor correction conversion

Most switch mode power supplies result in a non-linear impedance (load characteristic) to the mains input. Current taken from the mains supply occurs only at the highest voltage peaks and is stored in a large capacitor. The energy is taken from this capacitor storage, in accordance with the switch mode power supply operation characteristics. Government regulations dictate special requirements for the load characteristics of certain applications.

Two main requirements can be identified:

- Mains harmonics requirements EN61000-3-2
- Power factor (real power/apparent power)

The requirements enforce making the load to the mains voltage resemble a resistive load. The power supply input circuit must meet these requirements. Passive circuits (often a series coil) or active circuits (often a boost converter) can be used to modify the mains load characteristics as required.

An additional market requirement for the added mains input circuit is that works with a good efficiency and is low cost.

Using a boost converter to meet these requirements has the benefit of a fixed DC input voltage when combined with a resonant converter. The fixed input voltage ensures easier resonant converter design (especially for wide mains input voltage range applications) and the possibility to reach a higher efficiency.

2.3 TEA1716 resonant power supply control IC with PFC

The TEA1716 incorporates two controllers, one for Power Factor Correction (PFC) and one for a Half-Bridge resonant Converter (HBC). The controllers provide the drive function for the discrete MOSFET for the upconverter and for the two discrete power MOSFETs in a resonant half-bridge configuration.

The resonant controller part is a high-voltage controller for a zero-voltage switching LLC resonant converter.

The resonant controller includes a high-voltage level-shift circuit and several protection features such as overcurrent protection, open-loop protection, capacitive mode protection and a general-purpose latched protection input.

In addition to the resonant controller, the TEA1716 also contains a Power Factor Correction (PFC) controller. Efficient PFC operation is provided using functions such as:

- quasi-resonant operation at high-power levels
- quasi-resonant operation with valley skipping at lower power levels

In addition, the IC includes overcurrent protection, overvoltage protection and demagnetization sensing ensures safe operation in all conditions.

The proprietary high-voltage BCD PowerLogic process makes direct start-up possible from the rectified universal mains voltage in an efficient way. A second internal low-voltage SOI die is used for accurate, high-speed protection functions and control.

The TEA1716 controlled PFC and resonant converter topology is highly flexible and enables a broad range of applications for wide input AC mains voltages (70 V (AC) to 276 V (AC). The combination of PFC and resonant controller in one IC makes the TEA1716 suitable for compact power supplies with a high level of integration and functionality.

2.4 Features and benefits

2.4.1 General features

- Integrated PFC and HBC controllers
- Universal mains supply operation (70 V to 276 V (AC))
- High level of integration resulting in a low external component count and a cost effective design
- Enable input (enable only PFC or both PFC and HBC controllers)
- On-chip high-voltage start-up source
- Standalone operation or IC supplied from external DC source
- Low IC power consumption during burst mode operation

2.4.2 PFC controller features

- Boundary mode operation using on-time control
- Valley/zero voltage switching for minimum switching losses
- Frequency limiting to reduce switching losses
- Accurate boost voltage regulation
- Burst mode switching with soft-start and soft-stop

2.4.3 HBC controller features

- Integrated high-voltage level shifter
- Adjustable minimum and maximum frequency
- Maximum 500 kHz half-bridge switching frequency
- Adaptive non-overlap time
- Burst mode switching

2.4.4 Protection features

- Safe restart mode for system fault conditions
- General latched protection input for output overvoltage protection or external temperature protection
- Protection timer for time-out and restart
- OverTemperature Protection (OTP)
- Soft (re)start for both controllers
- UnderVoltage Protection (UVP) for mains (brownout), boost and IC supply
- Overcurrent regulation and protection for both controllers
- Accurate overvoltage protection for boost voltage
- Capacitive mode protection for HBC controller

2.5 Protection

The TEA1716 provides several protection functions that combine detection with a response to solve a problem such as overpower or bad half-bridge switching. Regulating the frequency can solve the problem or keep the IC operating safely until it is stopped and restarted (timer function).

2.6 Applications

- High-power adapters
- Low-power adapters
- Slim notebook adapters
- Computer power supplies
- LCD television
- Plasma television
- Office equipment
- Server supplies
- Professional lighting

3. Pin overview

Table 2. TEA1716 pin Overview

Pin number	Pin name	Description
1	COMPPFC	Frequency compensation for the PFC control loop Externally connected filter with typical values: 150 nF (33 kΩ + 470 nF)
2	SNSMAINS	Sense input for mains voltage Externally connected to resistive divided mains voltage This pin has four functions: • Mains enable level: $V_{start(SNSMAINS)}$ = 1.15 V • Mains stop level (brownout): $V_{stop(SNSMAINS)}$ = 0.9 V • Mains voltage compensation for the PFC control loop gain bandwidth • Fast latch reset: $V_{rst(SNSMAINS)}$ = 0.75 V The mains enable and mains stop level enable and disable the PFC. Enabling and disabling the resonant controller is based on the voltage on the SNSBOOST pin. The voltage on the SNSMAINS pin must be an averaged DC value, representing the AC line voltage. Do not use the SNSMAINS pin for sensing the phase of the mains voltage. An internal current source (33 nA) provides open-pin detection.
3	SNSAUXPFC	Sense input from an auxiliary winding of the PFC coil for demagnetization timing and valley detection to control the PFC switching. It is −100 mV level using a time-out of 50 μs. Connect the auxiliary winding to the pin via an impedance (recommendation: a 5.1 kΩ series resistor) to prevent damage of the input during surges (for example, lightning). An internal current source (33 nA) provides open-pin detection.
4	SNSCURPFC	Current sense input for PFC This input is used to limit the maximum peak current in the PFC core. The SNSCURPFC is a cycle-by-cycle protection. The PFC MOSFET is switched off when the level reaches 0.5 V. The internal logic controls a 60 μA current source connected to the pin. This current source is used to implement a soft-start and soft-stop function for the PFC to prevent audible noise in Burst mode. The pin is also used to enable the PFC. The PFC only starts when the internal current source (60 μA) is able to charge the soft-start capacitor to 0.5 V. A minimum soft-start resistor of 12 kΩ is required to ensure the enabling of the PFC. The value of the capacitor on the SNSCURPFC pin determines the soft-start and soft-stop timing in combination with the parallel resistor value.

Table 2. TEA1716 pin Overview *…continued*

Pin number	Pin name	Description
5	SNSOUT	Input for sensing the output voltage of the resonant converter indirectly. The SNSOUT pin is normally connected to an auxiliary transformer winding of HBC. The SNSOUT pin has two functions related to internal comparators: • Overvoltage protection: SNSOUT > 3.5 V; latched protection • Output Failed Start Protection (FSP): SNSOUT < 2.5 V; protection timer The protection timer is only active at start-up. It disables burst mode operation until the 2.5 V level is exceeded once. The pin also contains an internal switch to pull the voltage on the SNSOUT pin down to 0 V during burst mode operation (when not switching). This switching signal shows the burst mode timing and can be used for synchronizing external circuit functions. Before start-up the switch is activated shortly to reset the initial voltage on the SNSOUT pin to 0 V.
6	SUPIC	IC voltage supply input and output of the internal HV start-up source All internal circuits, except the high-voltage circuit, are directly or indirectly (via the SUPREG pin) supplied from this pin. The buffer capacitor on the SUPIC pin can be charged in several ways: • Internal High-Voltage (HV) start-up source • Auxiliary winding from HBC transformer or capacitive supply from switching half-bridge node • External DC supply, for example, a standby supply The IC enables operation when V_{SUPIC} reaches the 20 V (for a HV-start) or 15 V (for external supply) start level. It stops operating when the voltage drops under 13 V. A shutdown reset is activated at 7 V.
7	GATEPFC	Gate driver output for PFC MOSFET
8	PGND	Power ground Reference (ground) for HBC low-side and PFC driver.
9	SUPREG	Output of the internal regulator: 11.3 V. The supply created with this function is used for internal IC functions like the MOSFET drivers. It can also be used to supply an external circuit. The SUPREG pin can provide a current of at least 40 mA. The SUPREG pin becomes operational after pin SUPIC has reached its start level. The IC starts full operation when pin SUPREG has reached 10.7 V. UVP: If the SUPREG pin drops under 10 V after start-up, the IC stops operating. The current from the SUPIC pin is limited to 5.4 mA to allow recovery.
10	GATELS	Gate driver output for low-side MOSFET of HBC
11	n.c.	Not connected; high-voltage spacer

Table 2. TEA1716 pin Overview *…continued*

Pin number	Pin name	Description
12	SUPHV	High-voltage supply input for internal HV start-up source In a standalone power supply application, the SUPHV pin is connected to the boost voltage. The internal start-up source charges the capacitors on the SUPIC and SUPREG pins using a constant current. SUPHV operates at a voltage exceeding 25 V. Initially, the charge current is low (1.1 mA). When the voltage on the SUPIC pin exceeds the short circuit protection level of 0.65 V, the generated current increases to 5.1 mA. The source is switched off when the voltage on the SUPIC pin reaches 20 V, initiating a start-up operation. During the start-up operation, an auxiliary supply takes over the supply of the SUPIC pin. If the takeover is not successful, the source of the SUPHV pin is reactivated. A restart is executed (the voltage on the SUPIC pin is under 13 V).
13	GATEHS	Gate driver output for high-side MOSFET of HBC
14	SUPHS	High-side driver supply connected to an external bootstrap capacitor between the HB and SUPHS pins. The supply is obtained using an external diode between the SUPREG and SUPHS pins.
15	HB	Reference for the high-side driver GATEHS It is an input for the internal half-bridge slope detection circuit for adaptive non-overlap regulation and capacitive mode protection. The HB pin is externally connected to a half-bridge node between the MOSFETs of HBC.
16	n.c.	Not connected; high-voltage spacer
17	SNSCURHBC	Sense input for the momentary current of the HBC. If the voltage level (representing the primary current) is too high, internal comparators determine the regulation to a higher frequency ($V_{SNSCURHBC}$ = ±0.5 V) or to protection ($V_{SNSCURHBC}$ = ±1.75 V) by switching immediately to maximum frequency. The additional current from SNSCURHBC can compensate protection level variations due to HBC input voltage variations. The current leads to a voltage offset across the external series resistance value. The current measurement resistor and an extra series resistance which has a typical value of 1 kΩ normally provide this external series resistance.
18	SGND	Signal ground Reference (ground) for IC.
19	CFMIN	Oscillator pin The value of the external capacitor determines the switching frequency range of the HBC. A triangular voltage waveform is generated at C_{CFMIN} ($V_{l(CFMIN)}$ = 1 V and $V_{u(CFMIN)}$ = 3 V) to facilitate switching timing. A fixed minimum charge/discharging current of 150 μA determines the minimum frequency. During special conditions, the charge/discharging current is reduced to 30 μA to slow down the charging temporarily. The maximum frequency is determined using a fixed maximum charge/discharging current of 830 μA. An internal function limits the HBC operating frequency to 670 kHz.

Table 2. TEA1716 pin Overview *…continued*

Pin number	Pin name	Description
20	SNSBURST	Voltage sense input for burst mode operation Externally connected to SNSFB using a resistive divider When the voltage on SNSBURST drops under $V_{burst(SNSBURST)}$ (3.5 V), the HBC and PFC pauses its operation. When the voltage on SNSBURST increases to exceed $V_{burst(SNSBURST)}$ + internal hysteresis (3.53 V), HBC and PFC resume operation. The PFC resumes operation using a soft-start sequence. The HBC resumes operation without soft-start sequence. The burst mode transition level can be set using the values of the resistor divider. An internal switching current source of 3 μA creates an additional hysteresis in combination with the value of the resistor connected between SNSBURST and SNSFB. Using the total resistance value of the resistive divider, the total hysteresis on the SNSBURST pin can be set.
21	SNSFB	Sense input for HBC output regulation feedback voltage Normally, the SNSFB pin is connected via a pull-up resistor to the SUPREG pin and via an optocoupler to ground. These connections enable regulation of the voltage on the SNSFB pin. The regulation voltage range is between 4.1 V and 6.4 V. It corresponds with the maximum and minimum frequencies that the SNSFB pin controls. The SNSFB frequency range is limited to 60 % of the total frequency range. An internal voltage source of 7 V is connected to the SNSFB pin to obtain a correct start-up. It is only active at the initial start-up. When start-up is successful, the internal voltage source is switched off. The assumption is made when one of the following conditions are detected: • V_{SNSFB} > 8.25 V • V_{SNSOUT} > 2.5 V • $V_{SSHBC/EN}$ > 8.4 V The open-loop detection feature activates the protection timer when SNSFB exceeds 8.25 V. This voltage exceeding 8.25 V can only be obtained using the external pull-up resistor.

Table 2. TEA1716 pin Overview *…continued*

Pin number	Pin name	Description
22	SSHBC/EN	Combined soft-start/protection frequency control of HBC and IC enable input (PFC or PFC + HBC) Externally connected to a soft-start capacitor and an enable pull-down function The SSHBC/EN pin has three functions: • Enable PFC ($V_{SSHBC/EN}$ > 1 V) and PFC + HBC ($V_{SSHBC/EN}$ > 2 V) • Frequency sweep during soft-start from 3.2 V to 8 V • Frequency control during protection between 8 V to 3.2 V Seven internal current sources operate the frequency control. They depend on which of the following actions is required: • Soft-start + OverCurrent Protection (OCP): high/low charge current (160 μA/40 μA) + high/low discharge (160 μA/40 μA) • Capacitive mode regulation: high/low discharge current (1800 μA/440 μA) • General: Bias discharge current (5 μA)
23	RCPROT	Timer presetting for time-out and restart. The values of an externally connected resistor and capacitor determine the timing. Protection timer: One of the following protective functions activates the timer using a 100 μA charge current: • Overcurrent regulation (SNSCURHBC pin) • High-frequency protection • Open-loop protection (SNSFB pin) • Undervoltage failed start protection (SNSOUT pin); only at start-up The protection is activated when the level of 4 V is reached. The resistor discharges the capacitor and at 0.5 V, a restart is made. Restart timer: If a short-circuit protection event occurs on the SNSBOOST pin, the RCPROT capacitor is quickly charged using 2.2 mA. After the RCPROT voltage reaches 4 V, the capacitor is discharged and the IC restarts.
24	SNSBOOST	Sense input for boost voltage regulation (output voltage of the PFC stage) Externally connected to a resistive divided boost voltage. The SNSBOOST pin has four functions: • SNSBOOST pin short-circuit detection: $V_{SCP(SNSBOOST)} \leq 0.4$ V • Regulation of PFC output voltage: $V_{reg(SNSBOOST)} = 2.5$ V • PFC soft OVP (cycle-by-cycle): $V_{ovp(SNSBOOST)} \geq 2.63$ V • HBC Brownout function: – Converter enable voltage $V_{start(SNSBOOST)} = 2.3$ V – Converter disable voltage $V_{UVP(SNSBOOST)} = 1.6$ V

4. Application diagram

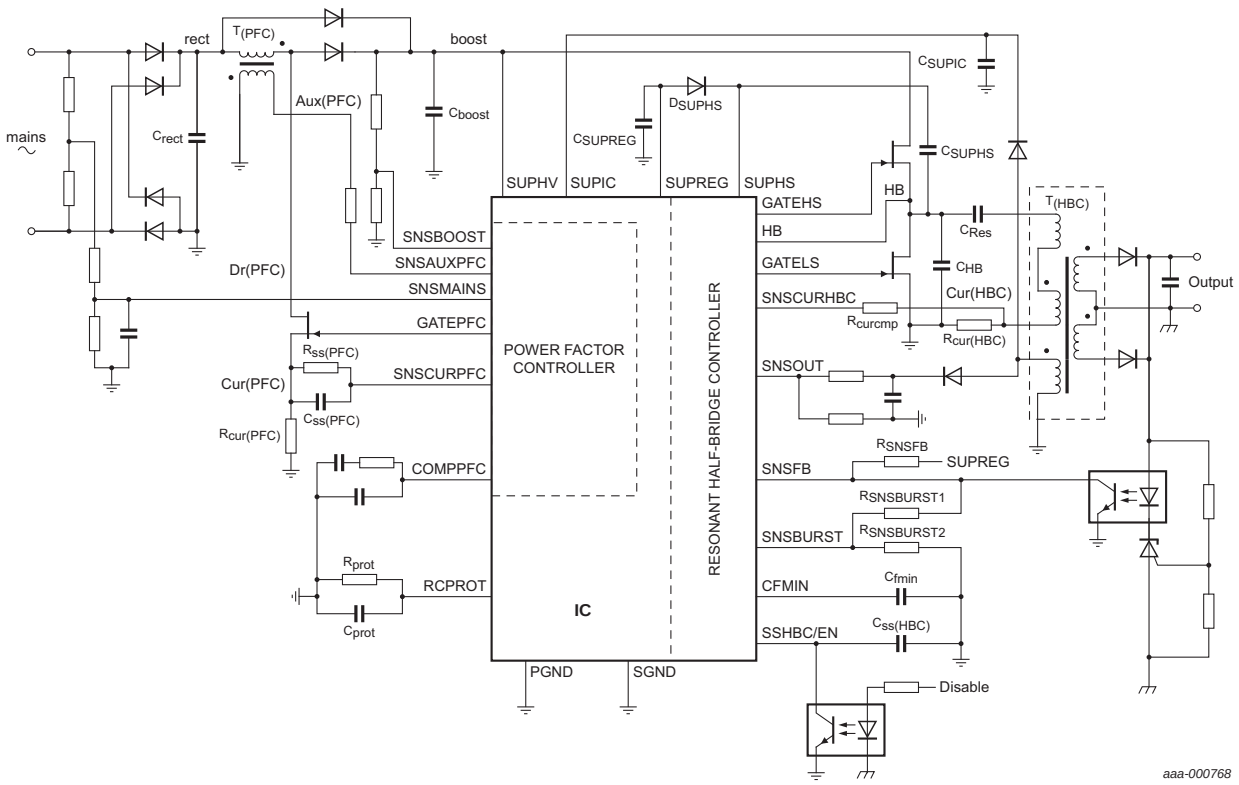
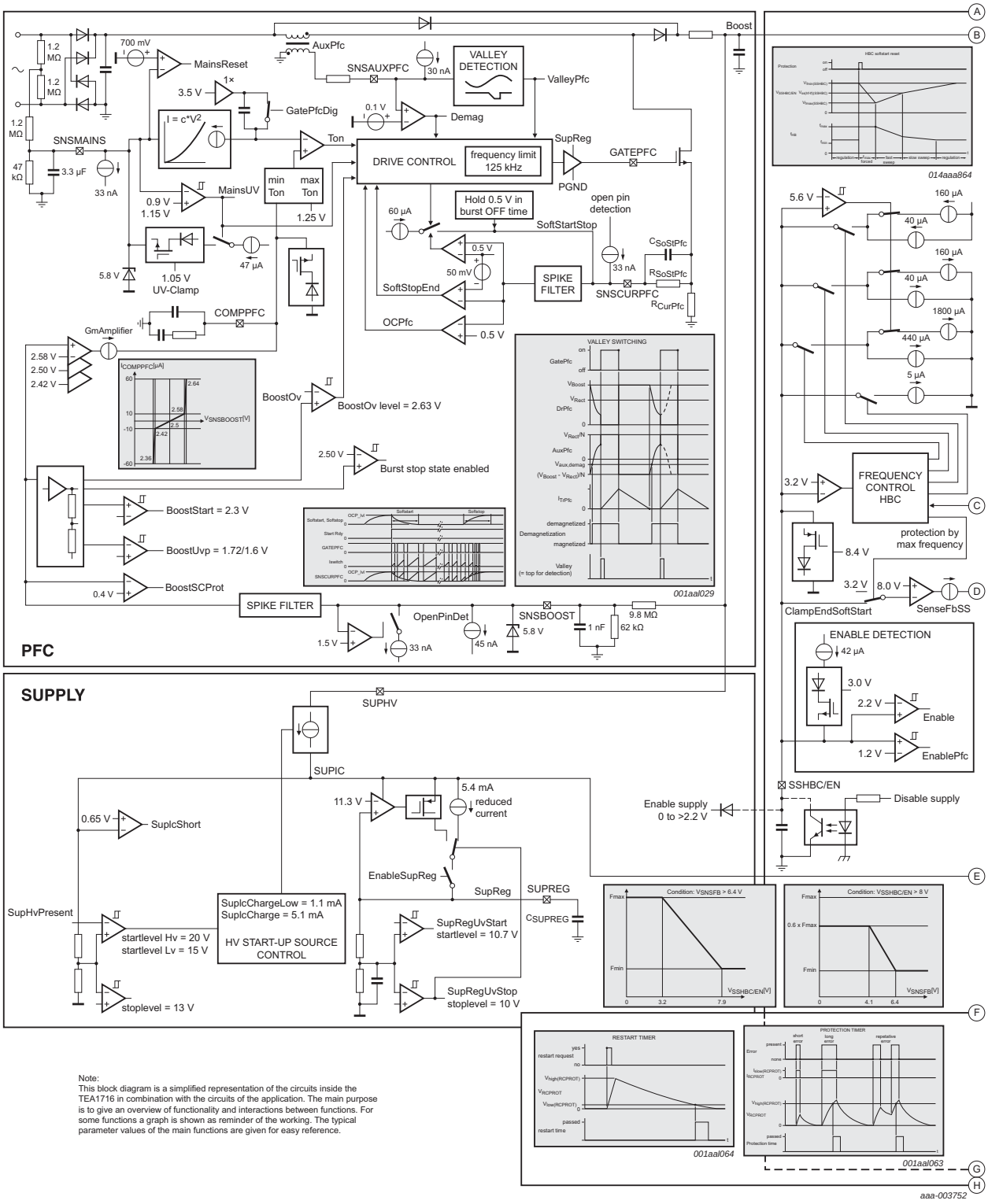


Fig 1. Basic application diagram TEA1716

5. Block diagram



Note:
This block diagram is a simplified representation of the circuits inside the TEA1716 in combination with the circuits of the application. The main purpose is to give an overview of functionality and interactions between functions. For some functions a graph is shown as reminder of the working. The typical parameter values of the main functions are given for easy reference.

Fig 2. TEA1716T block diagram - part 1

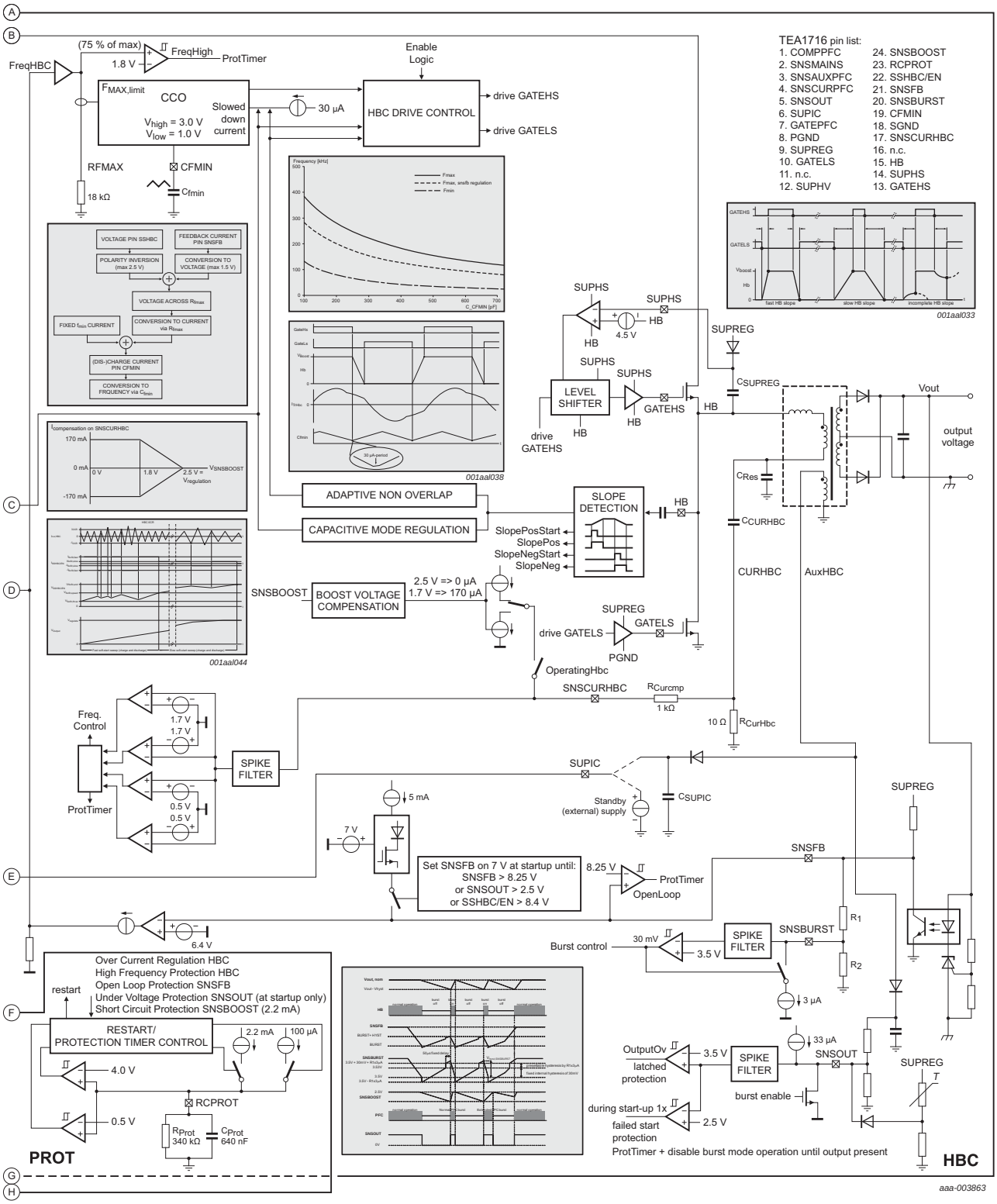


Fig 3. TEA1716T block diagram - part 2

6. Supply functions

6.1 Basic supply system overview

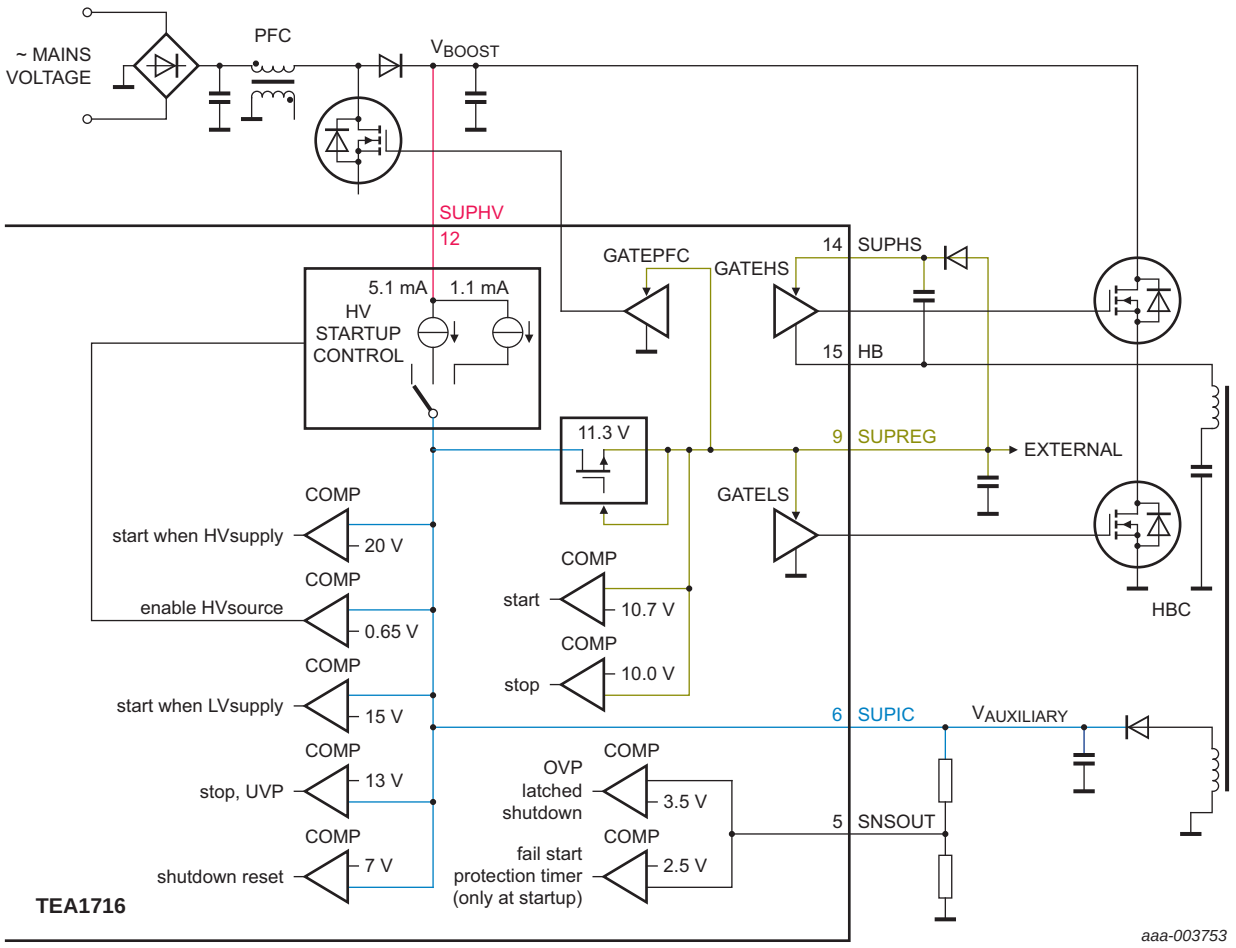


Fig 4. Basic overview internal IC supplies

6.1.1 TEA1716 supplies

The main supply for the TEA1716 is the SUPIC pin.

The SUPHV pin can be used to charge the capacitor on the SUPIC pin to start the supply. During operation, a supply voltage is applied to the SUPIC pin and the SUPHV source is switched off. The SUPHV source is only switched on again at a new start-up.

The internal regulator SUPREG generates a fixed voltage of 11.3 V to supply the internal MOSFET drivers GATEPFC, GATELS and GATEHS. To supply GATEHS, a bootstrap function using an external diode is used to make supply SUPHS.

SUPIC and SUPREG also supply other internal TEA1716 circuits.

6.1.2 Supply monitoring and protection

The supply voltages are monitored internally to determine when to initiate certain actions, like starting, stopping or protection.

In several applications, V_{SUPIC} can also be used to monitor the HBC output voltage by protection input SNSOUT. For example, using a voltage from an auxiliary winding construction.

6.1.3 Low-voltage IC supply (SUPIC pin)

The SUPIC pin is the main IC supply. All internal circuits are either directly or indirectly supplied from this pin, except the SUPHV circuit.

6.1.4 SUPIC start-up

Connect the SUPIC pin to an external buffer capacitor. The buffer capacitor can be charged in several ways:

- Internal High-Voltage (HV) start-up source
- Auxiliary supply, for example, from a winding on the HBC transformer
- External DC supply, for example, from a standby supply

The IC starts operating when the voltage on the SUPIC pin and the SUPREG pin reach the start level. The start level value of the SUPIC pin voltage (V_{SUPIC}) depends on the condition of the SUPHV pin.

6.1.4.1 SUPHV ≥ 25 V (V_{max})

$V_{SUPHV} \geq 25$ V is typically in a standalone application where the HV start-up source initially charges the capacitor on the SUPIC pin. The V_{SUPIC} start level is 20 V. The difference between start and stop levels (13 V) is used to allow C_{SUPIC} to discharge until the auxiliary supply can take over the IC supply.

6.1.4.2 SUPHV pin not connected or used

When the TEA1716 is supplied from an external DC supply, this is the case. The SUPIC start level is now 15 V. During start-up and operation, the external DC supply continuously supplies the IC. Do not connect the SUPHV pin for this kind of application.

6.1.5 SUPIC stop, undervoltage protection and short circuit protection

The IC stops operating when the SUPIC voltage drops under 13 V, the SUPIC pin UVP. While in the process of stopping, the HBC continues until the low-side MOSFET is active, before stopping the PFC and HBC operation.

SUPIC has a low-level detection at 0.65 V to detect a short circuit to ground. This level also controls the current source from the SUPHV pin.

6.1.6 SUPIC current consumption

The current consumption of the SUPIC pin depends on the state of the TEA1716.

- Disabled IC state:

  When the IC is disabled via the SSHBC/EN pin, the current consumption is low at 250 μA.

- C_{SUPIC} charge, C_{SUPREG} charge, thermal hold, restart and shutdown state:

  Only a small part of the IC is active during the charging of C_{SUPIC} and C_{SUPREG} before start-up, during a restart sequence or shutdown after activation of the protection. The PFC and HBC are disabled. The current consumption from SUPIC in these states is low at 400 μA.

- Boost charge state:

  PFC is switching and HBC is still off. The high-voltage start-up source current is large enough to supply SUPIC. The current consumption is therefore, under the maximum current (5.1 mA) that SUPHV can deliver.

- Operating supply state:

  Both PFC and HBC are switching. The current consumption is higher. The MOSFET drivers are dominant in the current consumption (see Section 6.4.5). Especially during the soft-start of the HBC (when the switching frequency is high) and also during normal operation. Initially, the stored energy in the SUPIC capacitor delivers the SUPIC current. After a short time, the supply source on SUPIC during normal operation takes over the supply of SUPIC.

- Burst mode operation:

  While the converters are not switching in the burst stop state, several internal circuits are switched off to reduce current consumption. Before starting a new burst, the internal circuits are switched on again during a period of 50 μs. In burst stop state, the current consumption is 700 μA.

6.2 SUPIC supply using HBC transformer auxiliary winding

6.2.1 Start-up using the SUPHV pin

In a standalone power supply application, the IC can be started using a high-voltage source such as the rectified mains voltage. The SUPHV high-voltage input pin can be connected to the boost voltage (PFC output voltage) for this purpose.

C_{SUPIC} and C_{SUPREG} are charged using the internal HV start-up source which delivers a constant current from the SUPHV pin to the SUPIC pin. SUPHV is operational at a voltage > 25 V.

When V_{SUPIC} is under the short-circuit protection level (0.65 V), the current from SUPHV is low (1.1 mA). This feature limits the dissipation in the HV start-up source when SUPIC is shorted to ground.

During normal conditions, SUPIC quickly exceeds the protection level and the HV start-up source switches to normal current (5.1 mA). The HV start-up source switches off when SUPIC has reached the start level (20 V). The current consumption from SUPHV is low (7 μA) when switched off.

When the voltage on the SUPIC pin has reached the start level (20 V), C_{SUPREG} is charged. When the SUPREG pin voltage reaches the level of 11.3 V, it enables operation of HBC and PFC.

The HBC transformer auxiliary winding supply must take over the supply of SUPIC before it discharges C_{SUPIC} to the SUPIC undervoltage stop level (13 V).

6.2.2 Block diagram for SUPIC start-up

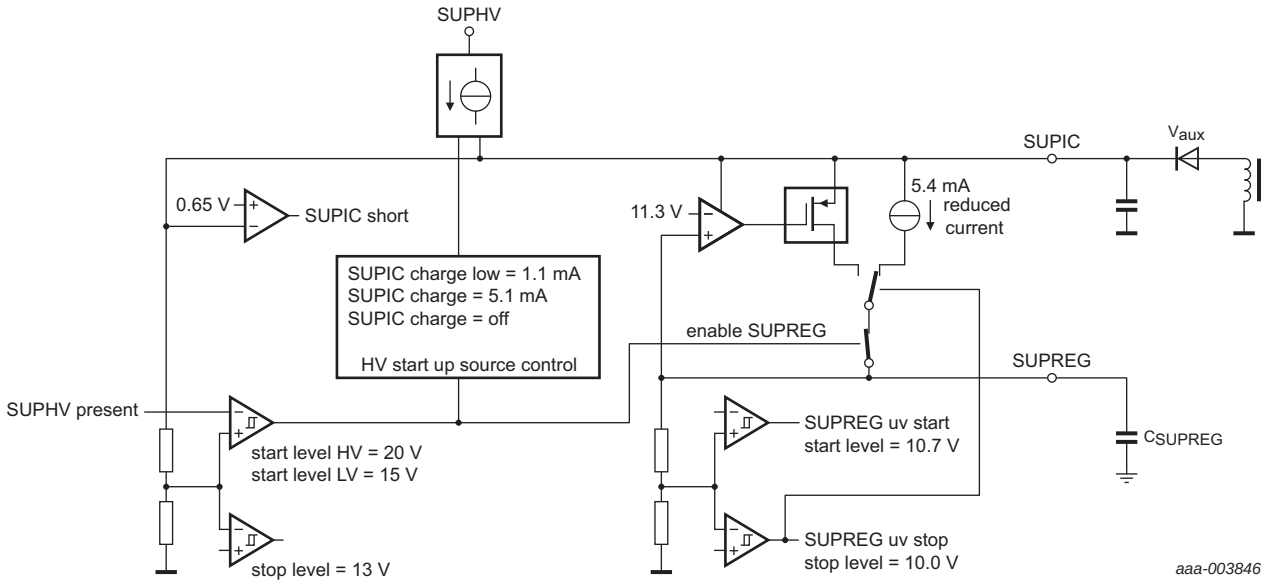


Fig 5. The SUPIC and SUPREG pins start-up using the SUPHV pin and the auxiliary supply

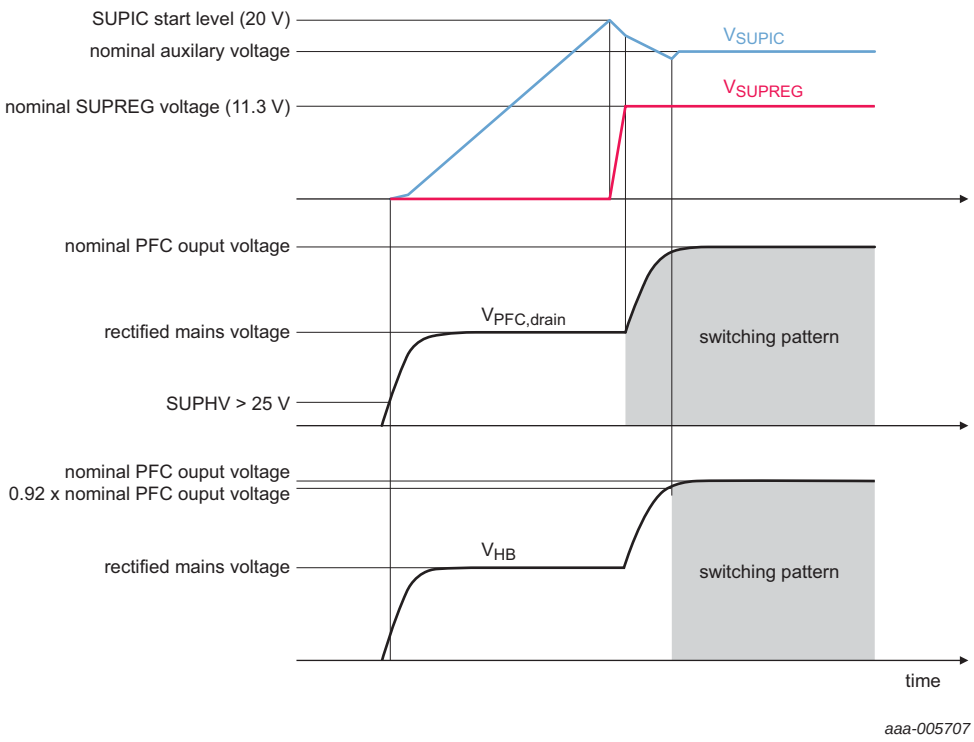


Fig 6. Typical start-up sequence using SUPHV current source

6.2.3 Auxiliary winding on the HBC transformer

An auxiliary winding on the HBC transformer can be used to obtain a supply voltage for the SUPIC pin during operation. As the SUPIC pin has a wide operational voltage range (13 V to 38 V), it is not a critical parameter.

However:

- The voltage on the SUPIC pin must be low to minimize power consumption.
- During burst mode operation and because of the supply's low current consumption, the bursts repetition frequency can become very low (for example at no output load). This behavior can cause an imbalance in the half-bridge switching leading to a serious drop in the auxiliary supply for the SUPIC pin. To maintain the HBC load balance and avoid the extra SUPIC pin voltage drop, replace the single-side rectified auxiliary supply (see Figure 5) with a center-tapped construction. The center-tapped construction comprises two windings and two diodes.
- The auxiliary winding supply must be an accurate representation of V_O to use the auxiliary winding voltage for the IC supply and HBC output voltage measurement (using SNSOUT).Physically place the transformer auxiliary winding on the secondary output side to ensure a good coupling.
- When mains insulation is included in the transformer, it can affect the auxiliary winding construction. Triple insulated wire is needed when the transformer auxiliary winding is placed on the transformer construction secondary area.

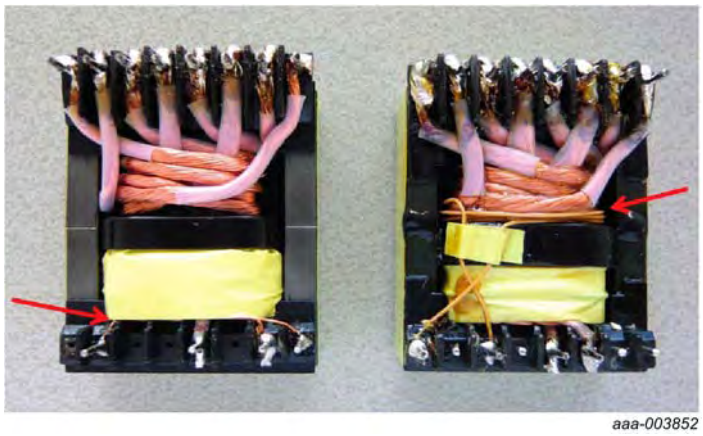


Fig 7. Transformer auxiliary winding on primary side (left, not preferred) and secondary side (right)

6.2.3.1 Auxiliary winding for the SUPIC and SNSOUT pins

The SNSOUT input provides a combination of three functions:

- Overvoltage protection: V_{SNSOUT} > 3.5 V, latched
- Output failed start protection: V_{SNSOUT} < 2.5 V; only active at start-up. At start-up, it disables burst mode operation until the 2.5 V level has been exceeded once
- An internal switch to pull the SNSOUT voltage to 0 V during burst mode operation (during the period of not switching: the burst stop state): This switching signal shows the burst mode timing and can be used for synchronizing external circuit functions

Remark: See Section 12.3 for more information on the SNSOUT functions.

A circuit using one transformer auxiliary winding to combine the SUPIC supply and the output voltage monitoring using the SNSOUT pin, is often used.

An independent construction for the SUPIC and SNSOUT pins is also possible. This construction is applied when the SUPIC pin is supplied using a separate standby supply. In this situation, the auxiliary winding is only used for output voltage sensing.

It is possible to use the SNSOUT pin as a general-purpose protection input instead of output sensing (see Section 12.3.1.3).

In a combined SUPIC and SNSOUT function using a transformer auxiliary winding, a good representation of the output voltage for SNSOUT measurement can only be obtained after addressing several issues.

The advantage of a good coupling/representation of the auxiliary winding with the output windings is that a stable auxiliary voltage is obtained for the SUPIC pin. A low SUPIC voltage value can be designed more easily for the lowest power consumption.

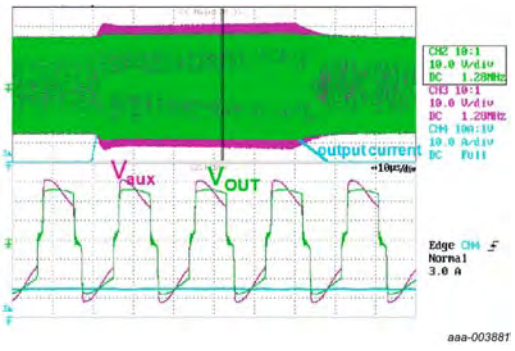
6.2.3.2 Auxiliary supply voltage variations because of output current

The HBC output causes variation on an auxiliary winding supply. At peak current loads, the regulation compensates the voltage drop across the series components in the HBC output stage (resistance and diodes). This results in a higher voltage on the windings at higher output currents because the higher currents cause a larger voltage drop across the series components.

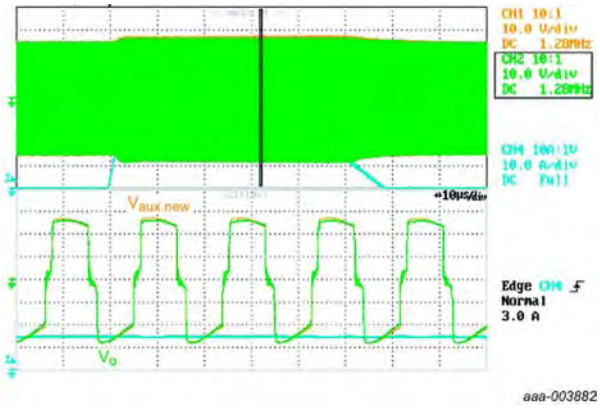
6.2.3.3 Voltage variations depending on auxiliary winding position: primary side component

V_{SNSOUT} and/or V_{SUPIC} can contain an amount of unwanted primary voltage component due to a less optimal position of the auxiliary winding. This component can seriously endanger the feasibility of the SNSOUT sensing function.

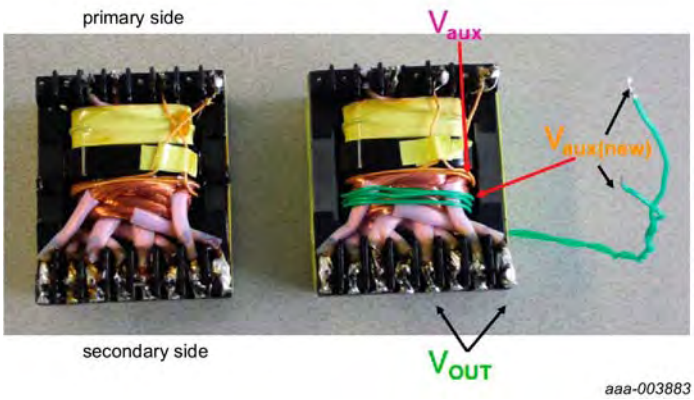
The coupling of the auxiliary winding with the primary winding must be as small as possible to avoid a primary voltage component on the auxiliary voltage. Place the auxiliary winding on the secondary windings and as physically remote as possible from the primary winding. The differences in results are shown in Figure 8 using comparison of the secondary side position.



a. Bad coupling V_{aux} to V_{out} at high output current



b. Correct coupling $V_{aux(new)}$ to V_{out} at high output current



c. Photograph example

Fig 8. Example of a (new) position of the auxiliary winding for a better coupling to the output voltage

6.3 SUPIC pin supply using external voltage

6.3.1 Start-up

When an external DC supply supplies the TEA1716, the SUPHV pin can remain unconnected. The SUPIC start-up level is now 15 V.

When the voltage on the SUPIC pin exceeds 15 V, the internal regulator is activated and charges C_{SUPREG}.

When the voltage on the SUPREG pin ≥ 10.7 V, GATELS is switched on for the bootstrap function to charge C_{SUPHS}. At the same time, the PFC operation is internally enabled. When all enable conditions are met, the TEA1716 starts the PFC function. When V_{boost} reaches approximately 90 % (SNSBOOST ≥ 2.3 V) of its nominal value, the HBC is started.

6.3.2 Stop

Operation of the TEA1716 can be stopped by switching off the external source for the SUPIC pin. When the voltage level on the SUPIC pin drops under 13 V, operation is stopped.

If the device is in the shutdown state (because of protection) and V_{SUPIC} drops under 7 V, the state is reset using internal logic.

6.4 SUPREG pin

The SUPIC pin has a wide voltage range for easy application. However, it cannot be used to supply the internal MOSFET drivers directly because the allowed gate voltage of many external MOSFETs is exceeded.

The TEA1716 contains an integrated series stabilizer to avoid this issue and create a few other benefits. The series stabilizer generates an accurate regulated voltage on the external buffer capacitor of the SUPREG pin.

The stabilized SUPREG voltage is used for:

- Supply of the internal PFC driver
- Supply of the internal low-side HBC driver
- Supply of the internal high-side driver using external components
- Reference voltage for optional external circuits
- Supply voltage for optional external circuits

The series stabilizer for the SUPREG pin is enabled after C_{SUPIC} has been charged. In this way, optional external circuitry on the SUPREG pin does not consume part of the start-up current during SUPIC pin (C_{SUPIC}) charging. The capacitor on the SUPIC pin acts as a buffer when charging the SUPREG pin and starting up the IC.

The SUPREG voltage must reach $V_{start(SUPREG)}$ and V_{SUPIC} its start-up level before the IC starts operating, ensuring that the external MOSFETs receive sufficient gate drive.

The SUPREG pin has an UnderVoltage Protection (UVP). When V_{SUPREG} drops under the 10.0 V, two actions take place:

- The IC stops operating to prevent unreliable switching because the gate driver voltage is too low. The PFC controller stops switching immediately, but the HBC keeps operating until the low-side stroke is active.
- The maximum current from the internal SUPREG series stabilizer is reduced to 5.4 mA. If there is an overload at the SUPREG pin using an external DC supply for the SUPIC pin, this action reduces the dissipation in the series stabilizer.

It is important to realize that the SUPREG pin can only source current.

The drivers of GATELS and GATEPFC are supplied using the SUPREG pin and draw current from it during operation depending on the operating condition. Some changes in value can be expected depending on current load and temperature:

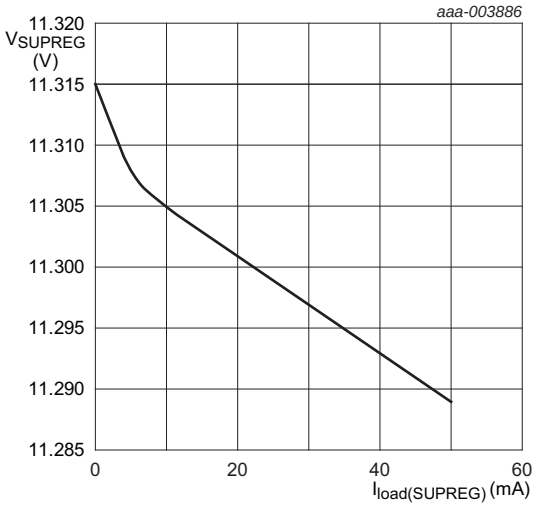


Fig 9. Typical SUPREG voltage as a function of load current

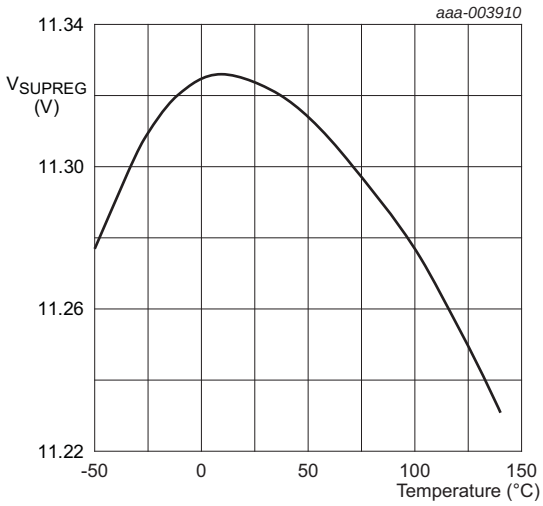


Fig 10. Typical SUPREG voltage as a function of temperature

6.4.1 Block diagram of SUPREG regulator

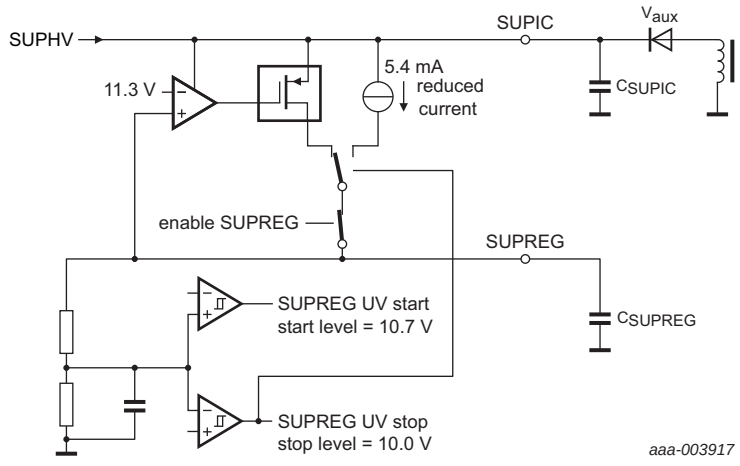


Fig 11. Block diagram of internal SUPREG regulator

6.4.2 SUPREG at start-up

SUPREG is supplied from the SUPIC pin. SUPIC is the unregulated external power source that provides the input voltage for the internal voltage regulator SUPREG.

At start-up the SUPIC pin must reach a specific voltage level before SUPREG is activated:

- Using the internal HV supply, SUPREG is activated when the SUPIC pin voltage ≥ 20 V.
- Using an external low-voltage supply, SUPREG is activated when the SUPIC pin voltage ≥ 15 V.

6.4.3 Supply voltage for the output drivers (SUPREG pin)

The TEA1716 has a powerful output stage for GATEPFC and GATELS to drive large MOSFETs. The SUPREG pin supplies a fixed voltage to the internal drivers.

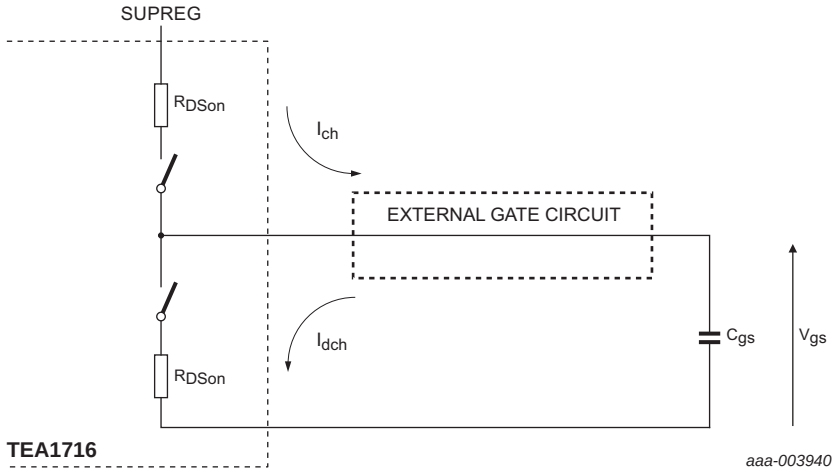


Fig 12. Simplified model of MOSFET drive

Figure 12 shows that current is taken from the SUPREG pin when the external MOSFET is switched on by charging the gate to a high voltage.

The shape of the current from the SUPREG pin at switch-on is related to:

- The supply voltage for the internal driver (11.3 V)
- The characteristics of the internal driver
- Charging the gate capacitance
- The gate threshold voltage for the MOSFET to switch on
- The external circuit to the gate

Remark: The switching moments of the GATEPFC and GATELS pins are independently in time. Charging C_{SUPHS} for the GATEHS function is synchronized in time with the GATELS pin but has a different shape because of the bootstrap function.

6.4.4 Supply voltage for the output drivers (SUPHS pin)

An external bootstrap buffer capacitor supplies the high-side driver. The bootstrap capacitor is connected between the high-side reference the HB pin and the high-side driver supply input the SUPHS pin. An external diode from the SUPREG pin charges this capacitor when HB is low. Selecting a suitable external diode can minimize the voltage drop between the SUPREG and SUPHS pins. Minimizing the voltage drop is especially important when using a MOSFET that requires a large amount of gate charge and/or when switching at high frequencies.

Instead of using the SUPREG pin as the power source for charging the SUPHS pin, another supply source can be used. In such a construction, it is important to check for correct start/stop sequences and to prevent that the SUPHS voltage exceeds 14 V (referenced to HB).

Remark: The current drawn from the SUPREG pin to charge C_{SUPHS} differs (in time and shape) from the current that the GATEPFC and GATELS drivers draw for each cycle.

6.4.4.1 Initial charging of the SUPHS pin

At start-up, the bootstrap function sets the GATELS high to switch on the low-side MOSFET to charge C_{SUPHS}. While C_{SUPHS} is being charged, the GATELS pin is switched on for charging. The PFC operation is started. The time between start of the charging and the start of the HBC operation is normally sufficient to charge C_{SUPHS} completely. The HBC operation starts when the $V_{SNSBOOST}$ reaches 2.3 V which is approximately 90 % of the nominal V_{boost}.

6.4.4.2 Current load on the SUPHS pin

The current taken from the SUPHS pin consists of two parts:

- Internal MOSFET driver GATEHS
- Internal circuit to control the GATEHS pin (37 μA, quiescent current)

Figure 13 shows that the driver GATEHS draws current at switch-on. The shape of the current from the SUPHS pin at switch-on is related to:

- The value of the supply voltage for the internal driver
- The characteristics of the internal driver
- The gate charged capacitance
- The gate switch-on threshold voltage for the MOSFET
- The external circuit to the gate

The voltage on the SUPHS pin can vary.

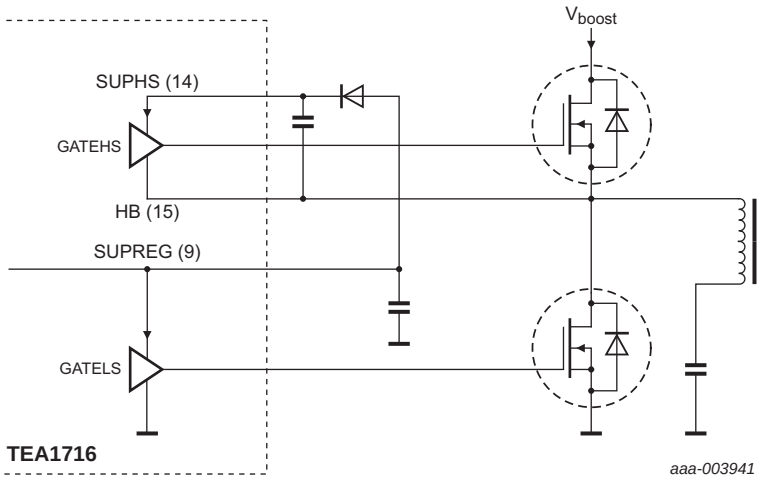


Fig 13. Typical application of SUPHS

6.4.4.3 Lower voltage on the SUPHS pin

During normal operation, each time the half-bridge node (HB) is switched to ground level, the bootstrap function charges C_{SUPHS}. The voltage value between the HB and SUPHS pins is normally lower than the voltage on the SUPREG pin (or other bootstrap supply input) because of the voltage drop across the bootstrap diode.

The voltage drop across the bootstrap diode is directly related to the amount of current that is required to charge C_{SUPHS}. The resulting voltage between the SUPHS and HB pins depends also on the time available for charging.

A large voltage drop occurs when an external MOSFET with a large gate capacitance has to be switched at high frequency (high current + short time).

During burst mode operation, a (too) low voltage on the SUPHS pin can occur. In burst mode, there are (long) periods of not switching. Therefore, long periods of no charging of the SUPHS pin can occur. During this time, the circuit C_{SUPHS} slowly discharges the supply voltage capacitor. When a new burst starts, the SUPHS voltage is lower than during normal operation. During the first switching cycles, C_{SUPHS} is recharged to its normal level. At low output power during burst mode, the switching frequency is normally rather high. The high switching frequency limits fast recovery of the voltage between the SUPHS and HB pin.

Although in most applications the voltage drop is limited, it is an important issue for evaluation. The voltage drop can influence the selection of the best diode type for the bootstrap function and the value of the SUPHS pin buffer capacitor.

6.4.4.4 SUPHS and HB voltage limits

The HB node and the SUPHS node are closely related because the internal high-voltage circuit is supplied using the voltage between these nodes. See Figure 13. The HB voltage limits are given related to the limits for the voltage on SUPHS.

The values for HB can be derived from the voltage limits specified for SUPHS using the practical voltage between both nodes: V_{SUPHS} to V_{HB}.

Table 3. Limiting values defined for V_{SUPHS} and V_{HB} in the data sheet

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SUPHS}	voltage on pin SUPHS	DC	–0.4	+570	V
		t < 0.5 s	–0.4	+630	V
		referenced to the HB pin	–0.4	+14	V

The voltage on HB (V_{HB}) is limited using the voltage restrictions on V_{SUPHS}.

V_{HB} (pin15):

- Min = –0.4 V – (V_{SUPHS} – V_{HB}) V
- Max (DC) = +570 V – (V_{SUPHS} – V_{HB}) V
- Max (t < 0.5 s) = +630 V – (V_{SUPHS} – V_{HB}) V

For example: If the high side supply = V_{SUPHS} – V_{HB} = 10 V, the minimum voltage allowed on HB = –10.4 V. Then Max (DC) = +570 V – 10 V = +560 V and Max (t < 0.5 s) = +630 V – 10 V = +620 V

The limits for the voltage between SUPHS and HB (V_{SUPHS} – V_{HB}) are given in Table 3:

- Min = –0.4 V
- Max = 14 V

6.4.5 MOSFET drivers consuming SUPIC power

The GATEPFC, GATELS and GATEHS drivers charge the gate capacitances of the external MOSFETs. During operation the GATEPFC, GATELS and GATEHS drivers are a major part of the power consumption from the SUPIC pin. The amount of energy required in time is linear to the switching frequency. Often, for the MOSFETs used, the total charge is specified for certain conditions. Using this figure an estimation can be made for the amount of current required from the SUPIC and SUPREG pins. In the TEA1716, the SUPREG pin supplies the GATELS and GATEHS pins. The SUPIC pin directly supplies the GATEPFC pin.

GATELS and GATEHS (driving a total of two MOSFETs):

$$\Delta I_{SUPIC} = 2 \times Q_{gate} \times f_{bridge} \quad (1)$$

Example:

- Q_{gate} = 40 nC
- f_{bridge} = 100 kHz

$$\Delta I_{SUPIC} = 2 \times 40\ nC \times 100\ kHz = 8\ mA$$

Remark: The calculated value is higher than the practical value because the switching operation deviates from the MOSFET specification for Q_{gate}.

GATEPFC:

$$\Delta I_{SUPIC} = Q_{gate} \times f_{PFC} \quad (2)$$

Example:

- Q_{gate} = 40 nC
- f_{PFC} = 100 kHz

$$\Delta I_{SUPIC} = 40\ nC \times 100\ kHz = 4\ mA$$

6.4.6 SUPREG supply voltage for other circuits

The regulated voltage from SUPREG can also be used as a regulated supply for an external circuit. The load of the external circuits affects the start-up time and the total load (IC plus external circuit) of SUPREG during operation.

6.4.6.1 Current available for supplying an external circuit from SUPREG

The total current available from the SUPREG pin is a minimum of 40 mA. To determine how much current is available for an external circuit, the current the IC is using must be known.

$$I_{SUPREG\_for\_external} = 40\ mA - I_{SUPREG\_for\_IC} \quad (3)$$

The MOSFET drivers GATELS and GATEHS consume most of the current from the SUPREG pin with respect to the IC. Other circuit parts in the IC consume a maximum current of 3 mA during normal mode operation. The current is only 0.7 mA during the burst-stop state in burst mode operation.

$$I_{SUPREG\_for\_IC} = I_{SUPREG\_for\_MOSFET\_drivers} + I_{SUPREG\_for\_other\_IC\_circuits} \quad (4)$$

$$I_{SUPREG\_for\_IC} = I_{SUPREG\_for\_MOSFET\_drivers} + 3\ mA\ max \quad (5)$$

$I_{SUPREG\_for\_MOSFET\_drivers}$ can be estimated using the method provided in Section 6.4.5.

6.4.6.2 An estimation using measurement

While supplying the circuit from an external power supply, the SUPIC pin current used is assumed as an initial approximation the current the IC circuits draw from the SUPREG pin. Using this value, an estimation can be made of the power available for external circuits.

Remark: The highest power consumption value is reached when the MOSFET drivers are switching at the highest frequency.

Example:

$$I_{SUPIC(max)\_measured} = 18\ mA$$

$$I_{SUPREG\_for\_IC} \approx I_{SUPIC(max)\_measured} = 18\ mA \quad (6)$$

$$I_{SUPREG\_for\_external} = 40\ mA - I_{SUPIC(max)\_measured} = 40\ mA - 18\ mA = 22\ mA$$

Remark: The voltage on the SUPREG pin must remain above the undervoltage protection level (10.0 V) to maintain full functionality. High external current loads during start-up can lead to problems.

6.5 Capacitor values on the SUPIC, SUPREG and SUPHS pins

A practical example is provided in Section 14.2.

6.5.1 The SUPIC pin

6.5.1.1 General

Use two types of capacitors on the SUPIC pin. An SMD ceramic type with a smaller value located close to the IC and an electrolytic type incorporating the major part of the capacitance.

6.5.1.2 Start-up

When a HV source provides the supply, a larger capacitor is required. The capacitor value must be large enough to handle the start-up before the auxiliary winding takes over the supply of the SUPIC pin.

Example of the value estimation:

- $I_{SUPIC(consumption\_during\_startup)}$ = 10 mA
- $\Delta V_{SUPIC(startup)}$ = 22 V − 15 V = 7 V
- $\Delta t_{vaux\ >15V}$ = 70 ms

$$C_{SUPIC} > I_{SUPIC(consumption\_during\_startup)} \times \frac{\Delta t_{vaux}}{\Delta V_{SUPIC(startup)}} = \quad (7)$$

$$10\ mA \times \frac{70\ ms}{7\ V} = 100\ \mu F$$

6.5.1.3 Normal operation

The main purpose of the capacitors on SUPIC is to keep the current load variations (for example gate drive currents) local at normal operation.

6.5.1.4 Burst mode operation

When burst mode operation is applied, the supply construction often uses an auxiliary winding and start-up from an HV source. While in the burst mode, there is a long period during which the auxiliary winding is not able to charge C_{SUPIC}. There is no HBC switching time between two bursts. The capacitor value on SUPIC must be large enough to keep the voltage above 13 V to prevent activating the SUPIC undervoltage stop level.

Example of a value estimation:

- $I_{SUPIC(between2bursts)}$ = 4 mA
- $\Delta V_{SUPIC(burst)} = V_{aux(burst)}$ − 15 V = 19 V − 15 V = 4 V
- $\Delta t_{(between2bursts)}$ = 25 ms

$$C_{SUPIC} > I_{SUPIC(between2bursts)} \times \frac{\Delta t_{between2bursts}}{\Delta V_{SUPIC(burst)}} = 4\ mA \times \frac{25\ ms}{4\ V} = 25\ \mu F \quad (8)$$

6.5.2 The SUPREG pin

The capacitor on SUPREG must not be much larger than the capacitor on SUPIC to support charging of SUPREG during an HV source start. This size difference prevents a severe voltage drop on the SUPIC pin due to the charging C_{SUPREG}. If the SUPIC pin is supplied using an external (standby) source, this point is not relevant.

The SUPREG pin supplies the current of the gate drivers. Using an SMD ceramic capacitor and a supporting electrolytic capacitor can keep current peaks local. This set-up is required to provide sufficient capacitance preventing a voltage drop during high current loads. The value of the capacitor on SUPREG must be larger than the total capacitance of the driven MOSFETs to prevent significant voltage drop. The total capacitance includes the SUPHS parallel load and bootstrap capacitor construction.

When considering the internal voltage regulator, the value of the capacitance on SUPREG must be ≥ 1 μF. Often a much larger value is used.

6.5.3 The SUPHS pin

The SUPHS capacitor must be much larger than the gate capacitance to support charging the gate of the high side MOSFET. This set-up prevents the gate charge causing a significant voltage drop on the SUPHS pin. When burst mode is applied, 37 μA is discharged from C_{SUPHS} during the time between two bursts.

7. MOSFET drivers: GATEPFC, GATELS and GATEHS pins

The TEA1716 provides three outputs for driving external high-voltage power MOSFETs:

- The GATEPFC pin for driving the PFC MOSFET
- The GATELS pin for driving the low-side of the HBC MOSFET
- The GATEHS pin for driving the high-side of the HBC MOSFET

7.1 The GATEPFC pin

The TEA1716 has a strong output stage for PFC to drive a high-voltage power MOSFET. SUPIC supplies the GATEPFC function.

7.2 The GATELS and GATEHS pins

Both drivers have identical driving capabilities for the gate of an external high-voltage power MOSFET. The low-side driver is referenced to the PGND pin and is supplied from the SUPREG pin. The high-side driver has a floating connection to the midpoint of the external half-bridge. It is referenced to HB. The high-side driver is supplied using a capacitor on the SUPHS pin. The capacitor is supplied using an external bootstrap function of the SUPREG pin. The bootstrap diode charges C_{SUPHS} is when the low-side MOSFET is on.

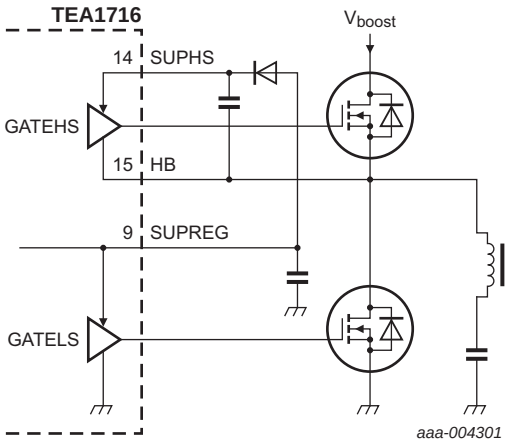


Fig 14. Supply system for GATELS and GATEHS

Both HBC drivers have a strong current source capability and an extra strong current sink capability. In general HBC operation, fast switch-on of the external MOSFET is not critical, as the HB node swings automatically to the correct state after switch-off. Fast switch-off, however, is important to limit switching losses and prevent delay especially at high frequency.

7.3 Supply voltage and power consumption

See Section 6.4.3 and Section 6.4.5 for a description of the supply voltages and power consumption by the MOSFET drivers.

7.4 General subjects on MOSFET drivers

7.4.1 Switch-on

The time to switch on depends on:

- The supply voltage for the internal driver
- The characteristic of the internal driver
- Charging the gate capacitance
- The gate threshold voltage for the MOSFET to switch on
- The external circuit to the gate

7.4.2 Switch-off

The time to switch off depends on:

- The characteristic of the internal driver
- Discharging the gate capacitance
- The voltage on the gate just before discharge
- The gate threshold voltage for the MOSFET to switch off
- The external circuit to the gate

The internal driver can sink more current than it can source because the timing for switching off the MOSFET is more critical than switching it on. At higher frequencies and/or short on-time, timing becomes more critical for correct switching. Sometimes, a compromise must be made between fast switching and EMI effects. A gate circuit between the driver output and the gate can be used to optimize the switching behavior.

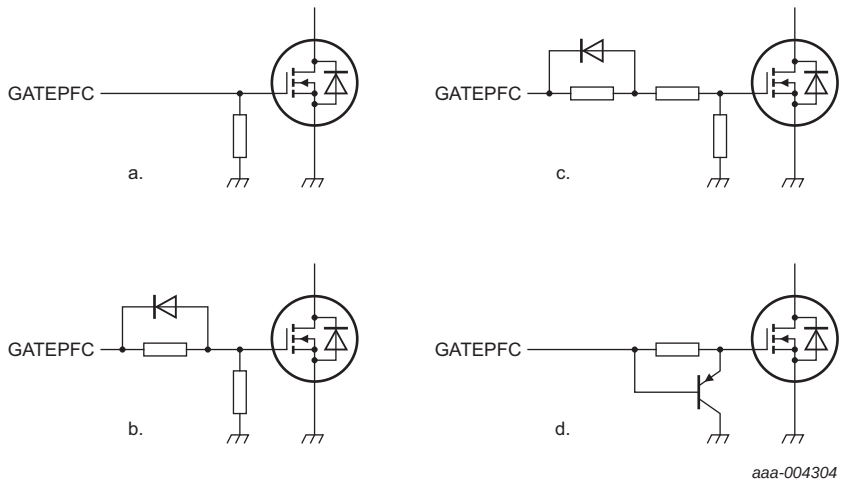


Fig 15. Examples of four different gate circuits

Switching on and off the MOSFETs using the drivers is approximated by alternating the charge and discharge of a MOSFET gate-source capacitance using a resistor (R_{DSon} of the internal driver MOSFET).

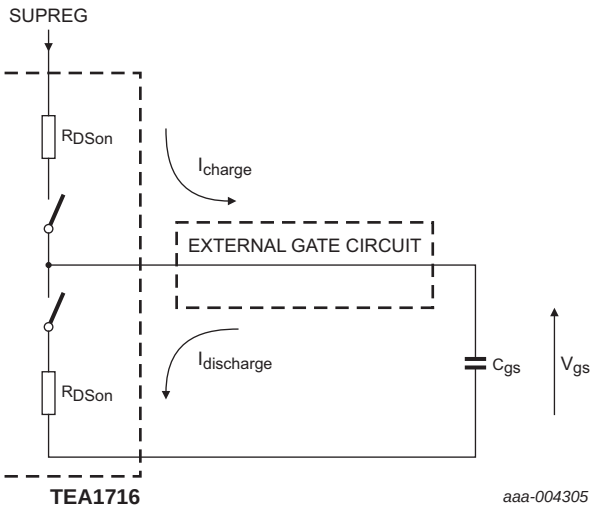


Fig 16. Simplified model of a MOSFET drive

7.5 Specifications

The main function of the internal MOSFET drivers is to source and sink current to switch on and off the external MOSFET.

The amount of current that can be sunk and sourced is specified to show the capability of the internal driver.

The simplified model in Figure 16 demonstrates that the charge and discharge current values depend on the supply and gate voltage conditions. The source current value is highest when the supply voltage is highest and the gate voltage 0 V. The sink-current value is highest when the gate voltage is highest.

Table 4. PFC and HBC driver specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PFC driver (GATEPFC pin)						
$I_{source(GATEPFC)}$	source current on pin GATEPFC	$V_{GATEPFC}$ = 2 V	-	–0.6	-	A
$I_{sink(GATEPFC)}$	sink current on pin GATEPFC	$V_{GATEPFC}$ = 2 V	-	0.6	-	A
		$V_{GATEPFC}$ = 10 V	-	1.4	-	A
HBC high-side and low-side driver (GATEHS and GATELS pins)						
$I_{source(GATEHS)}$	source current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 4 V	-	–310	-	mA
$I_{source(GATELS)}$	source current on pin GATELS	$V_{GATELS} - V_{PGND}$ = 4 V	-	–310	-	mA
$I_{sink(GATEHS)}$	sink current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 2 V;	-	560	-	mA
		$V_{GATEHS} - V_{HB}$ = 11 V	-	1.9	-	A
$I_{sink(GATELS)}$	sink current on pin GATELS	$V_{GATELS} - V_{PGND}$ = 2 V	-	560	-	mA
		$V_{GATELS} - V_{PGND}$ = 11 V	-	1.9	-	A

The supply voltage from the SUPREG pin for GATELS is constant at 11.3 V. The supply voltage for the GATEHS pin is lower and depends on the operating conditions (see Section 6.4.4).

7.6 Mutual disturbances of PFC and HBC

The charge and discharge currents for the MOSFET gate of the PFC and HBC are independently driven in time. Due to these current peaks being high, they can give disturbances on control and sense signals. As both the PFC and the HBC controllers are integrated in the TEA1716, the (large) driver currents of the GATEPFC and GATELS pins can also mutually interfere with the controller operation. Design the gate circuits and PCB layout (see Section 13.1) to prevent this.

A construction similar Figure 15(d) helps to keep the (fast and high) switch-off current local, for a high-power PFC MOSFET.

8. PFC functions

The PFC operates in Quasi-Resonant (QR) or Discontinuous Conduction Mode (DCM) using valley detection to reduce the switch-on losses. The maximum switching frequency of the PFC is limited to 125 kHz which reduces switching losses because of valley skipping. The reduction in switching losses is mainly near the zero voltage crossings of the mains voltage and very effective at low mains input voltage and medium/low output load condition.

The PFC is designed as a boost converter using a fixed output voltage. An advantage of such a fixed boost is that the HBC can be designed to a high input voltage, making the HBC design easier. Other advantage of the fixed boost is the possibility to use a smaller boost capacitor value or have a significant longer hold-up time.

In the TEA1716 system, the PFC is always active. The PFC is switched on first when the mains voltage is present. The HBC is switched on after the boost capacitor is charged to approximately 90 % of its normal value.

The system can be operated in burst mode for improved efficiency at low output loads. During burst mode, the HBC determines the on/off sequences and the PFC bursts simultaneously to improve efficiency results.

8.1 PFC output power and voltage control

The PFC of the TEA1716 is time controlled, so measuring the mains phase angle is not required. The on-time is kept constant during the half sine wave for a given mains voltage and load condition to obtain a good Power Factor (PF) and Mains Harmonics Reduction (MHR).

When on-time is constant, the switching current to the PFC output is proportional to the sine waveform input voltage.

An essential parameter for the PFC coil design is the highest peak current. This current occurs at the lowest input voltage at maximum power.

The maximum peak current $I_{p(max)}$ for a PFC operating in critical conduction mode can be calculated using Equation 9:

$$I_{p(max)} = \frac{2\sqrt{2} \times P_{i(max)}}{V_{min}\,(AC)} = \frac{2\sqrt{2} \times \frac{P_{o(nameplate)}}{\eta}}{V_{min}\,(AC)} \quad (9)$$

Example:

- Efficiency (η) = 0.9
- $P_{o(nameplate)}$ = 250 W
- V_{min} (AC) = 90 V

$I_{p(max)}$ = 8.73 A

$I_{p(max)}$ + 10 % = 9.60 A[1]

8.2 PFC regulation

8.2.1 Sensing V_{boost}

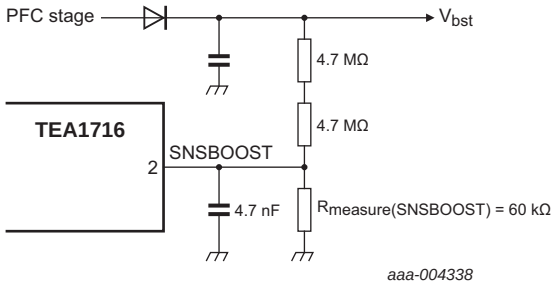


Fig 17. PFC output regulation example: SNSBOOST

The boost output voltage value is set between the PFC output voltage and the SNSBOOST pin using a resistor divider. When in regulation, the SNSBOOST voltage is kept at 2.5 V.

The resistor divider can have a total value up to 10 MΩ to limit power loss.

The measurement resistor between SNSBOOST and ground can be calculated using the following equation:

$$R_{measure(SNSBOOST)} = \frac{R_{boost} \times V_{reg(SNSBOOST)}}{V_{boost} - V_{reg(SNSBOOST)}} \quad (10)$$

Example:

- R_{boost} = 4.7 MΩ + 4.7 MΩ = 9.4 MΩ
- V_{boost} = 394 V

$$R_{measure(SNSBOOST)} = \frac{R_{boost} \times V_{reg(SNSBOOST)}}{V_{boost} - V_{reg(SNSBOOST)}} = \frac{9.4\ M\Omega \times 25\ V\ (typical)}{394\ V - 2.5\ V\ (typical)} = 60\ k\Omega$$

1.The TEA1716 PFC operates in Quasi Resonant (QR) mode using valley detection providing good efficiency. Valley detection requires additional ringing time within every switching cycle. This ringing time adds short periods of no power transfer to the output capacitor. The system must compensate this using a higher peak current. A rule of thumb is that the peak current in QR mode is maximum 10 % higher than the calculated peak current in critical conduction mode.

Use a capacitor on SNSBOOST to prevent wrong measurements due to MOSFET switching noise, mains surge events or ESD events. Also, place the measurement resistor and the filtering capacitor close to the IC in the PCB layout.

8.2.2 SNSBOOST pin open and short-circuit detection

The PFC does not start switching until the voltage on SNSBOOST exceeds 0.4 V. This set-up serves as short-circuit protection for the boost voltage and the SNSBOOST pin.

An internal current source draws a small amount of current from SNSBOOST. The current source prevents switching when the pin is left open as the voltage remains under 0.4 V. This combination also creates an Open-Loop Protection (OLP) when, for example, one of the resistors in the boost divider network is disconnected.

8.2.3 PFCCOMP in the PFC voltage control loop

The PFC output voltage is set and controlled using the SNSBOOST pin. The internal error amplifier using a reference voltage of 2.5 V senses the voltage on the SNSBOOST pin.

Near the regulation point (2.42 V < SNSBOOST < 2.58 V), the amplifier converts the input error voltage with a transconductance (g_m = 80 μA/V) to its output. Not near the regulation point (SNSBOOST < 2.42 V or SNSBOOST > 2.58 V) (g_m = 833 μA/V) to allow faster correction towards regulation.

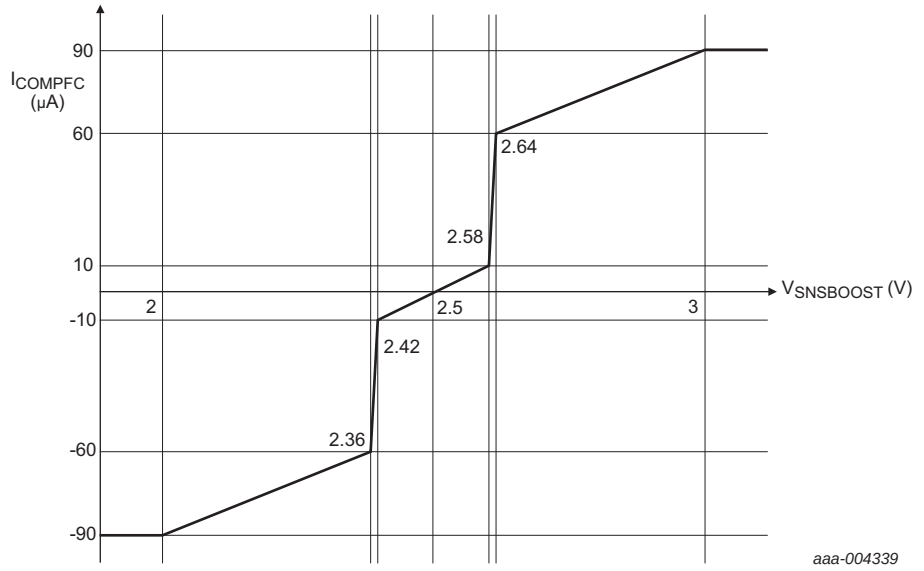


Fig 18. SNSBOOST-COMPPFC amplifier characteristic

The transconductance amplifier output is available at the COMPPFC pin for adding an external loop compensation network. The current from the error amplifier results in a loop voltage on the COMPPFC pin. This COMPPFC voltage and the voltage on the SNSMAINS pin, determine the PFC switch-on time.

A compensation network, typically consisting of one resistor and two capacitors at the COMPPFC pin, is used to stabilize the PFC control loop.

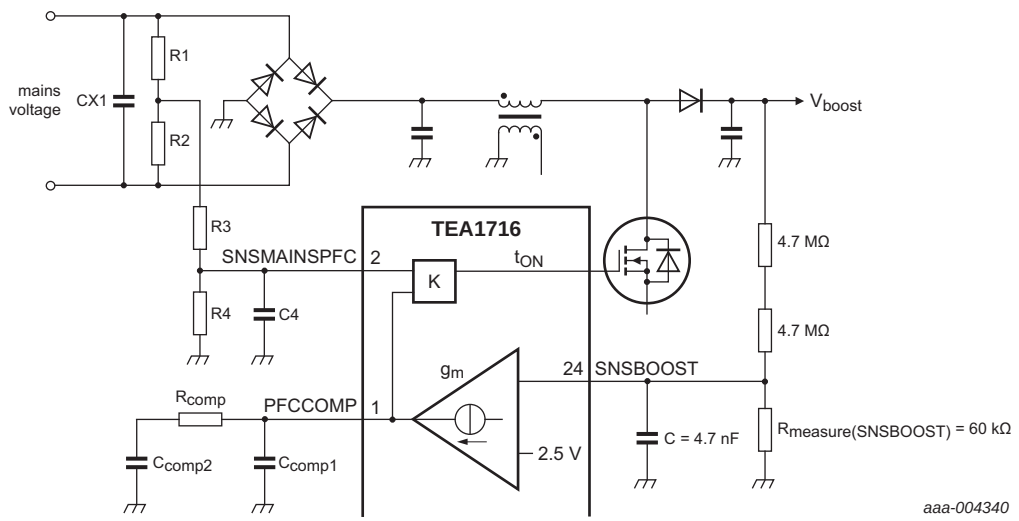


Fig 19. Basic PFC voltage control loop using PFCCOMP

The transfer function has a pole at 0 Hz, a zero at R_{comp}/C_{comp2} and a pole again at C_{comp1}/C_{comp2}. Set the zero frequency to 10 Hz while the next pole frequency is at 40 Hz. The zero point and pole frequencies of the compensation network can be calculated using Equation 11 and Equation 12.

$$f_z = \frac{1}{2\pi \times R_{comp} \times C_{comp2}} \tag{11}$$

$$f_{pole} = \frac{C_{comp1} + C_{comp2}}{2\pi \times R_{comp} \times C_{comp2} \times C_{comp1}} \tag{12}$$

A trade-off between power factor performance and transient behavior must be made. A lower regulation bandwidth leads to a better power factor but poorer transient behavior. A higher regulation bandwidth leads to a better transient response but a poorer power factor.

8.2.4 Mains compensation in the PFC voltage control loop

The mathematical equation for the transfer function of a power factor corrector contains the square of the mains input voltage.

$$K(V_{mains}) = \frac{A}{V_{mains}^{2}} \tag{13}$$

In a typical application, this results in a low bandwidth for low mains input voltages. At high mains input voltages, the MHR requirements can be hard to meet.

The TEA1716 contains a correction circuit to compensate for the mains input voltage influence. The average mains voltage is measured at the SNSMAINS pin and used for internal compensation. Figure 20 shows the relationship between the SNSMAINS voltage, the COMPPFC voltage and the on-time.

Using this compensation it is possible to keep the regulation loop bandwidth constant over the complete mains input voltage range. This compensation also yields a fast transient response on load steps, while still complying to class-D MHR requirements.

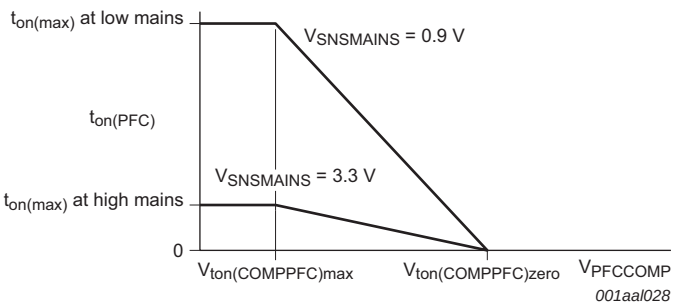


Fig 20. relationship between on-time, SNSMAINS voltage and COMPPFC voltage

8.3 PFC demagnetization and valley sensing

The PFC MOSFET is switched on for the next stroke when the MOSFET drain voltage is at its minimum (valley switching) to reduce switching losses and EMI (see Figure 10).

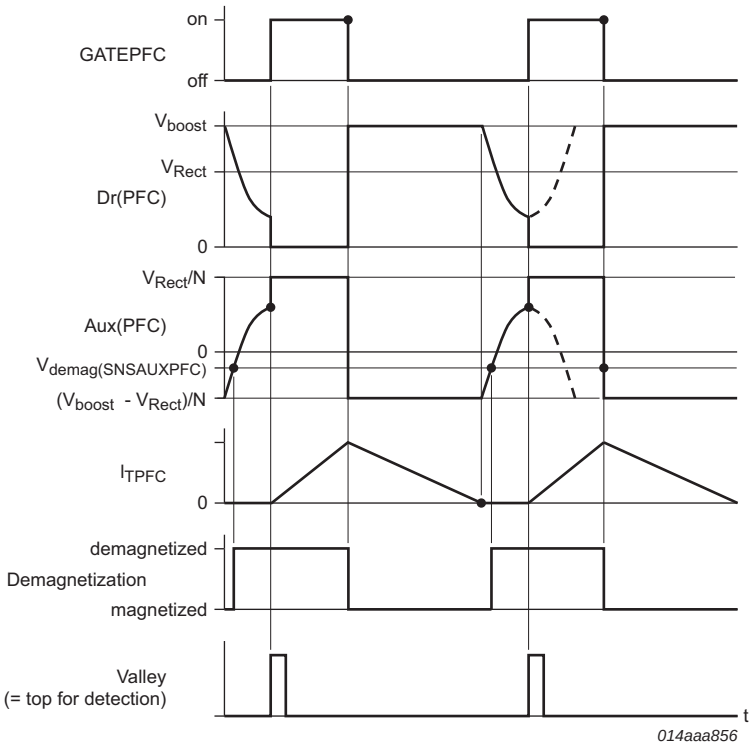


Fig 21. PFC demagnetization and valley sensing

The valleys are detected at the SNSAUXPFC pin. An auxiliary winding on the PFC coil provides a measurement signal on the SNSAUXPFC pin. It gives a reduced and inverted copy of the MOSFET drain voltage. When a valley of the drain voltage (top SNSAUXPFC voltage) is detected, the MOSFET is switched on.

If a top is not detected (valley at the drain) on the SNSAUXPFC pin within 4 μs after demagnetization is detected, the MOSFET is forced to switch on.

8.3.1 PFC auxiliary sensing circuit

Adding a 5 kΩ series resistor to the SNSAUXPFC pin protects the internal IC circuit against excessive voltage, for example, during lightning surges. Place this resistor close to the IC to prevent disturbances causing incorrect switching.

Maintain valley detection even at low ringing amplitudes. Set the voltage on the SNSAUXPFC pin as high as possible, while taking into account its absolute maximum rating of ±25 V.

The number of turns of the auxiliary winding on the PFC coil can be calculated using Equation 14:

$$V_{aux(max)} = \frac{V_{aux(PFC)}}{V_{L(max)}} \times N_p = \frac{25\ V}{415} \times 52 = 3.13 \rightarrow 3\ turns \quad (14)$$

$V_{SNSAUXPFC}$ is the absolute maximum voltage rating. $V_{L(max)}$ is the maximum voltage across the PFC primary winding and N_p is the number of turns on the PFC coil (for the example a value of 52 is used).

The boost output voltage at OverVoltage Protection (OVP) determines the maximum voltage across the PFC primary winding and can be calculated using Equation 15:

$$V_{L(max)} = \frac{V_{ovp(SNSBOOST)}}{V_{reg(SNSBOOST)}} \times V_{boost} = \frac{2.63\ V\ (typical)}{2.5\ V\ (typical)} \times 394 = 415\ V \quad (15)$$

Remark: In the example, a design value of 394 V is used for nominal V_{boost}.

When a PFC coil with a higher number of auxiliary turns is used, place a resistor voltage divider between the auxiliary winding and the SNSAUXPFC pin. The total resistive value of the divider must be less than 10 kΩ to prevent a delay of the valley detection combined with parasitic capacitances.

8.3.2 PFC frequency limit

The switching frequency is limited to 125 kHz to minimize the switching losses. If the frequency for quasi-resonant operation exceeds the 125 kHz limit, the system switches over to discontinuous conduction mode. The PFC MOSFET is only switched on at a minimum voltage across the switch (valley switching). One or more valleys are skipped, when required, to keep the frequency under 125 kHz (valley skipping).

The minimum off-time is limited to 50 μs after the last PFC gate signal to ensure proper control of the PFC MOSFET in all circumstances.

8.4 PFC OverCurrent Regulation/OverCurrent Protection (OCR/OCP)

The maximum PFC peak current is limited cycle-by-cycle by sensing the voltage across a measurement resistor $R_{sense(PFC)}$ in the source of the MOSFET. The voltage is measured using the SNSCURPFC pin and limited to 0.5 V. At this voltage level, the MOSFET is switched off.

Take a small voltage margin into account to avoid false triggering of the OCP. The value of the measurement resistor $R_{sense(PFC)}$ can be calculated using Equation 16:

$$R_{sense(PFC)} = \frac{V_{ocr(SNSCURPFC)} - V_{margin}}{I_{p(max)}} = \frac{0.52\ V - 0.1\ V}{8.73\ A} = 48\ m\Omega \quad (16)$$

The SNSCURPFC voltage senses an initial voltage peak when the PFC MOSFET switches on, because its (parasitic) capacitances are discharged. The SNSCURPFC pin has a leading edge blanking time of 310 ns to mask this event. It does not react to this initial peak.

8.4.1 PFC soft-start and soft-stop

The PFC has a soft-start function and a soft-stop function to prevent transformer noise/rattle at start-up or during burst mode operation. The soft-start slowly increases the primary peak current at the start of operation. The soft-stop function slowly decreases the transformer peak current before operation is stopped.

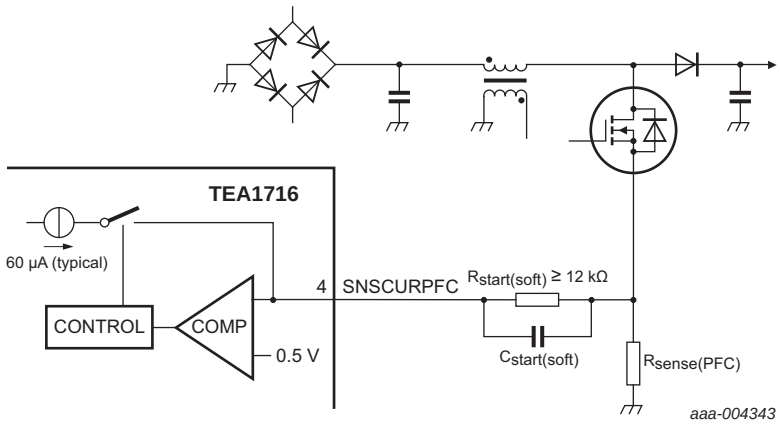


Fig 22. PFC soft-start and soft-stop setup

A resistor and a capacitor between the SNSCURPFC pin and the current sense resistor $R_{sense(PFC)}$ set both functions.

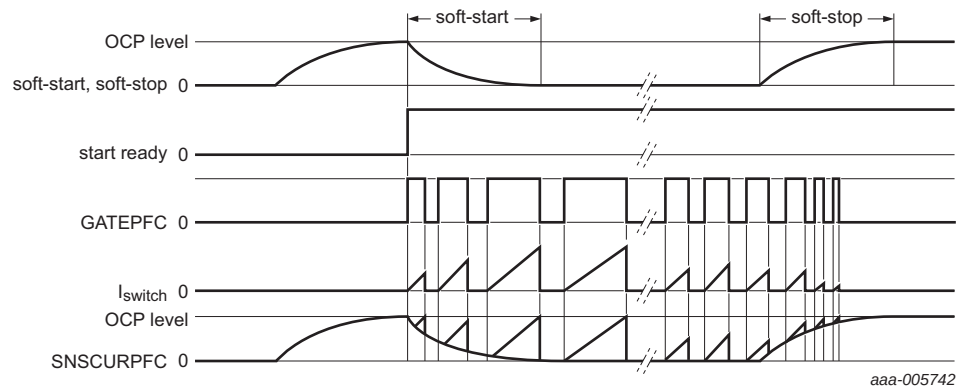


Fig 23. PFC soft-start and soft-stop

8.4.1.1 Soft-start

Before start of operation, an internal current source of 60 μA charges the capacitor to $V_{SNSCURPFC}$ = 60 μA × $R_{start(soft)}$. When the voltage on the SNSCURPFC exceeds the internal start voltage of 0.5 V, the operation can start. Choose a resistor $R_{start(soft)} \geq 12$ kΩ to ensure that the start voltage level is reached. At start-up the current source is stopped. The voltage on pin SNSCURPFC drops as $R_{start(soft)}$ discharges $C_{start(soft)}$. During this discharge, the peak current of each cycle increases until $C_{start(soft)}$ is fully discharged and the normal peak current regulation level (OCR/OCP) is reached. The normal peak current regulation level (OCR/OCP) is set using $R_{sense(PFC)}$.

The soft-start period can be calculated using Equation 17:

$$\tau = R_{start(soft)} \times C_{start(soft)} \quad (17)$$

8.4.1.2 Soft-stop

Soft-stop is achieved by switching on the internal current source of 60 μA again.

The current charges $C_{start(soft)}$. The increasing capacitor voltage reduces the peak current. When the voltage on the SNSCURPFC pin reaches 0.5 V, the operation is stopped.

The voltage is only measured during the off-time of the PFC power switch to prevent measurement disturbances during soft-stop.

8.4.2 Open and short protection (SNSCURPFC pin)

When the SNSCURPFC pin is open, the internal current source of 60 μA charges it to 0.5 V for soft-start. The PFC does not start switching because of OCP.

When the SNSCURPFC pin is short-circuited to ground, the PFC cannot start operation because the start level of 0.5 V has not been reached.

8.5 PFC boost OverVoltage Protection (OVP)

An overvoltage protection circuit is built in to prevent boost overvoltage during load steps and mains transients. When the voltage on the SNSBOOST pin exceeds 2.63 V, the switching of the power factor correction circuit is stopped. The PFC resumes switching when the voltage on the SNSBOOST pin drops under 2.63 V.

When the resistor between the SNSBOOST pin and ground is open, the overvoltage protection also triggers. In this situation, an internal current source of 45 nA to ground can increase the voltage on the SNSBOOST pin to the OVP level.

The voltage at which PFC OVP becomes active can be calculated using Equation 18:

$$V_{boost(ovp)} = \frac{V_{ovp(SNSBOOST)}}{V_{reg(SNSBOOST)}} \times V_{boost} = \frac{2.63\ V\ (typical)}{2.5\ V\ (typical)} \times 394 = 415\ V \quad (18)$$

Remark: In the example, a design value of 394 V is used for nominal V_{boost}.

8.6 PFC mains UnderVoltage Protection (UVP; brownout protection)

The voltage on the SNSMAINS pin is sensed continuously to prevent the PFC operating at very low mains input voltages. When the voltage on the SNSMAINS pin drops under 0.89 V, the switching of the PFC is stopped. This mains undervoltage protection is sometimes called brownout protection.

The voltage on the SNSMAINS pin must be an average DC value that represents the mains input voltage. The system works best using a time constant of approximately 150 ms for the SNSMAINS pin. When the SNSMAINS pin voltage drops, it is internally clamped to a value of 1.05 V. This clamp is 0.1 V under the start-up voltage (1.15 V) for the SNSMAINS pin. The clamping of the voltage ensures a fast restart when the mains input voltage returns after a mains dropout. The PFC (re)starts when the SNSMAINS voltage exceeds the start level of 1.15 V.

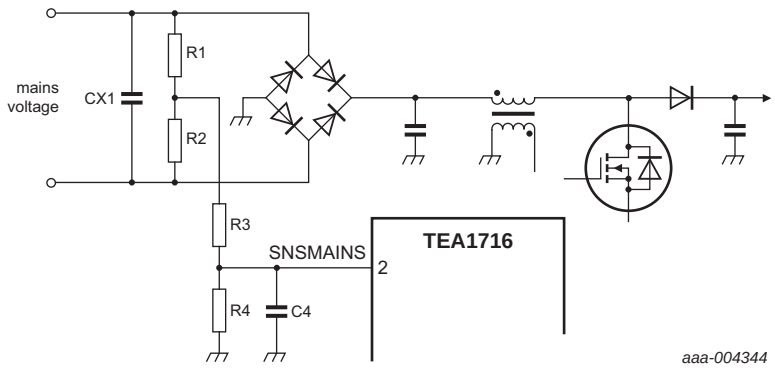


Fig 24. SNSMAINS circuitry

8.6.1 Undervoltage or brownout protection level

The AC input voltage is measured using R1 and R2. Each resistor senses half the sine cycle and as a result, both resistors have the same value. A typical resistor value of 2 MΩ for R1 and R2 can be applied to keep the bleeder loss low.

The average voltage sensed is calculated using Equation 19:

$$V_{av}\ (AC)\ =\ \frac{2\sqrt{2}}{\pi} \times V_{mains}\ (RMS/AC) \tag{19}$$

The SNSMAINS brownout protection (RMS) voltage level is calculated using Equation 20:

$$R_v\ =\ \frac{R1 \times R2}{R1 + R2}$$

$$V_{bo}\ =\ 2 \times \frac{\pi}{2\sqrt{2}} \times V_{uvp(SNSMAINS)} \times \left(\frac{R_v + R3}{R4} + 1\right) \tag{20}$$

Example:

Required: V_{bo} = 66 V (AC)

- $V_{uvp(SNSMAINS)}$ = 0.89 V
- R1 = R2 = 2 MΩ → R_v = 1 MΩ

$$V_{bo} = 2 \times \frac{\pi}{2\sqrt{2}} \times 0.89 \times \left(\frac{R_v + R3}{R4} + 1\right) \quad (21)$$

$$66 = 1.9771 \times \left(\frac{1\ \mathrm{M} + R3}{R4} + 1\right) \quad (22)$$

R3 = 560 kΩ, R4 = 47 kΩ

At the recommended time constant of 150 ms, using C4 = 3300 nF the SNSMAINS time constant can be determined:

$$t_{SNSMAINS} = R4 \times C4 = 47\ k\Omega \times 3300\ nF = 155\ ms \quad (23)$$

8.6.2 Measurement errors due to common-mode voltage

The TEA1716 SNSMAINS function is based on a DC voltage that represents the average value of the mains voltage.

The SNSMAINS voltage level can become incorrect when the supply is not running (not started yet). A distortion of the mains signal can lead to a voltage on the SNSMAINS pin that is too high before the supply starts. This means that the voltage is higher than the value that corresponds to the (differential) mains voltage.

A common-mode voltage between the circuit ground and the mains connections normally causes this distortion. When the diode bridge is not conducting (before the supply starts working), this distortion can have a major influence. The amount of distortion is also depending on the (test) setup. When the diode bridge is conducting (supply operates), the distortion is negligible.

When the supply starts operating, the voltage becomes correct again but is lower. This effect can influence the operation of the SNSMAINS function.

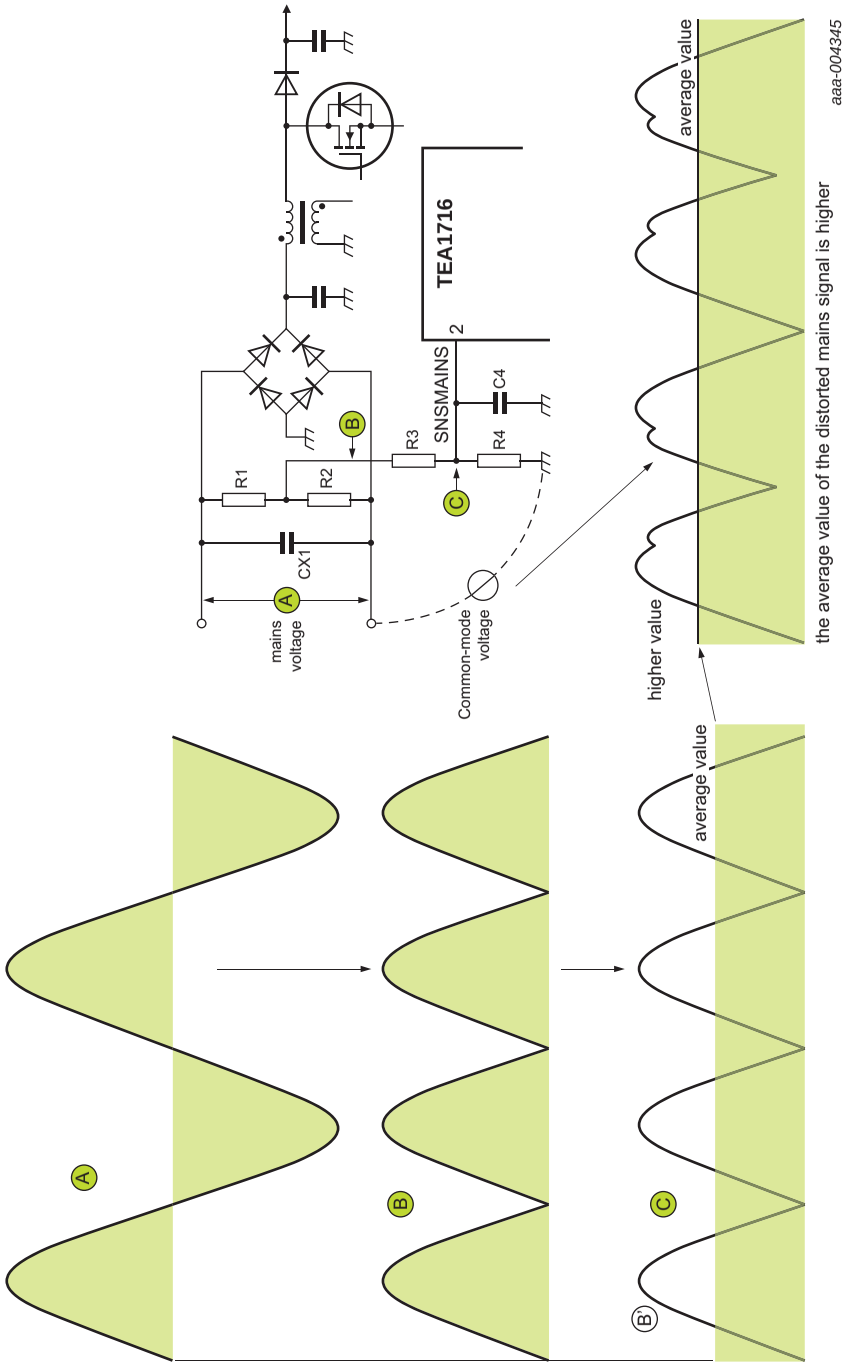


Fig 25. Higher SNSMAINS value because of measured signal distortion

The distortion can be reduced when a lower impedance is used for the measurement resistors R1, R2, R3 and R4.

A peak measurement method also helps to avoid influence of the interference but the resulting circuit behavior is different when compared to the average value measurement method.

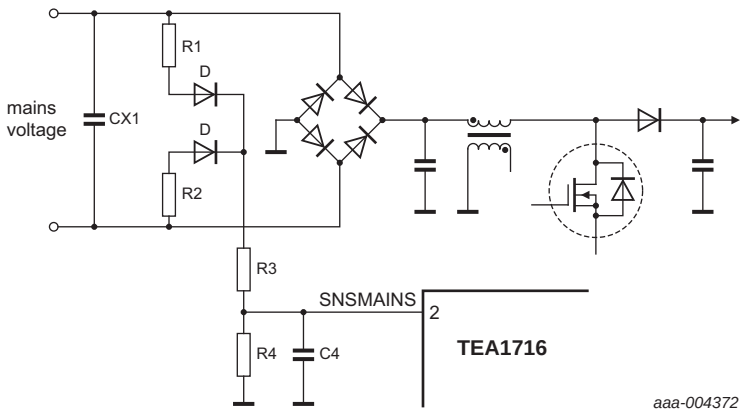


Fig 26. Example of a peak sensing SNSMAINS measurement circuit (adding two diodes D)

8.6.3 Discharging the mains input capacitor

There is often an application requirement to discharge the X-capacitors in the EMC input filtering within a certain time. The replacement values of R1, R2, R3 and R4 determine the resistance to discharge the X-capacitors in the input filtering. The replacement value can be calculated using Equation 24:

$$R_{dch} = R1 + \frac{R2 \times (R3 + R4)}{R2 + R3 + R4} \quad (24)$$

Example:

Required: t_{dch} < 600 ms

- R1 = R2 = 2 MΩ
- R3 = 560 kΩ
- R4 = 47 kΩ

$$R_{dch} = R1 + \frac{R2 \times (R3 + R4)}{R2 + R3 + R4} = 2\ M\Omega + \frac{2\ M\Omega \times (560\ k\Omega + 47\ k\Omega)}{2\ M\Omega + 560\ k\Omega + 47\ k\Omega} = 2465\ k\Omega \quad (25)$$

When adding a 220 nF capacitor, the time constant is:

$$t_{dch} = R_{dch} \times C = 2465\ k\Omega \times 220\ nF = 542\ ms \quad (26)$$

8.6.4 SNSMAINS open pin detection

The SNSMAINS pin, which senses the mains input voltage, has an integrated protection circuit to detect an open pin. When the pin is not connected, an internal current source of 33 nA either pulls the pin down under the stop level of 0.9 V or keeps it under the start level of 1.15 V.

When the SNSMAINS pin is shorted to ground, the results are similar.

9. HBC functions

9.1 HBC UVP boost

The TEA1716 begins operation when the input voltage is higher than approximately 90 % of the nominal boost voltage to ensure proper working of the HBC.

The voltage on the SNSBOOST pin is sensed continuously. When the voltage on SNSBOOST drops under 1.6 V, switching of the HBC is stopped when the low-side MOSFET is on. The HBC (re)starts when the SNSBOOST voltage exceeds the start level of 2.3 V.

9.2 HBC switch control

The internal control for the MOSFET drivers determines when the MOSFETs are switched on and off. It uses the input from several functions:

- An internal divider is used to provide the alternating switching of the high-side and the low-side MOSFET for every oscillator cycle
- The adaptive non-overlap (see Section 9.3) sensing on HB determines the switch-on moment
- The oscillator (see Section 9.4) determines the switch-off moment.
- Several protection functions and an enable function determine when the resonant converter is allowed to switch

9.3 HBC adaptive non-overlap

9.3.1 Inductive mode (normal operation)

The high efficiency of a resonant converter is the result of Zero-Voltage Switching (ZVS) of the power MOSFETs, also called soft switching. A small non-overlap time (also called dead time) is required between the on-time of the high-side MOSFET and low-side MOSFET to allow soft switching. During this non-overlap time, the primary resonant current charges/discharges the capacitance of the half-bridge between ground and the boost voltage. After charging/discharging, the body diode of the MOSFET starts conducting. There are no switching losses because the voltage across the MOSFET is zero.

This operating mode is called inductive mode because above a given switching frequency, the resonant tank inductive impedance part is dominant at a given power level.

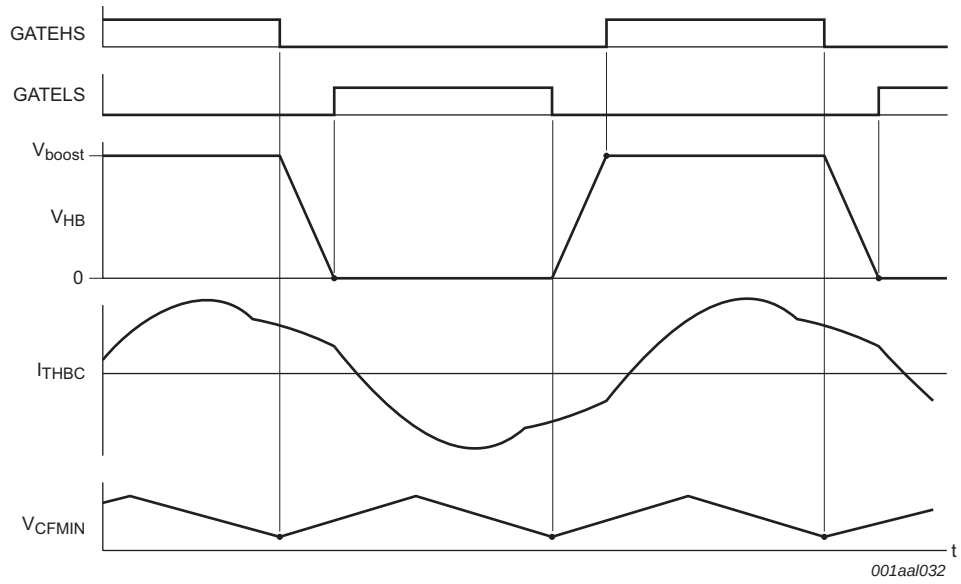


Fig 27. Inductive mode HBC switching

The time required for the transition of the HB depends on the amplitude of the resonant current at the moment of switching. There is a (complex) relationship between the amplitude, the frequency, the boost voltage and the output voltage. Ideally, the IC switches on the MOSFET when the transition of the HB has reached its end value. It must not wait longer, especially at high output load to prevent a swing back of the HB voltage.

The adaptive non-overlap function of the TEA1716 provides an automatic measurement and control function that determines when to switch on. As it uses actual measurement input, the control adapts for operation changes in time.

Presetting a fixed non-overlap time, which is always a compromise between different operating conditions, is not required because of this adaptive non-overlap function.

The adaptive non-overlap function senses the slope at HB after one MOSFET has been switched off. Normally, the slope at the HB starts directly. Once the transition of the HB node is complete, the slope ends. The adaptive non-overlap sensing detects the slope and the other MOSFET is switched on. The non-overlap time is automatically adjusted to the best value with the lowest switching loss, even if the HB transition cannot be fully completed.

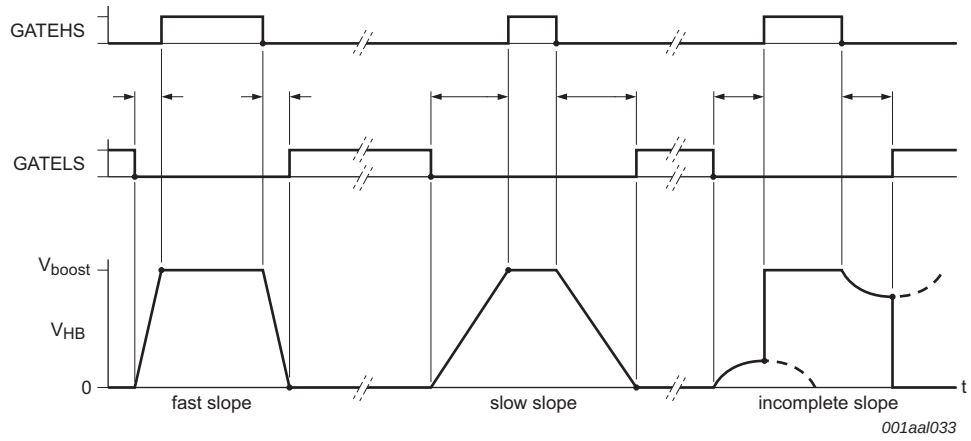


Fig 28. Adaptive non-overlap switching during normal operating conditions

The non-overlap time depends on the HB slope. However, it has an upper and lower time limit. An integrated minimum non-overlap time (maximum 160 ns) prevents accidental cross conduction in all conditions. The maximum non-overlap time is limited to the charging time of the oscillator. If the HB slope takes more time than the charging of the oscillator (25 % of HB switching period), the MOSFET is forced to switch on. In this case, the MOSFET is not soft switching. The maximum non-overlap time limit ensures that the on-time of the MOSFET is at least 25 % of the HB switching period at very high switching frequencies.

9.3.2 Capacitive mode

During error conditions (for example, output short circuit, load pulse too high) or special start-up conditions, the switching frequency can become too low for inductive operation. The resonant tank has a capacitive impedance. In capacitive mode, the HB slope does not start after the MOSFET has switched off. Do not switch on the other MOSFET in this condition. The lack of soft switching increases dissipation in the MOSFETs. The conducting body diode in the MOSFET at the switching moment can damage or even destroy the device very quickly.

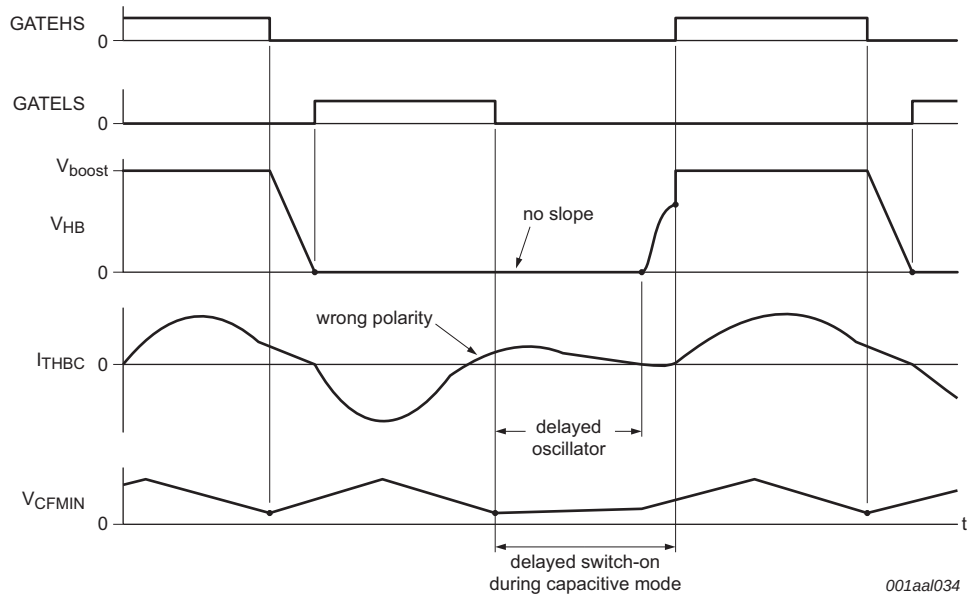


Fig 29. Capacitive mode HBC switching

The adaptive non-overlap system of the TEA1716 always waits until the slope at the half-bridge node starts. It guarantees safe/best switching of the MOSFETs in all circumstances. In capacitive mode, it can take half the resonance period before the resonant current changes back to the correct polarity and starts charging the half-bridge node. The oscillator remains in slow charging current mode until the half-bridge slope allows this relatively long waiting time (see Section 9.4.2 and Figure 34).

The MOSFET is forced to switch on when the half-bridge slope does not start at all and the slowed down oscillator reaches the high level.

The capacitive mode regulation function increases the oscillation frequency to bring the converter from capacitive mode to inductive operation again.

9.3.3 Capacitive Mode Regulation (CMR)

The adaptive non-overlap function prevents the harmful switching in Capacitive mode. However, an extra action is executed, which results in the CMR to end the Capacitive mode operation and return to Inductive mode operation.

Capacitive mode is detected when the V_{HB} slope does not start shortly (690 ns) after the MOSFET is switched-off. At detection of capacitive mode, $f_{sw(HBC)}$ is increased quickly. Discharging $C_{SSHBC/EN}$ with a high current (1800 μA) from the moment $t_{no\text{-}slope}$ = 690 ns has passed before the half-bridge slope starts to increase $f_{sw(HBC)}$. The resulting $f_{sw(HBC)}$ increase regulates the HBC back to the border between Capacitive mode and Inductive mode.

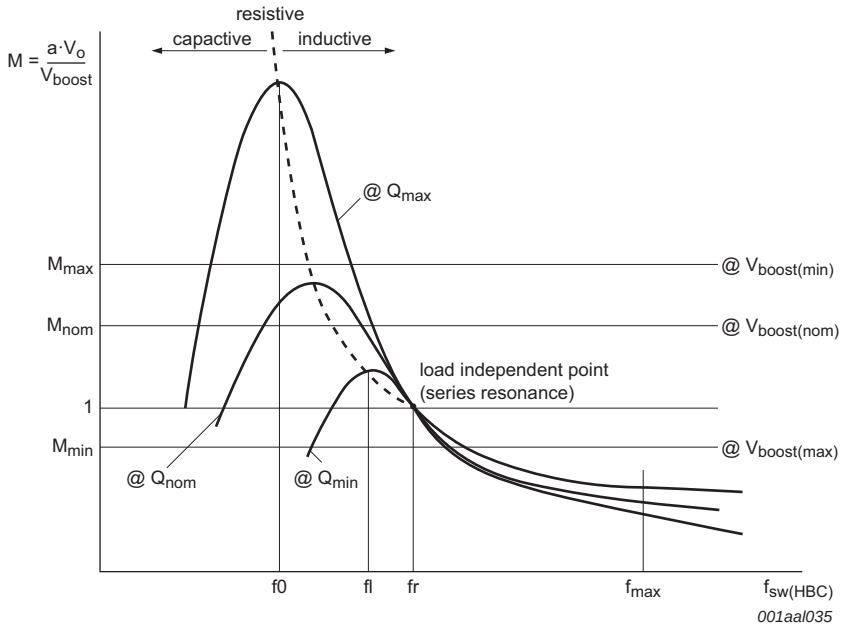
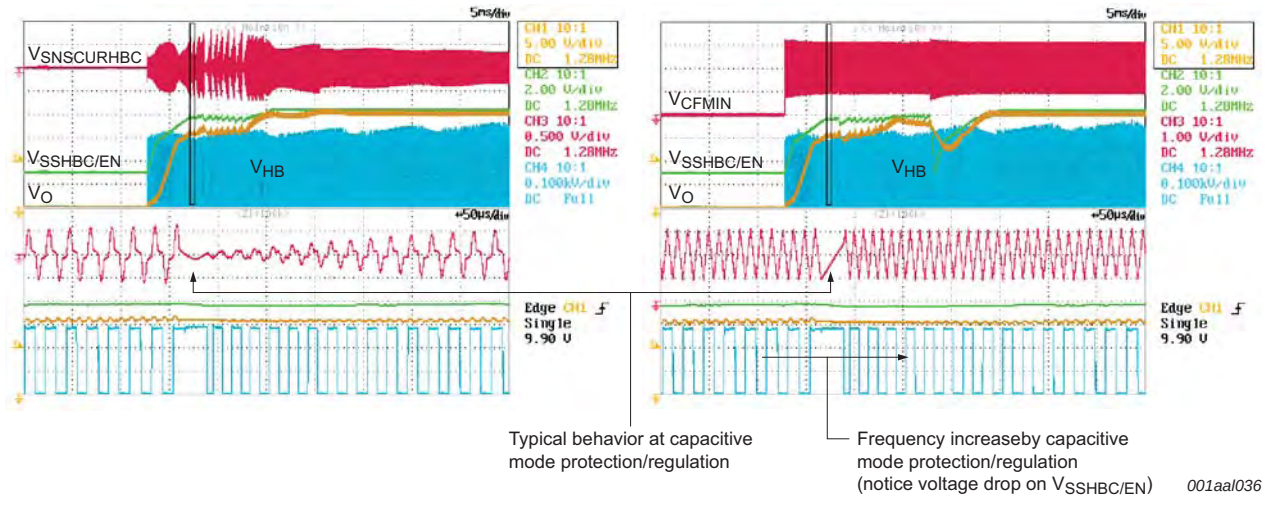


Fig 30. Capacitive/inductive HBC operating frequencies

The typical slowing of the oscillator combined with the discharging of the SSHBC/EN pin indicates the CMR of the TEA1716.



Oscilloscope traces contain normal time (top) and zoomed view (bottom)

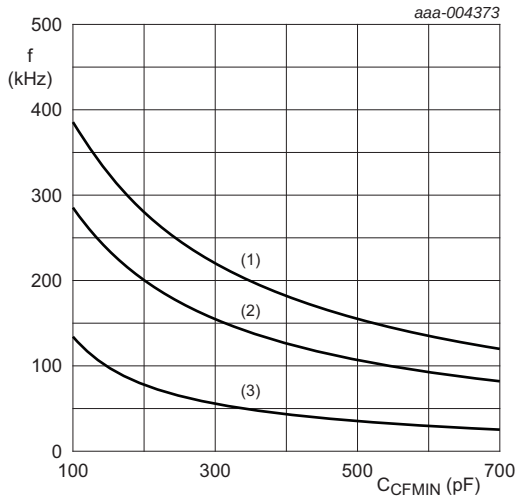
Fig 31. Typical protection and regulation behavior in capacitive mode (during bad start-up)

9.4 HBC oscillator

The slope controlled oscillator determines the switching frequency of the half-bridge. The oscillator generates a triangular waveform at the external capacitor $C_{CFMIN)}$.

9.4.1 Presetting the frequency range

The value of the capacitor on the CFMIN pin determines the frequency range.



(1) f_{max}

(2) f_{max}, SNSFB regulation

(3) f_{min}

Fig 32. Frequency range as function of C_{CFMIN}

The oscillator frequency depends on the charge and discharge current of the capacitor on the CFMIN pin. The charge and discharge current consists of a fixed part which determines the minimum frequency and the SNSFB and SSHBC/EN pins control functions drive a variable part.

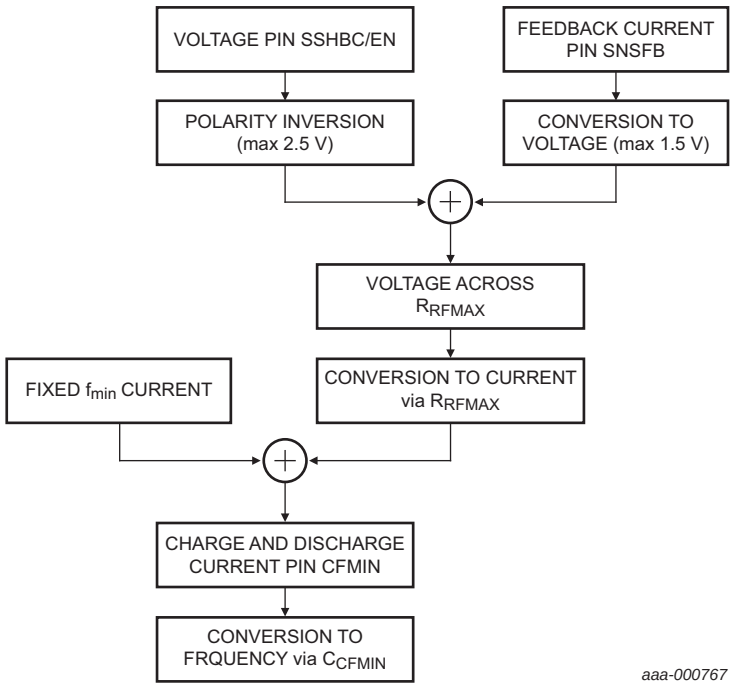


Fig 33. Determination of the oscillator frequency in normal operation

An exception is the situation that the HB slope is not detected immediately after switch-off. Until the HB slope is detected, only a small current source of 30 μA charges the oscillator capacitor.

9.4.2 Operational control

During operation, the state of the half-bridge node HB controls the oscillator. An internal slope detection circuit monitors the voltage on HB.

The charge current of the oscillator capacitor is initially set to a low value of 30 μA. After the start of the half-bridge slope is detected, the charge current is increased to the value corresponding to the operating frequency at that moment. Feedback on the SNSFB pin controls the working frequency. Normally, the half-bridge slope starts directly after switch-off of the MOSFET. The time with the low oscillator current (30 μA) is negligible.

The similarity between GATELS and GATEHS when switching is that the oscillator signal determines when to switch off. The HB sensing circuit determines when to switch on.

As HB sensing determines switching on and is therefore not fixed, the time between switching off one MOSFET and switching on the other one, is adaptive (adaptive non-overlap time or dead time). This non-overlap time has no influence on the oscillator signal.

The oscillator frequency controls the converter switching frequency by determining the time between two switch-off moments (including a small period when the oscillator current is only 30 μA).

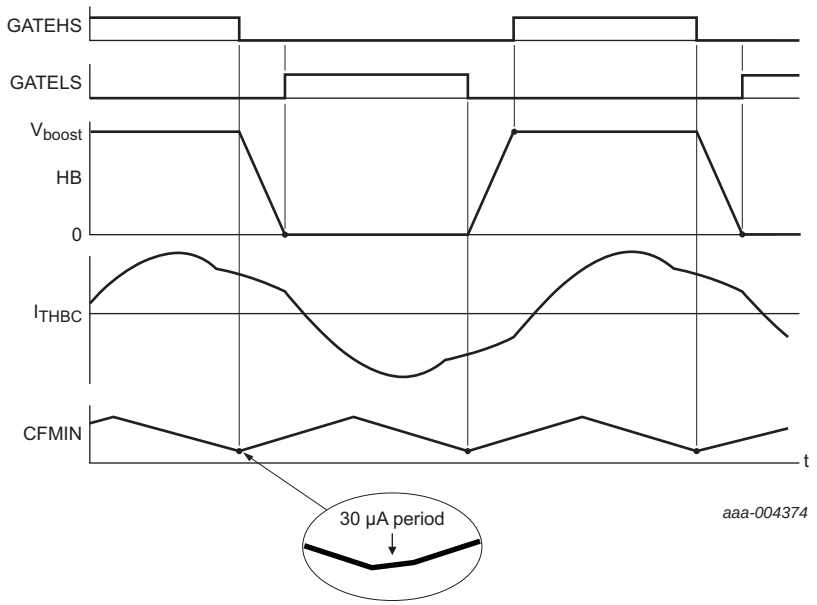
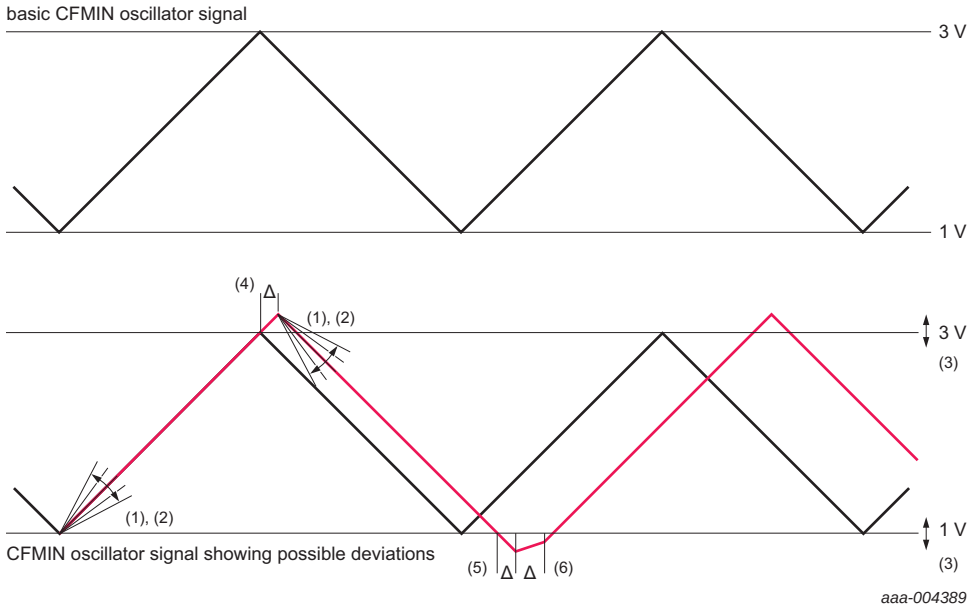


Fig 34. Timing overview of the oscillator and HBC drive

9.4.3 CFMIN oscillator frequency range

The oscillator frequency can be calculated using the capacitor value and the charge and discharge current value. At lower frequency values, a good representation of the practical result is provided. At higher frequencies several tolerances and delays cannot be neglected anymore and calculation becomes more complex.

Figure 35 provides graphs that include the deviation for higher frequencies and can be used for selecting a suitable CFMIN pin capacitor value.



Tolerances and delays:

(1) Value of capacitor on the CFMIN pin.

(2) Maximum and minimum value of charge and discharge currents on the CFMIN pin.

(3) The CFMIN pin switching levels ($V_{u(CFMIN)}$ = 3 V (typical) and $V_{l(CFMIN)}$ = 1 V (typical)).

(4) Switch from the CFMIN pin charge current to discharge current (CFMIN voltage overshoot) caused by internal comparator + switch operation.

(5) Time between the CFMIN pin reaching $V_{l(CFMIN)}$ = 1 V (typical) and switching off the gate drive caused by internal comparator + switch operation.

(6) Time between the CFMIN pin switching off the gate drive and the HB detecting the starting of the HB slope initiating a new oscillator cycle.

Fig 35. Tolerances and delays at high frequencies

9.4.3.1 Basic frequency calculation

$$f_{osc} = 2 \times f_{HB} \tag{27}$$

$$t_{ch} \approx t_{dch} \approx \frac{t_{osc}}{2} \tag{28}$$

$$\Delta V_{osc} = V_{u(CFMIN)} - V_{l(CFMIN)} = 3\ V\ (typical) - 1\ V\ (typical) = 2\ V \tag{29}$$

$I_{osc(min)}$ = 150 µA (typical); $I_{osc(max)}$ = 830 µA (typical)

$$f_{min(HB)} = \frac{I_{osc(min)}}{2 \times 2 \times C_{CFMIN} \times \Delta V_{osc}} = \frac{150\ \mu A\ (typical)}{8 \times C_{CFMIN}} \tag{30}$$

$$f_{max(HB)} = \frac{I_{osc(max)}}{2 \times 2 \times C_{CFMIN} \times \Delta V_{osc}} = \frac{830\ \mu A\ (typical)}{8 \times C_{CFMIN}} \tag{31}$$

Example:

- C_{CFMIN} = 330 pF
- $f_{min(HB)}$ = 57 kHz
- $f_{max(HB)}$ = 314 kHz; When typical delays are included, the expected maximum frequency is only 210 kHz

Figure 32 shows practical values including typical delays.

9.4.3.2 Calculation of the maximum frequency for SNSFB regulation

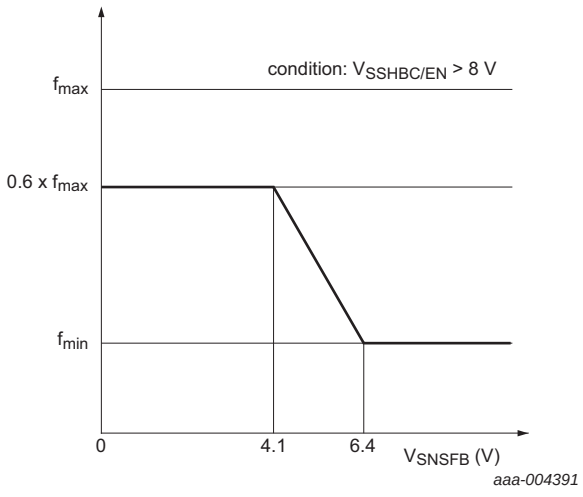
the SNSFB function only regulates part of the total frequency range. This part is the lower 60 % of the total range.

$$f_{max(SNSFB)} = f_{min(HB)} + 0.6 \times (f_{max(HB)} - f_{min(HB)}) \quad (32)$$

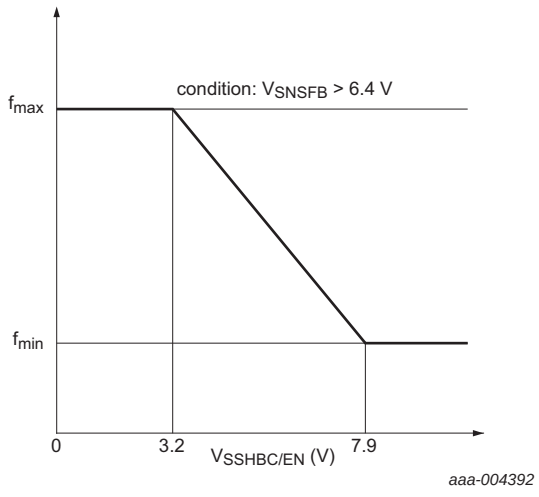
For example (see Section 9.4.3.1):

- $f_{min(HB)}$ = 57 kHz
- $f_{max(HB)}$ = 314 kHz

$$f_{max(SNSFB)} = 57\ kHz + 0.6 \times (314\ kHz - 57\ kHz) = 211\ kHz$$



a. Regulation via SNSFB



b. Regulation via SSHBC/EN

Fig 36. Frequency range for regulation

9.4.4 High-Frequency Protection (HFP)

Normally, the converter does not operate continuously at the preset maximum frequency. This maximum frequency is only used for a short time during soft-start or temporary fault/overload conditions.

When the operating frequency remains at, or close to, maximum frequency for a longer period, a fault condition is assumed and a protection activated.

When the frequency is higher than approximately 75 % of the frequency range, the protection timer is started.

Remark: During normal regulation, the maximum frequency leads to only 60 % of the present range because the SNSFB regulation is limited to this value. The high frequency that triggers the HFP must be a combination of the SNSFB and SSHBC/EN functions.

9.5 HBC feedback (SNSFB)

A typical power supply application contains mains insulation in the HBC. On the secondary (mains insulated) side, the output voltage is compared to a reference and amplified. The TEA1716 is normally placed on the primary side. The output of the error amplifier is transferred to the primary side via an optocoupler. The output of the optocoupler on the primary side can be connected to SNSFB in combination using pull-up resistor R_{SNSFB}.

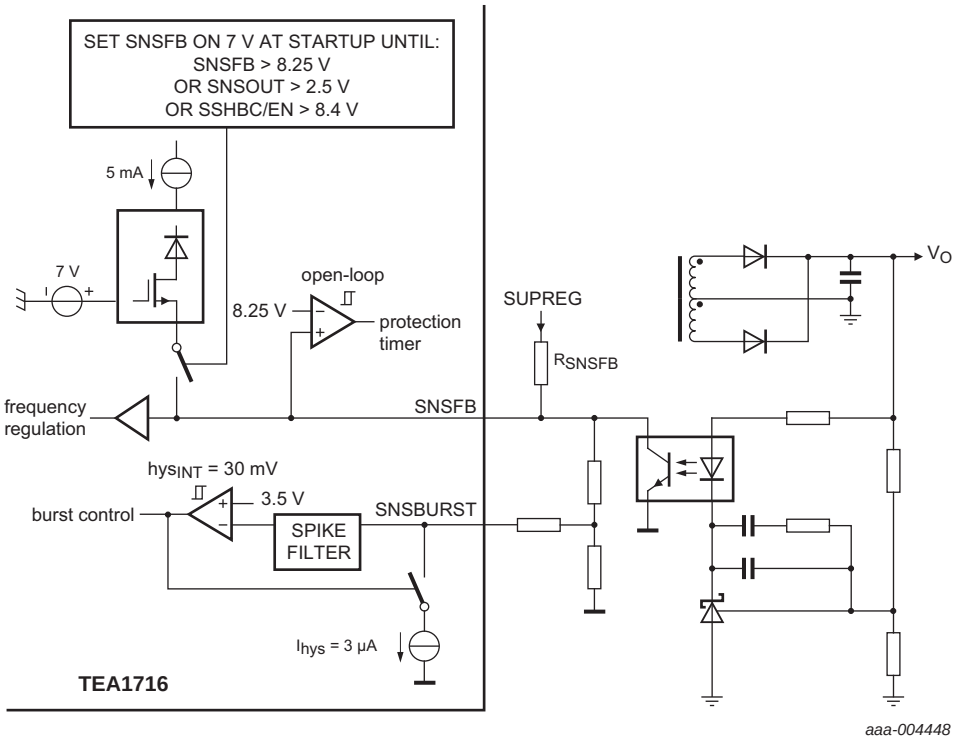


Fig 37. Typical basic SNSFB application

The frequency regulation function senses the voltage on SNSFB.

The SNSFB regulation can control 60 % of the total preset frequency range. The remaining upper part of the frequency range is only reached via control of SSHBC/EN for soft-start or protection (see Section 9.4.3.2 and Figure 36).

Figure 36 shows the frequency regulation as a function of the voltage on the SNSFB pin.

9.5.1 SNSFB pull-up resistor and low-power consumption

A resistor R_{SNSFB} can be connected between SNSFB to SUPREG to generate the voltage on SNSFB for regulation. An optocoupler can sink current from SNSFB to obtain the regulation voltage.

The value of this pull-up resistor R_{SNSFB} determines how much current is used to obtain a certain regulation voltage. Using a higher value for R_{SNSFB}, the current consumption can be minimized for low-power consumption in a standby or no-load state.

Remark: A low current consumption for the SNSFB function also results in a low current in the drive of the optocoupler by the secondary error amplifier. It is important to select a suitable optocoupler type for reliable operation at low current.

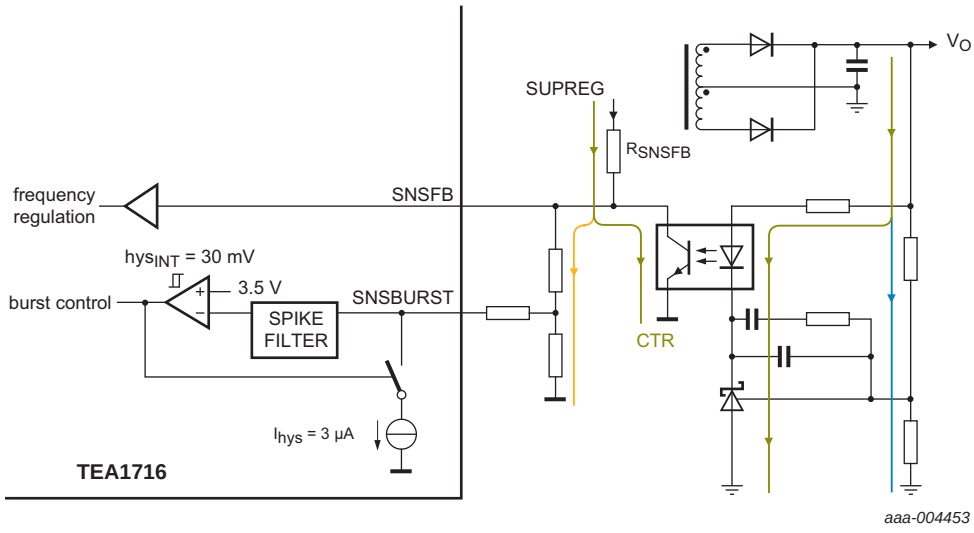


Fig 38. Current flows in the SNSFB circuit that contribute to the power consumption

9.5.2 Start-up voltage source

The SNSFB function requires an external pull-up function to provide a proper feedback function.

At start-up this pull-up function is sometimes not immediately operational. An internal source is activated putting 7 V on SNSFB to ensure a correct start-up in such a situation. This source is only active at start-up and is switched off when the start-up is completed.

Start-up is complete when one of these conditions is detected:

- $V_{SNSFB} > 8.25$ V
- $V_{SNSOUT} > 2.5$ V
- $V_{SSHBC/EN} > 8.4$ V

When using a pull-up function with resistor R_{SNSFB} as shown in Figure 37, the internal start-up source is redundant because the SUPREG pin voltage is active before the HBC controller operation starts.

9.5.3 HBC Open-Loop Protection (OLP)

The resonant controller of the TEA1716 contains an Open-Loop Protection (OLP) circuit. This protection monitors the voltage on the SNSFB pin.

Under normal operating conditions, the optocoupler current pulls down the voltage at the SNSFB pin. An error in the feedback loop can cause the current to be very low with the HBC controller delivering maximum output power. In this situation, the voltage on the SNSFB pin remains high.

When the voltage on the VSNSFB pin exceeds the 8.25 V level of an internal comparator, the protection timer RCPROT is started (see Figure 37).

Remark: The start-up voltage source described in Section 9.5.2 can prevent an open-loop protection at start-up. This function depends on the construction of the pull-up function on the SNSFB pin. In the situation shown in Figure 37 this is not the case.

9.6 The SSHBC/EN pin soft-start and enable

The SSHBC/EN pin provides the following three functions:

- It enables the PFC (> 1.2 V) and PFC plus HBC (> 2.2 V)
- It performs an HBC frequency sweep during soft-start from 3.2 V to 8 V
- It provides frequency control during protection.

The following internal current sources operate the frequency control depending on the required action:

- Soft-start, overcurrent protection:
  - High charge or low charge (respectively 160 μA or 40 μA)
  - High charge or low discharge (respectively 160 μA or 40 μA)
- Capacitive mode regulation
  - High charge or low discharge (respectively 1800 μA or 440 μA)
- General
  - Bias discharge (5 μA)

A comparator detects the end of start-up when the voltage on the SSHBC/EN pin exceeds 8.25 V. This level enables burst mode operation if it was not already enabled (see Section 10.5).

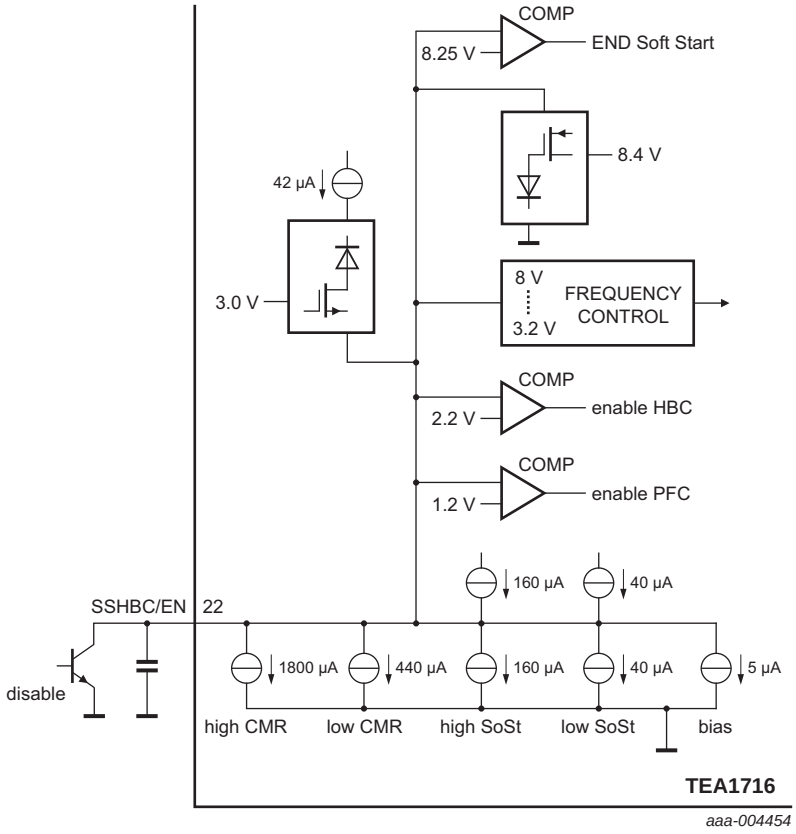


Fig 39. SSHBC/EN: overview of sources, clamps and level

9.6.1 Switching on and off using an external control function

The SSHBC/EN pin can be used to switch on and off the converters using an external control function.

A microcontroller often drives this function from the secondary side of the optocoupler. The main power supply (PFC + HBC) can be switched off for standby mode and switched on for normal operation. In such a concept a separate standby supply is required to supply the microcontroller functions during standby. It is also possible to switch/keep off the HBC and only have the PFC operational.

The TEA1716 also offers the possibility to switch on/off using the SNSBURST function. This function is intended for burst mode operation where the duration of the on-state and off-state are short.

9.6.1.1 Switching on and off using the SSHBC/EN pin

When a voltage is present at the SUPHV pin or at the SUPIC pin, a current from the SSHBC/EN pin charges the external capacitor. If the pin is not pulled-down, this current increases the voltage to 3 V. The IC is fully enabled because the voltage is greater than both the PFC (1.2 V) and PFC and HBC (2.2 V) enable levels.

The IC can be fully disabled by pulling down the SSHBC/EN pin to under 1.2 V. The PFC controller stops switching immediately, but the HBC continues until the low-side stroke is active. The pull-down current must be greater than the current capability from the internal soft-start clamp: that is, 42 μA.

PFC only active

Pulling down the voltage on the SSHBC/EN pin under the PFC + HBC enable level (2.2 V) but keeping it above the PFC enable level (1.2 V), only disables the HBC. This method is used when there is another power converter connected to the PFC boost voltage. The low-side power switch of the HBC is on when the HBC is disabled using the SSHBC/EN pin.

HBC only active

The TEA1716 is not designed to provide this operation mode. However, it can be realized by forcing a voltage on the SNSBOOST pin higher than 2.63 V but under 5 V. This activates the PFC output overvoltage protection. The PFC operation is stopped (put on hold). The HBC operates because SNSBOOST exceeds its start level of 2.3 V (boost UVP).

The HBC only mode of operation is not generally needed in an application but it can be useful for start-up and debugging purposes during analyses or evaluation.

9.6.1.2 Hold and continue

The SNSBURST function can be used to start and stop the PFC and HBC. This method is intended for burst mode operation to switch off the converters for only a short time.

9.6.2 Soft-start HBC

SSHBC/EN provides the soft-start function for the resonant converter.

The relationship between the switching frequency and the output current/power is not constant. It depends on the output voltage and the boost voltage. The relationship can be complex. The TEA1716 has a soft-start function to ensure that the resonant converter starts or restarts with safe currents.

This soft-start function forces a start at high frequency so that currents are acceptable in all conditions. The soft-start slowly decreases the frequency until the output voltage regulation has taken over the frequency control. The limitation of the output current during start-up also limits the output voltage rise and prevents an overshoot.

During soft-start, in parallel to the soft-start frequency sweep, the SNSCURHBC function monitors the primary current. If a temporary overpower situation occurs, it can activate regulation.

The soft-start uses the voltage on the SSHBC/EN pin. An external capacitor on the SSHBC/EN pin sets the timing (duration) of the soft-start event.

As the SSHBC/EN pin is also used as enable input, the soft-start functionality is above the enable related voltage levels (see Figure 39).

9.6.2.1 Start-up voltage levels

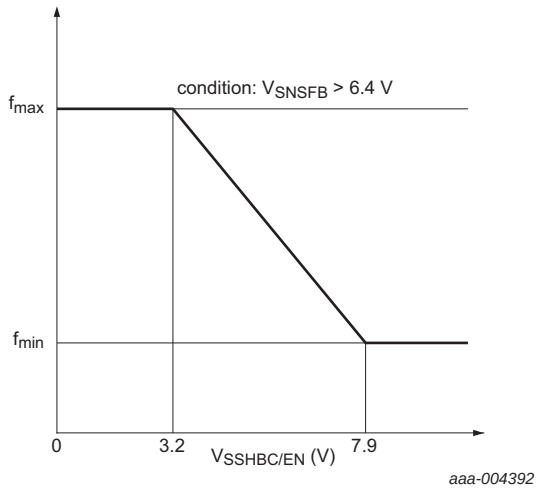


Fig 40. Operating frequencies related to the SSHBC/EN voltage

At start-up, the voltage on the SSHBC/EN pin is low which corresponds to the maximum frequency. During the soft-start procedure, the external capacitor is charged. The voltage on the SSHBC/EN pin rises and the frequency decreases. The contribution of the soft-start function ends when the SSHBC/EN pin exceeds 7.9 V.

The voltage on the SSHBC/EN pin is clamped at 8.4 V and remains at that level during normal operation.

When the voltage on the SSHBC/EN pin is reduced during protection or regulation, the voltage is clamped at 3.0 V. The clamp ensures a quick response so that the operating frequency can be reduced again. Under 3.2 V, the discharge current is reduced to 5 μA.

9.6.2.2 The SSHBC/EN pin charge and discharge

Initially, at start-up, the soft-start external capacitor on the SSHBC/EN pin is only charged to obtain a decreasing frequency sweep from maximum to operating frequency.

In addition to the function to soft-start, the SSHBC/EN pin is used for regulation purposes such as overcurrent regulation. Therefore the voltage on the capacitor on the SSHBC/EN pin can vary by charging and discharging it by internal current sources.

For example, in case of overcurrent regulation, a continuous alternation between charging and discharging of the SSHBC/EN capacitor occurs. The voltage on the SSHBC/EN pin can be regulated in this way, so it overrules the signal on the feedback input SNSFB.

The charge or discharge current can have either a high value ±160 μA or a low value ±40 μA. The two-speed soft-start sweep of the TEA1716 allows a combination of a resonant converter short start-up time and stable regulation loops such as overcurrent regulation.

In some cases, a situation occurs where overcurrent regulation is activated during the soft-start sequence. This results in a feedback controlled or corrected soft-start.

The fast charge or discharge speed is used for the upper frequency range where $V_{SSHBC/EN}$ is under 5.6 V. In the upper frequency range, the current and power in the converter do not react strongly to frequency variations.

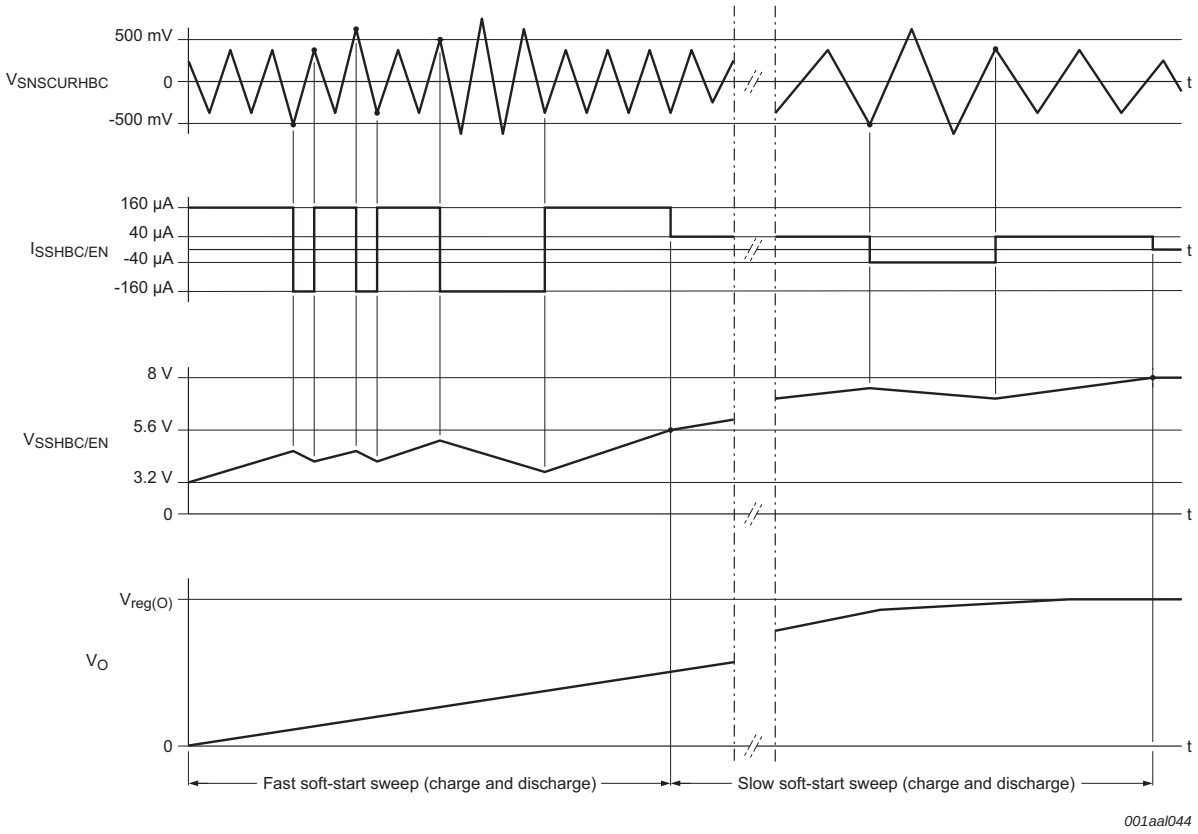


Fig 41. OverCurrent Regulation (OCR) during start-up

The slow charge or discharge speed is used for the lower frequency range where $V_{SSHBC/EN}$ is above 5.6 V. In the lower frequency range, the current in the converter reacts strongly to frequency variations.

Burst mode

The soft-start capacitor is not charged or discharged during the no-operation time in burst mode operation. The voltage on the SSHBC/EN pin does not change during this time.

9.6.2.3 SNSFB and SSHBC/EN pins: soft-start reset; operating frequency control

The SNSFB and SSHBC/EN pins can control the operating frequency simultaneously. The SSHBC/EN pin is dominant to provide protection and soft-start capability. Additionally, there is an internal soft-start reset mechanism that overrules the control inputs for both pins and immediately sets the frequency to maximum.

9.6.2.4 Soft-start reset

Some protective functions require a fast correction of the operating frequency to the maximum value, but do not require to stop switching. The overcurrent protection is an example (see Table 1).

When this protection is activated, the control input of the oscillator is disconnected internally from the soft-start capacitor at the SSHBC/EN pin. The switching frequency is immediately internally set to maximum. In most cases, the change to the maximum switching frequency restores the safe switching operation. When the SSHBC/EN pin voltage reaches 3.2 V, the oscillator control input reconnects to the pin and the normal soft-start sweep follows. Figure 42 shows the soft-start reset and the two-speed frequency downward sweep.

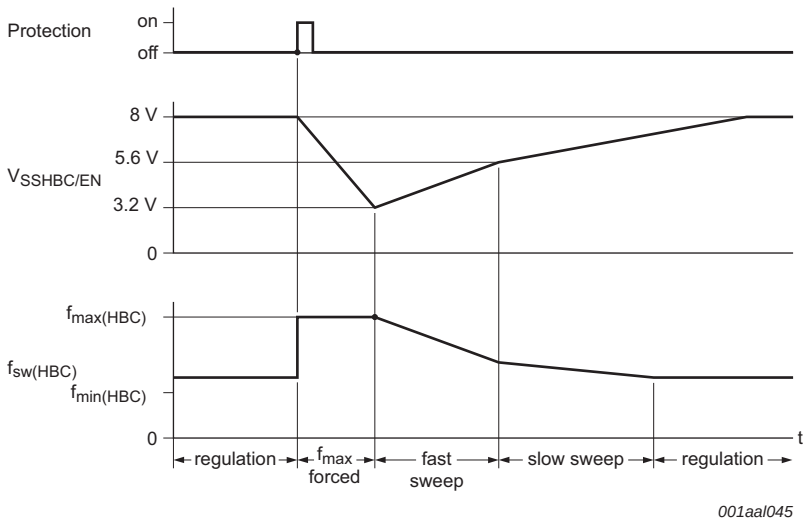


Fig 42. Soft-start reset and two-speed soft-start

The soft-start reset is also used to ensure a safe start-up at maximum frequency when SSHBC/EN or a restart enable the HBC. The soft-start reset is not used when the operation has been stopped for burst mode.

9.7 HBC overcurrent protection and regulation

Measurement of the primary resonant current indicates the converter output power level generated. If a fault or output overload condition occurs, this current often increases considerably. The converter can remain operational during a temporary fault or overload condition by monitoring this current and then taking appropriate action.

The resonant controller of the TEA1716 has two functions when in an overcurrent condition:

- OverCurrent Regulation (OCR) slowly increases the frequency and the protection timer is started.
- OverCurrent Protection (OCP) steps to maximum frequency.

A boost voltage compensation function is included to reduce the variation in the preset protection level of the resonant current.

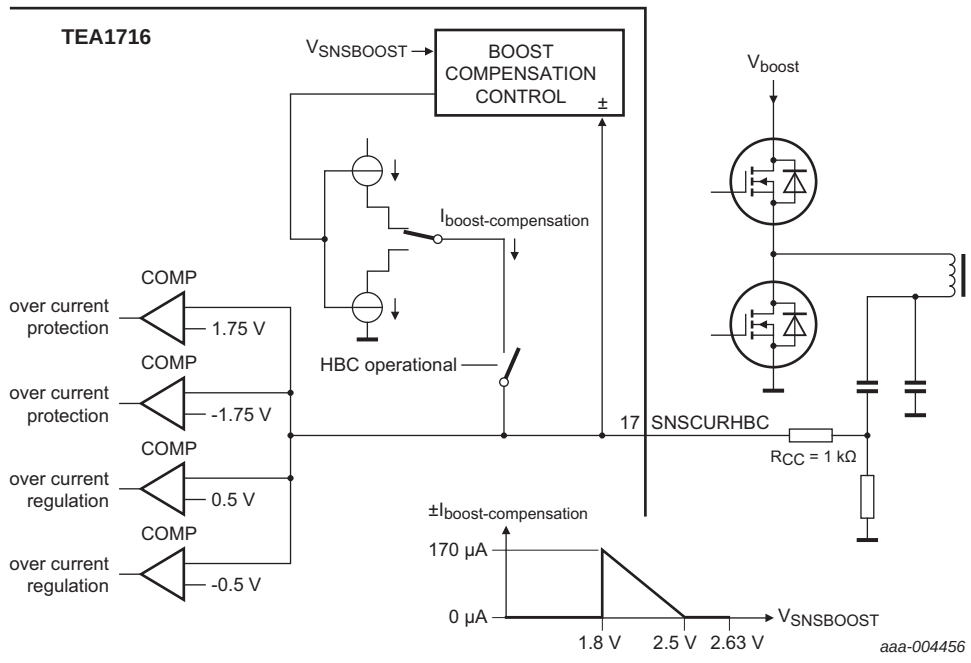


Fig 43. SNSCURHBC

9.7.1 HBC overcurrent regulation

The lowest comparator level of ±0.5 V at the SNSCURHBC pin belongs to the OverCurrent Regulation (OCR) level. There is a comparator for both the positive and negative polarity. If either level is exceeded, the frequency is slowly increased. Discharging the soft-start capacitor accomplishes this. Every time the OCR level is exceeded, this state is latched until the next stroke and the soft-start discharge current is enabled. When both the positive and negative OCR levels are exceeded, the soft-start discharge current flows continuously. In this way, the operating frequency is slowly increased until the resonant current value reaches the preset value.

The behavior during OCR can be observed on the SSHBC/EN pin as a regulation voltage.

When an OCR situation is present for a long time, a serious fault condition is assumed. During OCR, the protection timer is activated. The charging of the protection timer is active approximately a half period cycle after the ±0.5 V level is exceeded. If the detection levels are continuously exceeded, the timer capacitor is charged continuously. However, if the detection levels are exceeded occasionally, the timer capacitor is charged accordingly (see Section 12.4 for more information about the charging/discharging of the protection timer). The restart state is activated when the RCPROT pin voltage reaches the protection level of 4 V.

9.7.1.1 Start-up

The overcurrent regulation limits the output current during start-up effectively. A smaller soft-start capacitor can be chosen to allow faster start-up. The small soft-start capacitor sometimes results in an excessive output current. However, the OCR function can slow down the frequency sweep to keep the output current within the limits.

9.7.2 HBC overcurrent protection

In most cases, the overcurrent regulation can keep the current under the set maximum values. However, OCR is not fast enough to limit the current for all error conditions. OCP is implemented to protect against extreme error conditions.

The internal OCP level is set at ±1.75 V for the SNSCURHBC pin. This level is higher than the OCR level of ±0.5 V. When the OCP level is reached the frequency immediately jumps to the maximum via a soft-start reset procedure, the $V_{SSHBC/EN}$ sweeps down normally.

The chosen maximum soft-start frequency value must limit sufficiently the output power under these conditions.

The behavior during OCP can be observed on the SSHBC/EN pin as a new soft-start. Depending on the (over)load or fault condition during this new soft-start, OCR or OCP can be reactivated.

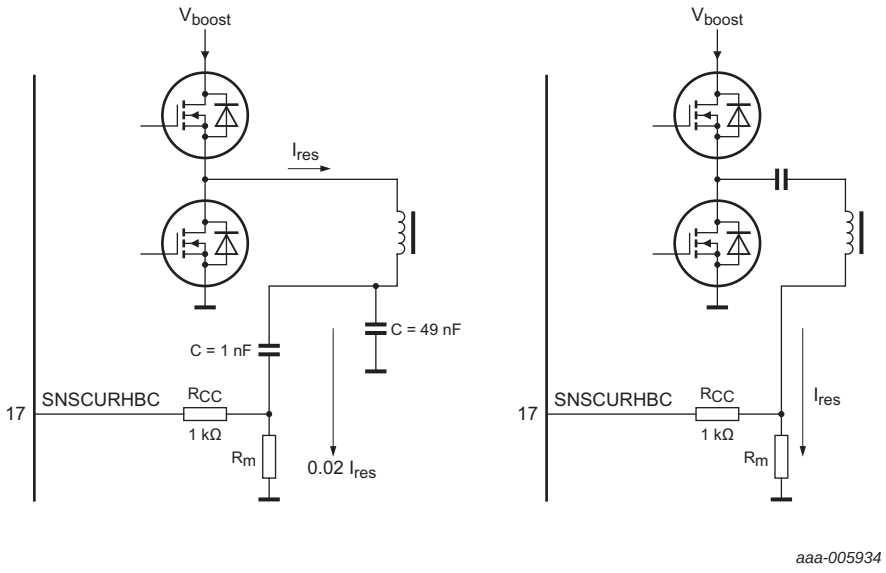
9.7.3 SNSCURHBC boost voltage compensation

The primary current, also called resonant current, is sensed via the SNSCURHBC pin. It senses the momentary voltage across an external current sense resistor. Using the momentary current signal allows fast OCP and simplifies the stability of the OCR. The OCR and OCP comparators compare the voltage on the SNSCURHBC pin to the maximum positive and negative values.

The primary current is higher for the same output power when the boost voltage is low. A boost compensation is included to reduce the dependency of the protected output current level for the boost voltage. The boost compensation sources and sinks a current from the SNSCURHBC pin. This current creates a voltage drop across the series resistor R_{cc}. A typical value for this resistor is 1 kΩ.

The amplitude of the current depends linearly on the boost voltage. At nominal boost voltage, the current is zero and the voltage across the current sense resistor is also present on the SNSCURHBC pin. At the boost start level $V_{SNSBOOST}$ = 1.8 V and the current is maximum 170 μA. The direction of the current, sink or source, depends on the active gate signal. The voltage drop created across R_{cc} reduces the voltage amplitude at the pin. The result is a higher effective current protection level. The R_{cc}value of sets the amount of compensation.

9.7.4 Current measurement circuits



Left is circuit a, right is circuit b.

Fig 44. SNSCURHBC: resonant current measurement configurations

9.7.5 Basic relationship between HBC output current and SNSCURHBC protection levels

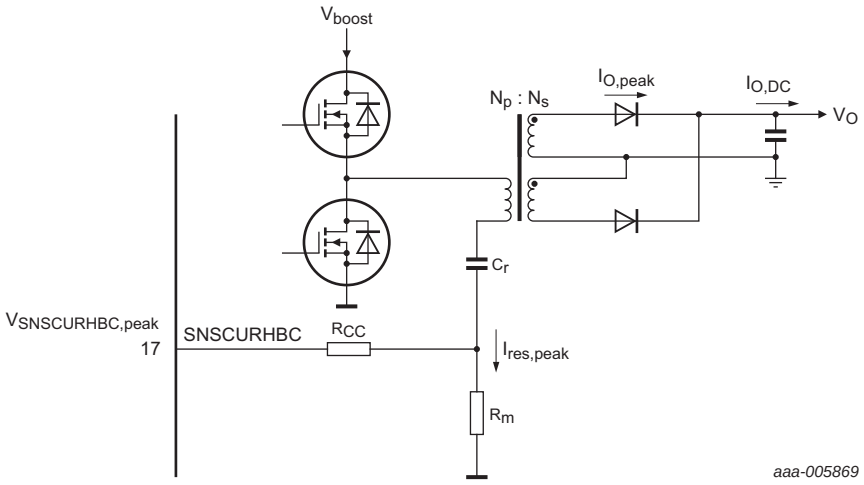


Fig 45. Voltage on SNSCURHBC related to the output current

The relationship between the voltage on the SNSCURHBC pin and the primary converter current is defined by measuring resistor R_m.

$$V_{SNSCURHBC,peak} = R_m \times I_{res,peak} \quad (33)$$

If the circuit used is Figure 44 type a:

$$V_{SNSCURHBC,peak} = R_m \times \left(\frac{C_{r,par}}{C_{r,par} + C_r}\right) \times I_{res,peak} \quad (34)$$

The effective transformer turns ratio defines the relationship between the primary and the secondary converter currents.

$$I_{res,peak} = \frac{N_s}{N_p} \times I_{O,peak} \quad (35)$$

In practice, the effective ratio between the currents is lower than the theoretical ratio of N_s/N_p. A measurement shows the correct value for a specific design.

The relationship between the peak output current and the DC output current depends on the shape of the peak current. In practice, the multiplication factor (MF) is determined for a specific design near the protection level. Normally, a value close to 2.

$$I_{O,peak} = MF_{peak-to-DC} \times I_{O,DC} \quad (36)$$

When combining the various equations the total relationships:

$$V_{SNSCURHBC,peak} = R_m \times \frac{N_s}{N_p} \times MF_{peak-to-DC} \times I_{O,DC} \quad (37)$$

9.7.6 SNSCURHBC PCB layout

As the SNSCURHBC pin must be able to sense the measurement signal accurately cycle-by-cycle at higher frequencies, it is rather susceptible to disturbances. Place the series resistor R_{cc} close to the IC in order to reduce the length of the track that can pick up disturbing signals. As the impedance of the measurement resistor is normally low, the signal track between R_{cc} and the measurement resistor is not critical regarding disturbance.

10. Burst mode operation

10.1 The burst mode operation principle

Burst mode operation can be used to improve the converter efficiency at low output loads.

Temporarily interrupting the switching minimizes losses during the idle time. It is easy for the converter to deliver sufficient power during a short conversion time (a burst) because the average power required for the output is very low.

The burst mode operation of the TEA1716 is based on interrupting the switching while maintaining regulation. Using the SNSBURST function, the regulation voltage on the SNSFB pin can be monitored to determine when the converter must stop switching. The voltage on the SNSBURST pin controls stopping and restarting. When restarting after an interruption, no HBC soft-start is applied as the system is still in regulation (close to the regular working point). The regulation loop of the HBC system (normally the output voltage) determines the timing of switch-on and switch-off. In this way, a small ripple on the output voltage is deliberately created during burst mode operation.

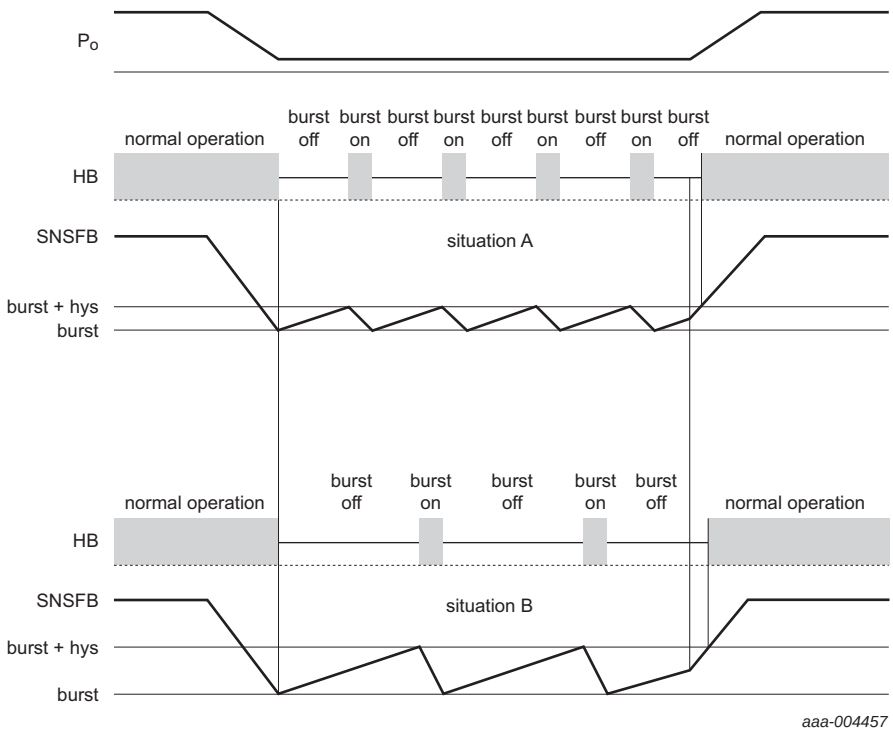


Fig 46. Principle of burst mode operation with V_{SNSFB} shown using two different hystereses

10.2 Advantages of burst mode for HBC

The main reason for applying burst mode in a resonant converter is to improve the efficiency at low output power by reducing power losses.

The graphs in Figure 47 and Figure 48 show the improvement principle in an example of a 250 W resonant converter including (non-bursting) PFC.

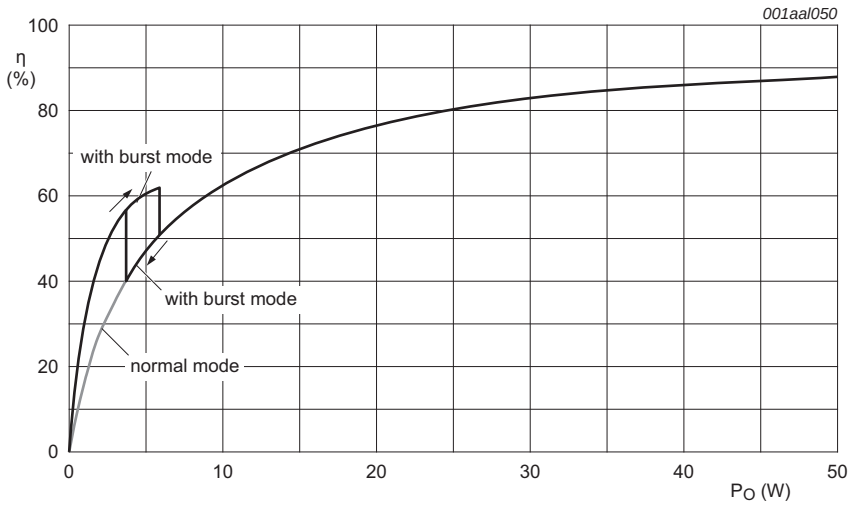


Fig 47. Improved efficiency by HBC burst mode in a 250 W converter

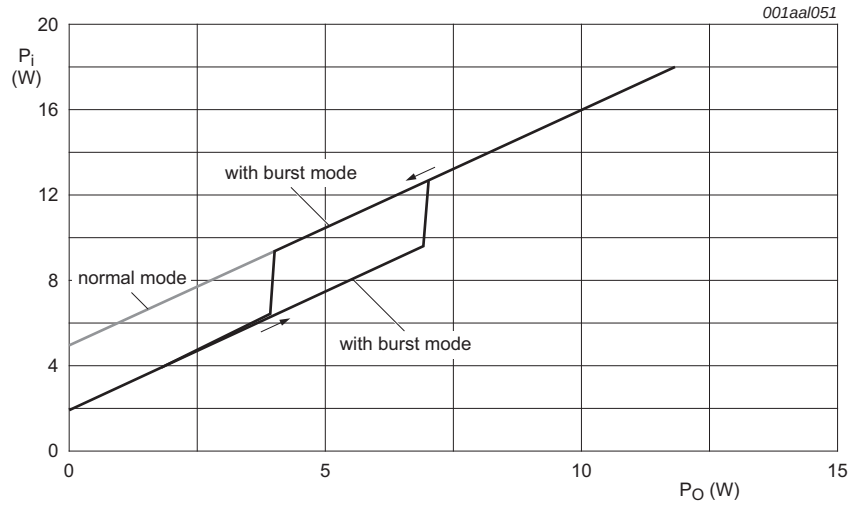
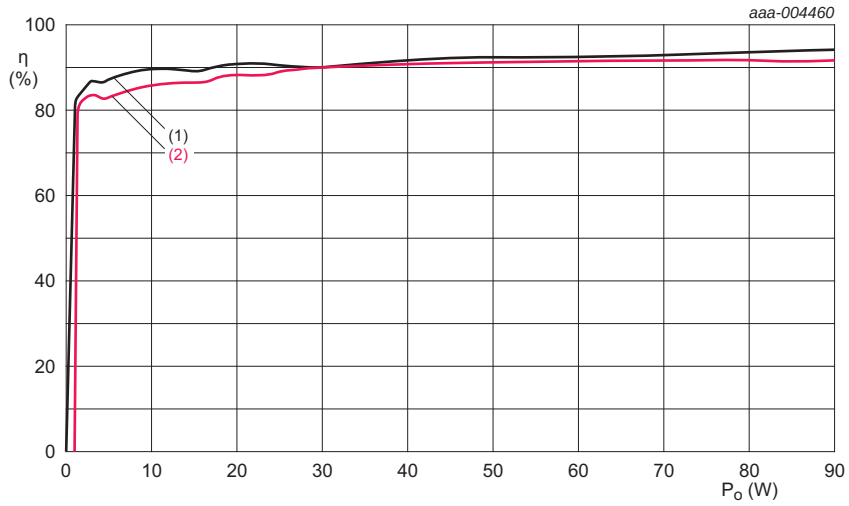


Fig 48. Reduced losses by HBC burst mode in a 250 W converter

10.3 Advantages of burst mode for HBC and PFC simultaneously

The TEA1716 provides a burst mode system that simultaneously switches the HBC and PFC. In this way, the power is transferred directly from the input to the output during the burst period. The HBC determines the repetition time of the burst and the PFC follows. In the burst period, the PFC operates in normal regulation.

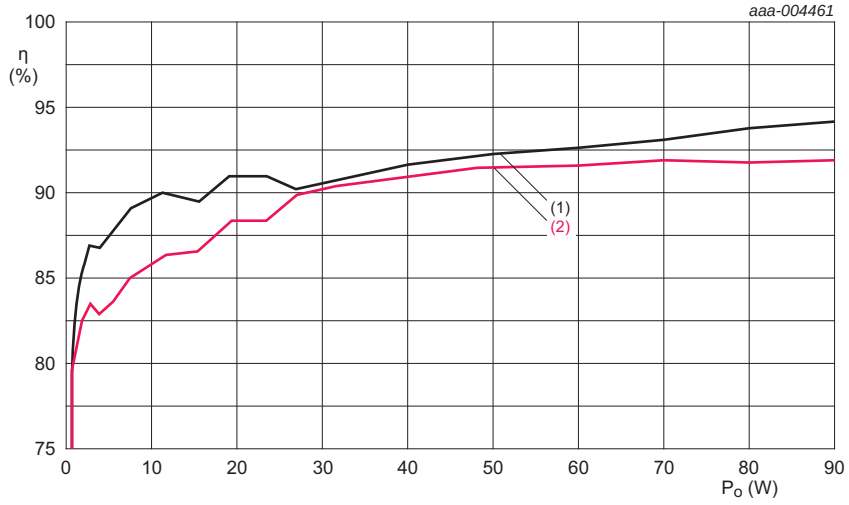
PFC bursting provides an extra power consumption reduction. The results of practical examples are shown in Figure 49, Figure 50 and Figure 51.



(1) V_{mains} = 230 V

(2) V_{mains} = 100 V

a. Full scale efficiency graph

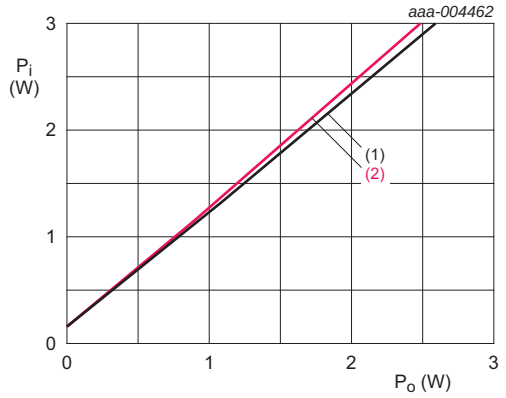


(1) V_{mains} = 230 V

(2) V_{mains} = 100 V

b. Efficiency graph zoomed

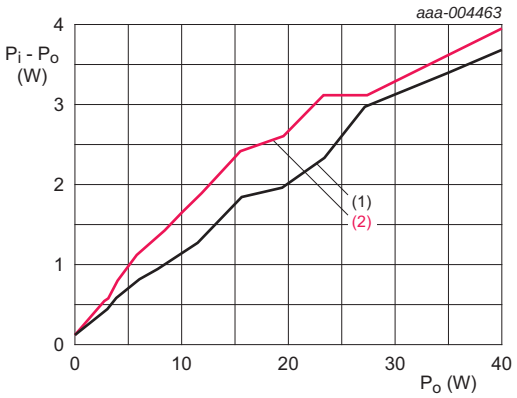
Fig 49. Increased efficiency at low output power



(1) V_{mains} = 230 V

(2) V_{mains} = 100 V

Fig 50. Input power 90 W adapter at low output power in burst mode operation



(1) V_{mains} = 230 V

(2) V_{mains} = 100 V

Fig 51. 90 W adapter losses in burst mode under P_o = 27 W

10.4 Burst mode controlled using the SNSBURST pin

The HBC and the PFC of the TEA1716 can be operated in Burst mode. In Burst mode, the converters operate for a limited time and are then non-operational for a period. Burst mode operation increases the efficiency during low-load conditions.

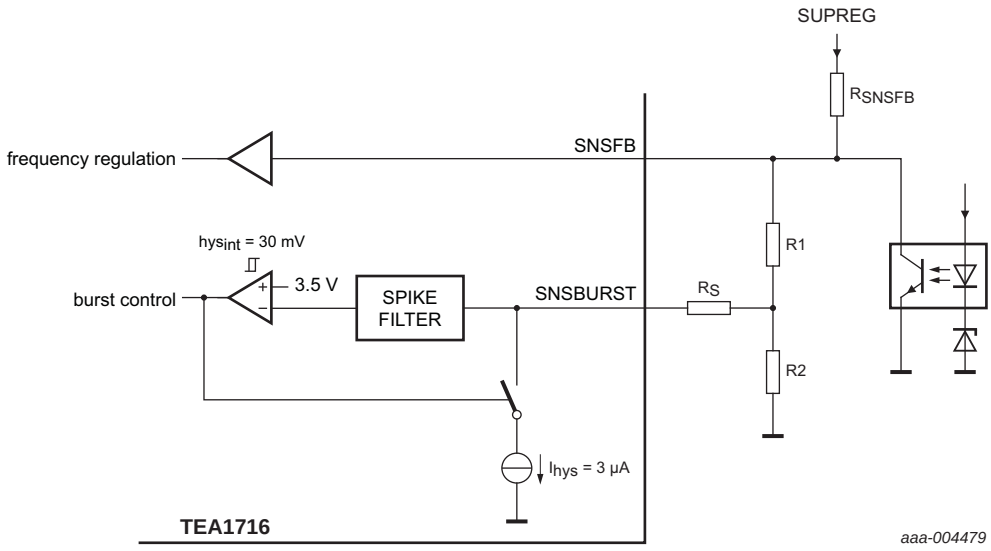


Fig 52. Circuit for burst mode operation with SNSFB and SNSBURST levels

The voltage on the SNSBURST pin defines the transition from operational supply state (burst-on period) to burst stop state (burst-off period) and back.

The voltage on the SNSFB pin represents the level of power that is converted. The voltage on the SNSBURST pin can be related to the SNSFB pin using an external resistor divider. Pin SNSBURST has an internal switching reference level of 3.5 V and a fixed hysteresis of 30 mV.

Additionally, a switched current of 3 µA flowing into the SNSBURST pin and the resistance value of the external divider determine the effective additional hysteresis (3 µA × (R1 + RS)). The current flows when SNSBURST pin the voltage is under 3.5 V (= burst-off period). It stops when the voltage exceeds 3.53 V (3.5 V + 30 mV). The operation of the HBC controller is suspended when the voltage on the SNSBURST pin drops under 3.5 V. The PFC operation is conditionally suspended at the same moment. However, the PFC can continue when the boost voltage is still under the regulation level. When the PFC regulation level is reached, it stops using a soft-stop. The HBC stops almost directly when the GATELS pin becomes active.

The burst stop state is entered when both PFC and HBC have stopped switching. In the burst stop state, the current consumption of the IC is low and the SNSOUT pin is pulled low. This SNSOUT signal reflects the IC state. It can be used for synchronizing additional functionality in the application.

When the voltage on the SNSBURST pin exceeds 3.53 V (3.5 V + 30 mV), the TEA1716 exits the burst stop state and enters the operational supply state. A settling time of approximately 50 µs allows internal supplies to stabilize before starting the burst. The PFC starts its operation using a soft-start. The HBC resumes operation without a soft-start sequence.

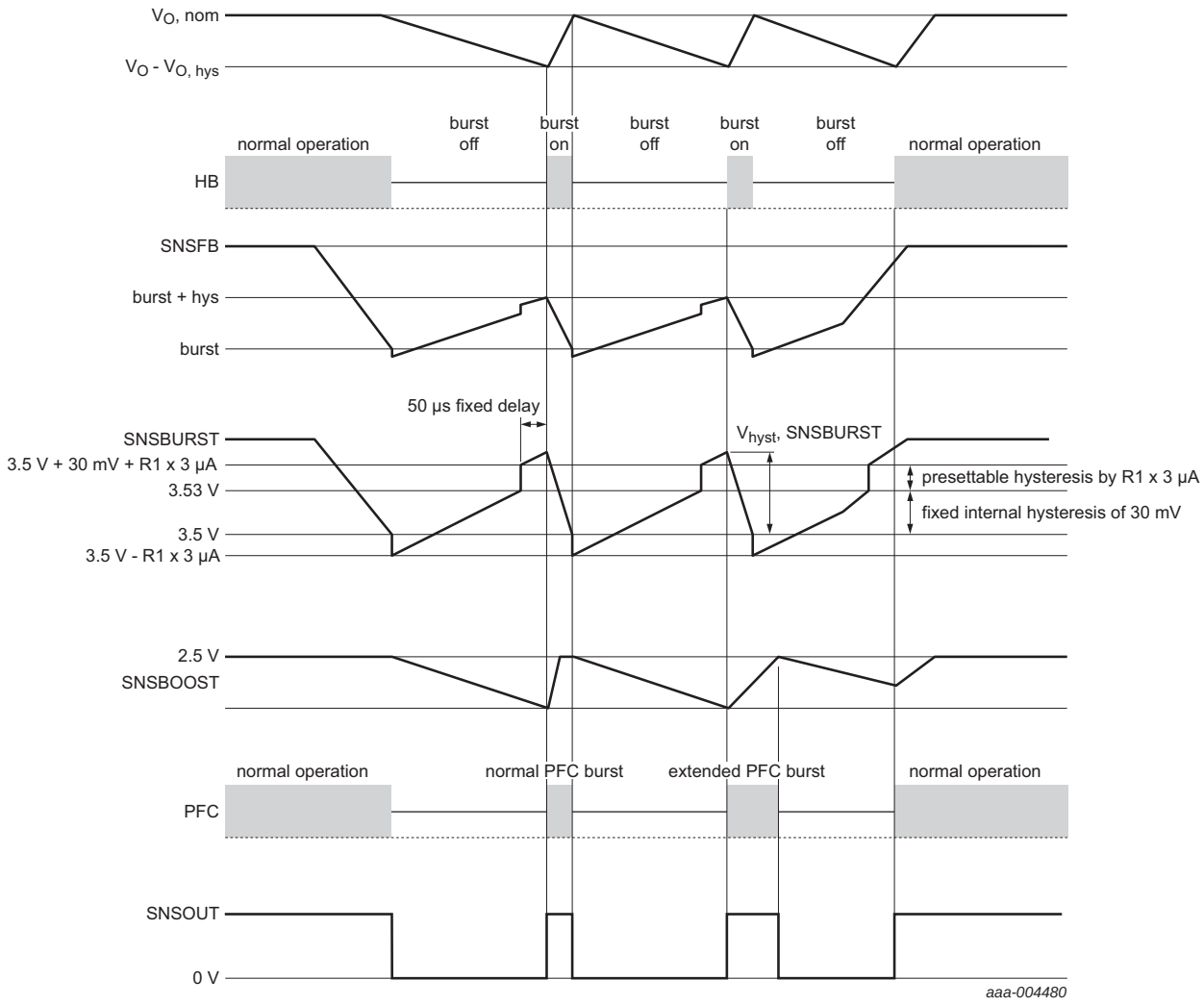
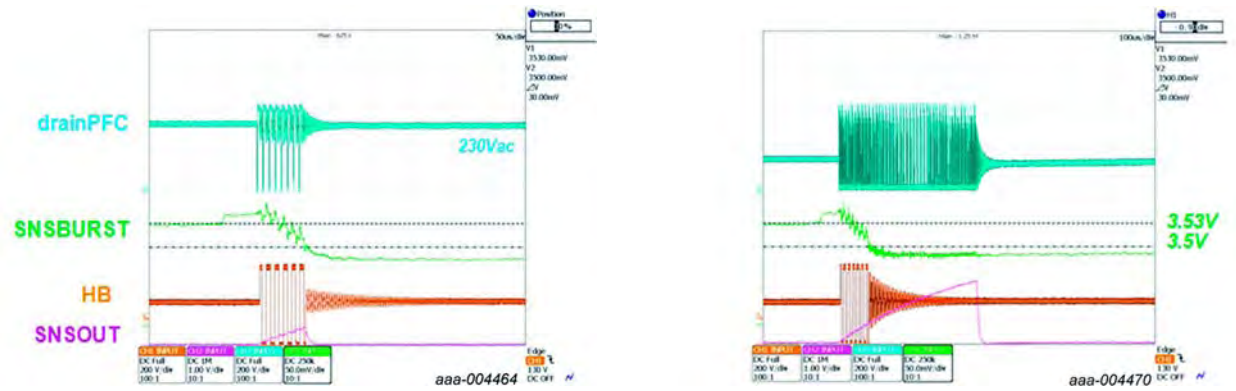


Fig 53. Burst mode operation with SNSBURST levels and SNSOUT signal



a. Standard burst

b. Burst with a longer PFC burst duration

Fig 54. TEA1716: HBC and PFC in burst mode operation

During start-up, burst mode operation is not enabled until the SNSOUT pin has reached 2.5 V to avoid unwanted activation.

10.5 Burst mode disabled at start-up

Burst mode operation is not enabled during start-up until the voltage on the SNSOUT pin has exceeded 2.5 V once to avoid unstable start-up behavior.

The period for disabling burst mode operation can be preset by designing the rise time of the SNSOUT voltage (see Section 11.6.2). The design must be made in a moderate way to avoid problems for the remaining SNSOUT functionality.

10.6 Choice of burst level and hysteresis level

The voltage levels (that represent power levels) for bursting are set using a resistive divider from the SNSFB pin to the SNSBURST pin.

The basic choice for the voltage level can be made experimentally. In certain cases, the choice is made to obtain the lowest input power at a certain output power. For example at P_o = 0 W or at P_o = 250 mW.

See Section 11 for a practical implementation method of the burst mode and the discussion of potential problems.

10.6.1 SNSBURST circuit

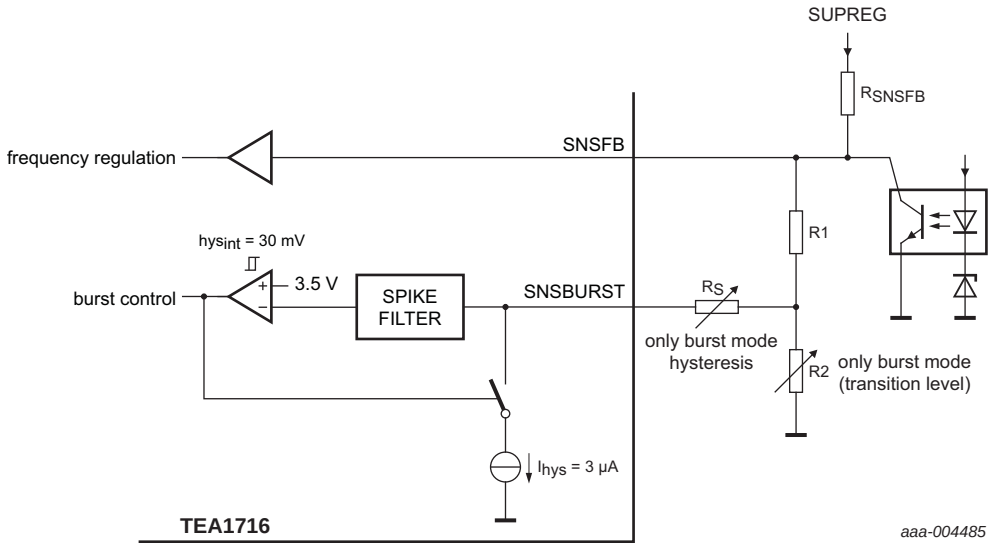


Fig 55. Typical SNSBURST circuit showing the independent functions of Rs and R2

- R_{SNSFB}

  Pull-up resistor on the SNSFB pin to supply the voltage that is required for the SNSFB regulation. The amount of current that the optocoupler draws determines the voltage value on the SNSFB pin. This function does not influence the burst mode function setting but it contributes to the feedback signals dynamic behavior (also in burst mode operation).

  The value of the resistor is important for the power consumption at light load. It determines the bias current setting on the primary and secondary side of the feedback circuit (see Section 9.5.1).

- R1

  Determines the transition level from burst mode to normal mode by its value in relationship to R2. The R1 value also determines the part of the burst mode hysteresis that can be preset in combination with the internal 3 μA current source.

- R2

  Determines the transition level from burst mode to normal mode by its value in relationship to R1. Using R2, the transition level can be preset independently from the hysteresis (preset by R1 and R_S).

- R_S

  R_S is an optional component for obtaining a large hysteresis. The value of RS (together with R1) determines the presettable part of the burst mode hysteresis combined with the internal 3 μA current source. Using R_S the hysteresis can be preset independently of the transition level (preset by R1 and R2). Normally, R_S is not needed and can be set to 0.

10.6.2 Burst mode level

From the $P_o - V_{SNSFB}$ characteristic a level can be selected for the transition between burst mode operation and normal mode operation. The SNSBURST comparator level is 3.5 V.

$$V_{SNSBURST} = V_{SNSFB} \times \frac{R2}{R1 + R2} = 3.5\ V \quad (38)$$

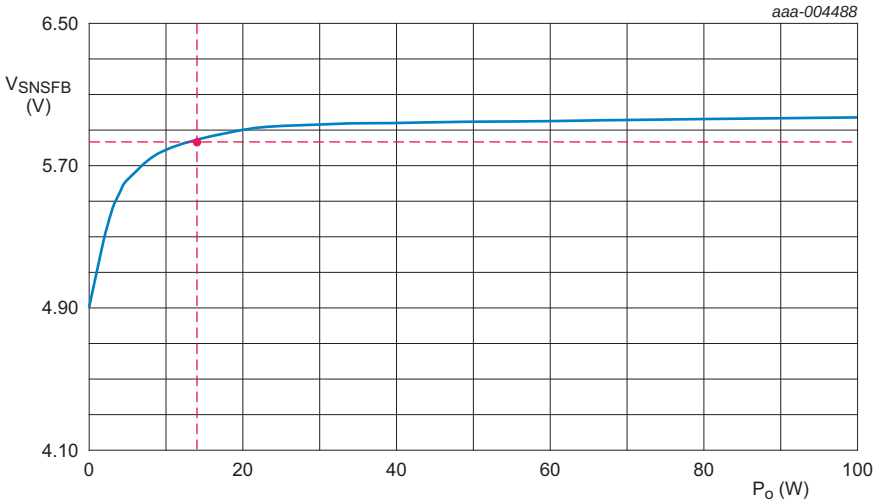
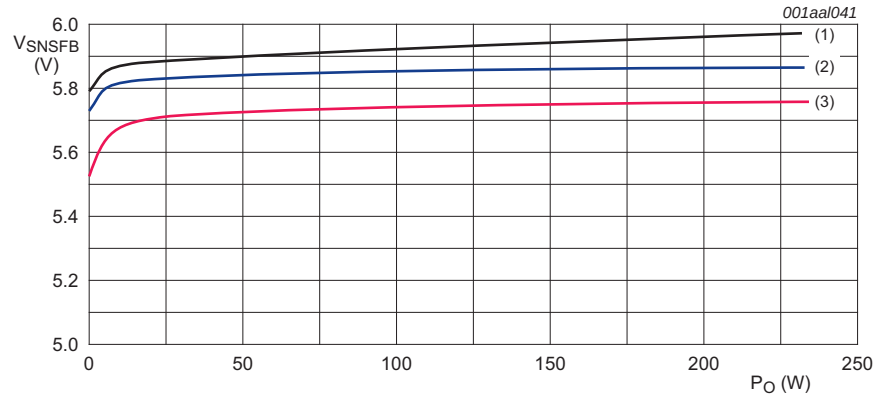


Fig 56. Example of selecting a burst (transition) level

10.6.3 Burst level and variations on V_{boost}

The resonant converter input voltage V_{boost} influences the relationship between the HBC output power level and the SNSFB pin regulation voltage (see Figure 57). This behavior can have a serious influence on the burst mode operation because it operates on a preset SNSFB voltage level. By a changing boost voltage (V_{boost}), the voltage on the SNSFB pin stands for a different power level.



(1) V_{boost} = 310 V (DC)

(2) V_{boost} = 350 V (DC)

(3) V_{boost} = 390 V (DC)

Fig 57. Voltage on the SNSFB pin as a function of output power

10.6.4 Presetting the amount of hysteresis

Figure 55 shows the burst mode circuit.

The SNSBURST hysteresis has two components:

- A fixed internal hysteresis of 30 mV
- A hysteresis that can be preset by 3 μA × (R1 + R_S)

Hysteresis on the SNSBURST pin:

$$V_{hys(SNSBURST)} \approx V_{hys(SNSBURST)int} + I_{hys(SNSBURST)int} \times (R1 + R_S) \quad (39)$$

$$V_{hys(SNSBURST)} \approx 30\ mV + 3\ \mu A \times (R1 + R_S) \quad (40)$$

The hysteresis on the SNSBURST pin results in a hysteresis on the SNSFB pin:

$$V_{hys(SNSFB)} \approx V_{hys(SNSBURST)} \times \left(1 + \frac{R1}{R2}\right) \quad (41)$$

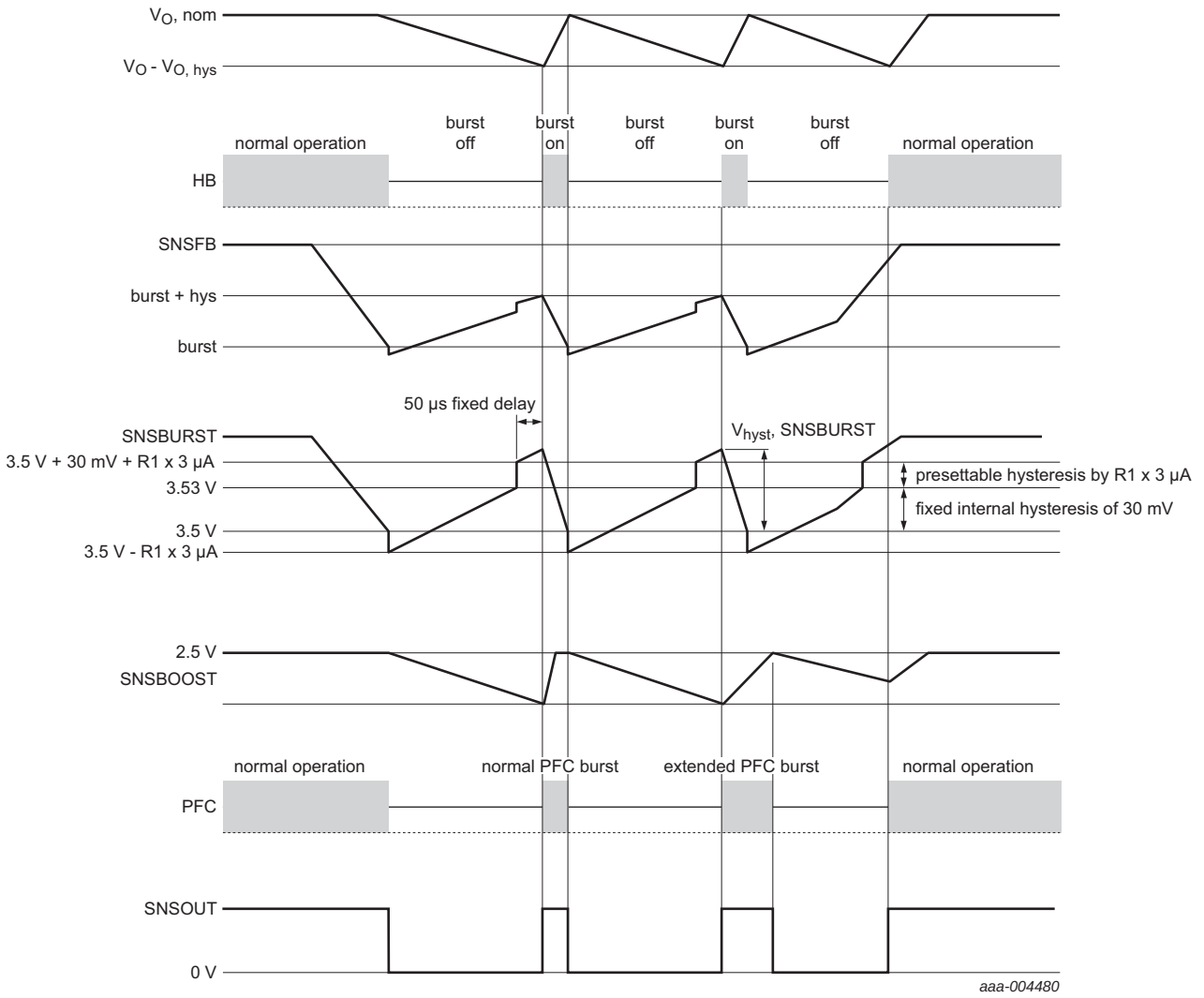
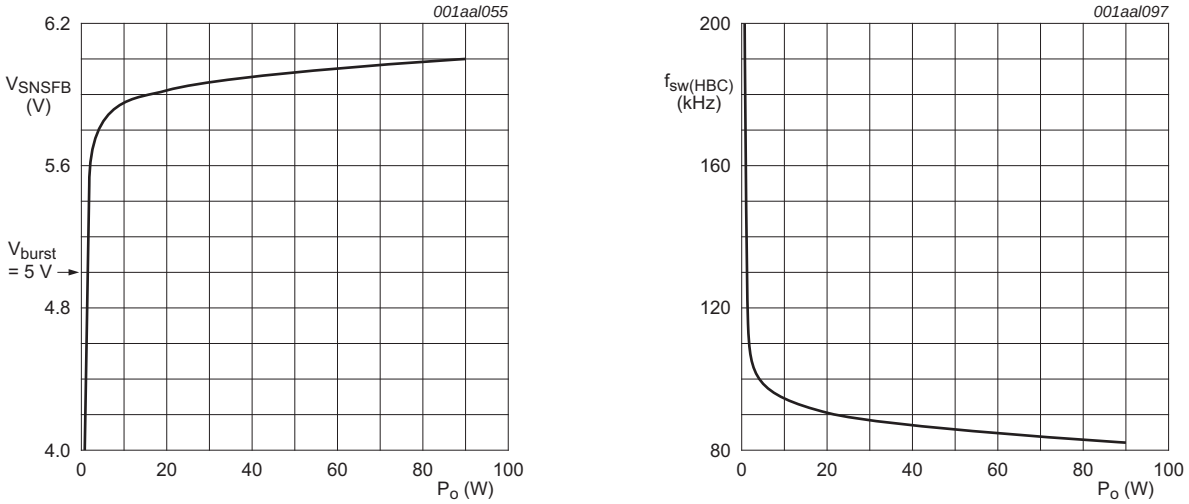


Fig 58. Burst mode operation sequences

10.7 Output power - operating frequency characteristics

Figure 57 shows that it is critical to make a design choice for a certain SNSFB voltage to start bursting. There is a risk that, due to spread, the system can either remain in burst mode or never reach burst mode operation at all.

The dimensioning of the LLC can be made more suitable for burst mode. The standard approach is to design the system in such a way that it cannot regulate to no-load, even at the highest frequency. During the lowest loads, the frequency required for regulation must become infinite. A voltage level can easily be chosen to ensure that burst mode is activated at the lowest load and the remaining load conditions operate in normal mode. The burst mode now enables the system to operate at no-load.



a. Voltage on the SNSFB pin as a function of output power

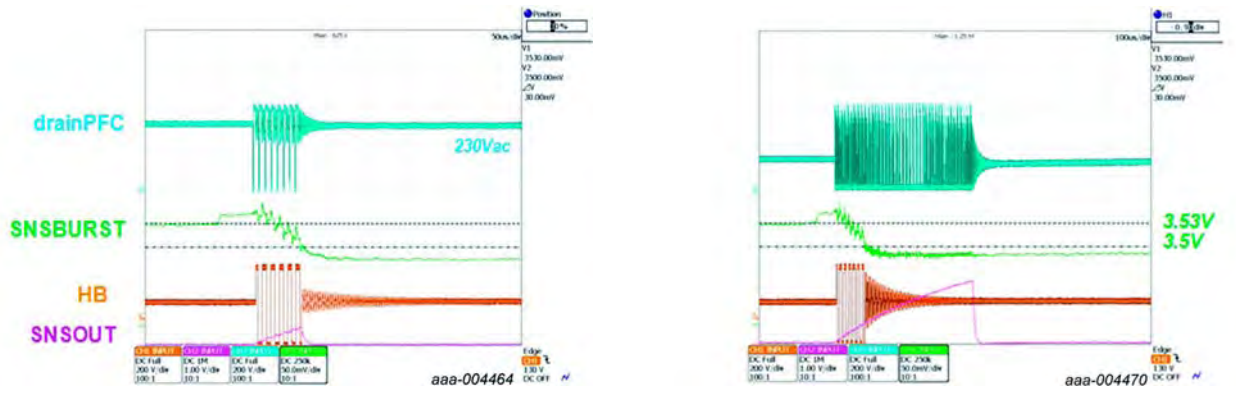
b. Frequency as a function of output power

Fig 59. Normal mode output power characteristics (Adapted for easy implementation of burst mode comparator level detection)

10.8 PFC converter and resonant converter simultaneous bursting

When in the burst mode, PFC operation stops when the resonant converter is not switching. In most cases, this feature saves extra energy consumption by reduced switching losses from the PFC converter.

In some situations, the duration of the HBC burst is not long enough to reach the PFC regulation level. In the TEA1716, the PFC can continue operation until the correct PFC output voltage is reached to avoid unstable behavior.



a. Standard burst

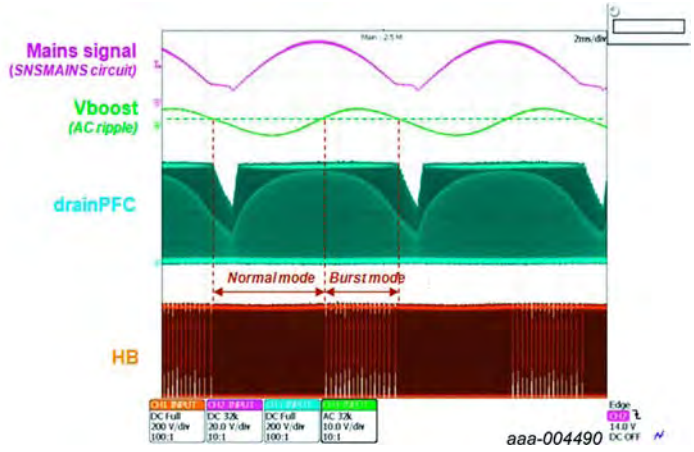
b. Burst using a longer PFC burst duration

Fig 60. Example of a longer burst duration for PFC

10.8.1 Alternating between burst and normal operation

Interaction between the PFC and the resonant converters in burst mode can lead to a situation where the system alternates between burst and normal modes under certain output power conditions.

Normally, variations of the boost voltage at a power output that is close to the transition level between burst and normal modes cause the alternating behavior. At this level, the output power is already relatively large which causes some mains voltage-related ripple on the boost voltage.



Depending on the boost voltage (V_{boost}) level (ripple due to mains voltage variation), the system is in burst mode or normal mode operation

Fig 61. Operation when the output power is near the burst transition level

10.9 Design guidelines for burst mode operation

- Design for a stable PFC (nominal) output voltage during burst mode.
- Optimize the regulation feedback loop for normal mode first for performance on steady operation, start-up/shutdown and load steps. The feedback must follow the output voltage accurately.
- After optimizing the normal operation, the burst mode operation can be implemented.
- The best efficiency is achieved when the number of cycles for each burst is as small as possible (only a few cycles). Use a resistor to tune the SNSBURST/SNSFB circuit so it presets the SNSFB burst level and hysteresis.
- Feed forward capacitors are often used in the error amplifier circuit. Optimizing behavior with such improvements must be performed moderately, while constantly checking the results in burst and normal modes for the different test conditions. An improvement for one condition often gives an undesired effect in another condition.
- System and component tolerances play a significant role in production performance variations. Some performance margins on the nominal design can help to handle this spread.

Section 11 shows a method for making choices in burst mode operation illustrated with practical examples and advice.

10.10 Lower SUPHS in burst mode

During the idle time, C_{SUPHS} is not charged.

During normal operation, each time the half-bridge node HB is switched to ground level, the external diode bootstrap function between the SUPHS and SUPREG pins charges the SUPHS capacitor. In burst mode, there are periods of non-switching, and therefore no charging of the SUPHS pin. During this time, the circuit supplied by the SUPHS pin slowly discharges the supply voltage capacitor. When a new burst starts, the voltage on the SUPHS pin is lower than in normal operation. During the first switching cycles, C_{SUPHS} is charged to its normal level. It is important that, during these first recharge cycles, the SUPREG pin does not drop under the protection level of 10 V.

10.11 Audible noise

The converted energy does not contribute much to generate audible noise because the burst mode is normally used when the output power is low. The magnetization current, however, is still present during low loads and is the dominant energy during burst mode.

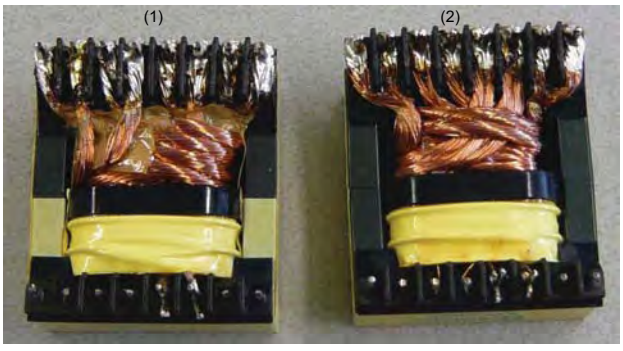
Switching the converter sequences on and off continuously at a certain speed and duration can lead to audible noise. The main mechanism for producing noise is the interruption of magnetization current sequences leading to a mechanical force. The core of the resonant transformer is especially susceptible and starts acting like a loudspeaker.

When burst mode is applied during higher output power conditions, the converted energy also leads to an increased risk of audible noise.

10.11.1 Measures in the resonant transformer construction

Adapting the mechanical transformer construction is required to prevent problems with audible noise under specific conditions.

One measure is to adhere the core parts to each other using a material with damping (vibration absorbing) properties. A combination can be made using the air gap construction. Other vibration damping measures can also help when audible noise is a critical issue for a product.



001aal056

(1) Left-hand transformer using glue on the wire to reduce audible noise

(2) Right-hand transformer using a standard construction

Fig 62. Transformer construction

10.11.2 Burst power-dependent noise level

The amount of audible noise is related to the amount of energy in each burst.

The magnetization current of the resonant converter determines the amount of energy at low output power. The amount of transferred energy is low. Use the burst mode only at low power to avoid problems with audible noise. When the transition level between normal and burst modes is chosen at a higher output power, the audible noise level is larger.

Overshoot on feedback voltage

When the output load is increased, the system reverts to normal operation. The transition from burst mode to normal mode is based on the feedback voltage. In certain burst conditions, the feedback voltage can overshoot. The system is kept in burst mode at higher output power levels than intended. As the power level in this situation is larger, the amount of noise is also larger.

10.12 Enable/disable burst mode switch

In microcontroller operated applications such as a TV, a clear separation is made between normal operation and standby operation.

An enable/disable function can be added to avoid the resonant converter going into burst during short periods of low load in normal operation. An extra enable/disable switch function on the SNSBURST pin can be used to implement this function.

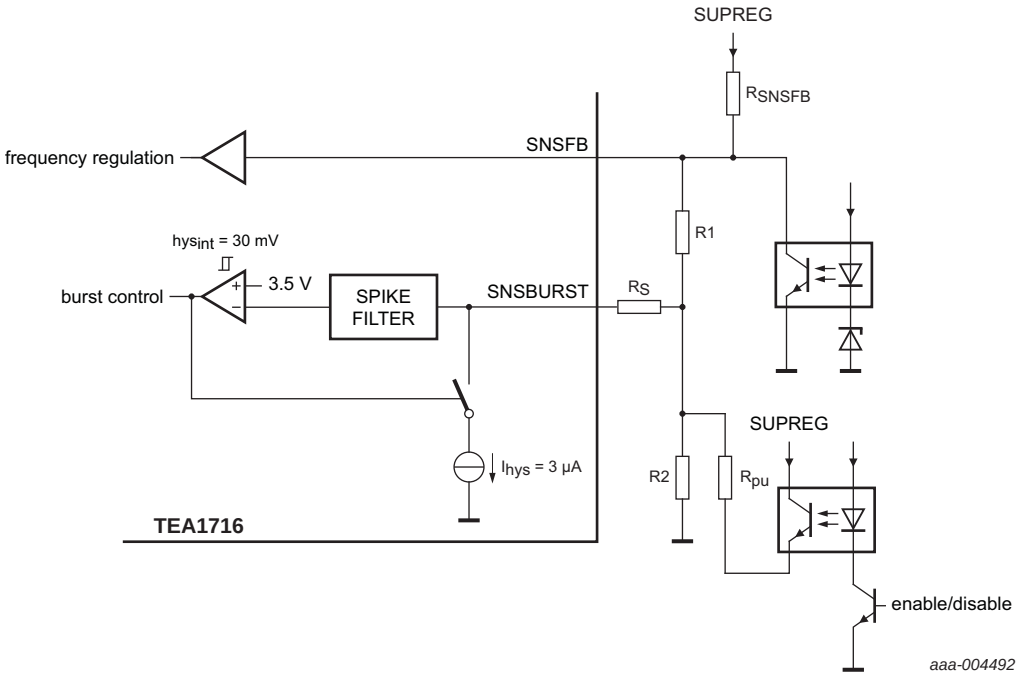


Fig 63. Enable/disable burst mode switch

The enable/disable function can also be used to implement a better defined transition for entering and leaving burst mode operation. See Section 11.11.

10.13 Unused burst mode

When the burst mode is not required, ensuring that the SNSBURST level does not drop under 3.5 V can prevent it from starting.

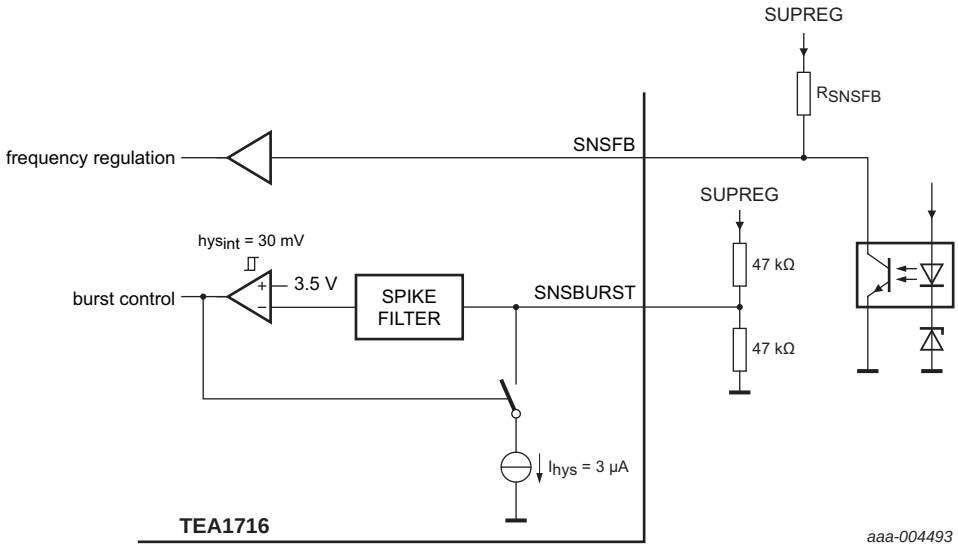


Fig 64. Burst mode operation unused

11. Practical issues when implementing burst mode operation

A step-by-step method can be followed to implement burst mode operation:

1. Measure the behavior of the LLC converter in normal operation mode.
2. Determine the transition (power) level from burst mode to normal mode operation.
3. Make the corresponding SNSBURST resistor divider and preset the hysteresis.
4. Check the burst mode operation.
5. Tuning in practice to obtain the "best" performance (or compromise).
6. Potential problems in the feedback for regulation SNSFB.

11.1 Measure the behavior of the LLC converter in normal operation mode

It is important to know the (typical) relationship between the feedback voltage (SNSFB) and the output power as preparation for making a design choice on the burst transition level.

This relationship is derived in normal mode operation to obtain the information over the complete output power range.

- Disable burst mode operation by connecting the SNSBURST pin to the SNSFB pin.

  The voltage on SNSBURST does not (normally) drop under 3.5 V and therefore does not enable bursting. R_{BURST1} = 0 Ω.
- Vary the output power (current) and measure the voltage on the SNSFB pin as follows:
  - Measuring several points statically
  - Applying a dynamic current load (see Section 11.4 and Figure 68)
  - Measure directly the SNSFB voltage at the desired burst level

Table 5. Data measurement from normal operation

	Practical measurement data from normal operation (not burst mode)													Point
P_o (%)	0	1	2	3	4	5	10	20	30	40	60	80	100	**13.94**
V_{SNSFB} (V)	4.90	5.10	5.30	5.45	5.55	5.62	5.79	5.90	5.93	5.94	5.95	5.96	5.97	**5.83**
f_{HB} (kHz)	113	104	95	89	84	81	74	69	67	67	66	66	66	**72**

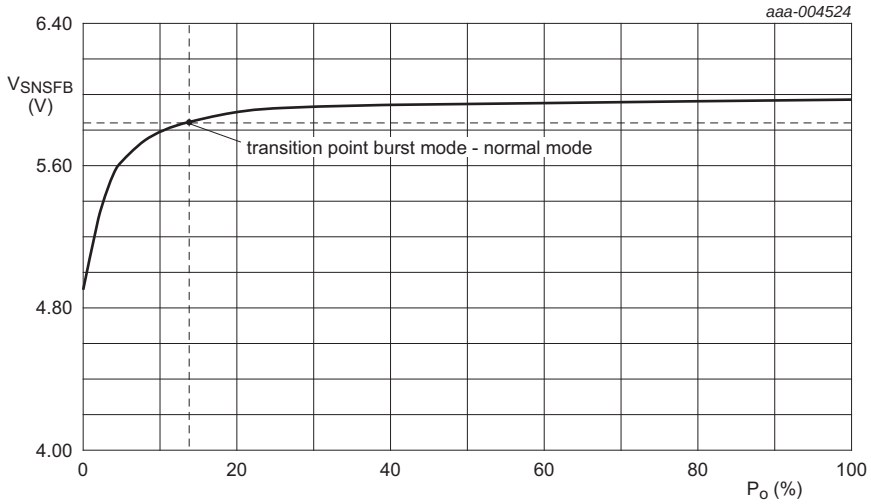


Fig 65. Example of a measured P_o against SNSFB relationship using a choice of the transition point

11.2 Determine the power level at which the supply operates in burst mode

Examples of goals that determine the choice of burst mode transition level are:

- Improve the efficiency curve to reach a higher efficiency at lower power levels; make a flatter efficiency characteristic
- Obtain the lowest losses at certain power levels: lowest power consumption at no-load or in standby (P_o = 250 mW)
- Improve efficiency or reduce losses but with a low(er) level of audible noise

A point on the P_O against SNSFB curve can be selected from the information obtained: the SNSFB voltage level value.

11.3 Calculate the SNSBURST circuit values corresponding to the chosen SNSFB voltage

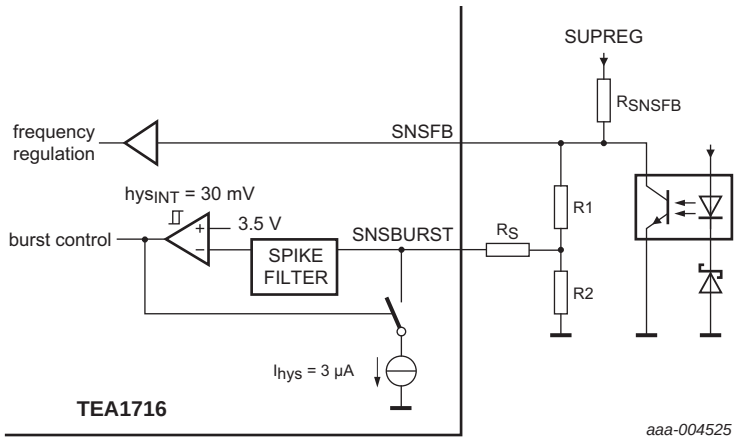


Fig 66. SNSBURST: standard basic application

The SNSBURST comparator level is 3.5 V.

$$V_{SNSBURST} = V_{SNSFB} \times \frac{R2}{R1 + R2} = 3.5\ V \quad (42)$$

Remark: R_S is an optional component that can be used to increase/optimize the amount of hysteresis (independently from the resistive divider R1 and R2). Normally, this component is not required and its value can be set to 0.

Estimate the required amount of hysteresis on SNSFB and/or SNSBURST.

The hysteresis on the SNSBURST pin consists of two parts:

- Fixed internal hysteresis of 30 mV
- User preset hysteresis by 3 µA × (R1 + R_S)

Hysteresis on the SNSBURST pin:

$$V_{hys(SNSBURST)} \approx V_{hys(SNSBURST)int} + I_{hys(SNSBURST)int} \times (R1 + R_S) \quad (43)$$

$$V_{hys(SNSBURST)} \approx 30\ mV + 3\ \mu A \times (R1 + R_S) \quad (44)$$

Hysteresis SNSFB:

$$V_{hys(SNSFB)} \approx V_{hys(SNSBURST)} \times \left(1 + \frac{R1}{R2}\right) \quad (45)$$

Example (see Figure 65):

- SNSFB burst point: 5.83 V
- Small hysteresis on SNSBURST: R_S = 0 Ω
- Presettable hysteresis: 30 mV

Hysteresis SNSBURST:

$$V_{hys(SNSBURST)}\ (presettable) \approx 3\ \mu A \times (R1 + R_S) = 30\ mV \quad (46)$$

- R_S = 0 kΩ
- R1 = 10 kΩ

$$V_{hys(SNSBURST)} \approx 30\ mV + 3\ \mu A \times (10\ k\Omega + 0\ \Omega) = 60\ mV \quad (47)$$

Burst point SNSBURST:

$$V_{SNSBURST} = V_{SNSFB} \times \frac{R2}{R1 + R2} \quad (48)$$

$$3.5\ V = 5.38\ V \times \left(\frac{R2}{10\ k\Omega + R2}\right) \quad (49)$$

$$3.5\ V \times (10\ k\Omega + R2) = 5.38\ V \times R2 \qquad R2 = 15\ k\Omega$$

Hysteresis SNSFB:

$$V_{hys(SNSFB)} \approx V_{hys(SNSBURST)} \times \left(1 + \frac{R1}{R2}\right) \quad (50)$$

$$V_{hys(SNSFB)} \approx 60\ mV \times \left(1 + \frac{10\ k\Omega}{15\ k\Omega}\right) = 100\ mV \quad (51)$$

The hysteresis on the SNSBURST and SNSFB pins results in a small amount of ripple on the output voltage (see Figure 67).

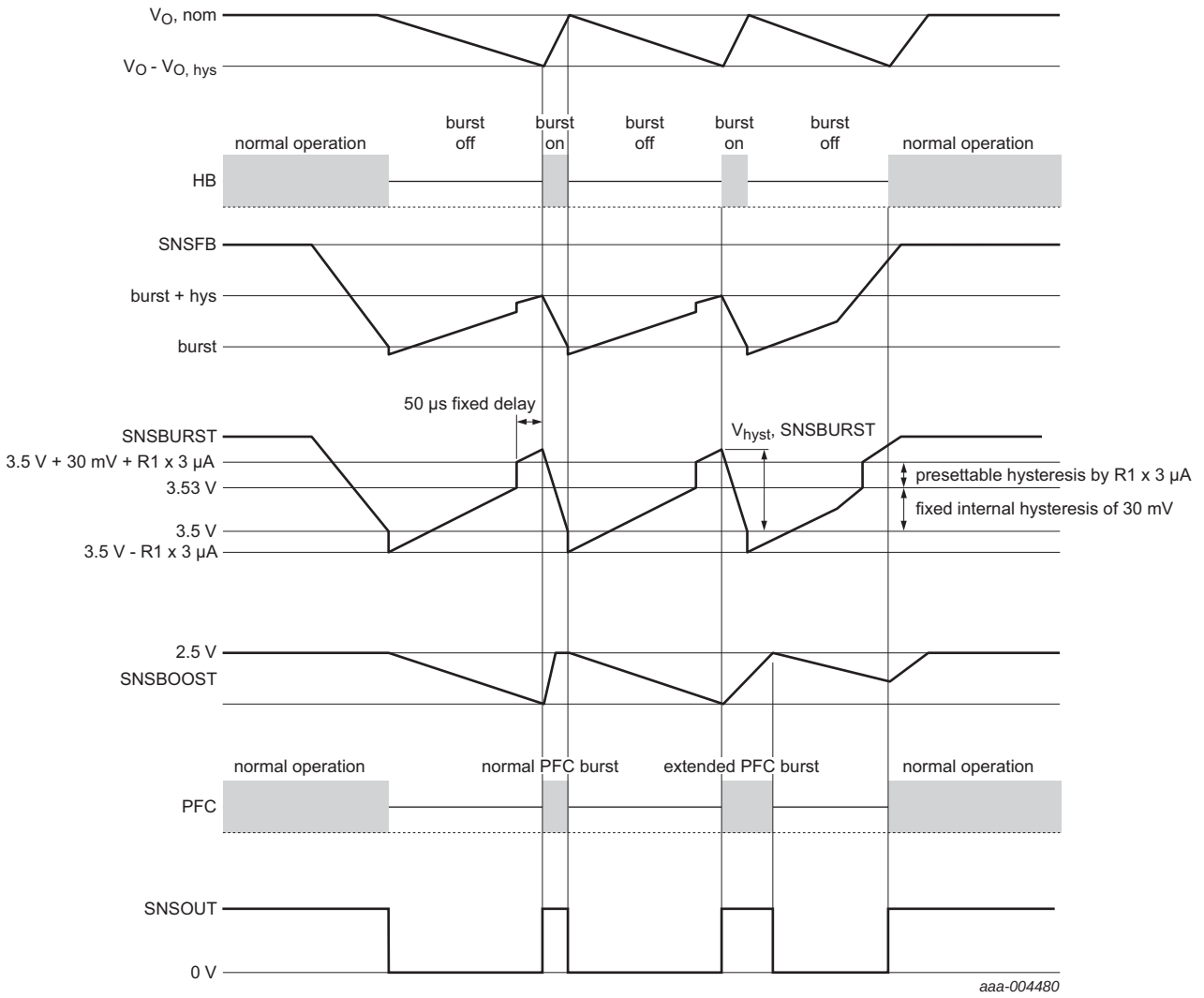
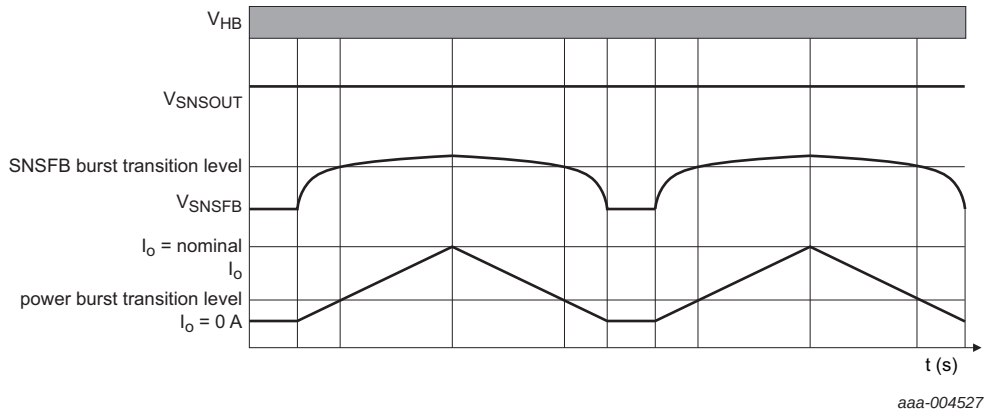


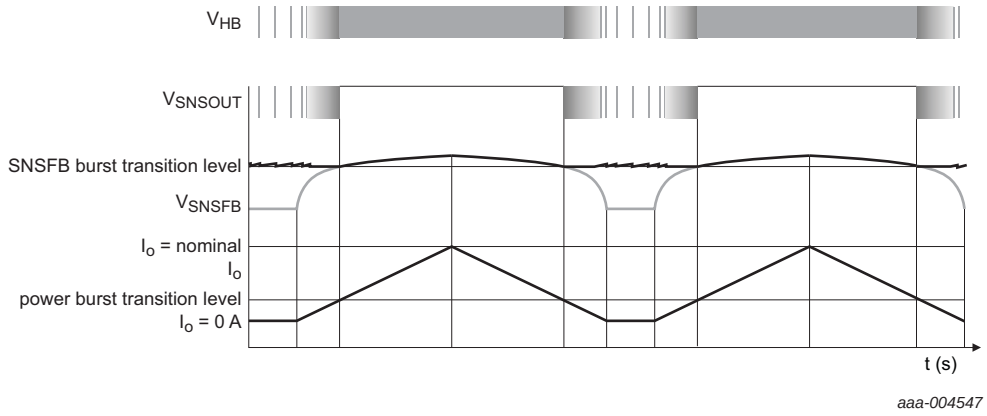
Fig 67. Burst mode operation sequences

11.4 Check the burst mode operation

A complete feedback behavior check of an application can be made by applying an output current/power sweep from 0 to nominal. Figure 68 shows an example of a sawtooth shaped current load to check the regulation behavior in an oscilloscope picture. This method can be used before and after the implementation of the burst mode.



a. Normal operation



b. Burst mode operation

Fig 68. Example of checking the operation/regulation over the complete power range

11.5 Feedback circuit for regulation

There are several aspects that require attention when designing the output voltage sensing circuit that provides the regulation by pin SNSFB:

- Stable regulation at all power levels
- Smooth start-up behavior (Section 11.6)
- Good dynamic behavior at load steps (Section 11.7)
- Good dynamic behavior in burst mode operation for best power saving (Section 11.8)

The first three aspects are valid for all regulated power supplies. A normal design effort gives a good result. When adding burst mode operation the options in design become more restricted and more complex. When combined with challenging power-saving targets, it can become difficult to reach the required behavior for all items in all conditions. Items 1 and 2 often contradict items 3 and 4.

11.6 Output voltage during start-up

In most applications, it is important to have a smooth rise of the output voltage.

In a system that includes burst mode operation, the general advice to obtain good start-up behavior is; make a good start-up behavior with the burst mode temporarily disabled. Then when the start-up behavior in this situation is correct, implement and optimize the burst mode while continually rechecking the start-up for correct functioning.

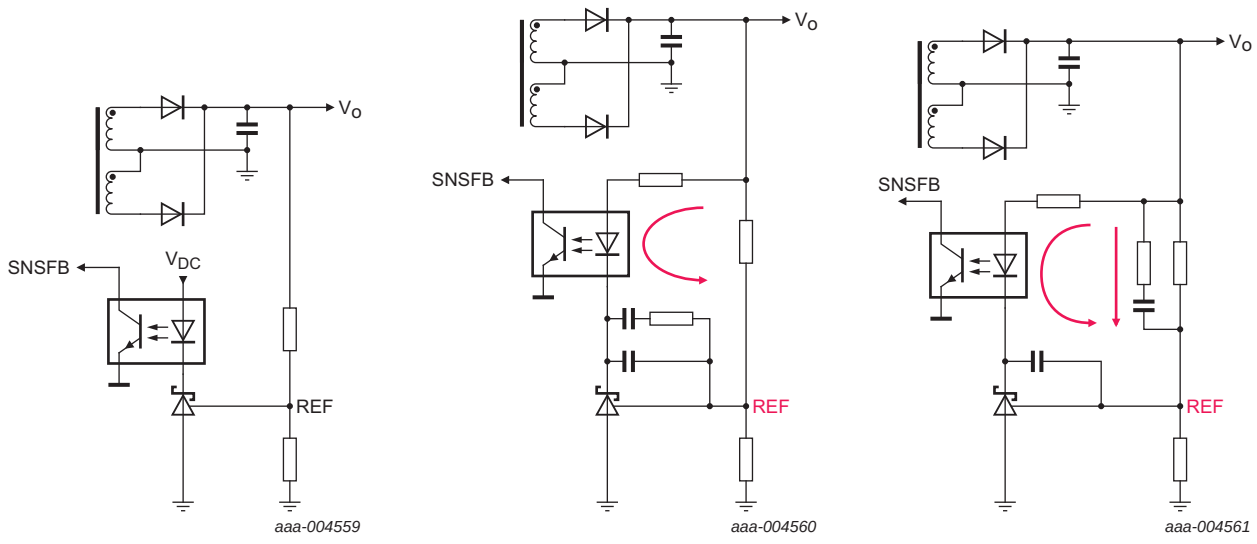
11.6.1 Output voltage variation because of error amplifier circuit

A capacitive path is added in the error amplifier circuit for good regulation effect during load variations. Figure 69 shows the basic circuit and two practical circuit examples. The capacitive path can have a negative effect on the output voltage rise during start-up when the capacitive coupled effect is too strong. As the voltage on the reference pin rises faster than the real output voltage, the error amplifier concludes that the nominal output voltage is reached before it is. It reacts by reducing the amount of output power via the feedback signal. The effect is that the output voltage rise shows a hiccup (see Figure 70).

Using the capacitive feedback in a moderate way can prevent this problem.

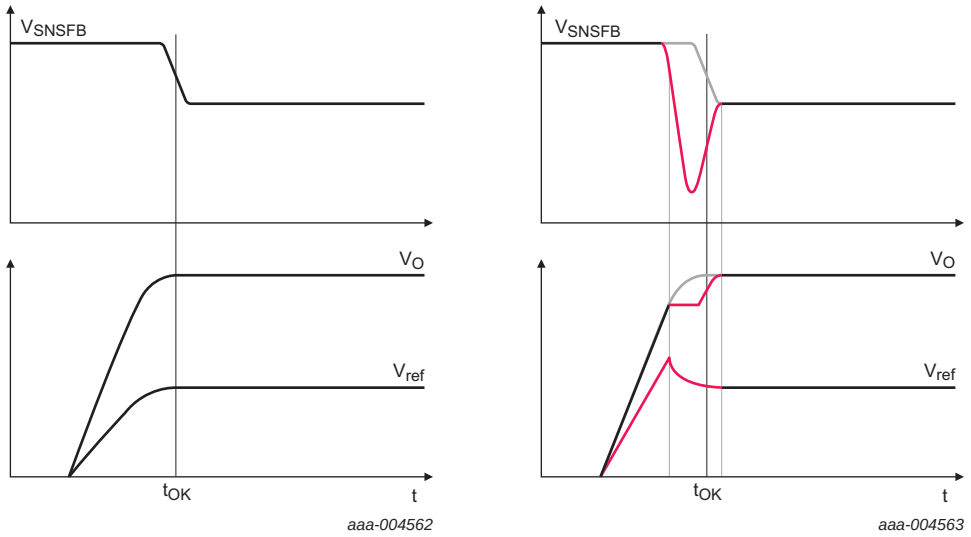
The value of the capacitor and the value of a possible series resistor determine the capacitive feedback.

A trade-off between the dynamic behavior (load variations and burst mode operation) and the start-up behavior can be required.



a. Principle feedback circuit b. Practical example circuit 1 c. Practical example circuit 2

Fig 69. Examples of two feedback circuits that use a capacitive path



a. Proper star-up behavior

b. Wrong start-up behavior because of the effect of the capacitive path being too strong

Fig 70. Good and bad start-up behavior by regulation

11.6.2 Burst mode disabled at start-up by the SNSOUT pin

The TEA1716 provides a Failed Start Protection (FSP) detecting the SNSOUT voltage level of 2.5 V.

During start-up, the output voltage is under $V_{fsp(SNSOUT)}$ for a certain time. This situation is not considered an error condition if it does not last longer than expected. The protection timer is started when V_{SNSOUT} is under 2.5 V during start-up for this reason. Under normal conditions, the output voltage exceeds the 2.5 V level before the protection time is expired and no protective action is taken.

During start-up, until the voltage on the SNSOUT pin reaches 2.5 V, burst mode operation is disabled. This function is implemented to avoid extra complications during start-up like in the situation shown in Figure 70 and Figure 72.

If necessary, the SNSOUT pin voltage increase during start-up can be modified to suppress burst mode operation for a longer period than the start-up time for the output voltage. By suppressing it, the first period of regulation operates in normal mode. Suppression can be done with a capacitor connected to ground. This function prevents unstable behavior at the start of the regulation.

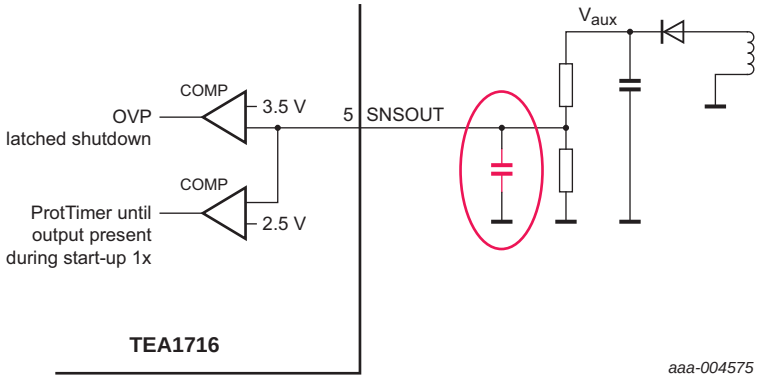


Fig 71. A capacitor on SNSOUT

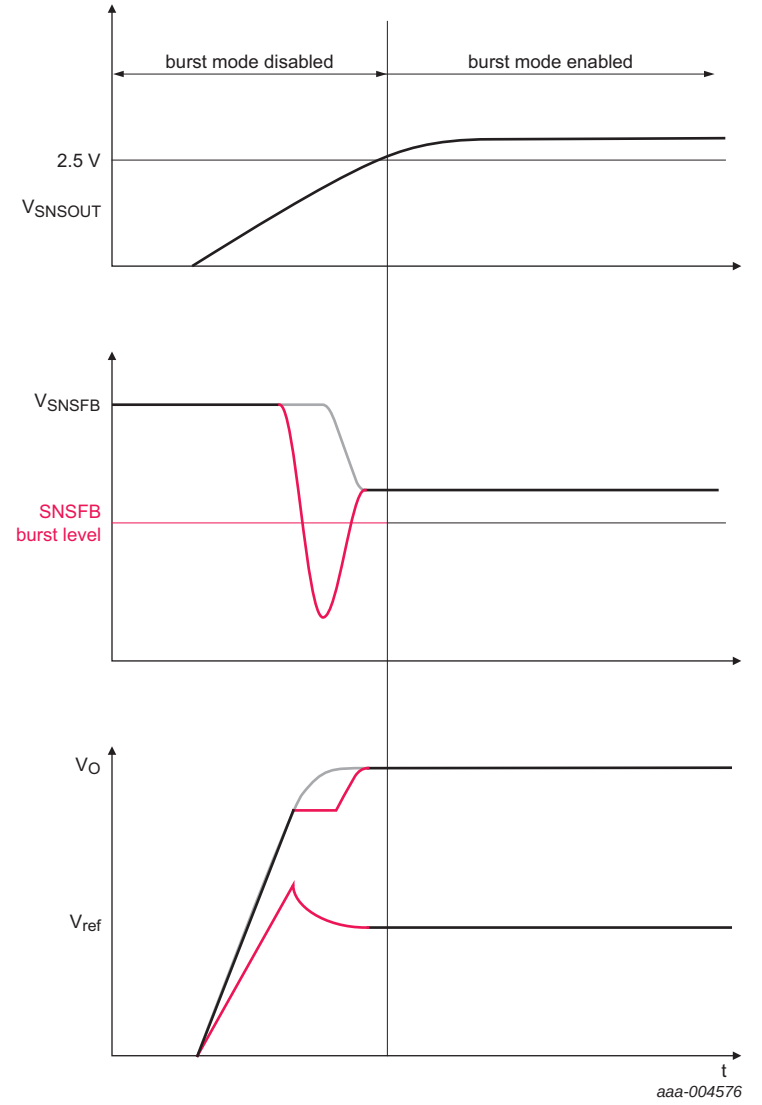


Fig 72. Burst mode operation disabled during start-up by SNSOUT voltage

When the SNSOUT pin reaches 2.5 V, burst mode operation is enabled and remains enabled until the TEA1716 stops operating and restarts, a restart or start-up is made.

11.6.3 Start-up time shorter than half a mains period

Keep the start-up time shorter than one half of the mains cycle period to avoid modulation of the output voltage by the rectified mains shape. Normally, the start-up time is within 16.6 ms and can be set using a capacitor value of 220 nF connected to the SSHBC/EN pin.

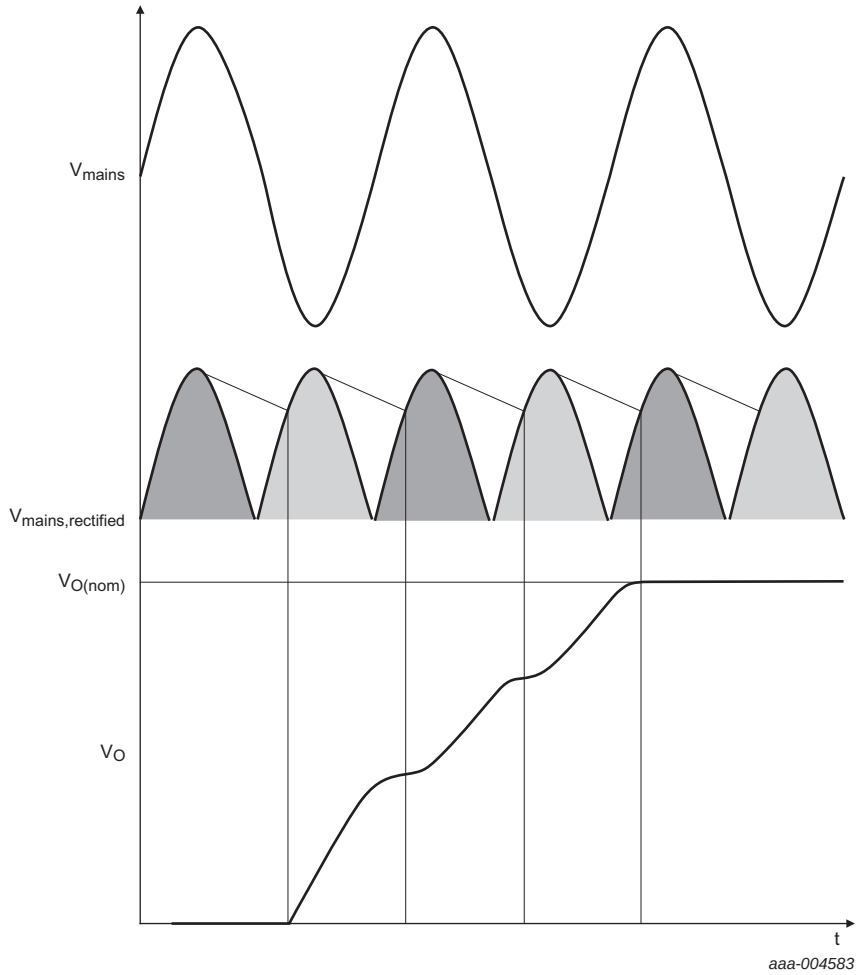


Fig 73. Output voltage rise variations because of modulation from the mains voltage

11.7 Load step behavior

Testing for load steps in burst mode operation can be critical depending on the dynamic behavior of the feedback loop.

Normally, the most critical conditions are:

- Entering normal mode using a step-up just after burst
- Entering burst mode using a step-up just after step-down

In general, the best method to obtain good performance is to follow the output voltage accurately by regulation. This way the feedback regulation reacts instantaneously and the load step is handled without problems.

In some cases, the dynamic behavior is modified to obtain a better power consumption performance in low-load conditions. This change can result in a feedback overshoot/undershoot behavior that gives a delay in the reaction on load steps. Modify the burst level, hysteresis (Section 11.3) or add an extra circuit (Section 11.9.1) to improve the power consumption performance under low load conditions.

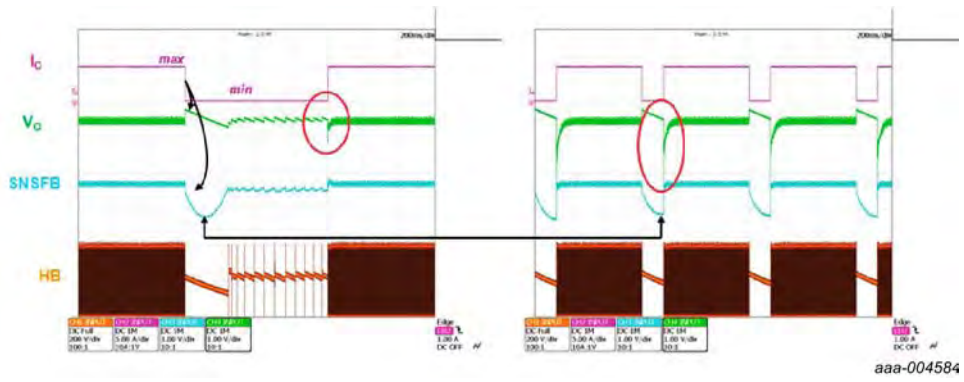


Fig 74. Critical load step conditions during burst mode operation

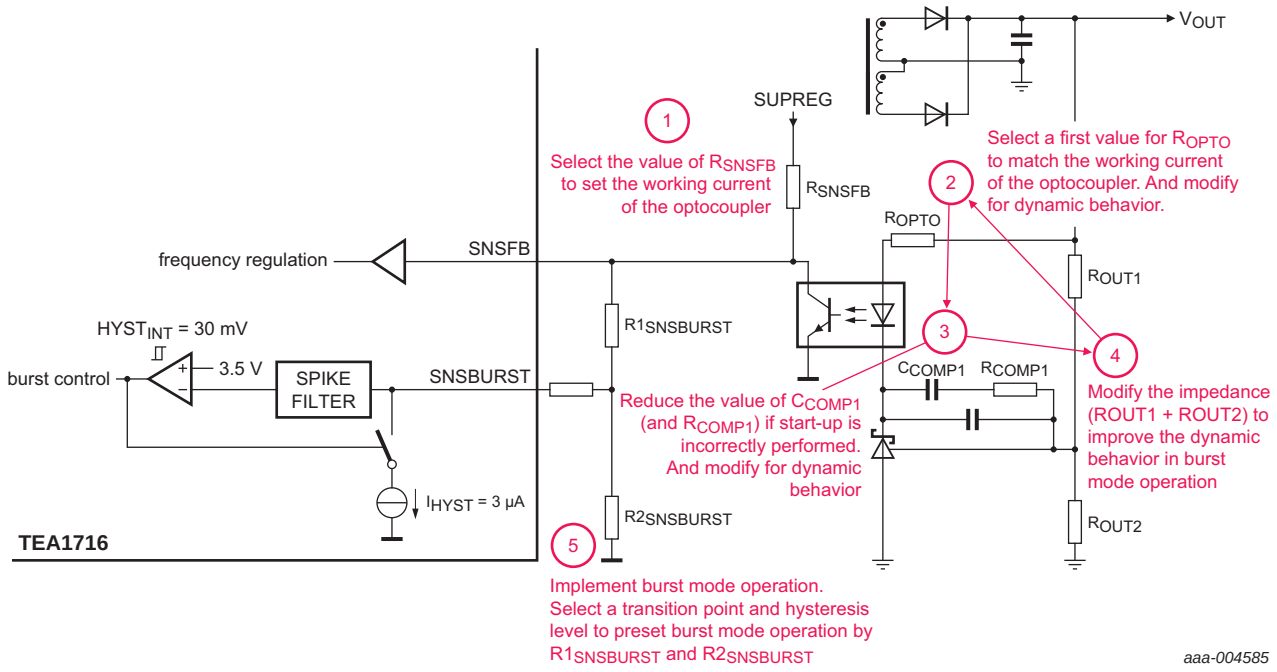
11.8 Optimize burst mode feedback behavior

Implementing burst mode operation requires some iterative practical optimization to meet all requirements.

Items to check are:

- Start-up behavior at different load conditions (smooth output voltage rise; see Section 11.6)
- Load step behavior (see Section 11.7)
- Burst mode operation: stable running at different load conditions
- Burst mode operation: transitions burst and normal mode
- Burst mode performance: low no-load or standby power consumption
- Normal mode: stable regulation at high output power

Figure 75 shows a way to implement and optimize a design.



(1) Start by implementation for normal mode operation: step 1 to 4.

(2) Implement burst mode operation step 5.

(3) Check (and modify) steps 2 to 4 to obtain good burst mode behavior. After completion, check the normal mode behavior again. When a modification is done (and also when step 5 is modified again), repeat the complete step 2 to 4.

Remark: Use the burst mode disable function on the SNSOUT pin to help preventing start-up problems.

Fig 75. Method to implement and optimize burst mode

11.9 Short burst duration for best no-load performance

Burst mode switching implemented in the TEA1716 uses an extra-high output current generated during the first cycle from the start behavior. Normally, the following cycles deliver much less output current due to a relatively high switching frequency.

The lowest losses are obtained using the high power current in the first cycles and limiting the number of cycles that generate less power.

A short burst duration is obtained using:

- Choice of a high Burst mode power level (see Section 11.2 and Section 11.3)
- A small burst hysteresis (see Section 11.3)
- An external switch that enforces a short duration

11.9.1 External switch to obtain a shorter burst duration

The SNSOUT function provides a synchronization signal during Burst mode operation. This signal can be used to pull down the voltage on the SNSFB pin faster than it normally does using the feedback signal. The synchronization signal results in an earlier stopping of the burst.

Figure 76 shows the principle. The capacitor on the SNSOUT pin determines when the switch is closed. The resistor R_{switch} determines the amount of current that is taken from the SNSFB pin to lower its voltage temporarily. Take the base current into account as it effects on the SNSOUT circuit when a bipolar transistor is used as the switch. When a MOSFET is used, select a type that is suitable for switching at a rather low gate voltage (< 3 V).

Keep in mind that the SNSFB regulation by the secondary error amplifier in principle compensates the lower voltage on the SNSFB pin. This method can work well because of the short duration of the event and the limit dynamics.

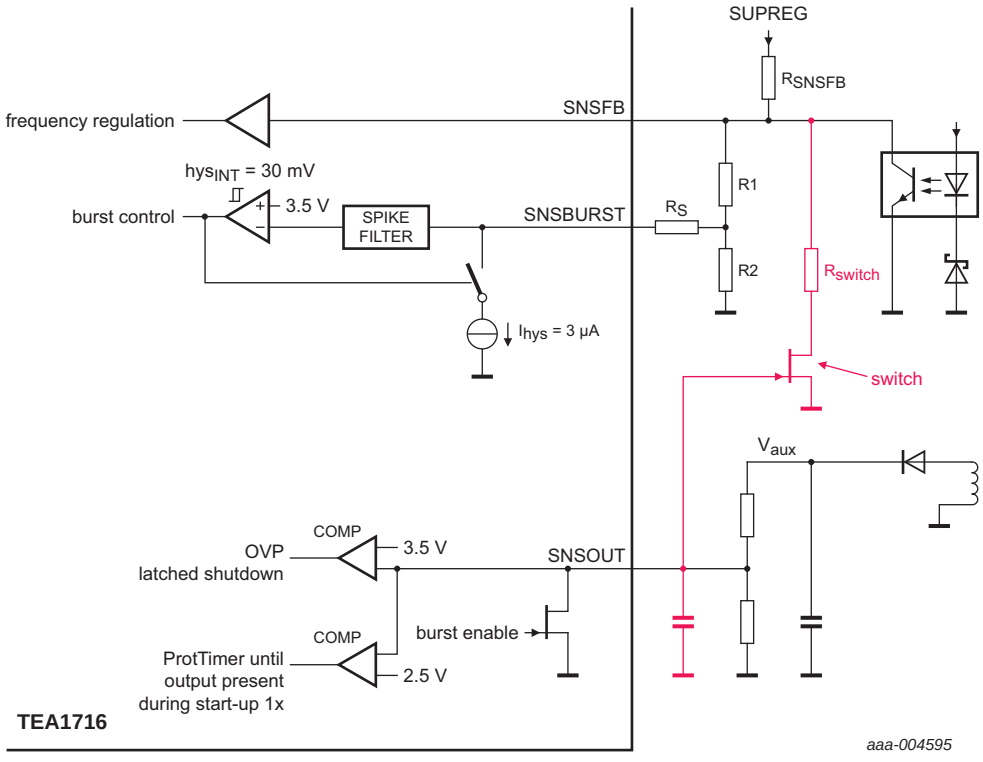


Fig 76. External switch driven using the SNSOUT signal to obtain a short duration

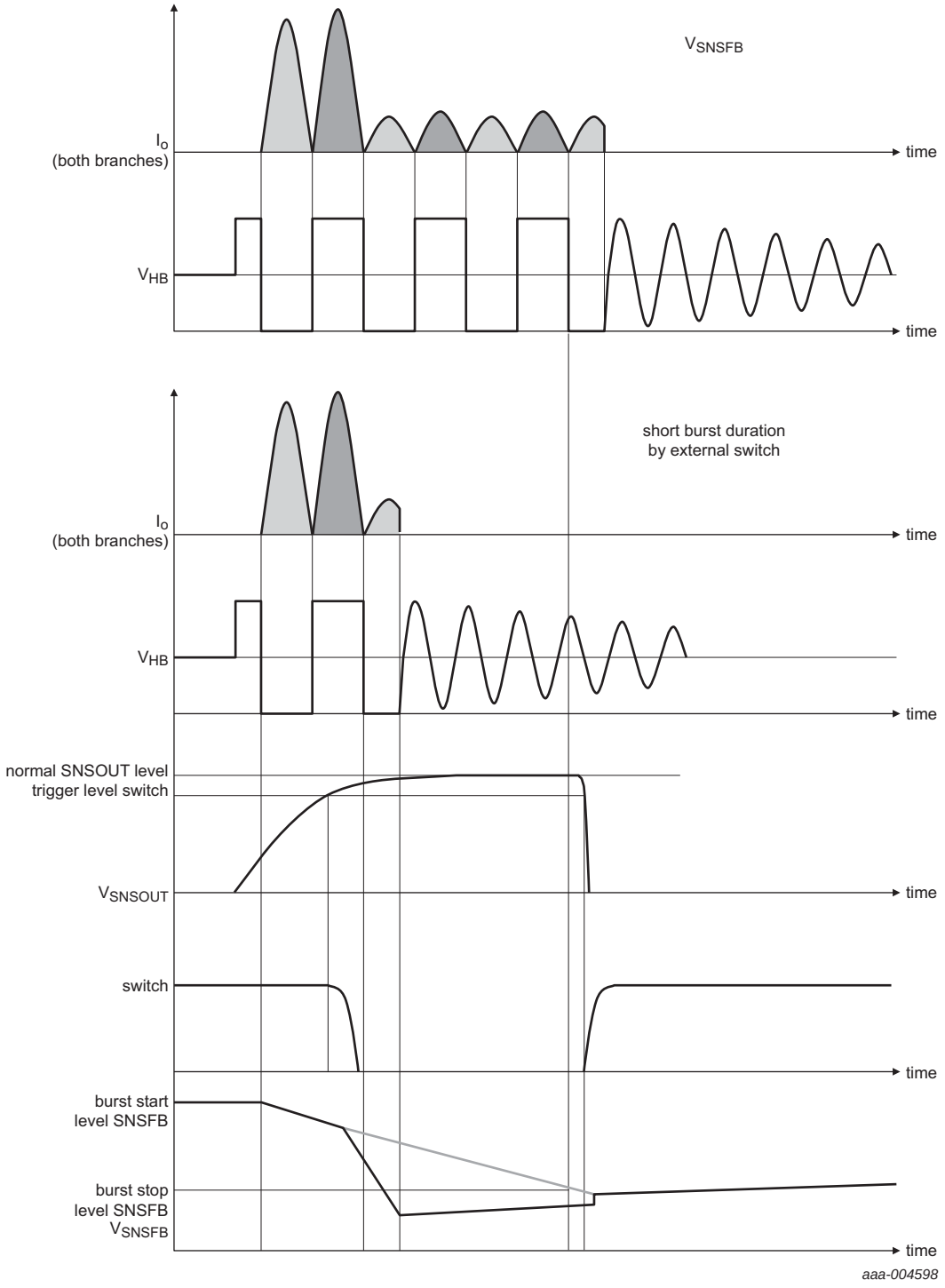


Fig 77. Shorter burst duration by external switch

11.10 Tolerances in the burst mode application

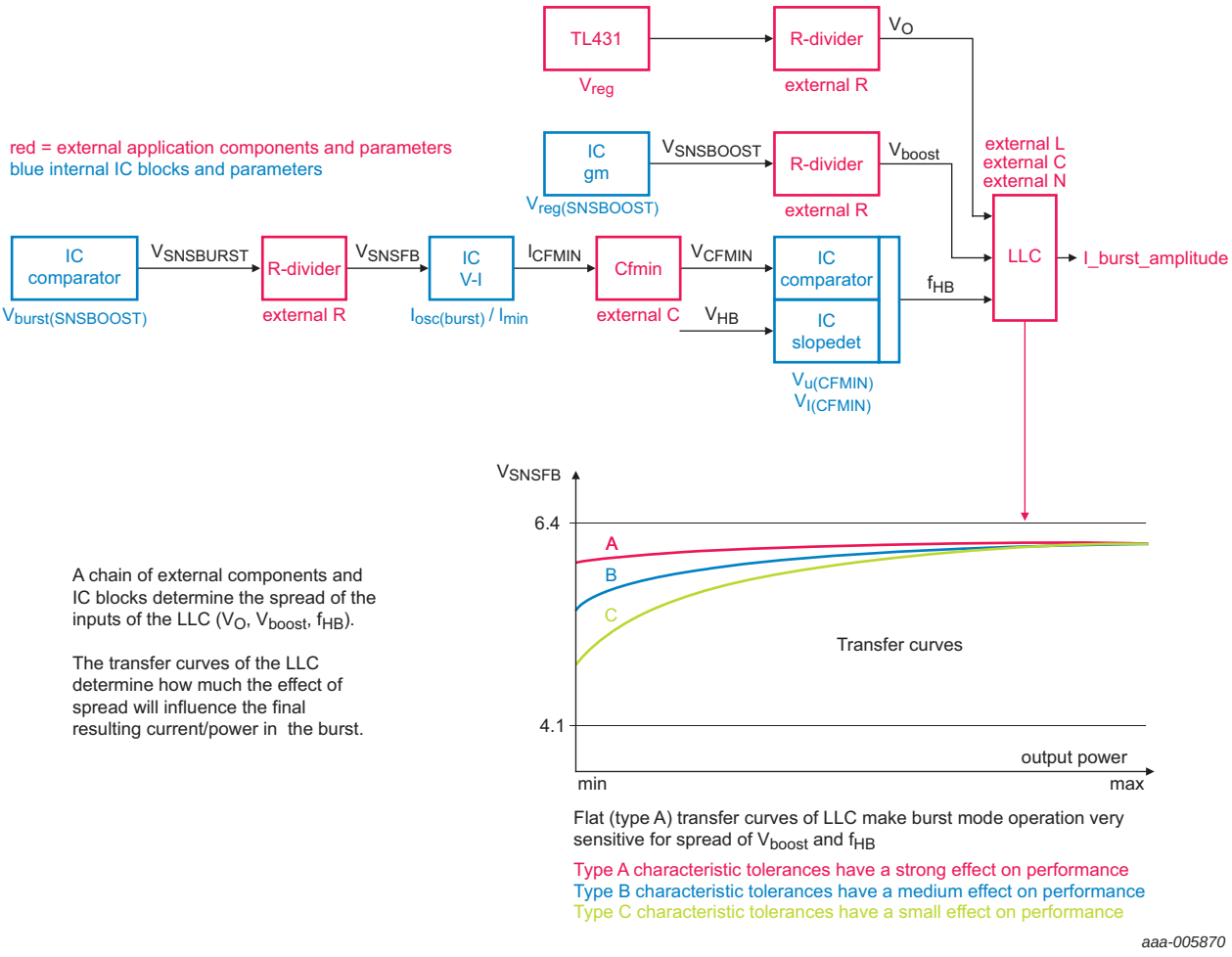


Fig 78. Overview of spread sources that influence the burst mode operation

11.10.1 Power transfer curves

The power transfer curves amplify the tolerance effects.

11.10.1.1 Flat curves (type A)

Flat curves are a result of a small frequency change (= change in feedback voltage) leading to a large change in power. This characteristic is typical for operation near the resonant frequency where the switching frequency is almost independently from the output power.

This type of transfer curve is very suitable for high-efficiency applications that use synchronous rectification circuits in the output stage.

The transfer curve is not very suitable for burst mode operation. A small parameter change because of tolerances has a major impact on the final result. The extra circuit discussed in Section 11.11 can help to avoid most of the burst mode problems when this type of transfer curve is required.

11.10.1.2 Gradual curves (type C)

Gradual curves are a result of a large frequency change (= change in feedback voltage) required to change the output power. Typically for this characteristic, the maximum output power operates near the resonant frequency (for best efficiency) and the frequency increases as the output power decreases. The output current runs in continuous current mode (the output current is not yet zero when it is switched off for the next cycle).

This type of transfer curve is suitable for burst mode operation because changes due to tolerance only have a minor impact on the performance.

11.10.1.3 Changing the characteristic of the transfer curve

A basic method to change a transfer curve from type A to type C is to modify the LLC transformer turns ratio or the input/output voltage ratio slightly.

11.10.1.4 Secondary rectifying by Synchronous Rectification (SR)

When SR is used, curve type A is often required to obtain proper working of the SR function. Implement an additional burst mode enable/disable circuit to define the transition level between the modes (see Section 11.11).

11.11 External enable/disable burst mode circuit

An external enable/disable function can be used for a better defined transition for entering and leaving burst mode operation.

In the normal TEA1716 application, the SNSFB voltage is used to determine when to enter and when to leave Burst mode operation. The accuracy is limited because the SNSFB voltage depends on several parameters.

Figure 79 shows the usage of an external circuit that controls when to enter and when to leave the Burst mode operation.

The use of such a circuit is attractive when secondary sensing circuits are already required because of other requirements. The use of an IC that includes most circuits provides an easy implementation with good accuracy.

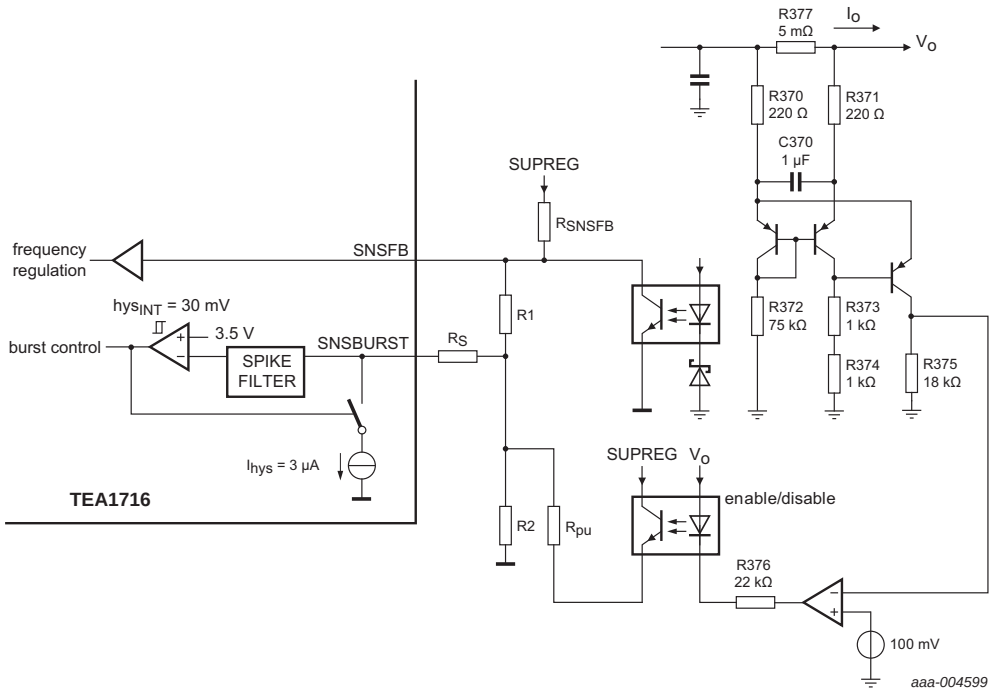


Fig 79. Example of burst mode enable/disable by output current sensing

11.11.1 Choosing a burst power level

When an external burst mode enable/disable circuit is used, the SNSBURST pin power level can be set with more freedom (the switching frequency during a burst).

In the standard basic application (Figure 66) the power/frequency level during burst mode is close to the level of entering/leaving burst mode operation. This level is a high frequency that represents a low-power level.

Now a lower frequency can be chosen (using the values of R1 and R2) to obtain more power in each burst which makes it more efficient. The duration of each burst can be shorter because the power in each cycle is higher.

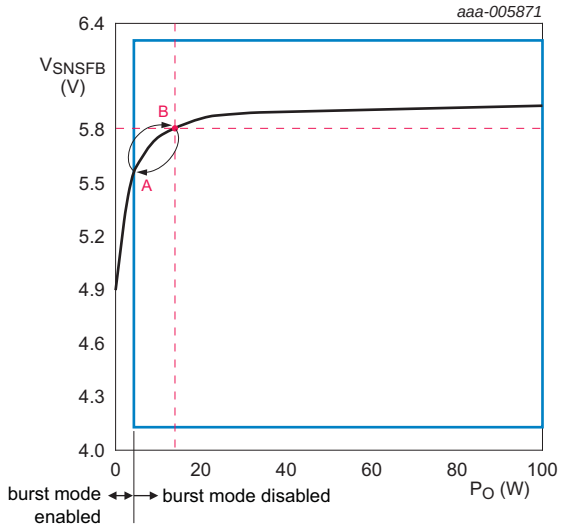


Fig 80. Using an external burst mode enable/disable function that is set at a lower power level than the preset SNSBURST level

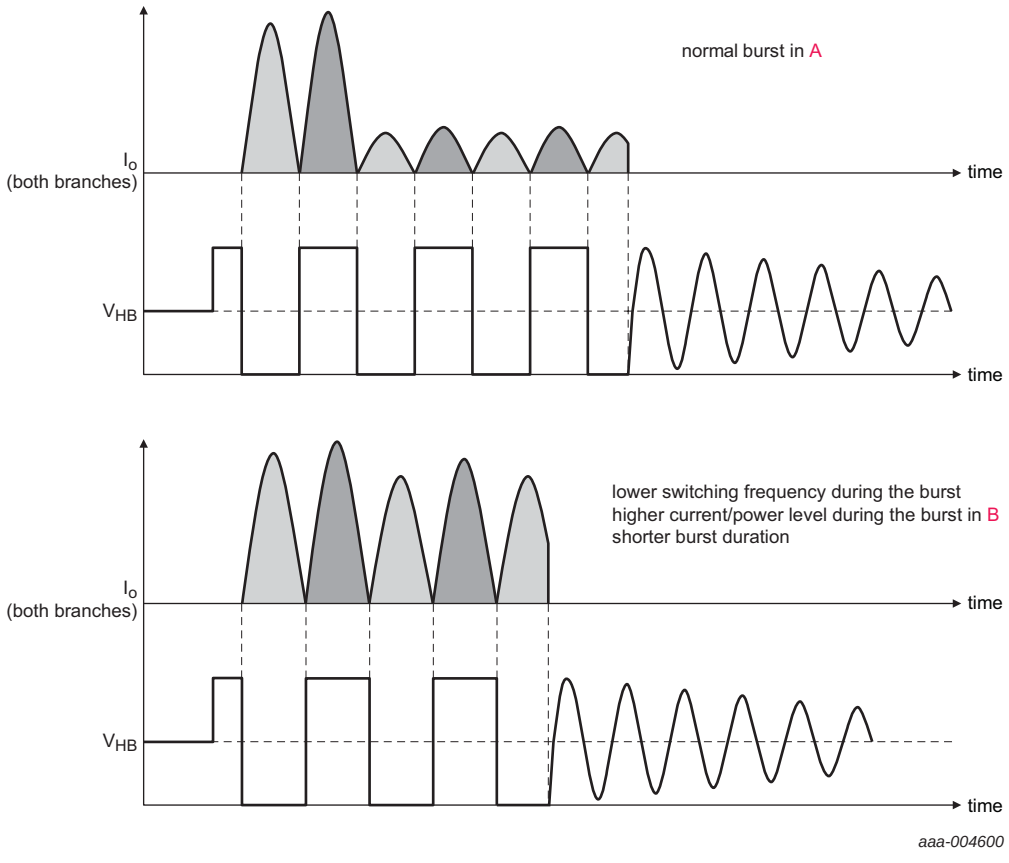


Fig 81. Higher power level during the burst when using an external burst mode enable/disable function

12. Protection functions

12.1 Protective functions overview

Table 6. Overview protective functions

Protected Part	Symbol	Protection	Affected	Action	Description
IC	UVP-SUPIC	undervoltage protection SUPIC	IC	disable	Section 6.1.5
IC	UVP-SUPREG	undervoltage protection SUPREG	IC	disable	Section 6.4
IC	UVP-supplies	undervoltage protection supplies	IC	disable and reset	-
IC	SCP-SUPIC	short circuit protection SUPIC	IC	low HV start-up current	Section 6.1.5
IC	OVP-output	overvoltage protection output	IC	shutdown	Section 12.3.1
IC	FSP-output	failed start protection output	IC	restart after protection time	Section 12.3.2
IC	OTP	overtemperature protection	IC	disable	Section 12.2.1
PFC	OCR-PFC	overcurrent regulation PFC	PFC	switch-off cycle-by-cycle	Section 8.4
PFC	UVP-mains	undervoltage protection mains	PFC	hold switching	Section 8.6.1
PFC	OVP-boost	overvoltage protection boost	PFC	hold switching	Section 8.5
PFC	SCP-boost	short circuit protection boost	IC	restart	Section 8.2.2
HBC	UVP-boost	undervoltage protection boost	HBC	disable	Section 9.1
HBC	OLP-HBC	open-loop protection HBC	IC	restart after protection time	Section 9.5.3
HBC	HFP-HBC	high-frequency protection HBC	IC	restart after protection time	Section 9.4.4
HBC	OCR-HBC	overcurrent regulation HBC	HBC IC	HBC: increase frequency IC: restart after protection time	Section 9.7.1
HBC	OCP-HBC	overcurrent protection HBC	HBC	step to maximum frequency	Section 9.7.2
HBC	CMR	capacitive mode regulation	HBC	increase frequency	Section 9.3.2
HBC	ANO	adaptive non-overlap	HBC	prevent hazardous switching	Section 9.3

12.2 IC protection functions

12.2.1 OverTemperature Protection (OTP)

The TEA1716 contains an accurate internal OverTemperature Protection (OTP). When the junction temperature exceeds the overtemperature level of 140 °C, the IC enters the Thermal hold state. The Thermal hold state is left when the temperature has dropped by 10 °C.

The circuit resumes operation with a complete restart including a soft-start of PFC and HBC.

12.3 SNSOUT protection

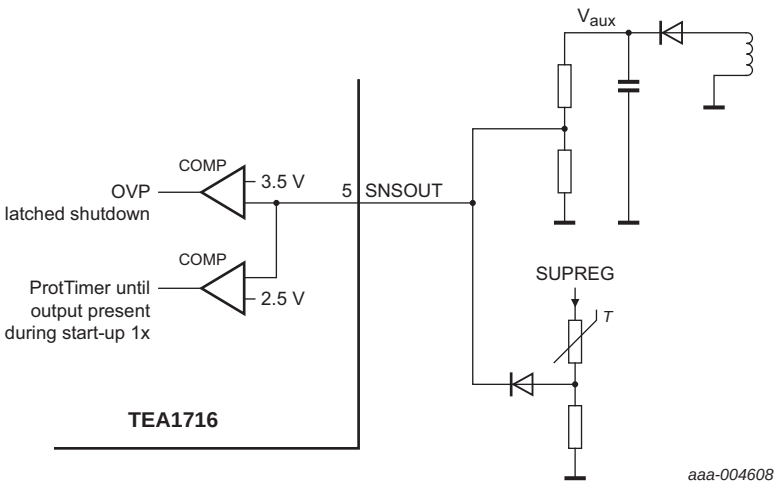


Fig 82. SNSOUT functions

12.3.1 OverVoltage Protection (OVP) output

The TEA1716 has an overvoltage protection intended for monitoring the HBC output voltage. It is one of the functions that is combined on the SNSOUT pin.

12.3.1.1 Auxiliary winding

When dealing with a mains insulated converter, the HBC output voltage can be measured using the auxiliary winding of the resonant transformer. A special transformer construction is required to measure the secondary voltage of the primary circuit auxiliary winding accurately.

This winding must have a good coupling with the secondary winding and a minimum coupling with the primary winding to facilitate working correctly. In this way, a good representation of the output voltage situation is obtained (see Figure 5 and Section 6.2.3.1).

Triple insulated wire can be used to meet the mains insulation requirements.

12.3.1.2 Principle of operation

The voltage is sensed at the SNSOUT pin using an external rectifier and a resistive divider. Overvoltage is detected when the voltage on the SNSOUT pin exceeds 3.5 V. After detecting OVP, the TEA1716 enters the Latched protection shutdown state.

12.3.1.3 Connecting external measurement circuits

When latched protection is required for other detection circuits, it can be added to the SNSOUT pin using a series diode.

12.3.1.4 Latched protection

Only an overvoltage detection on the SNSOUT pin leads to a latched shutdown protection state. The voltage on the SNSOUT pin must exceed 3.5 V for the device to enter a Latched shutdown state.

Resetting a Latched protection shutdown state

When a Latched protection shutdown state has occurred, this state is reset by one of the following actions:

- The voltage on the SUPIC pin drops under 7 V and the voltage on the SUPHV pin is lower than 7 V
- The voltage on the SNSMAINS pin drops under 0.8 V and then rises to exceed 0.85 V
- The voltage on the SSHBC/EN pin is pulled under 1.2 V (PFC enable level)

In most cases, a reset by SNSMAINS is activated before a reset by SUPIC/SUPHV. This condition restarts before the internal latch is reset using the SUPIC and SUPHV pin voltages.

When resetting by interrupting the mains input, some time is still required to lower the voltage on the SNSMAINS pin to under 0.8 V. The time depends on the component values used on the SNSMAINS circuit and the value of the mains voltage. Another aspect is bridge rectifier leakage allowing the SNSMAINS pin voltage to increase due to the rectified mains voltage capacitor (reverse current through the diodes). At moderate rectifier temperatures, reverse current can be ignored. At high temperatures, it is a significant parameter.

A reset possibility by external control (for example microcontroller) is available using the SSHBC/EN function.

12.3.2 Failed Start Protection (FSP) output

The TEA1716 has an undervoltage protection intended for monitoring the HBC output voltage during start-up. It is one of the functions that is combined on the SNSOUT pin.

12.3.2.1 Principle of operation

The voltage is sensed at the SNSOUT pin using an external rectifier and a resistive divider. At start-up the protection timer RCPROT is activated until the voltage on the SNSOUT pin exceeds 2.5 V.

If the undervoltage state is still active when the timer reaches the protection level, the controller stops. The restart timer later restarts the controller.

At start-up, the SNSOUT voltage rise can be influenced to define the burst mode disable period. A longer burst mode disable period can prevent unstable regulation at start-up. This period must not last too long to avoid triggering of the FSP when the RCPROT timer ends.

12.3.3 OVP and FSP combinations

12.3.3.1 Circuit configurations

The following list contains examples of configurations for which certain functions on the SNSOUT pin are disabled:

- OVP functional and FSP disabled (see Section 12.3.3.2)
- FSP functional and OVP disabled (see Section 12.3.3.3)
- Both OVP and FSP disabled (see Section 12.3.3.4)

Remark: Burst mode operation can be implemented in the examples because it does not depend on the FSP functionality.

12.3.3.2 OVP functional and FSP disabled

In some applications, activation of the FSP on the SNSOUT pin must be prevented. Disabling FSP can be realized by adding a circuit that forces the voltage on the SNSOUT pin to exceed 2.5 V.

Practical example

The SNSOUT pin voltage can be forced to exceed 2.5 V when an external fixed voltage low-impedance resistive divider is added and connected using a diode to the SNSOUT pin. This simple circuit is not very accurate but it does provide the basic capability to disable the SNSOUT pin FSP function.

Remark: OVP still functions because the diode is blocking for higher voltage values on the SNSOUT pin.

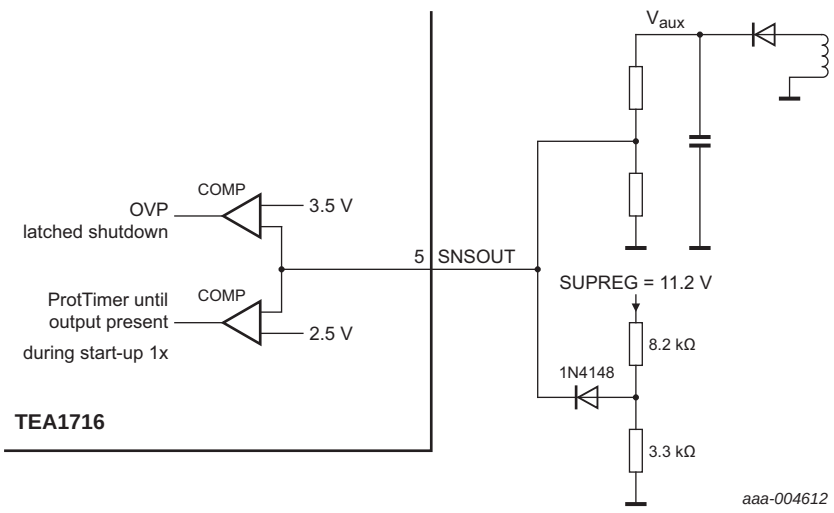


Fig 83. Example of disabling the FSP function of SNSOUT

12.3.3.3 FSP functional and OVP disabled

In some applications, activation of the SNSOUT pin overvoltage protection must be prevented. Disabling OVP can be realized by adding a circuit that prevents that the voltage on the SNSOUT pin exceeds 3.5 V.

Practical example

The SNSOUT pin voltage can be forced to exceed 2.5 V when an external fixed voltage low-impedance resistive divider is added and connected using a diode to the SNSOUT pin. This simple circuit is not very accurate but it does provide the basic capability to disable the OVP function of the SNSOUT pin.

Remark: FSP still functions because the diode is blocking for lower voltage values on the SNSOUT pin.

Another possibility is to add a Zener diode to the SNSOUT pin to limit the voltage on the pin.

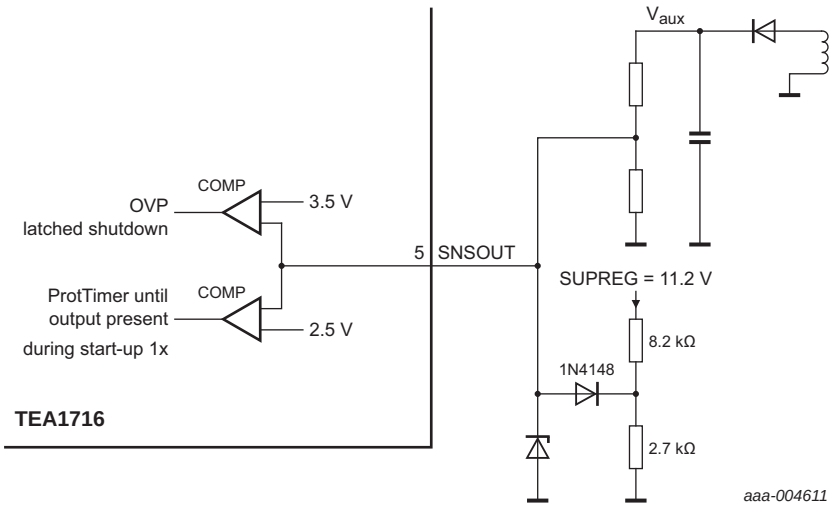


Fig 84. Example of disabling the OVP function of the SNSOUT pin

12.3.3.4 Both OVP and UVP disabled

When the OVP or FSP functions are not required, a fixed voltage between 2.5 V and 3.5 V can be applied to the SNSOUT pin. To create the fixed voltage, use a resistive divider referenced to the SUPREG pin.

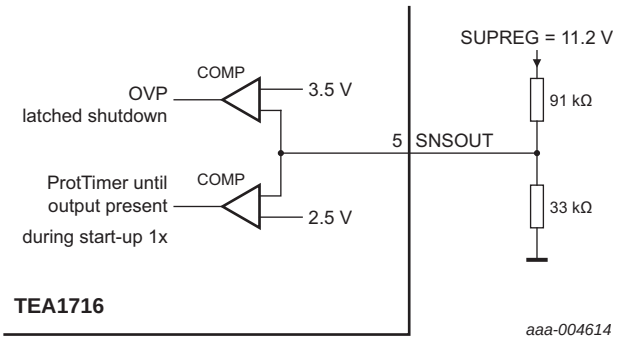


Fig 85. Example of disabling both the UVP and the OVP functions of the SNSOUT pin

12.4 Protection timer

The TEA1716 has a programmable timer that is used for the timing of several forms of protection. The timer is used in two ways:

- As a protection timer
- As a restart timer

The values for both types can be preset independently using an external resistor and capacitor connected to the RCPROT pin.

12.4.1 Block diagram of the RCPROT function

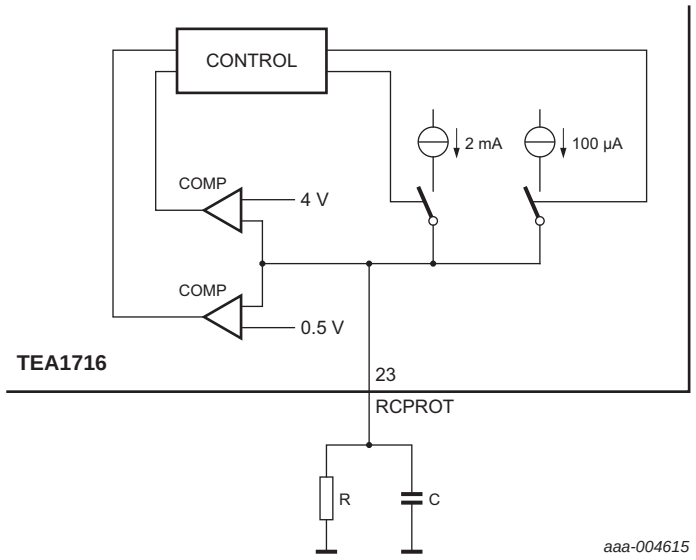


Fig 86. Block diagram of the RCPROT function

12.4.2 RCPROT working as protection timer

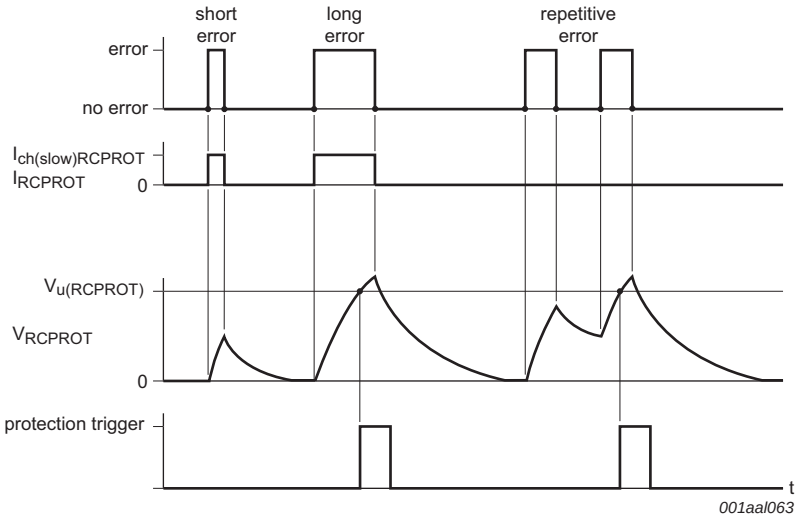


Fig 87. RCPROT protection timer operation

Figure 87 shows the operation of the protection timer. When an error condition occurs, a fixed current of 100 µA flows from the RCPROT pin and charges the external capacitor. The voltage rises exponentially due to the external resistor. The protection time is passed when the upper switching level of 4 V has been reached. The appropriate protective action is executed. The current source is stopped and the external resistor discharges the RCPROT pin capacitor.

When the error condition ends before 4 V is reached, the current source is stopped and the capacitor discharges through the external resistor. No further action is taken.

If the error condition is permanent, the system fluctuates between stop and restart.

The protection timer is activated as follows:

- Overcurrent regulation on the SNSCURHBC pin
- High-frequency protection
- Open-loop protection on the SNSFB pin
- Failed start protection on the SNSOUT pin; only at start-up

It is allowed to force the activation of protection (and restart) by increasing the RCPROT pin voltage above 4 V (but no higher than 12 V) using an external circuit.

12.4.3 RCPROT utilized as a restart timer

During certain error conditions, it can be necessary to disable the IC temporarily. Disabling the IC temporarily is especially useful in cases where an error can overheat components. A temporary disabling of the IC allows power supply components to cool down, after which the IC must automatically restart. The restart timer determines the time to restart.

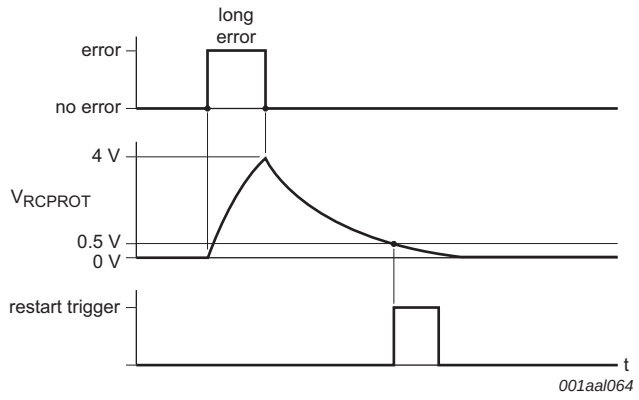


Fig 88. RCPROT operating as a restart timer

Normally, the capacitor is discharged to 0 V. When a restart is requested, a current of 2.2 mA quickly charges the external capacitor until it reaches the 4 V upper switching level. After the external capacitor is charged, the RCPROT pin becomes high-ohmic and the external resistor discharges the external capacitor. The restart time is exceeded when the lower switching level of 0.5 V is reached. The IC is restarted and the C_{RCPROT} is further discharged. This condition is only activated if a short circuit protection of the SNSBOOST pin occurs.

12.4.4 Dimensioning the timer function

The required restart time determines the time constant t_{RCPROT} defined as the R and C values.

$$t_{RCPROT} = \frac{-t_{restart}}{In_{(V_{l(RCPROT)}/V_{u(RCPROT)})}} = \frac{-t_{restart}}{In_{(0.5/4)}} = 0.48 \times t_{restart} \quad (52)$$

Using this time constant and the required protection time t_{prot}, the value of R and C can be calculated using Equation 53:

$$R = \frac{V_{u(RCPROT)}}{I_{slow(RCPROT)} \times \left(1 - e^{-\frac{t_{prot}}{t_{RCPROT}}}\right)} = \frac{4}{100\ \mu A \times \left(e^{-\frac{t_{prot}}{t_{RCPROT}}}\right)} \quad (53)$$

$$C = \frac{t_{RCPROT}}{R}$$

Example:

- $t_{restart}$ = 500 ms
- t_{prot} = 30 ms
- t_{RCPROT} = 240 ms
- R = 341 kΩ
- C = 705 nF

13. Miscellaneous advice and tips

13.1 PCB layout

13.1.1 General setup

The TEA1716 contains two largely independently converter controllers in one package. Separate the PFC and HBC circuits physically on the PCB to avoid mutual interference.

13.1.2 Grounding

Connect SGND and PGND directly under the IC (on the ground plane if possible) to avoid false signal detection by driver current disturbance (see Figure 91).

A star grounding construction provides the lowest risk of mutual converter disturbance or signal detection disturbance. In this system, the central star point can be chosen at the V_{boost} capacitor ground.

Avoid high currents in grounding tracks that are meant for signal measurement.

13.1.3 Current loops

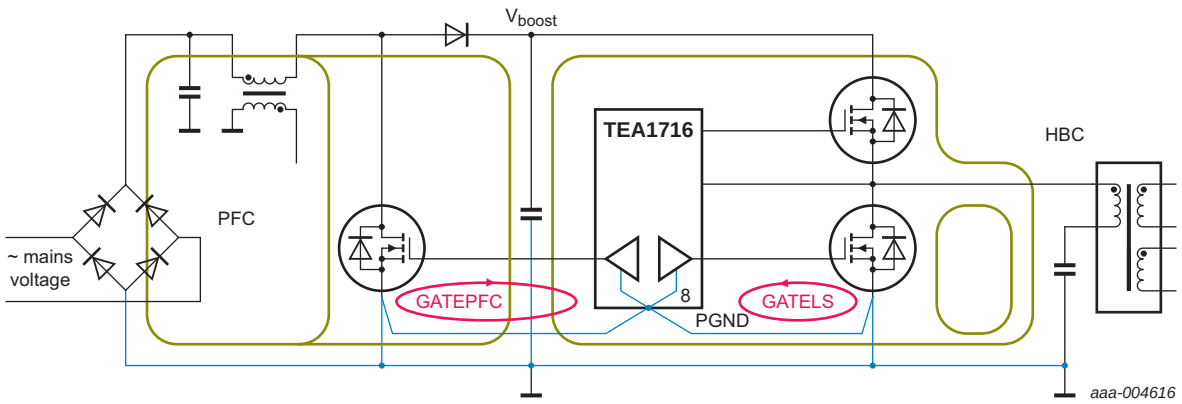


Fig 89. Grounding structure and current loops GATEPFC and GATELS

13.1.4 Grounding layout example

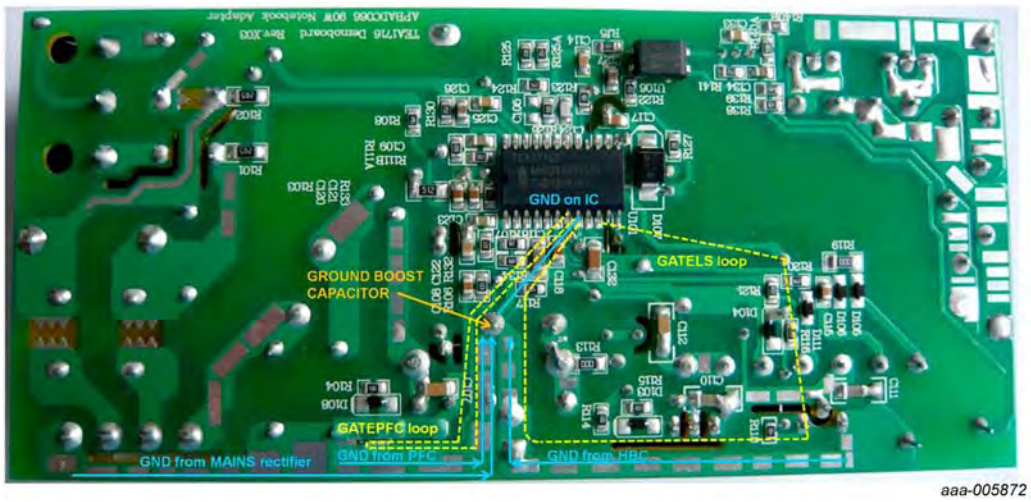


Fig 90. Grounding layout example with star point at the boost capacitor

13.1.5 Miscellaneous

13.1.5.1 Connecting SNSCURHBC (pin 17)

Place a series resistor in the SNSCURHBC connection as close as possible to pin 17. This action is important for avoiding disturbance pickup. Also, avoid capacitive coupling between the connection to pin 17 and the HB track (to pin 15) that contains high dV/dt signals.

13.1.5.2 CFMIN (pin 19)

Connect the oscillator capacitor on pin CFMIN (pin 19) to SGND (pin 18) using short tracks to prevent pickup of disturbances by an external field.

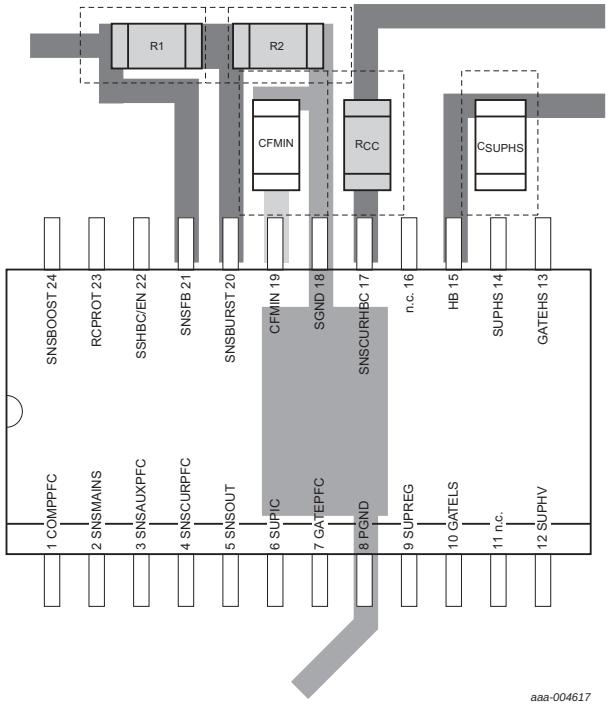


Fig 91. PCB layout: connecting the SGND, PGND, CFMIN, SNSCURHBC and SNSBURST pins

13.2 Starting/debugging partial circuits

When starting a newly built application or when an error is observed during operation, it is possible to activate step-by-step circuit parts. This debugging enables errors to be located easily and an evaluation to be performed under conditions that restrict the influences from other circuit parts.

The following provides a step-by-step sequence for debugging:

- only HBC with protection disabled
- only HBC with protection disabled and variable DC input voltage
- only HBC with protection enabled
- only PFC
- complete application with PFC and HBC

The best approach is to check the HBC converter first and then the PFC converter.

13.2.1 HBC only

A proposal for the set-up (temporary additions to the existing application to force operation) and the sequence for disabling/enabling the different functions is shown in Figure 92. A moderate current load can be applied to the converters output to check correct functioning.

The CFMIN, GATELS, GATEHS and HB pins can be monitored to assess the operation of the converter/controller.

Practical tip: When the PFC function is disabled, the boost voltage can be provided if an AC or DC voltage is applied to the mains input connections.

Check the regulation by increasing the input voltage V_{boost} for the following situations in the sequence given:

1. Initially, at V_{boost} = 0 V:

   The running frequency is low with a short on-time and a long off-time. This condition is due to the HB detection not working properly at low voltages and the internal slope detection (HB) not detecting a proper (fast) slope. A quick check of the PFC operation is made when the external supply voltage is lowered from 2.7 V to under 2.5 V on the SNSMAINS and SNSBOOST pins. Lowering the voltage allows the gate-drive pulses on the GATEPFC pin to be seen. Varying the voltage shows changes in the on-time. After this check, revert the voltage to 2.7 V to continue the HBC-only start-up (see Section 13.2.2.1).
2. Increase the value of V_{boost}.

   At a certain input voltage, HB detection works correctly and the frequency to drive maximum power is minimal. If the HB slope remains slow, the output current is probably low. Increasing the output current probably results in correct HB switching.
3. When the V_{boost} input voltage has reached a level closer to the nominal operating voltage, the correct output voltage is reached and regulation starts working. This results in a frequency increase using the input voltage increase until the nominal working voltage of V_{boost} is set.
4. When the basic functioning of the HBC is working well, including SNSFB regulation, protective functions can be added one-by-one. Proper functioning or a requirement for change can be evaluated.
5. When a self-supplying application is used, the external supply voltage can be removed when the system works well at the nominal V_{boost} voltage. The system can now start using the internal high-voltage start-up supply and an auxiliary winding can take over the SUPIC supply.

Remark: If, during debugging or starting, a protection has been activated, switching the SUPIC supply off and on to reset a latched protection state can be required.

Remark: Burst mode operation presetting is sometimes not correct yet. Burst mode operation during debugging makes analyses more complex. To avoid burst mode operation during debugging, the voltage on pin 20 (SNSBURST) can be temporarily forced to a higher level. Short circuit pin 20 (SNSBURST) to pin 21 (SNSFB) is often sufficient.

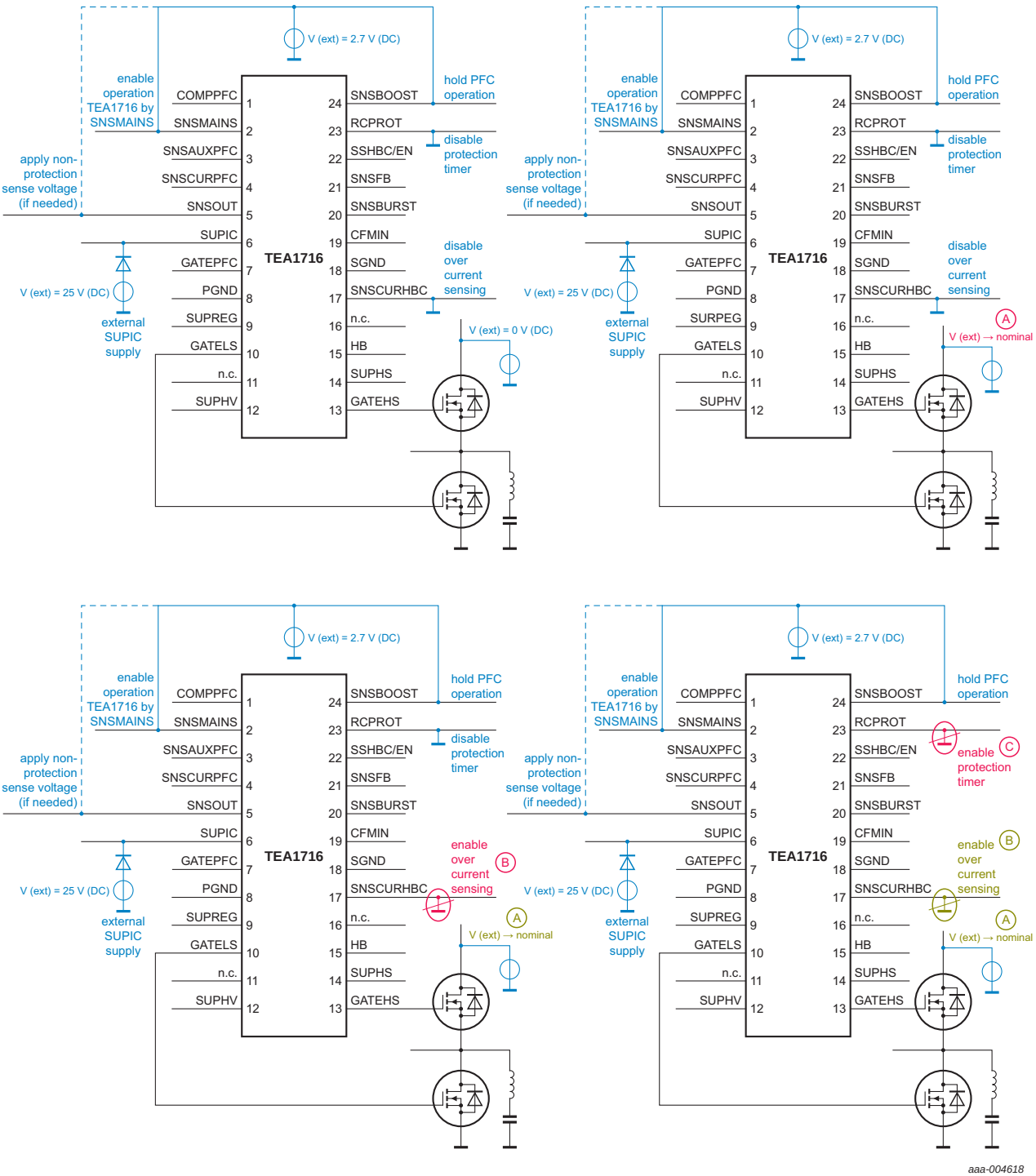


Fig 92. HBC only - start-up and debugging step-by-step

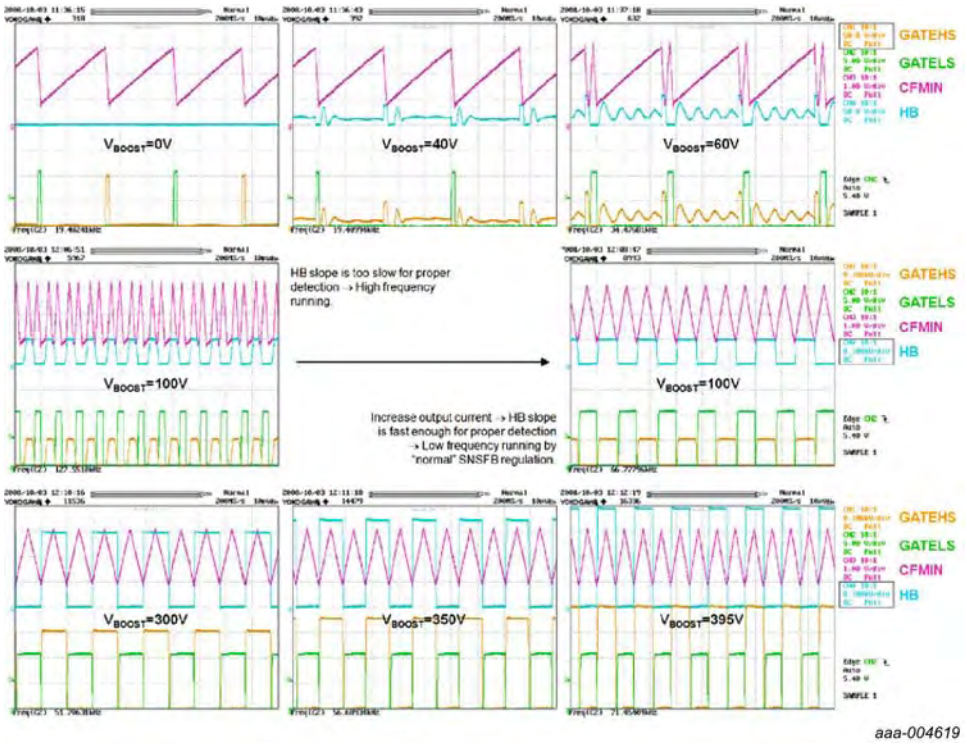


Fig 93. Typical signals during a separate HBC start-up for an increase in V_{boost}

The following list provides an association between pins and the protection states for which they are being monitored:

- SSHBC/EN:

  When the TEA1716 lowers the voltage to this pin, it indicates a protection with correction to high frequency.

- CFMIN:

  Incorrect detection of the HB slope or a possible capacitive mode detection is observed showing a (partially) slow oscillator signal.

- PGND and SGND:

  If the TEA1716 detects HB operation while there is zero input voltage, it indicates that the connection between these pins at the IC is not present. Gate currents lead to false HB-slope detection.

- SNSCURHBC:

  Any disturbances on this pin (voltage spikes) can lead to an increase of frequency while the original measurement voltage/signal is OK.

- SNSOUT:

  The voltage on this pin must be between 2.5 V (at least exceeding this value one time) and 3.5 V for normal operation. A voltage can be forced to this value to avoid protection. However, it is often related (by a resistive divider) to pin SUPIC and is correct when pin SUPIC is supplied externally.

- RCPROT:

  Several protection functions charge the timer capacitor.

13.2.2 PFC only

The HBC function is disabled when SSHBC/EN is kept/forced under 2.2 V. A voltage higher than 1.2 V can enable the PFC function. Applying an additional voltage (from an external supply) of approximately 1.5 V on the SSHBC/EN pin enables PFC-only operation.

The set-up is similar to that used for HBC-only operation but for extra safety, the V_{boost} connection to the high-side switch of the HBC can be disconnected. In addition, a small load can be connected on V_{boost} to prevent voltage overshoot and control the output power capability.

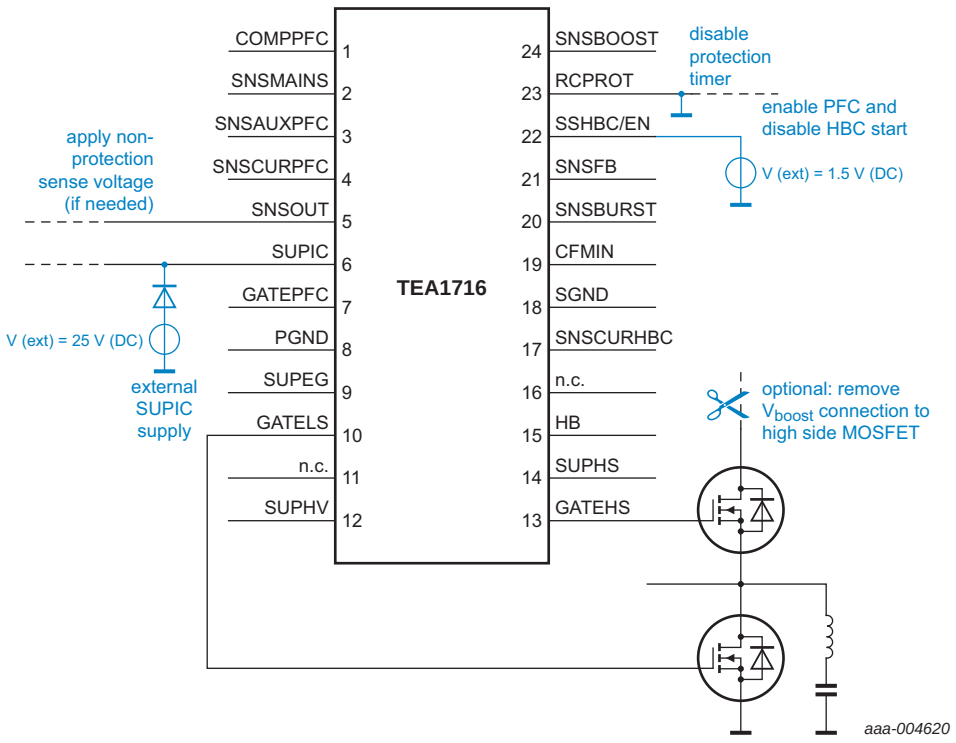


Fig 94. Start-up/debugging for PFC only

13.2.2.1 Operational check without mains voltage

Without mains input voltage, drive pulses can be observed on the GATEPFC pin. Reduce the (external) voltage on the SNSMAINS and SNSBOOST pins to under 2.5 V, Lower voltages lead to a longer on-time. See Section 13.2.1. Under 0.89 V, pulses stop because of SNSMAINS UVP and restart when the level increases above 1.15 V.

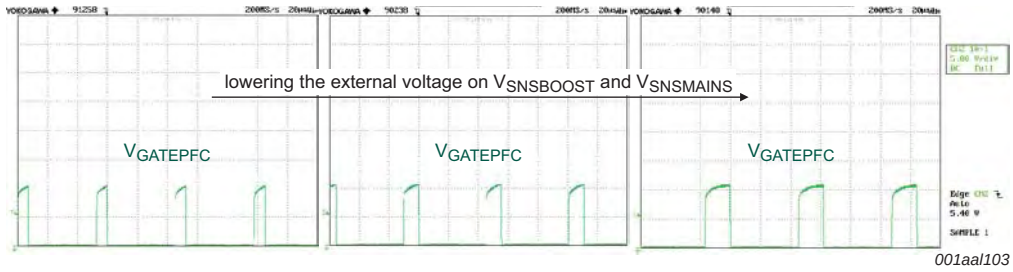


Fig 95. Typical GATEPFC signals without mains voltage

13.2.2.2 Operational check with mains voltage

There is no simple step-by-step method for gradually increasing the mains voltage to start PFC operation. Full mains voltage is applied to check the PFC functionality. Remove any external voltage source on the SNSMAINS and SNSBOOST pin.

If a problem with too high an output voltage is expected, temporarily increase in value the output measurement resistor from SNSBOOST to ground. This leads to a lower output voltage regulation setting.

Apply a DC voltage to the mains input instead of the usual AC voltage to be able to observe PFC operation more easily using an oscilloscope. This results in more stable signals for evaluation.

13.2.2.3 HBC and PFC operation

When both converters work properly independently, they can be checked working simultaneously. Remove the additions used for start-up and debugging.

Remark: A (normal) ripple voltage on V_{boost} results in some continuous frequency variations in the HBC for compensation. At high output power, the voltage ripple on V_{boost} is larger.

14. Examples of applications

14.1 Example of an IC evaluation test setup

An example of a test/evaluation setup is provided in Figure 96. This setup can be used for:

- Checking if an IC is still functional (not defect)
- Evaluation of specific IC functions or pin properties with limited interference from the total system

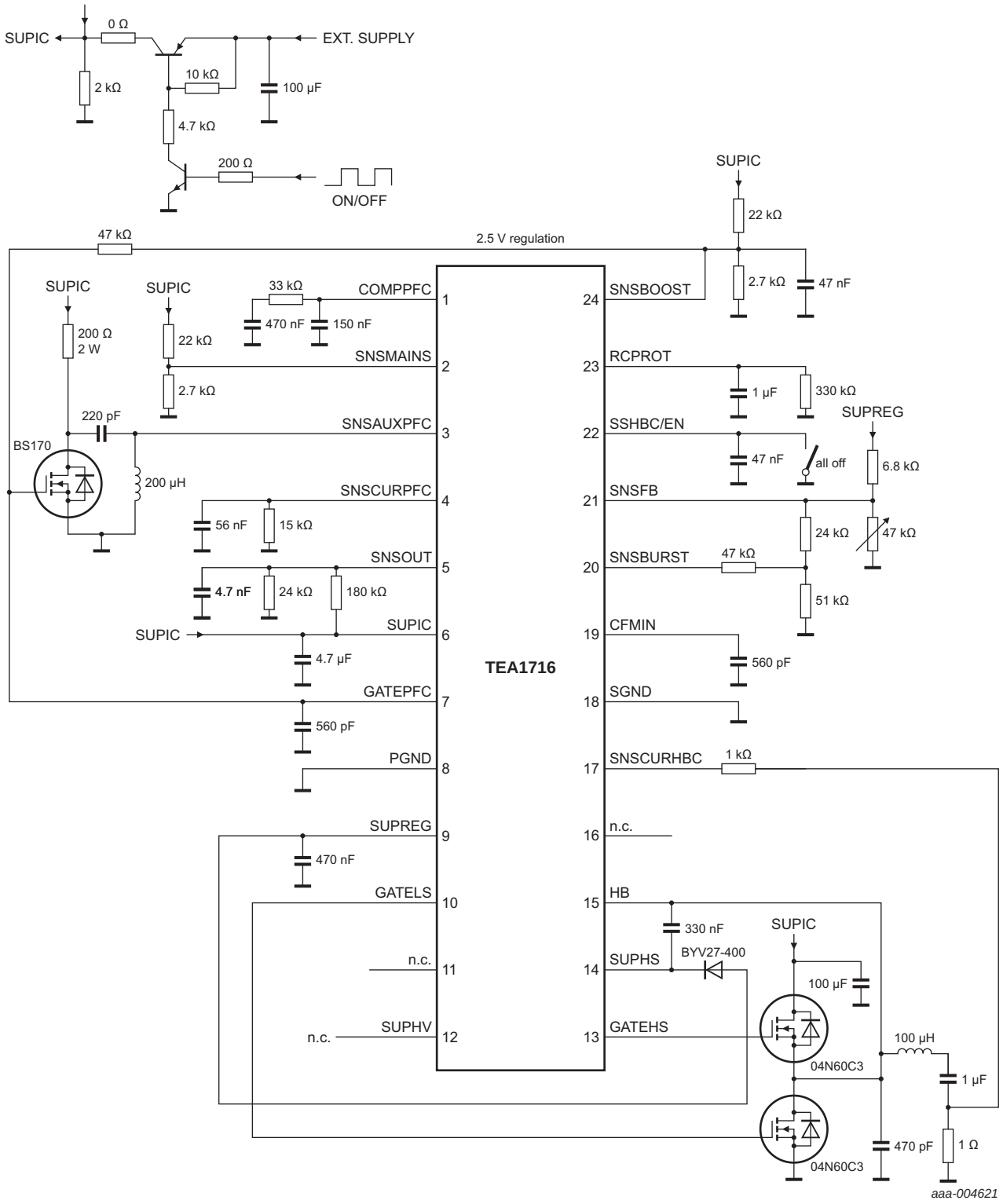


Fig 96. Example of a basic IC test setup on a single low voltage supply (28 V)

14.2 Example of a 90 W notebook adapter application

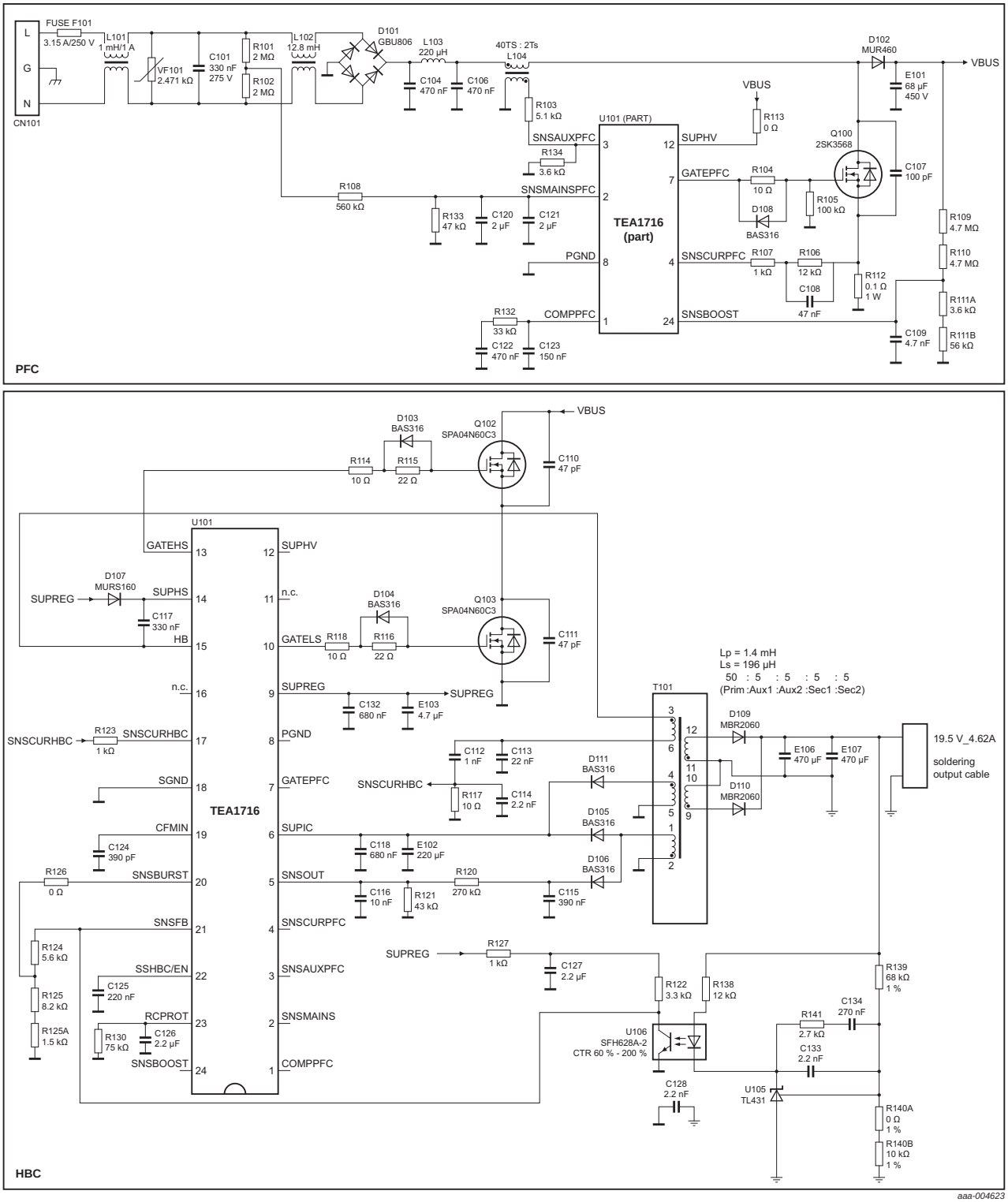


Fig 97. Application 90 W notebook adapter

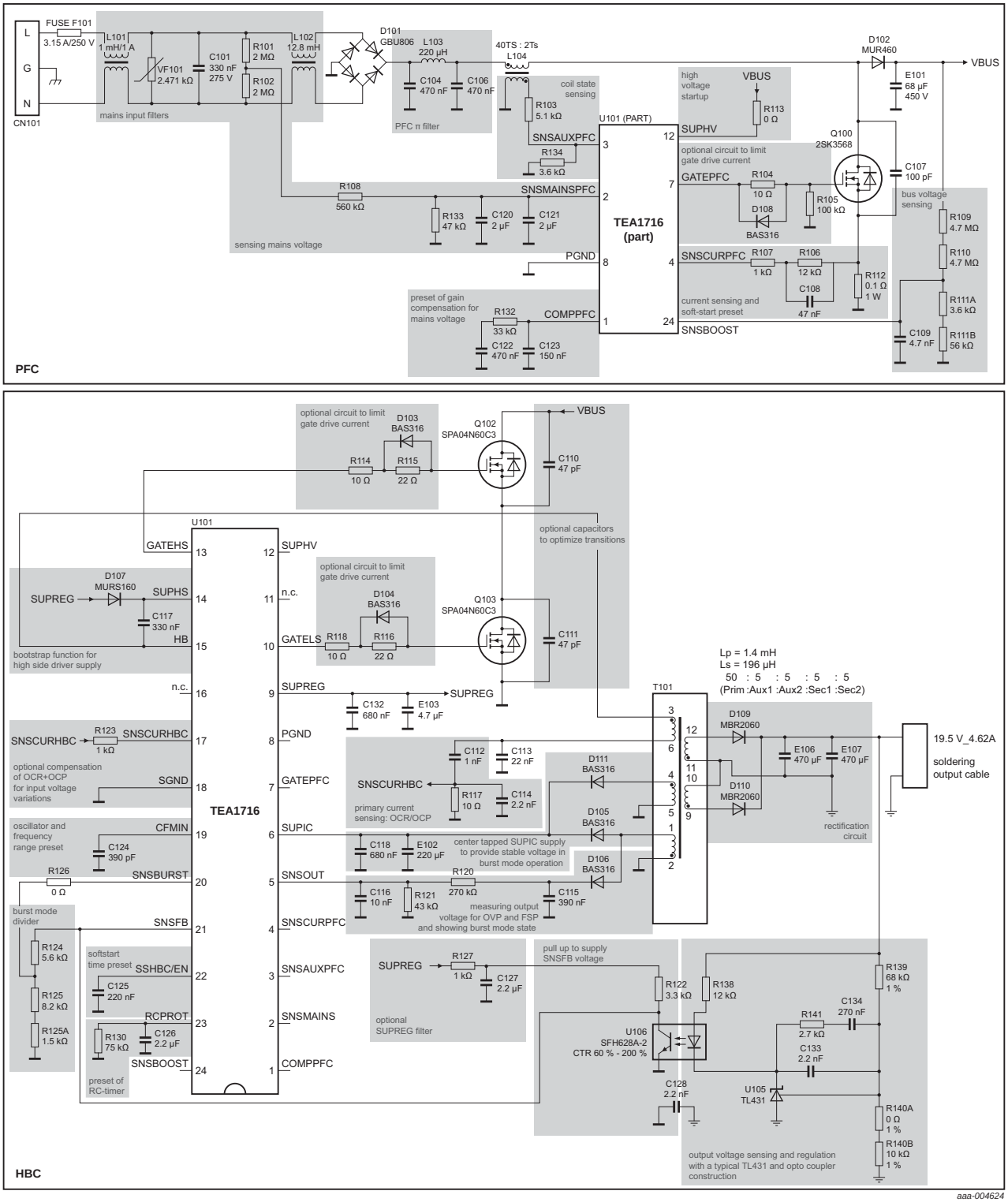


Fig 98. Application 90 W notebook adapter with functional blocks

15. Abbreviations

Table 7. Abbreviations

Acronym	Description
ADT	Adaptive Dead Time
BCD	Bipolar CMOS DMOS
CMR	Common-Mode Rejection
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
FSP	Failed Start Protection
HB	Half-Bridge
HBC	Half-Bridge Converter
HFP	High-Frequency Protection
HV	High-Voltage
IC	Integrated Circuit
LCD	Liquid Crystal Display
LLC	Resonant tank or converter (Lm +Lr +Cr in series)
OCP	OverCurrent Protection
OCR	OverCurrent Regulation
OLP	Open-Loop Protection
OPTO	OPTO-coupler
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PCB	Printed-Circuit Board
PFC	Power Factor Converter
PWM	Pulse Width Modulation
SCP	Short Circuit Protection
SOI	Silicon-On Insulator
UVP	UnderVoltage Protection

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