

## MC68302 Confidence Test Software

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### **1 INTRODUCTION**

This Application Note contains the design for a confidence test program (CT302) that tests the MC68302 Integrated Multi-Protocol Processor. A working knowledge of the MC68302 is assumed. This document uses the same nomenclature as the MC68302 User's Manual.

CT302 is a general-purpose confidence test software that executes directly on the MC68302 under test. Its purpose is to confirm the absence of hardware failures within a specific MC68302 unit and thereby increase the confidence in the unit's continued correct operation. CT302 is intended for power-on reset and warm reset situations where the results of the confidence test are used by system software to determine whether to continue operation or not. Like all such self-test software, CT302 cannot be expected to guarantee the detection of all hardware failures all the time (as the hardware failure can cause even perfect software to operate incorrectly).

The function of this Application Note is to describe the test algorithms and methodology. The control flow of the whole confidence test program is given along with details of the MC68302 resources needed to perform tests. The tests run in an incremental fashion so that, where possible, resources are tested before they are used. Pseudo-code and source code for all test are available on a computer diskette, detailed in Appendix 1.

### **2 FUNCTIONALITY**

CT302 uses a 'test before use' policy where ever possible, e.g. RAM shall be tested before it is used for other tests. It is accepted that this is impossible in many situations, e.g. the CPU.

CT302 is completely autonomous and does not require human intervention, any other software, external connections or hardware (except the implied use of program and data memories storage and processor vector memory space where necessary).

The following functions are tested as completely as possible within the limits of the above-mentioned restrictions:

- CPU instructions, addressing modes and registers
- On-chip dual-port RAM
- System control register
- Independent DMA controller

- Timers
- Interrupt controller
- Parallel I/O
- Serial Communications Controllers (SCCs)
  - each channel in UART, HDLC and transparent modes
- Serial DMA controller
- SCC physical interfaces
- Serial communications port (SCP)

In addition, as much external (non-MC68302) RAM as required to test any of the above functions is tested. A basic ROM test is included.

An error reporting mechanism using registers is included, making CT302 operating platform independent. On completion of the tests, errors are reported to the user using a mechanism appropriate to the hardware test platform. This mechanism can be changed when the test software is ported to other hardware platforms.

### **3 PERFORMANCE CRITERIA**

Many end users will have restrictions on program memory space and system initialisation time, or both. CT302 is designed to minimise program space and to execute as quickly as possible. Memory tests are modular and individually removable so that end users can elect to omit either large or long-executing tests.

### **4 TEST METHODOLOGY**

CT302 operates in an incremental manner, using only, where possible, resources that have already been tested and function. When a hardware error is detected, it is noted and the tests continue. If a resource required in a particular test has failed previous tests, the test is not run.

Using this approach, CT302 can detect simple errors and continue past them. Major errors or system errors cannot be bypassed and these cause CT302 to end without testing all features of the MC68302.

CT302 is designed to be a generic MC68302 confidence test program that is not invasive on the resident firmware. CT302 is designed to run whenever the MC68302 is reset and configures the chip according to some basic system dependant information. On completion of CT302, the MC68302 and system should be fully reconfigured by the user's firmware.

Because CT302 is non-intrusive, non-interactive with human operators nor use special purpose hardware and is generic, some features of the MC68302 cannot be tested. Tests that require special external circuitry are not used. Wherever possible, output signals are not driven when CT302 is running but with some tests this cannot be avoided. Details of these tests are given later in this document. Similarly, CT302 does not rely on specific input signals.

#### 4.1 CT302 Initialisation

CT302 source code can easily be ported to MC68302 systems. Sections not required can be removed and new modules testing external peripherals added. The user provides some basic information about his system, such as ROM and RAM locations, length and access time, at code compilation time.

### 3 ERROR & STATUS REPORTING

Two 32-bit M68000 data registers are used to report CT302 progress and test results. The Results Register, D0, contains one bit for each functional block of the MC68302 which is set when a test fails. Successful completion of all tests leaves the Results Register clear. The Progress Register, D1, also contains one bit for each functional block of the MC68302 that is set when the test has been completed, independent of the test result.

Bit allocations for the Results and Progress Registers are given in Figure 1. Bit allocations are the same for both registers.

Failure of any one test on a functional block results in the relevant bit in the Results Register being set. Tests do not continue on a failed functional block after one error is noted.

CT302 uses the Results Register to see what resources are available to it. When a failed resource is needed, CT302 skips the current test and does not set the relevant bit in the Progress Register. In this way it is possible to continue testing the MC68302 after some faults have been detected.

31	30	29	28	27	26	25	24
0	0	0	0	0	SDMA	External RAM	Transp 3

23	22	21	20	19	18	17	16
Transp 2	Transp 1	HDLC 3	HDLC 2	HDLC 1	UART 3	UART 2	UART 1

15	14	13	12	11	10	9	8
IDMA	Chip Selects	SCP	Sys Cntl 2	S/w watchdog timer	Interrupt controller	Timer 2	Timer 1

7	6	5	4	3	2	1	0
Port B	Port A	Internal RAM 2	Sys Cntl 1	CPU 2	Internal RAM 1	ROM	CPU 1

**Figure 1. Results and Progress Registers**

## **6 TEST DETAILS**

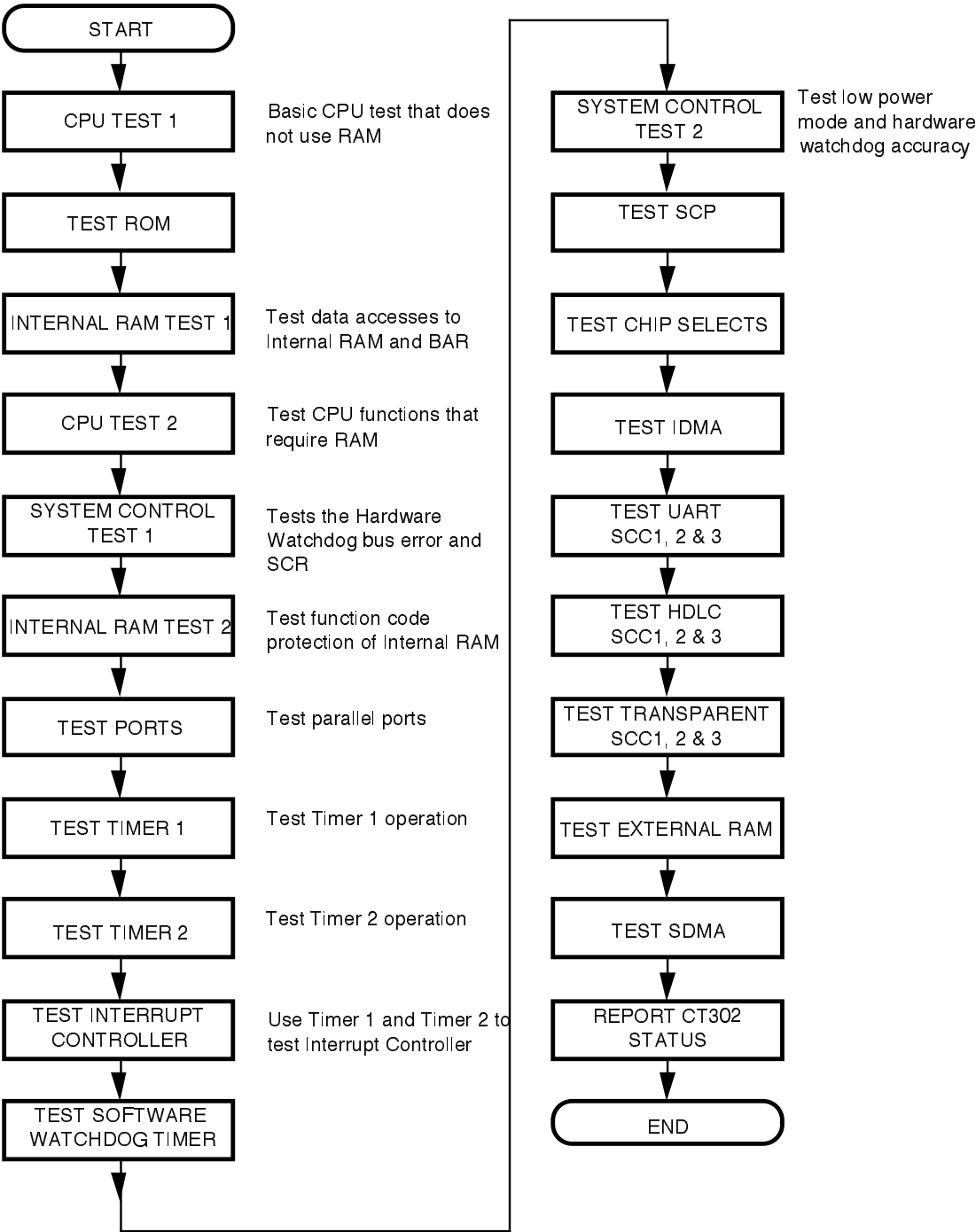
This section gives some details of the tests performed on each block of the MC68302, their requirements, scope and drawbacks and how they fit together. When testing an MC68302 on-chip peripheral, firstly all registers are written and read to check correct register access. Once register access is verified, the peripheral is enabled and its functions tested. Register failure in a peripheral is reported as a complete peripheral failure.

### **6.1 Control Flow**

Figure 2 illustrates the flow control of CT302 showing the order that tests are run and the resources they need. All test routines are called, regardless of whether all resources are required, and each routine checks to determine if all resources it needs are functional. If the complete set of resources required by a test are not available then control is passed to the next test block. This allows tests at the end of the control flow to be carried out even if certain earlier ones have failed.

### **6.2 Status Reporting**

Reporting the test results is the final CT302 function; the routine uses the results and progress registers to output the test results. The output mechanism uses TRAP calls which should be rewritten to customise CT302 to target boards and use resources that may or may not have been. The routine given in the Application Note is ported to the MC68302 ADS board and uses TRAP calls to print data on a terminal.

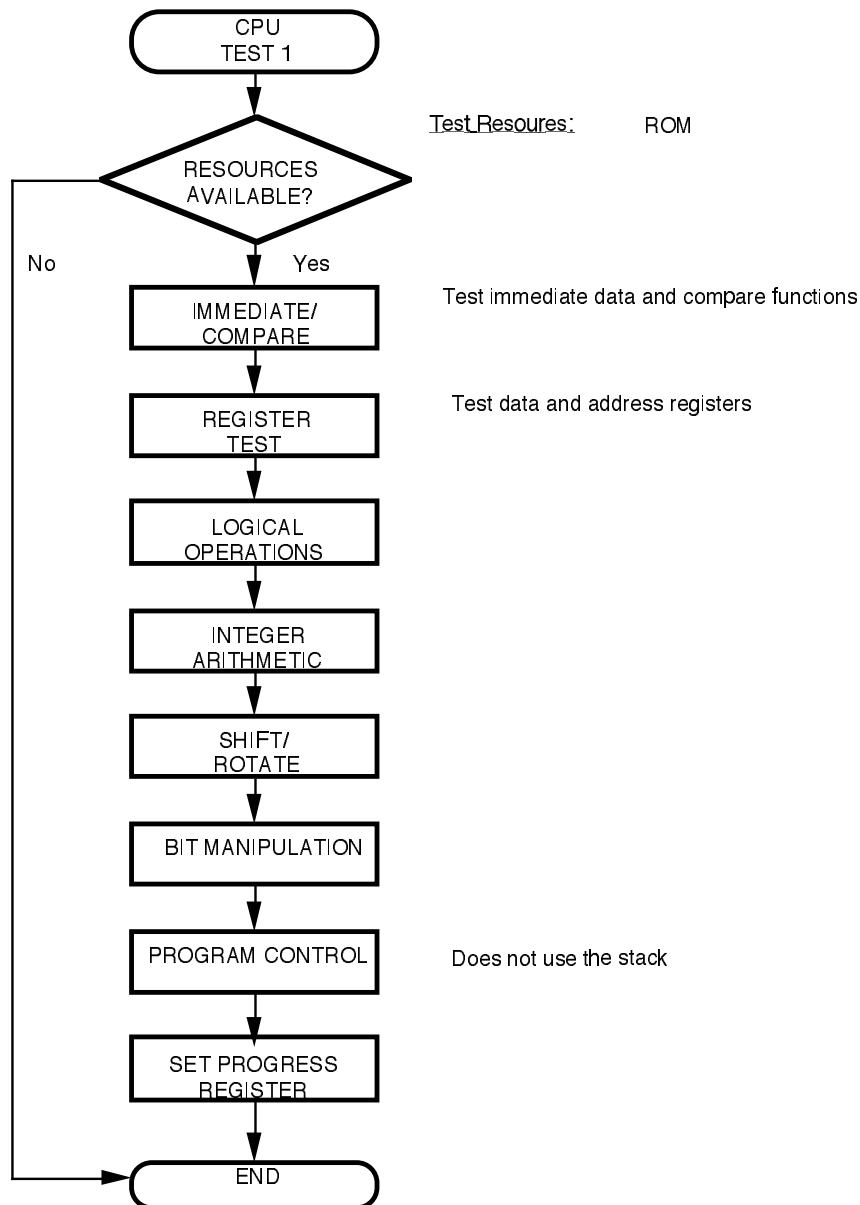


**Figure 2. CT302 Control Flow**

## 6.3 CPU

The CPU tests check operation of the M68000 processor on the MC68302. The tests assume that ROM functions even though it has not yet been tested. CPU testing occurs in two phases: with and without RAM. The first phase is a general check using no stack operations. After the internal RAM is verified, the CPU stack is located in internal RAM and CPU tests are completed. Figure 3 illustrates the CPU tests. The results of the tests are verified by other means.

At various times the "quick" mode of an instruction is used. This is forced because dedicated logic is exercised by the quick instructions.



**Figure 3a** CPU Test 1 Control Flow

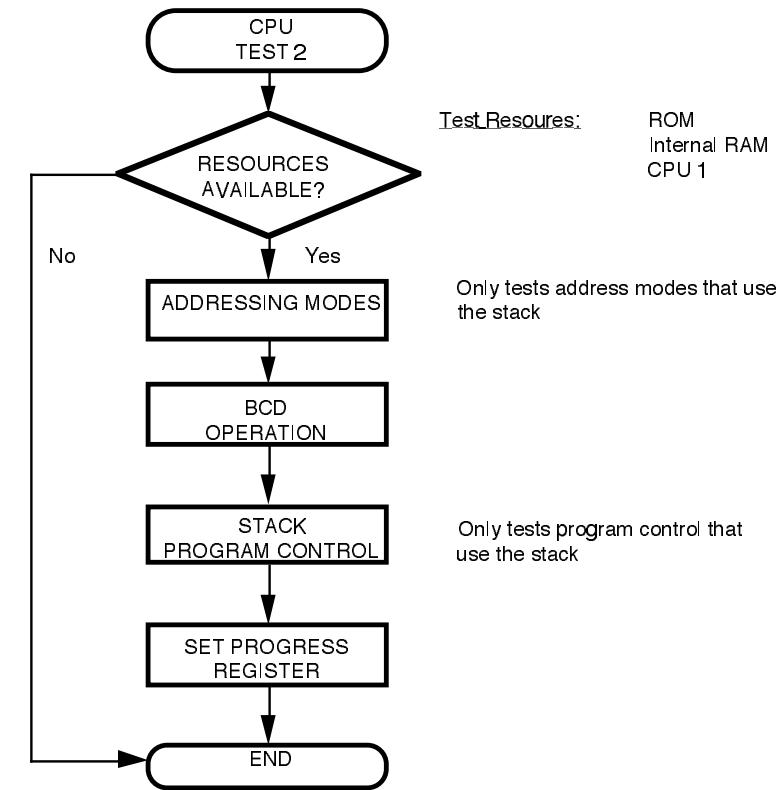


Figure 3b. CPU Test 2 Control Flow

6.4 ROM

The ROM tests are crucial to operation of any system: without correct ROM operation, no other CT302 tests are run.

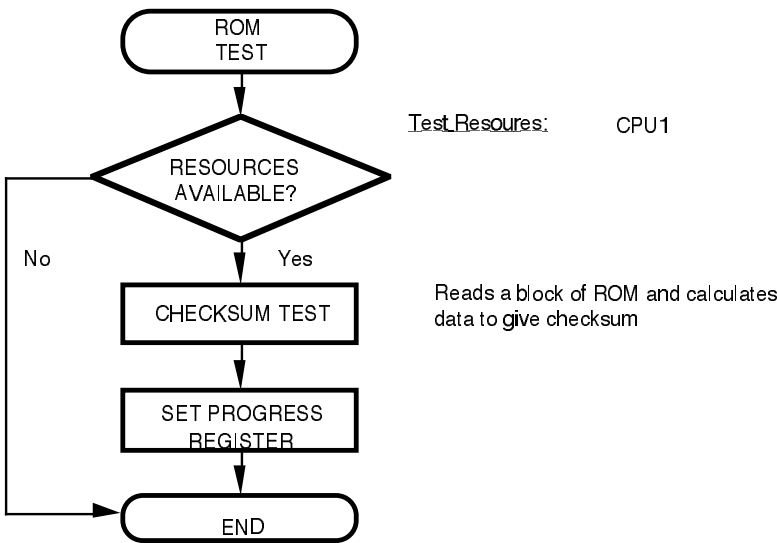


Figure 4. ROM Test Control Flow

Figure 4 illustrates the ROM test. A small area of ROM is reserved for storing a specific data pattern. A checksum is calculated for this area and compared to a checksum stored in the ROM. This allows the ROM test program to give a degree of confidence on the portion of the ROM containing the CT302 program is functional. It does not check the remainder of the ROM which is customer specific.

## 6.5 Internal Dual Port RAM

The internal memory tests verify operation of the MC68302 internal memory as a read/write storage area and access control using the function codes. The test routines are split into five modules described below. Figure 5 illustrates the internal RAM tests.

The internal RAM tests are split into two phases. The first four of the modules described below verify operation of the RAM array and are run in the first phase. The second phase checks the internal RAM's function code protection mechanism and requires the hardware watchdog timer.

Correct CPU and ROM operations are required before the first phase of the internal memory test is run. The hardware watchdog timer is an additional resource needed in the second phase of the internal RAM tests.

### 6.5.1 Data write with read-back compare

This test writes several data patterns, for example \$0, \$5, \$A and \$F, to memory and then reads the data back into a CPU register. The register contents are then compared with the original data. Read and write cycles are both byte and word wide. The outcome of this test verifies correct storage operation to RAM.

### 6.5.2 Write data address to memory

This test uses the current memory address as a data value to store at that address. This stored value is then read-back and compared with the original address value. If the comparison is correct then all address lines must be functioning correctly. The whole of memory is filled with data before the read-back operation begins.

### 6.5.3 Memory Fill and Test

All internal RAM is filled with a background pattern of \$0. A selected location is then loaded with a varying data pattern such as \$1234. The module then checks all other locations to determine if any location containing the background pattern has been modified. This test checks that the address and data lines are correctly connected.

### 6.5.4 Walking 0's and 1's

This is a bit oriented test which, after block filling memory with 1's, sets every bit to 0 and then back to 1 sequentially. When the bit is set to 0, the data is compared with the known correct value to check for correct operation of each bit of RAM.



### 6.5.5. Function Code Protection

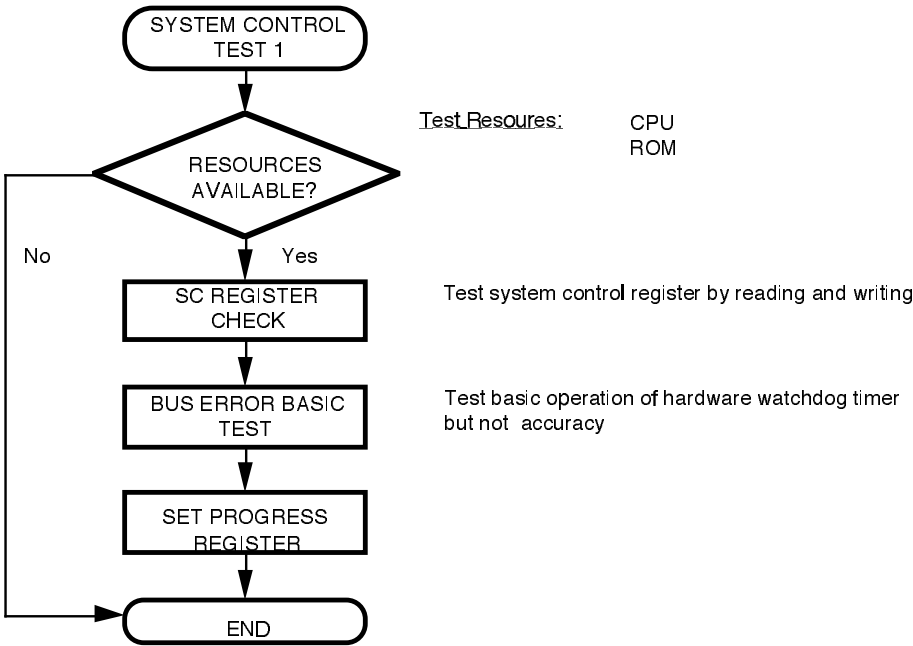
The MC68302 internal RAM can be programmed to check the function code bits when accesses are made to it. This protection mechanism is tested by locating the internal RAM in supervisor space with the CPU stack in internal memory and then making a user data access to internal memory. A bus error should be generated.

### 6.6 System Control

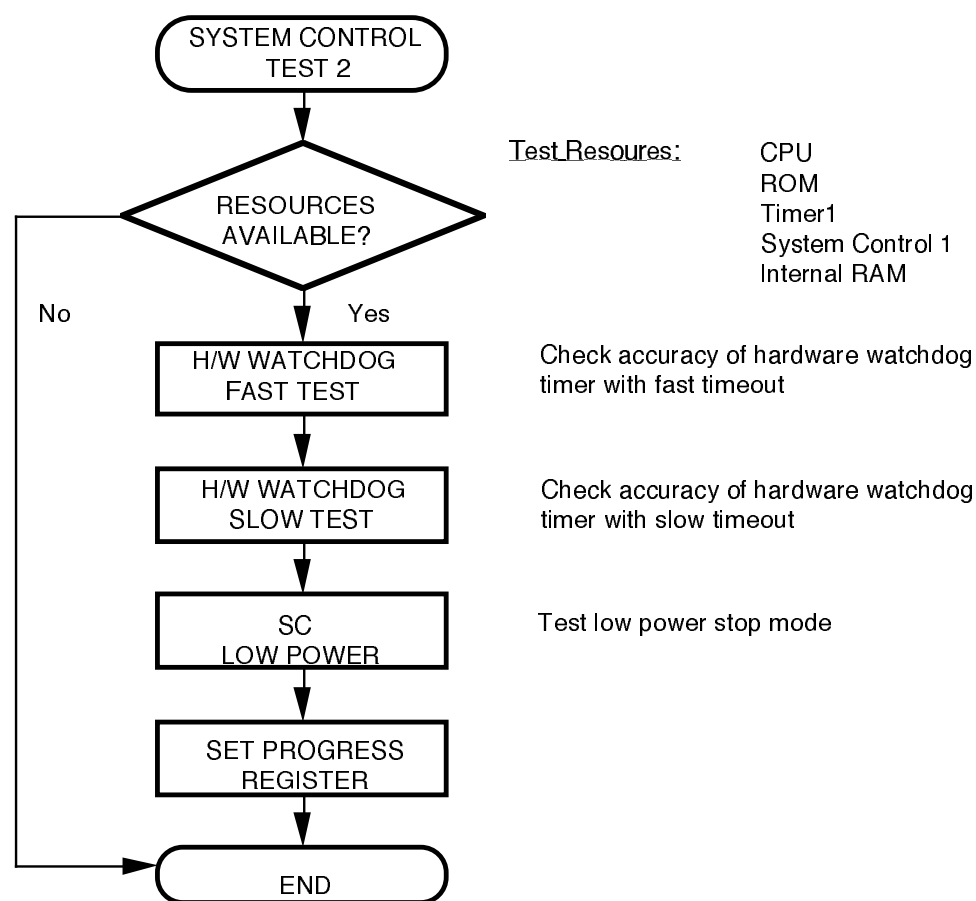
MC68302 system control features are controlled through the base address register and system control register. System control features are tested in two phases: the first test simply verifies the registers and hardware watchdog timer and the second test checks the low power logic and accuracy of the hardware watchdog timer. The tests are split this way because the second set require timer 1.

The first system control tests write and read the MC68302 system control and base address register. Without correct operation of these registers, no on-chip peripherals or memory can be accessed and the device is defective.

The MC68302 hardware watchdog timer generates bus errors so it must be tested early in CT302 because it is widely used by other tests. The CT302 bus error exception routine simply returns to CT302 after setting a flag to indicate that a bus error was received. To test the hardware watchdog timer, an unused area of the MC68302 memory map called NOMEM is required. When NOMEM is accessed, DTACK must not be returned. The first system control tests simply look for operation of the hardware watchdog timer; its accuracy is checked in the second system control tests.



**Figure 5a System Control Test 1 Control Flow**



**Figure 5b. System Control Test 2 Control Flow**

The low power logic is tested for basic operation in the second set of system control tests using a timer 1 interrupt to bring the MC68302 back into full operation. Complete testing of the low power logic cannot occur because this would reset the MC68302 and require external power measurement circuitry.

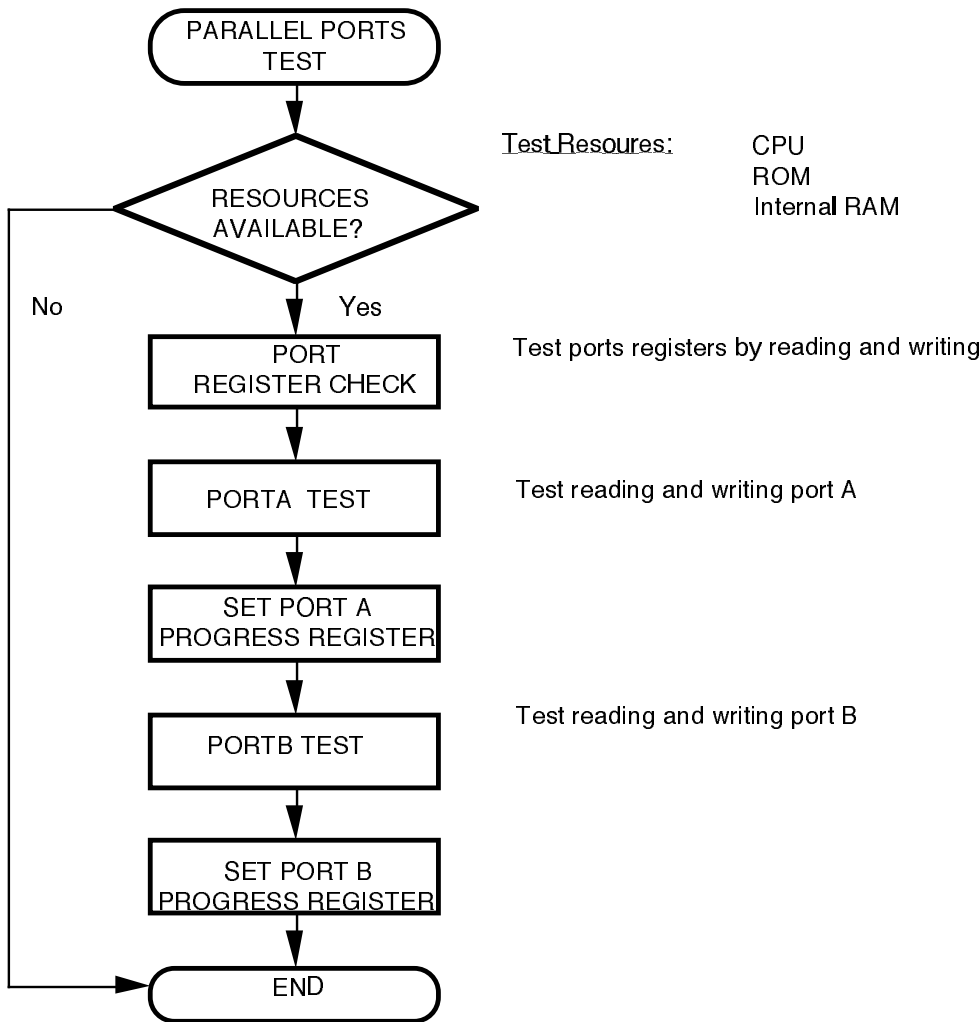
The following system control features are not tested because special hardware is required: read-modify-write cycle special treatment, external master access to MC68302 registers, slave mode operation, use of the bus clear signal, internal bus arbitration and the freeze debugging logic. The dock control register, a new feature of revision C devices, and its associated functions are not tested.

For all CT302 tests, it is assumed that the MC68302 hardware watchdog timer is the only active bus error generator in the system.

## 6.7 Parallel Ports

Port A and B control registers are written and read to verify register access. The two ports are then made output ports and specific data values are written to the output latch and read back to test the data registers. Figure 6 illustrates this test.

Full input, output and interrupt testing is not possible without special external hardware.



**Figure 6. Parallel Ports Test Control Flow**

**6.8 General Purpose Timers**

Timer 1 and timer 2 are tested for basic operation using each different internal clock source and various clock prescalers. The timer counter free-run and restart operations are both tested. During basic operation tests, timer accuracy is tested by comparing timer results with a software counter. To maintain the software counter accuracy, its code is run from internal memory with interrupts disabled. Figure 7 illustrates the timer tests.

Timer interrupts are not tested in these tests because interrupt controller operation has not been verified. Timer operation with external clocks is not checked.

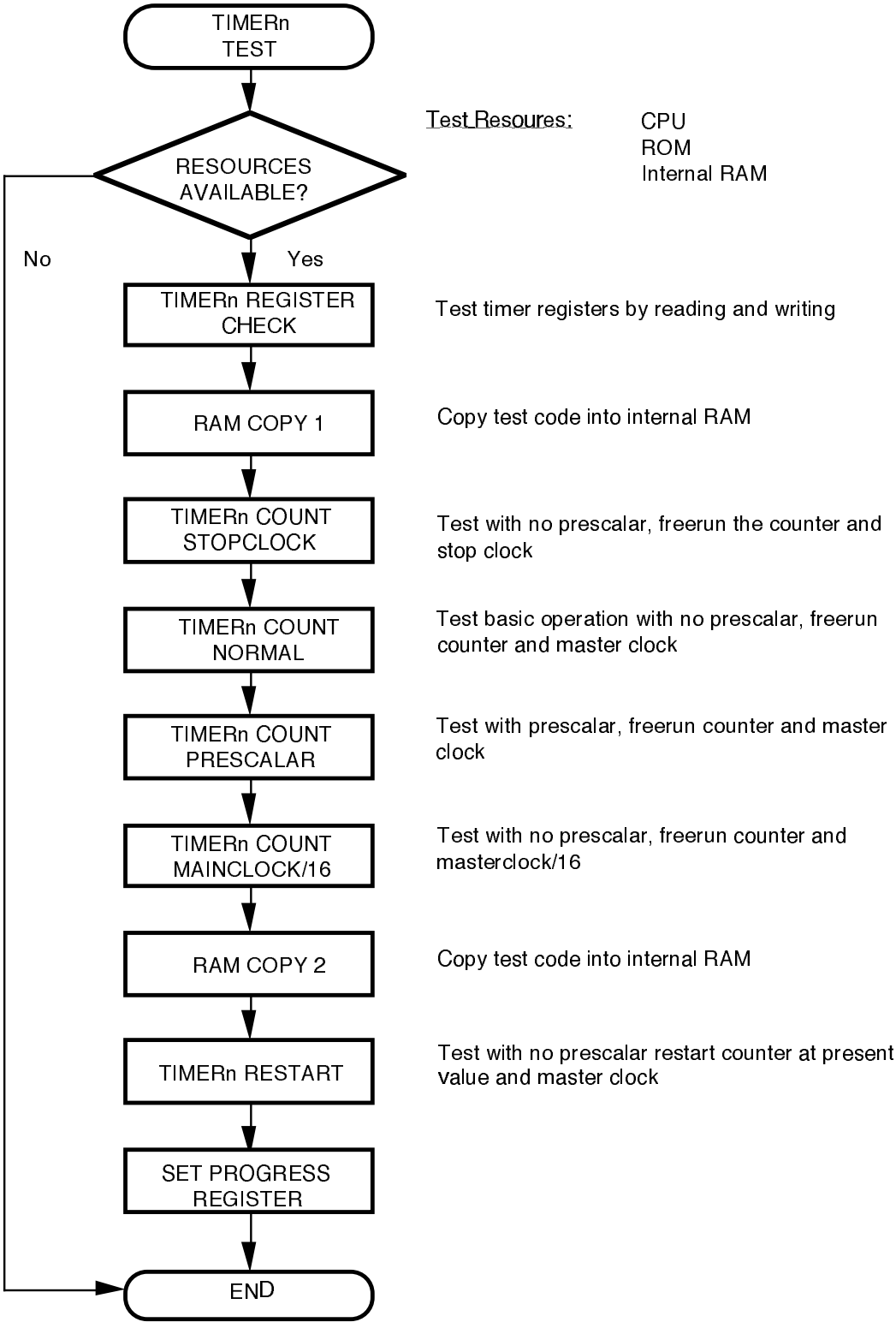


Figure 7. Timer Test Control Flow

6.9 Interrupt Controller

This module tests the interrupt controller and timer1 interrupt at the same time. Until now, no other interrupt sources have been tested.

To check the interrupt controller, interrupts are generated by both general purpose timers and correct operation of the MC68302 interrupt controller is checked. Tests check the interrupt mask and vector generation logic as well as the CPU interrupt mask function. Failure of this test could be caused by either the interrupt generation logic in the timers or the interrupt controller itself.

Interrupts from parallel port B and external sources are not checked because this would require special hardware.

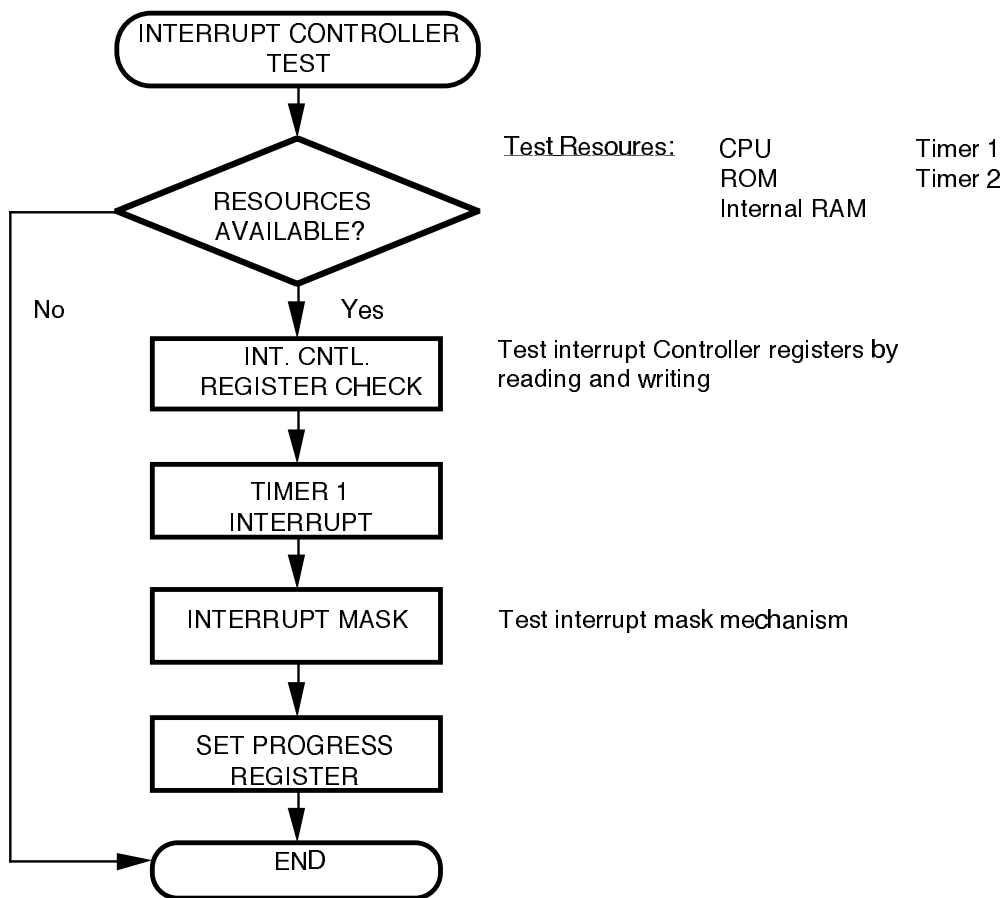


Figure 8. Interrupt Controller Test Control Flow

6.10 Software Watchdog Timer

The software watchdog timer has no event register so it must be tested after the interrupt controller is verified.

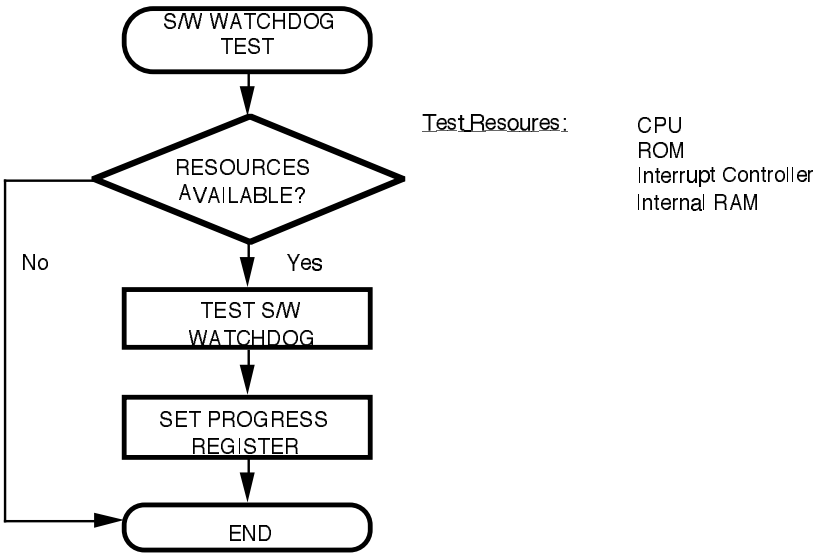


Figure 9. Software Watchdog Timer Test Control Flow

6.11 SCP

Operation of the full-duplex serial communications port (SCP) is tested in loopback mode at low and high speeds with the clock inverted and non-inverted. SCP interrupt generation is also checked. The SCP data rate is checked by timing its character transmission/reception using timer 1. Transmitted data appears on the SCP output pins during the tests.

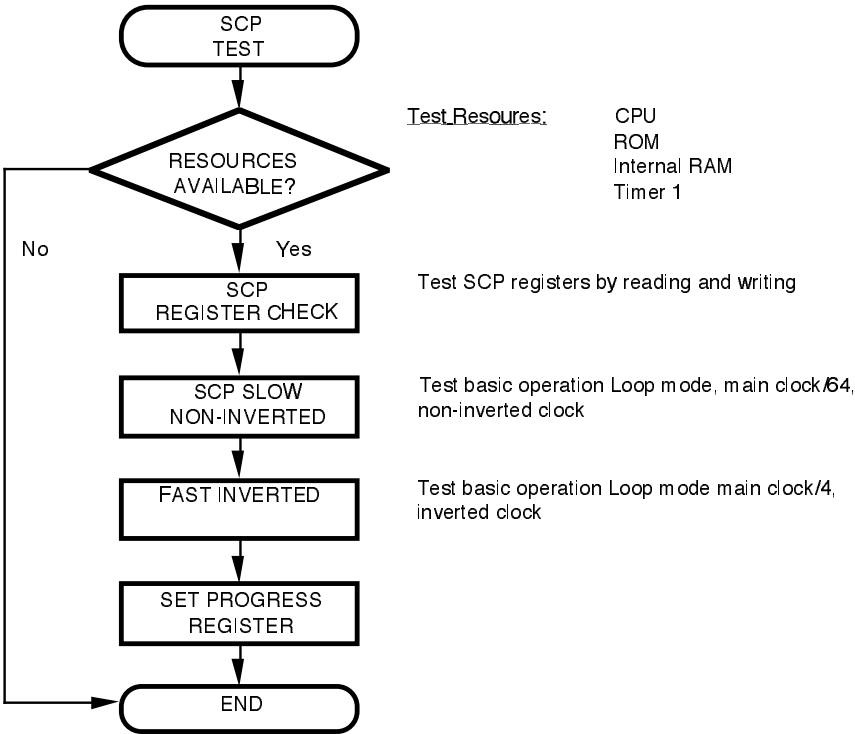


Figure 10. SCP Test Control Flow

6.12 Chip Selects

Operation of the MC68302 chip select, wait state and protection logic is verified. Figure 11 illustrates the chip select test.

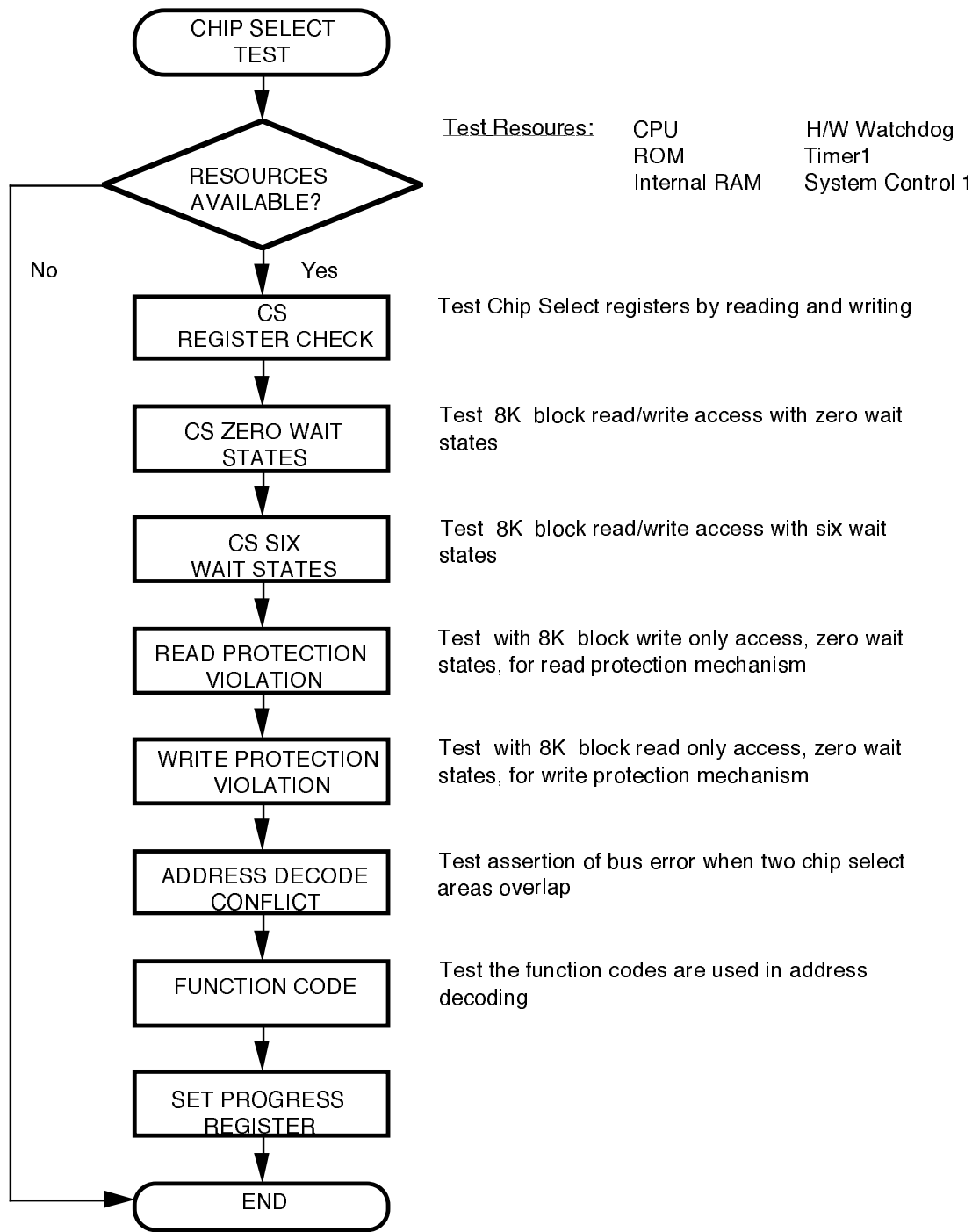


Figure 11. Chip Select Test Control Flow

The wait state generator is tested by repeatedly accessing one location which lies in an area decoded by one chip select and timing the total time for 100 accesses. The wait state test code runs from MC68302 internal memory so that program

memory access time is minimised and defined. Wait state logic is only tested once rather than with each chip select because there is only one wait state generator.

The protection logic stops accesses to areas where they are not allowed. These include incorrect function codes and read/write protection violations. Chip selects are configured for one type of access and then a different type is made. If a bus error results, the protection logic is functioning.

During the chip select tests, the area of unused memory map called NOMEM is used, as described in section 4.6. It is assumed that there are no external wait state generators or watchdog timers active during chip select tests.

If the target system uses chip select 0 to select ROM, the chip select 0 tests need to be removed because it is reprogrammed.

### 6.13 IDMA

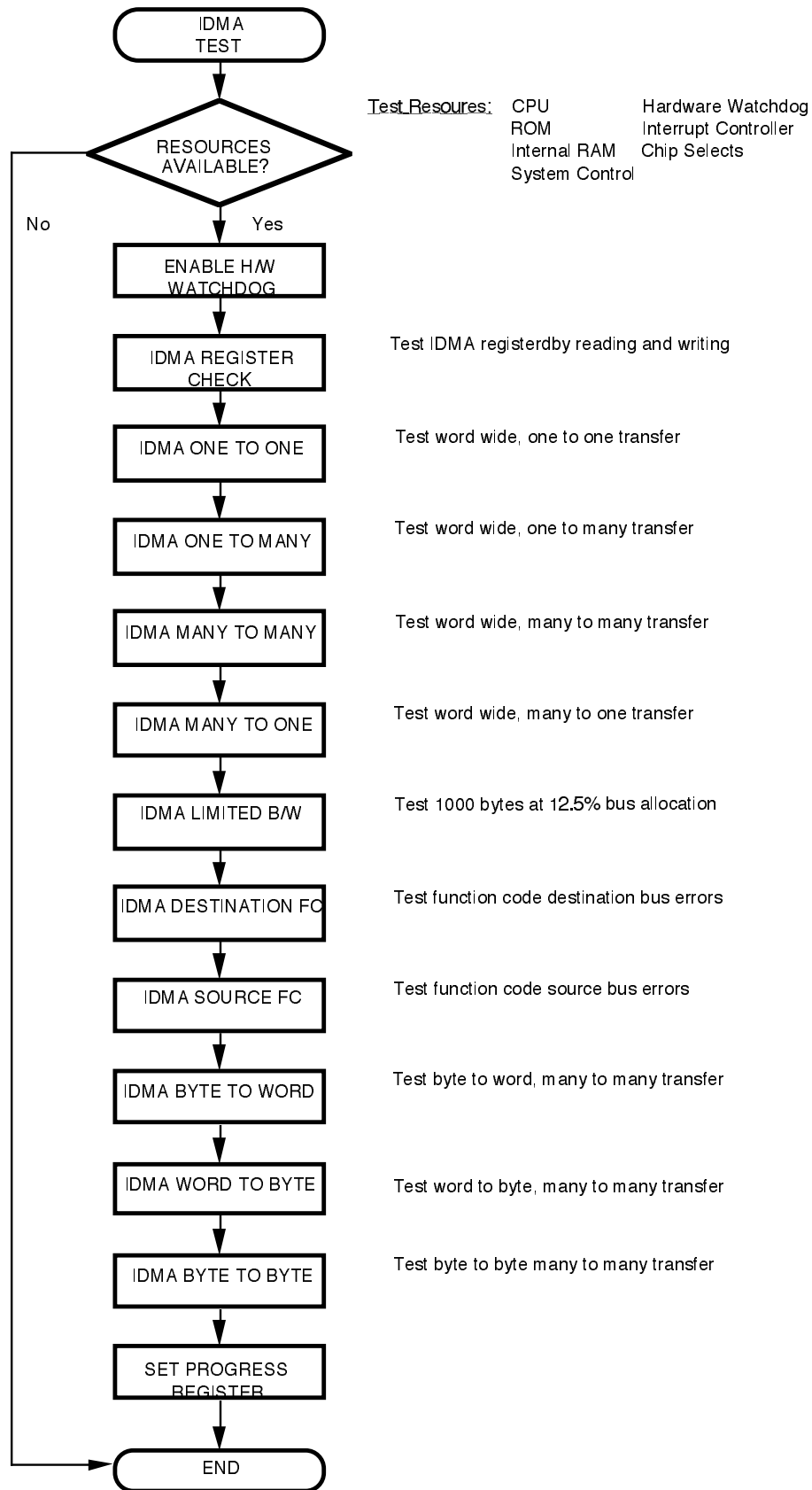
Operation of the IDMA hardware is tested by moving data between locations in internal RAM. Internal memory is used because external RAM has not yet been verified and it guarantees access time which simplifies the IDMA bus bandwidth tests. The only difference when using external memory would be to exercise the bus interface but this has already been verified in the ROM tests. Figure 12 illustrates the IDMA test. The following IDMA operations are tested:

- One to one transfers
- One to many transfers
- Many to one transfers
- Many to many transfers
- Data packing (byte to word and word to byte transfers)

Additionally, IDMA transfers are run with various function codes and limited bus bandwidth. The function code tests involve transferring data between protected areas and causing bus errors. The limited bandwidth tests use timer 1 to see how long transfers take. IDMA interrupts are tested.

The IDMA external request, acknowledge and termination signals and their functions cannot be tested because these would require special external hardware.





**Figure 12 IDMA Test Control Flow**

#### **6.14 UART Mode SCCs**

All three SCCs are tested in UART mode working with data buffers located in internal RAM (the SDMA and external memory has not yet been verified). Tests place the SCCs in loopback mode and do not drive the physical interface pins. Figure 13 illustrates the UART tests. Tests cover all the main features of UART operation:

- Basic transmission and reception in loopback
- Parity
- Data rate check
- Idle transmission and detection
- Character length
- Reception without receive buffers
- Interrupt generation

UART mode is the first of the serial tests and configures the serial interfaces and general control logic for the serial channels. This is not subsequently retested with the SCCs in other modes. If the UART tests fail because of a microcode fault (the microcode storage, retrieval and execution unit) then all SCCs will fail other communication protocol tests unless the fault is an isolated error in the microcode itself.

Testing in UART mode does not cover: multidrop mode, fractional stop bits, framing and noise errors, modem control line operation, break transmission and detection, control character use, asynchronous DDCMP operation and receiver FIFO overrun errors.

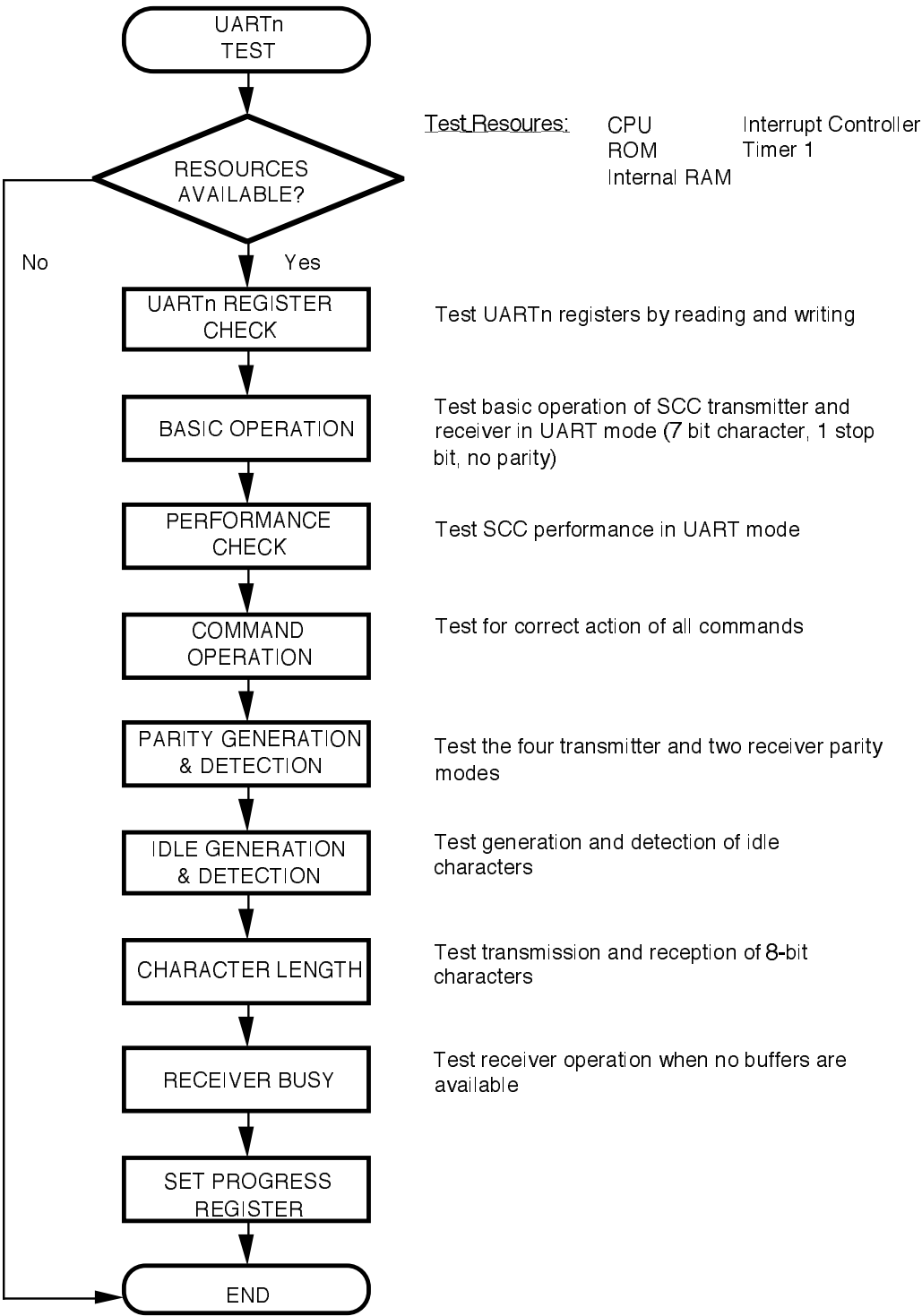
#### **6.15 HDLC Mode SCCs**

All three SCCs are tested in HDLC mode working with data buffers located in internal RAM (the SDMA and external memory has not yet been verified). Tests place the SCCs in loopback mode and do not drive the physical interface pins. Figure 14 illustrates the HDLC tests. Tests cover all the main features of HDLC operation:

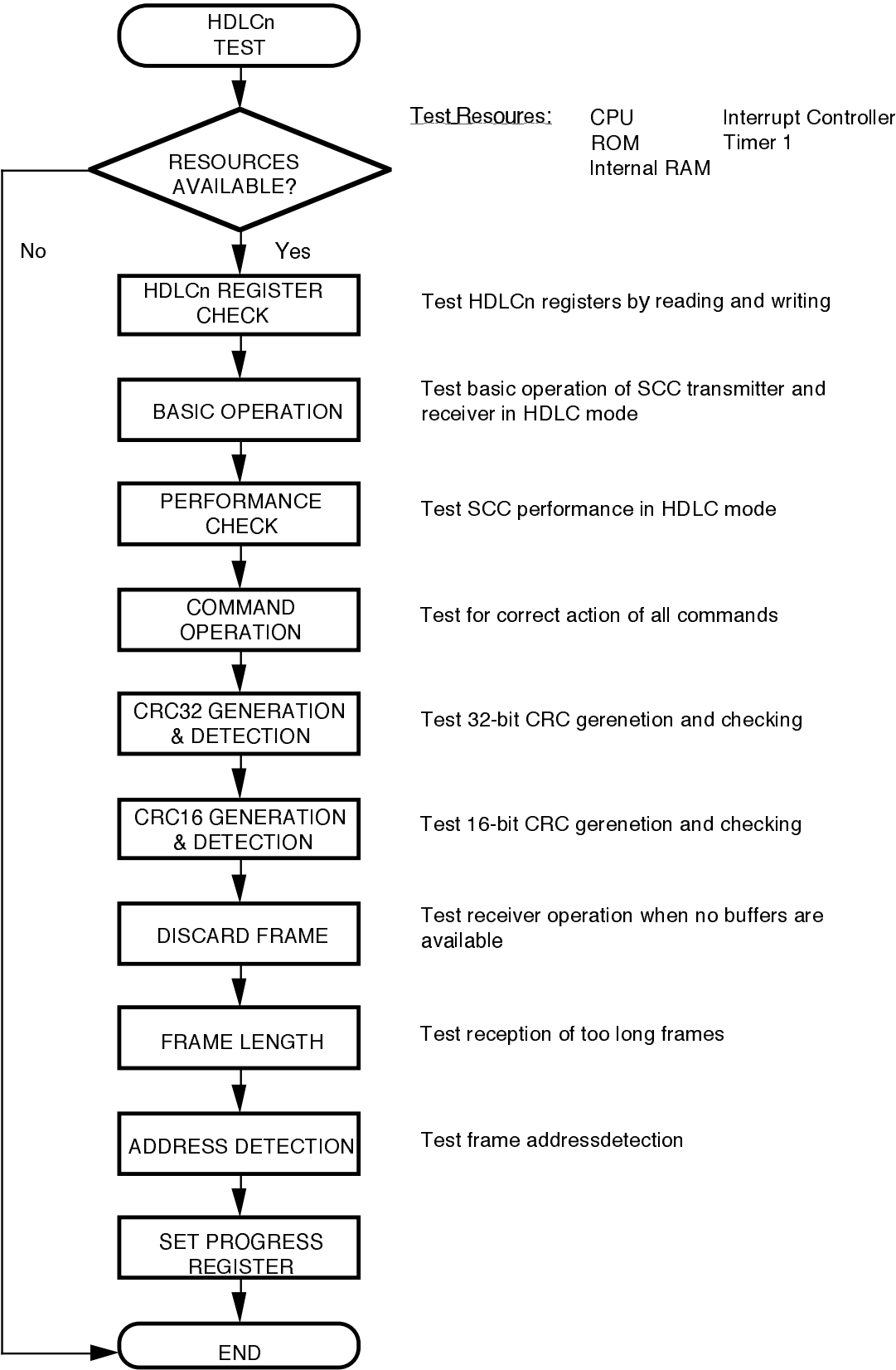
- Data transmission and reception in loopback mode (including multiple buffer handling)
- Data rate check
- CRC transmission and reception
- Address matching on reception
- Reception of long frames
- Reception of frames when no buffers are available
- Interrupt generation

In HDLC mode, the general serial interface and control logic blocks are not tested because this has been verified in the UART tests. Detailed tests are made on one SCC to check the HDLC microcode and less rigorous tests are performed on the other two SCCs just to test the HDLC hardware.

SCC testing in HDLC mode does not cover: data encoding format, modem control line operation and errors, non-octet aligned errors, abort characters, flag sharing, transmitter underrun and receiver FIFO overrun errors.



**Figure 13. UART SCC Test Control Flow**



**Figure 14. HDLC SCC Test Control Flow**

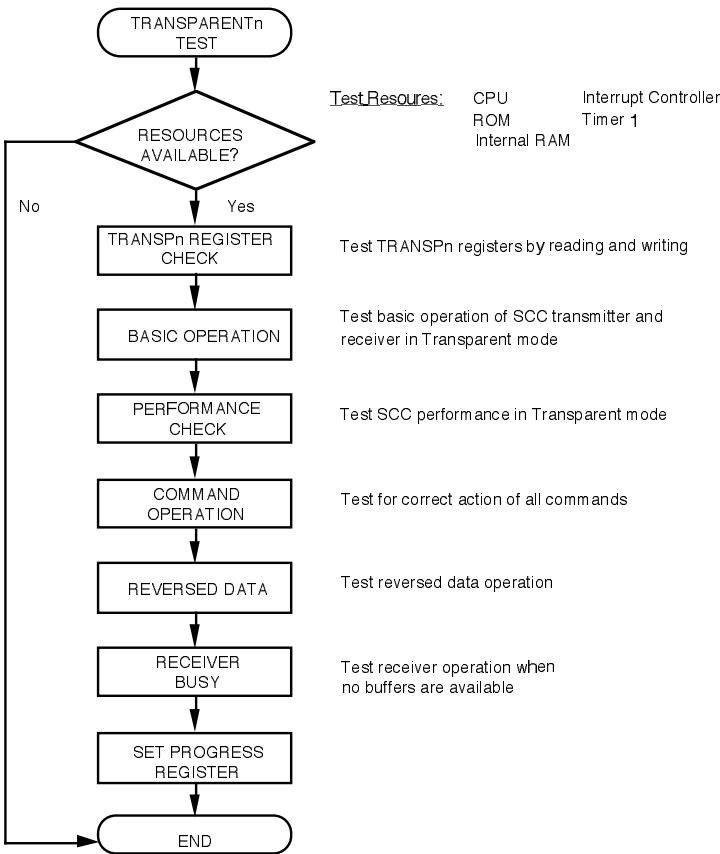
### 6.16 Transparent Mode SCCs

All three SCCs are tested in transparent mode working with data buffers located in internal RAM (the SDMA and external memory has not yet been verified). Tests place the SCCs in loopback mode and do not drive the physical interface pins. Tests cover all the main features of transparent operation:

- Data transmission and reception in loopback mode
- Data rate check
- Detection of synchronisation characters
- Basic transmission and reception with reversed data
- Interrupt generation

The transparent mode provides no framing or error checking that need testing. The test of reversed data (transmit and receive most significant bit first) cannot be a comprehensive test because the end result is the same as with non-reversed data. The only way to test the reversed data option fully would be with external hardware.

SCC testing in transparent mode does not cover: external sync mode, data bit reversal, modem control line operation and errors, transmitter underrun and receiver FIFO overrun errors.



**Figure 15. Transparent SCC Test Control Flow**

6.17 External RAM

External RAM is tested using the same algorithms as the MC68302 internal RAM. Correct CPU, ROM, the RAM chip select and hardware watchdog timer operations are required before the internal memory is checked.

6.18 SDMA

SDMA tests can only occur when external RAM is working. SCC1 is configured to transmit from and receive to external data buffers so that the SDMA is exercised. An area of undecoded memory is used to test the SDMA interrupt function. Only one SCC is used because there is only one SDMA in the MC68302. Figure 16 illustrates the SDMA test procedure.

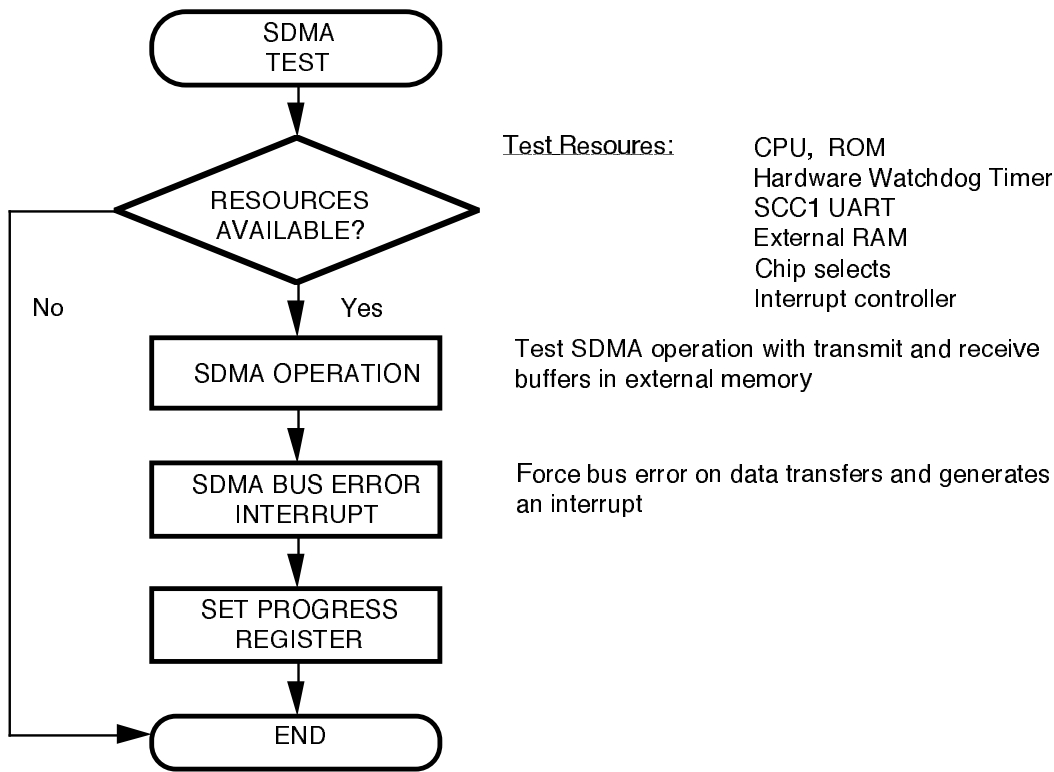


Figure 16. SDMA Test Control Flow

7. References

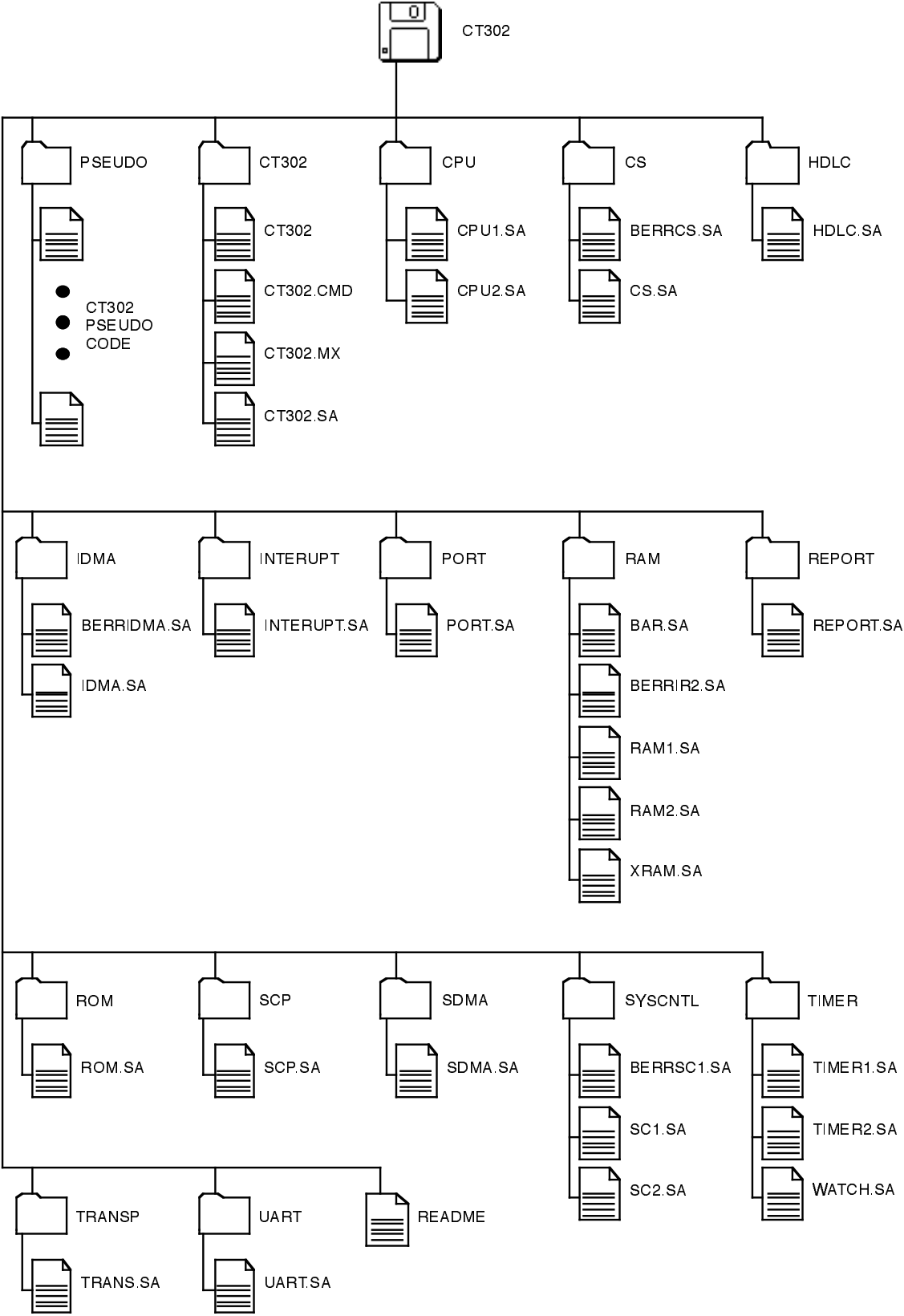
MC68302 User's Manual, Revision 2, Motorola order code MC68302UM/AD.

MC68000 User's Manual, Revision 7, Motorola order code MC68000UM/AD.

**Appendix 1. CT302 Directory Structure**

CT302 source code and pseudo code files are available on a PC format disk. Figure A.1 shows the directory structure on the CT302 disk. Pseudo code files are in directory PSEUDO. Batch assembly files are provided in directory CT302. Source code files are contained in individual directories, labelled appropriately. File CT302.MX is a file of S-records for the complete CT302 software ready to run on an MC68302 ADS board.

Certain filenames have been truncated to fit the PC format filename specification. The INTERRUPT directory and file INTERRUPT.SA have had their names truncated from INTERRUPT and INTERRUPT.SA respectively. Also, file CT302.CMD has been truncated from CT302.CMDS.



**Figure A1 CT302 Disk Directory Structure**



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