AN98091

CFL 13 W demo PCB with UBA2021 for integrated lamp-ballast designs

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Document information

Info	Content
Keywords	CFL ballast, UBA2021, compact, half-bridge, driver circuit
Abstract	A description is given of a 13 W electronic CFL ballast (SMD demo board PR38922 and leaded demo board PR39001), which is able to drive a standard NXP PLC 13 W and similar lamps. The ballast is based on a voltage fed half-bridge inverter topology. It is designed for a nominal mains input voltage of 230 V (RMS) ± 15 %. The half-bridge switching devices (discrete power MOSFET PHU2N60 or the rugged PHU2N50) are driven and controlled by the UBA2021 high voltage IC. Therefore this UBA2021 IC contains a driver circuit (with integrated high-side drive and bootstrap circuit), an oscillator, and a control and timer circuit for starting up, preheating, ignition, lamp burning and capacitive mode protection. The circuit is intended for integrated ballast-lamp designs

Revision history

Rev	Date	Description
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1. Introduction

A small and low cost electronic CFL ballast has been designed, which is able to drive a 13 W NXP PLC lamp or similar 13 W Compact Fluorescent Lamps (CFL). The circuit is intended for integrated ballast-lamp designs. Therefore no additional protection against lamp removal is required.

A voltage fed half-bridge inverter has been chosen as lamp driver circuit. The inverter has been designed for a nominal input voltage of 230 V (RMS) ± 15 %, 50 Hz / 60 Hz. The key component in this circuit is the UBA2021 Integrated Circuit (IC). This UBA2021 is a high voltage driver IC, which provides all the necessary functions for a correct preheat, ignition and burn-state operation of the lamp. Besides these control function the UBA2021 provides the level-shift and drive function (high-side driver and bootstrap circuit included) for the two discrete power MOSFETS PHU2N60.

The key issues for this design are: compact, low cost and low component count. The UBA2021 IC has a few peripheral components. Only a minimum amount of components are required for the optimal balance between maximum design flexibility and low component count. Furthermore, all components are of compact size.

For a reliable system operation and a long lamp life, the fluorescent lamp is preheated first, after switch-on. This preheat is controlled by the UBA2021 IC. The electrode currents and voltages meet the requirements to obtain a proper electrode-emitter temperature. This results in a smooth ignition of the lamp at a much lower ignition voltage, with less component stress and/or electrical stress.

In the burn phase, the operation frequency is approximately 43 kHz, so no interference with infrared communication systems (32 kHz / 36 kHz) will occur. Furthermore, this frequency is kept below 50 kHz (third harmonic < 150 kHz), which meets a better RFI performance. During steady state operation, the frequency is determined by a feed-forward control. The result is a constant level of light output over a large mains voltage range (approximately 200 V / 250 V).

The 13 W CFL ballast with UBA2021 is available on two versions of printed circuit boards. Printed-circuit board (PCB) PR38922 is a miniaturized version with SMD components (referred to as SMD version). PCB PR39001 consists of leaded components only (referred to as leaded-version). Both PCBs contain the same electrical circuit. Their board designs (PCB layout) meet the requirements for a good EMC performance.

2. Circuit and system description

The following provides a detailed block level overview of the CFL ballast.

2.1 Block diagram

The CFL ballast has been designed for a mains voltage range of 230 V (RMS) ± 15 %, 50 Hz / 60 Hz. Basically, the circuit consists of two sections: the AC bridge rectifier and the half-bridge inverter. Figure 1 shows the block diagram of the circuit. A complete schematic diagram is given in Figure 2.

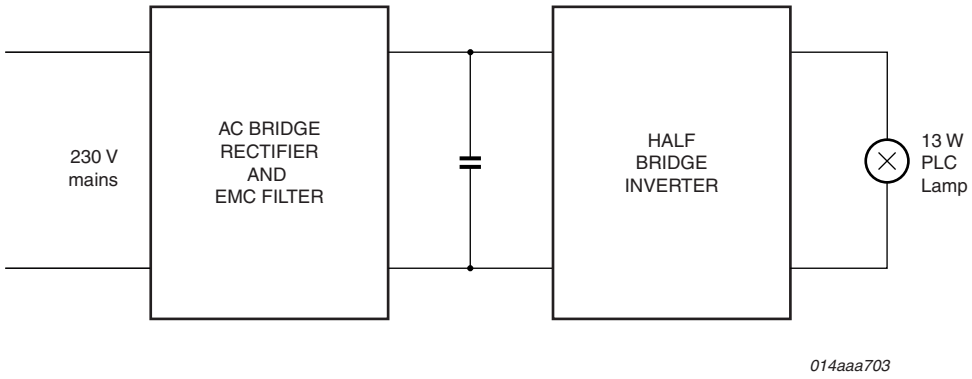


Fig 1. CFL ballast block diagram

The AC mains voltage is rectified by four bridge rectifying diodes and the DC supply voltage for the half bridge inverter is smoothed by a buffer capacitor. An EMC-filter is used to minimize the disturbance towards the mains. The half-bridge inverter is a voltage fed type and has been designed to operate a 13 W PLC lamp or similar lamps.

The voltage fed inverter belongs to a group of high frequency resonant inverters, which are very attractive to drive lamp circuits. They can achieve a high efficiency, due to the zero-voltage switching principle. This reduces the switching losses of the two power MOSFETS PHU2N60 to a minimum, so the power loss is MOSFET ON-loss. Therefore the steady state operation (thermal resistance and ON-loss) determines the choice of MOSFET type (by R_{DSon}). During ignition and preheat, the total MOSFET current has to be below the specified maximum rating. All together the PHU2N60 ($R_{DSon} < 6\ \Omega$, $V_{ds\text{-}max} = 600$ V) suits best with this application.

Remark: A further increased thermal management will be achieved, when rugged types PHU2N50 will be used. The PHU2N50 power MOSFETS have a lower R_{DSon} and high repetitive avalanche energy ratings ($V_{ds\text{-}max} = 520$ V).

2.2 Start-up phase

After switch-on of the system, the rectified mains voltage is applied to the buffer capacitor C2. This capacitor smoothes the ripple voltage, caused by the (doubled) mains frequency. The result is a high DC voltage V_{hv}, which is an input for the half-bridge inverter (power components: Q1, Q2, L2, C5, the lamp, C3 and C4). The inductor L1 is used as an EMI-coil. This L1 will minimize disturbances towards the mains. In Section 4.2, a measurement of the conducted EMI is given.

During the start-up phase, the low voltage supply capacitor C8 is charged, out of the high DC voltage, via the resistors R3, R5 and the UBA2021 IC (start-up supply path). As soon as the supply voltage V_S over C8 reaches 5.5 V the UBA2021 resets. After this initial reset MOSFET Q2 is set conductive and MOSFET Q1 is non-conductive. This allows the bootstrap capacitor C9 to be charged as well by the UBA2021 IC (via an internal bootstrap circuit). The supply voltage V_S further increases and the circuit starts oscillating at $V_S > 12$ V. The system is now in the preheat phase.

2.3 Preheat phase

The MOSFETs Q1 and Q2 are brought in conduction. This introduces a square-wave voltage V_{hb} across the half-bridge midpoint, that is between zero and V_{hv}. The start frequency of this voltage, V_{hb}, is approximately 90 kHz. Under these conditions the circuit formed by C12, C7, D6 and D5 can take over the low voltage supply function from the start-up supply path. C12 and C7 are also used as a snubber circuit for the half-bridge switches.

During the whole preheat phase, the half-bridge frequency is well above the resonance frequency of L2 and C5, so the voltage across C5 is low enough (< 200 V (RMS)) to keep the lamp non-ignited (see Section 5: CFL 13 W - LC and LCR curves). The combination of L2 and C5 is determined by the required lamp current and operation frequency in the burn phase. The preheat phase gives an additional requirement for the limit of the minimum value of C5 at given L2, determined by the non-ignition voltage of the lamp (< 200 V (RMS)).

At start frequency, a small AC current starts floating from the half-bridge midpoint, through L2, C5 and the lamp electrodes. The frequency now gradually decreases and the AC current increases. The slope of decrease in frequency is determined by the value of capacitor C6. The decrease stops (approximately 1.5 ms after switch-on) when a defined value of the AC current through R4 is reached, which is a reference for the AC current through the lamp electrodes. The UBA2021 now controls the AC current through the lamp electrodes, by measuring the voltage drop across R4. This control point is called preheat operation point. In Section 4, an oscillogram of this controlled preheat is given (see Figure 5 and Figure 6).

For a time period of approximately 300 ms (preheat time), defined by capacitor C10 and resistor R2, the system stays in the preheat operation point where the lamp electrode current is controlled. This allows both lamp electrodes to heat up in a defined, optimal way. The electrodes-emitters are powered and large quantities of electrons are emitted into the lamp. Ignition of the lamp can now take place at a much lower ignition voltage, under less electrical stress of the circuit and with less stress to the lamp. To obtain a long life time of the lamp, this defined electrode preheat, followed by a smooth ignition is very important.

2.4 Ignition phase

After expiration of the preheat time, the UBA2021 further decreases the switching frequency of the half bridge.

The load is still inductive so the lamp voltage (AC voltage across C5) goes up as the frequency goes down. Typically, the lamp ignition voltage can exceed 460 V (RMS), which even guarantees lamp ignition at low temperatures. The combination of values for lamp coil L2 and lamp capacitor C5 has been chosen in such a way that the voltage across the lamp can reach these high levels. The minimum required ignition voltage will determine a limit for the maximum value of C5 at a given L2.

During actual ignition, the operation frequency of the half bridge is a few kHz above the resonance frequency of series circuit formed by L2, C5 and the electrodes. After ignition of the lamp, transition to the burn phase takes place (see Section 5). The operating frequency normally decreases to the bottom frequency f_{bottom}. This will be done in one continuous frequency sweep down from the preheat phase. The UBA2021 IC can make the transition to burn phase in two ways:

- Reaching the f_{bottom}
- Reaching the ignition-time

f_{bottom} is approximately 33 kHz and is set by R2 and C11. The ignition time is approximately 280 ms (defined as 15/16 part of the preheat time, determined by R2 and C10).

2.5 Burn phase

In the burn phase the circuit normally tends to drop down to f_{bottom} (= 33 kHz). However, a feed-forward control becomes active after the ignition phase. The principle of feed-forward control will be explained below. For now it is important to know that the operation frequency is kept at approximately 43 kHz for a nominal input of 230 V (RMS) by this feed-forward control. The half bridge now supplies a square-wave voltage with an amplitude equal to half the rectified mains voltage and a frequency that is equal to 43 kHz, to the lamp circuit. Basically, the lamp can be seen as a resistive load in parallel to lamp capacitor C5.

The half-bridge inverter, in combination with the lamp circuit formed by L2, C5 and the lamp, has been designed for a nominal mains voltage of 230 V (RMS). The steady state operating point of a 13 W PLC lamp is approximately that of a lamp voltage of 75 V, a lamp current of 170 mA, and a lamp power of 13 W. These values have to be met at a mains voltage of 230 V (RMS), in order to obtain a long lamp life.

It can be calculated that for the actual values of L2, C5 and a 13 W PLC lamp, the total circuit delivers the desired lamp power (at the desired steady-state lamp voltage, lamp current and nominal mains input voltage). However, other L2/C5-combinations are also possible. Parameters like the preheat operation point, the minimum required ignition voltage and component tolerances determine which combination suites best. The result is that an inductance of L2 = 3.1 mH as ballast coil and lamp capacitor C5 = 3.9 nF give the best over all performance (see Section 5 CFL 13 W - LC and LCR curves).

Above a defined voltage level, the switching frequency of the half bridge also depends on the amplitude of the mains voltage. In the burn phase, the current through R3 and R5 is monitored by the UBA2021 IC. Indirectly this current is proportional to the amplitude of the applied mains voltage. The UBA2021 IC uses the variation of mains voltage amplitude information to increase/decrease the operating frequency. The effect is that the lamp power stays more or less the same over an input mains voltage range from 200 V/250 V. This principle is called the feed-forward control (see Section 4.2).

Normally an increase of the mains voltage (above 230 V (RMS)) would result in an increase of the lamp power, because the half-bridge inverter is a voltage fed type. This increased lamp power could further result in high temperatures of or in the lamp. Eventually this will cause an early failure of the lamp. The feed-forward control of the UBA2021 IC protects the lamp and the circuit against the increase of lamp power.

In order to prevent feed-forward control on the ripple (100 Hz/120 Hz) of V_{hv}, the UBA2021 IC uses C10 to filter out this ripple.

2.6 Capacitive mode protection

To protect the power circuit against excessive electrical stress a capacitive mode protection has been implemented in the UBA2021 IC. This protection will become active during the ignition and burn phase. Therefore the UBA2021 IC checks the zero-voltage switching condition each half-bridge switching cycle. This is done by monitoring the voltage across R4. If this voltage is below 20 mV typical at the time of the turn-on of Q2, capacitive mode operation is assumed.

As long as this capacitive mode is detected, the UBA2021 IC increases the switching frequency. This will limit the half-bridge output-current to a maximum value. If no capacitive mode is detected, the frequency drops down again to the feed-forward frequency (43 kHz).

3. CFL 13 W demonstration applications

Two versions of the 13 W CFL application were made. Demonstration board PR38922 is a SMD version. PR39001 is a leaded version. Both demonstration boards are based on the same schematic diagram as shown in Figure 2.

3.1 Schematic diagram

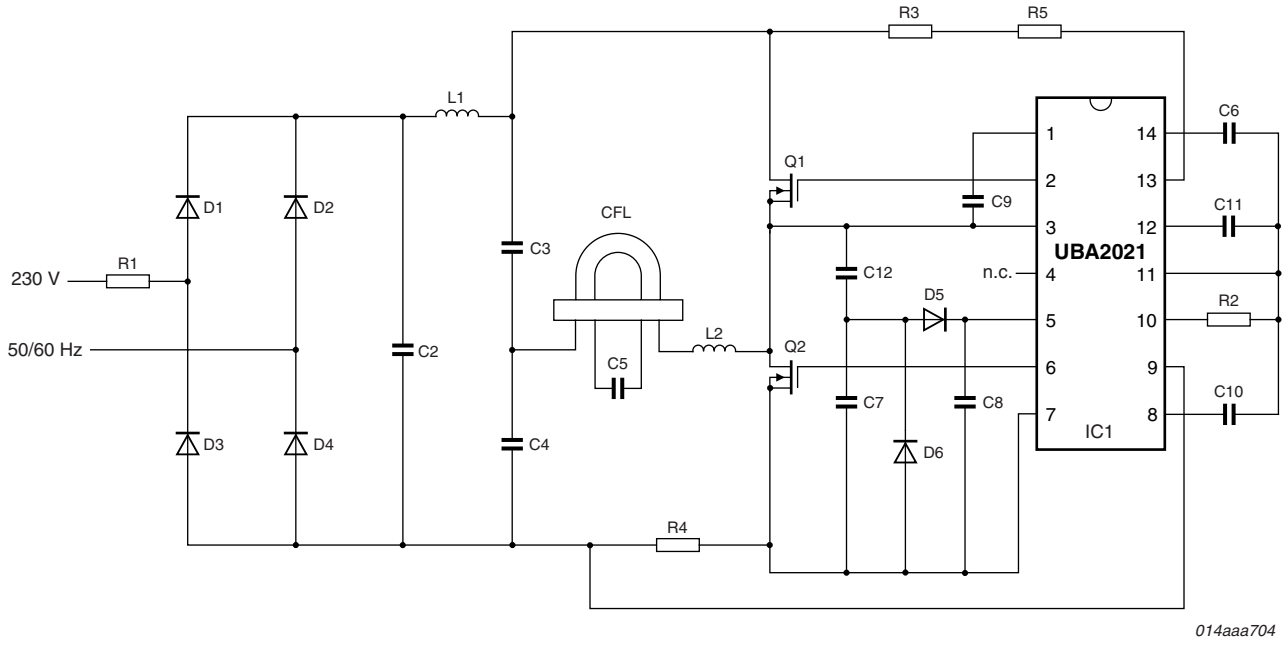


Fig 2. Schematic diagram

3.2 Demonstration board PR38922 (SMD version)

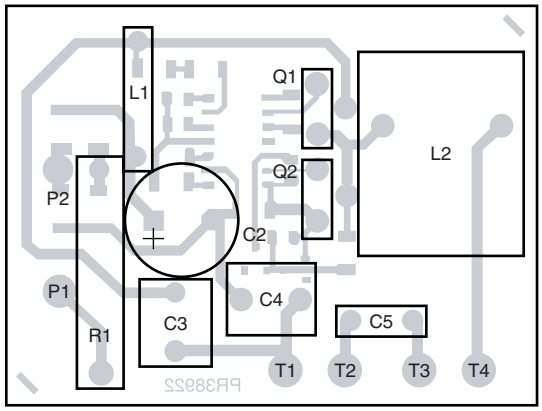


Fig 3. PR38922 component layout

Remark: The actual size of the PR38922 PCB SMD version is 33 mm × 44 mm.

3.2.1 Component parts list PR38922 (SMD version)

Table 1. Component parts list

Component	Value/type	12NC NXP order number
R1	47 Ω - PR02	2322 194 13479
R2	27 kΩ - RC02G	2322 723 61273
R3, R5	200 kΩ - RC02G	2322 723 61204
R4	1.3 Ω - RC02G	2322 723 61138
D1, D2, D3, D4	BYD17M - SOD87	9338 122 70115
D5, D6	BAS16 - SOT23	9334 606 20212
C2	3.3 μF/400 V - RLH151	2222 151 56338
C3, C4	100 nF/250 V - MKP465	2222 465 90001
C5	3.9 nF/400 V - MKP370	2222 370 90149
C6	47 nF/50 V - X7R 0805	2222 590 16636
C7	680 pF/50 V - NP0 0805	2222 861 12681
C8	100 nF/50 V - X7R 0805	2222 580 16741
C9, C10	100 nF/50 V - X7R 1206	2222 581 16641
C11	150 pF/50 V - NP0 0805	2222 861 12151
C12	470 pF/500 V - NP0 1206	2222 971 11545
L1	820 μH - 140 mA	TAIYO UDEN
L2	3.1 mH - CE167v	8228 001 32541
Q1, Q2	PHU2N60E/PHU2N50E	9340 555 65127
IC1	UBA2021T - S014	9352 112 50112

3.3 Demonstration board PR39001 (leaded version)

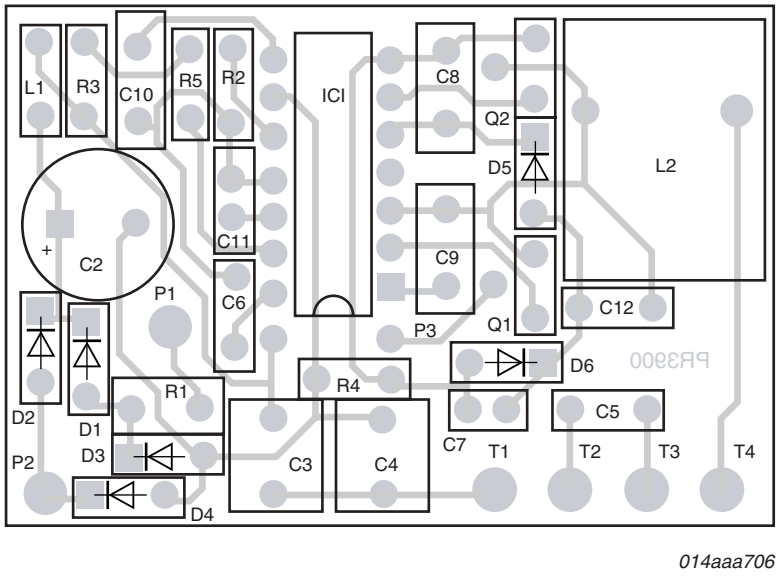


Fig 4. PR39001 component layout

Remark: The actual size of the PR39001 PCB; Leaded version is 34 mm × 50 mm.

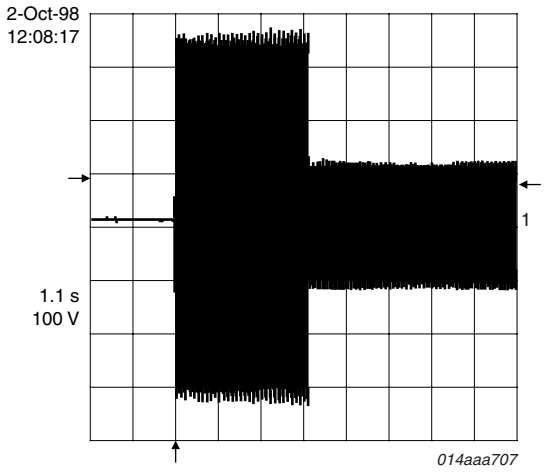
3.3.1 Component parts list PR39001 (Leaded version)

Table 2. Component parts list

Component	Value/type	12NC NXP order number
R1	47 Ω - PR02	2322 194 13479
R2	27 kΩ - SFR25	2322 181 43273
R3, R5	200 kΩ - SFR25	2322 181 43204
R4	1.3 Ω - SFR25	2322 181 43138
D1, D2, D3, D4	BYD12M	9340 552 67143
D5, D6	1N4531	9332 039 80113
C2	3.3 μF/400 V - RLH151	2222 151 56338
C3, C4	100 nF/250 V - MKP465	2222 465 90001
C5	3.9 nF/400 V - MKP370	2222 370 90149
C6	47 nF/100 V - MKT370	2222 370 21473
C7	680 pF/100 V - C630	2222 630 02681
C8, C9, C100	100 nF/63 V - MKT370	2222 370 75104
C11	150 pF/100 V - C631	2222 631 34151
C12	470 pF/500 V - C655	2222 655 03471
L1	820 μH - 140 mA	TAIYO UDEN
L2	3.1 mH - CE167v	8228 001 32541
Q1, Q2	PHU2N60E/PHU2N50E	9340 555 65127
IC1	UBA2021 - DIP14	9352 634 34112

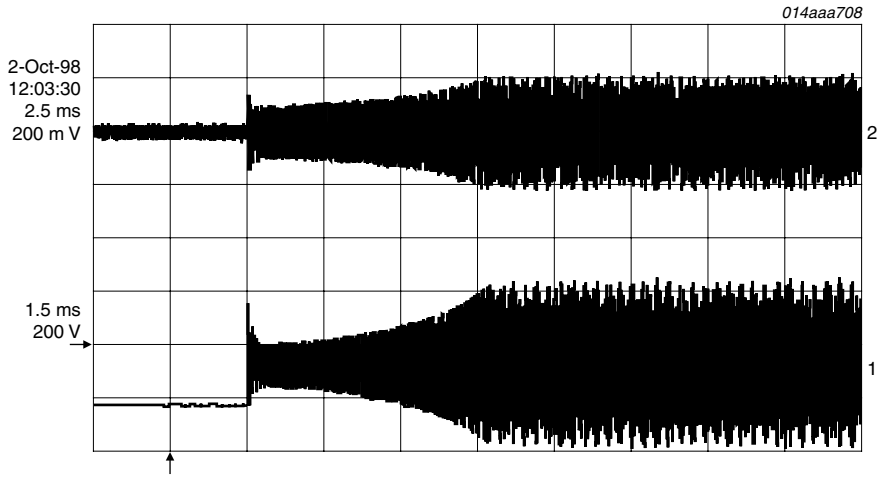
4. Performance

4.1 Oscillograms



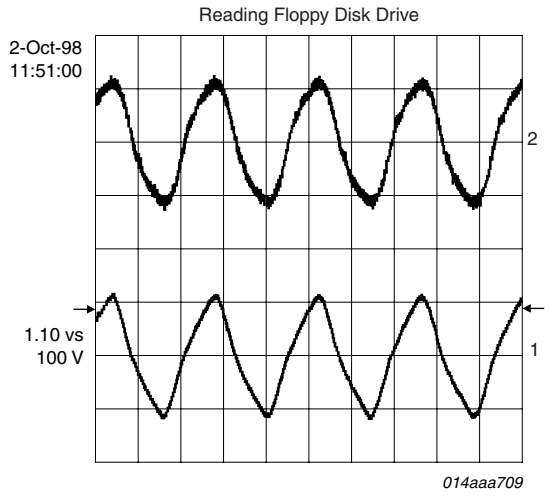
(1) CH1 lamp voltage: 100 V/div; time base: 100 ms/div

Fig 5. Preheat (± 300 ms), ignition (not visible) and burn phase



(1) CH1 lamp voltage: 200 V/div and CH2 electrode current: 500 mA/div; time base: 0.5 ms/div

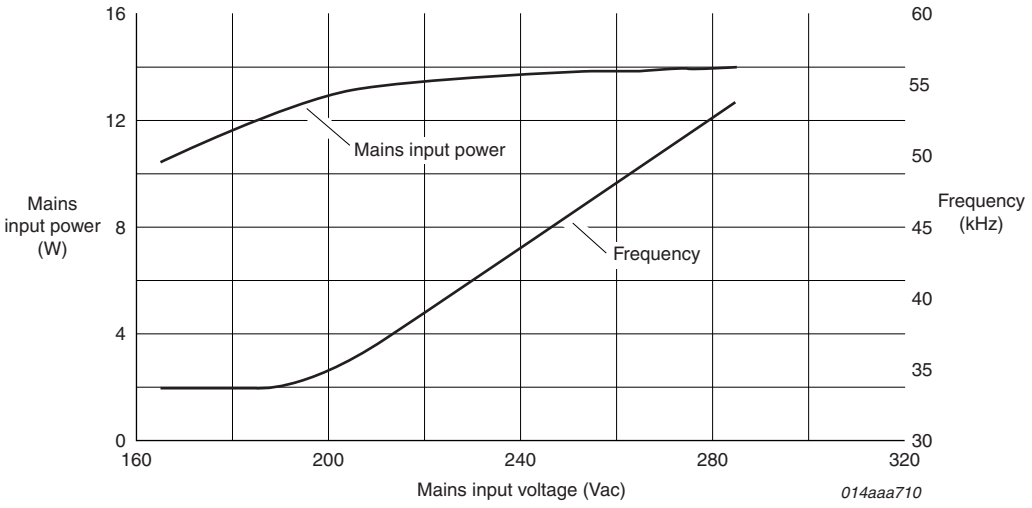
Fig 6. From start-up to controlled preheat within 1.5 ms



(1) CH1 lamp voltage: 100 V/div and CH2 lamp current: 200 mA/div; time base: 10 ms/div

Fig 7. Burn phase: lamp voltage 75 V and lamp current 170 mA

4.2 Impact of the feed-forward frequency



(1) Input voltage increase → feed-forward frequency increase → constant input/output power

Fig 8. Impact of feed-forward frequency: input power versus input voltage

4.3 EMI measurement

The mains terminal disturbance (conducted EMI) of the 13 W CFL circuit was measured according procedure 96EMC3005.1 "Conducted emission with an Artificial Mains Network". All measured values are average voltages in dBμV. As a comparison the CISPR15 average limit is given too.

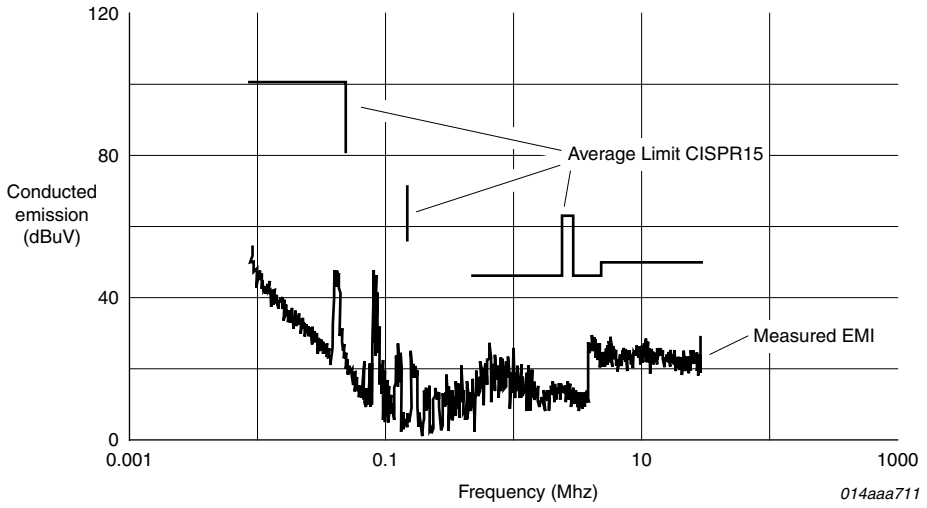
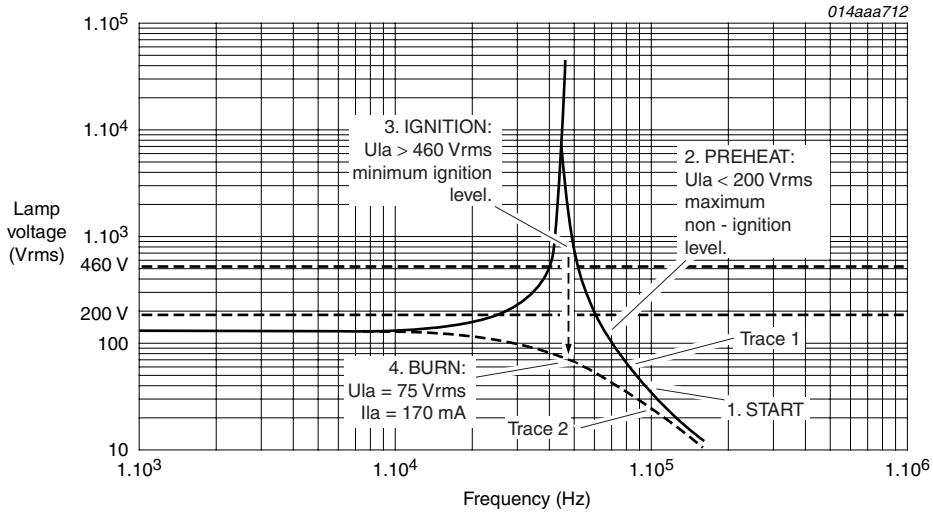


Fig 9. Conducted EMI

5. Appendix 1: CFL 13 W - LC and LCR curves

The MathCad software program was used to calculate and optimize the CFL 13 W circuit dimensioning. The lamp coil (L2) and igniter capacitor (C5) were calculated according these LC (trace 1: start, preheat, ignition phase) and LCR curves (trace 2: burn phase), at given phase boundaries and lamp operation point.



(1) Horizontal: frequency in Hz; vertical: lamp voltage in volts

Fig 10. CFL 13 W LC and LCR curves

UBA2021 sweep through the phases 1, 2, 3 and 4 via trace 1 and trace 2:

1. Start phase: f_{start} is 90 kHz.
2. Preheat phase: controlled; lamp voltage (Ula) < non-ignition level of the lamp (< 200 V (RMS)); $f_{preheat}$ is 65 kHz.
3. Ignition phase: lamp voltage (Ula) > minimum ignition level of the lamp (> 460 V (RMS)); $f_{ignition}$ is approximately 50 kHz → after strike-through of the lamp: transition from LC to LCR curve (dashed arrow: trace 1 to trace 2).
4. Burn phase: lamp operation point set (75 V/170 mA); f_{burn} is 43 kHz (feed-forward active).

6. Appendix 2: UBA2021 additional circuits for additional performance

6.1 Circuit 1: Protection with latch to prevent the power circuit against lamp removal and/or broken lamp (non ignition)

An extra protection circuit with latch, formed by Rs, D, R1, C1, R2, T1 and T2, can be added to any standard UBA2021 application, see Figure 11. In this way a protection against lamp removal and/or broken lamp is implemented.

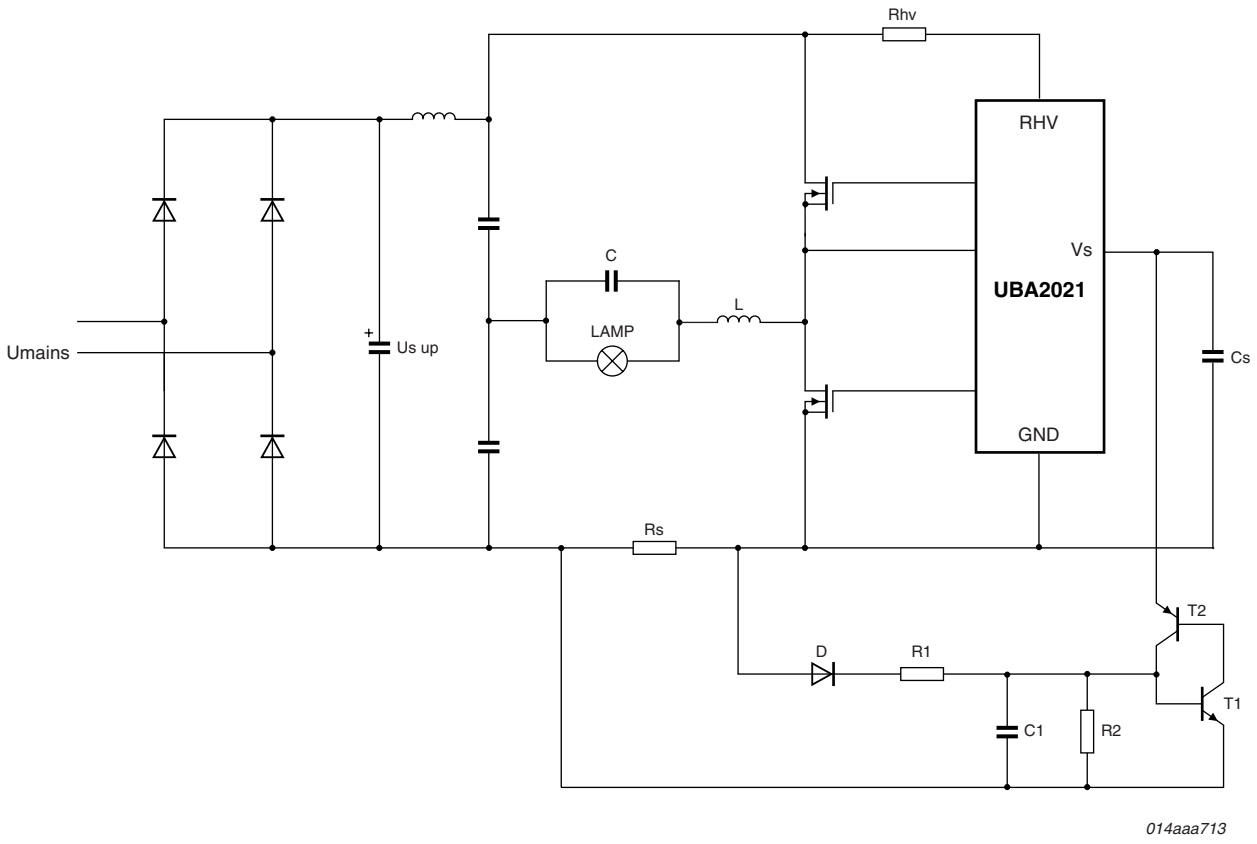


Fig 11. Protection circuit with latch

When the current through the sense resistor Rs becomes too high, due to a lamp removal and or a broken lamp, the voltage across C1 will increase and set T1 conducting. The diode D takes care that only single-sided current info is used to trigger. R1, R2 and C1 form a low pass filter to prevent against triggering during the ignition state and to build in some adjustable trigger sensitivity.

As soon as T1 is set conducting, also transistor T2 becomes conducting. The effect is that the supply capacitor Cs will be discharged through T2 and T1 and the supply voltage drops. When the supply voltage is lower than the stop-of-oscillation level (approximately 10 V), the UBA2021 circuit stops oscillating. This means that the current through the sense resistor Rs becomes zero and it can not keep T1 conducting anymore. However, T2 now keeps T1 in conduction (T1 and T2 form a discrete latch circuit) and the voltage across the supply capacitor Cs is kept low enough to keep the circuit non-oscillating. The latch current is provided via Rhv, the UBA2021 internal start-up path and Vs. The only way to start the circuit again, after turning in a correct lamp, is removing the mains voltage. So a simple turn Off/On of the mains voltage will restart the lamp.

6.1.1 Circuit 1 dimensioning (only additional part)

- T1 has to be kept conductive during lamp removal or broken lamp. This means that the latch current through Rhv.

$$Irhv = \frac{Usupmin}{Rhv} \quad (1)$$

Must be larger than:

$$Irhv \geq \frac{0.7V}{R2} \quad (2)$$

In formula this is:

$$R2 \geq Rhv \times \left(\frac{0.7}{Usupmin}\right) \quad (3)$$

- R1 can be used to set the exact trigger DC-level. Together with R2 they form a divider for DC. Also R1 forms a low pass filter in combination with R2 and C1, to make the circuit less sensitive for transients and during ignition. This implies that the time constant formed by the parallel resistance R1//R2 and capacitor C1 has to be large enough to prevent unwanted triggering. With R2 already fixed both R1 and C1 can be calculated easily.

6.2 CIRCUIT 2: Voltage doubler circuit and UBA2021 for 100 V (AC)/120 V (AC) mains

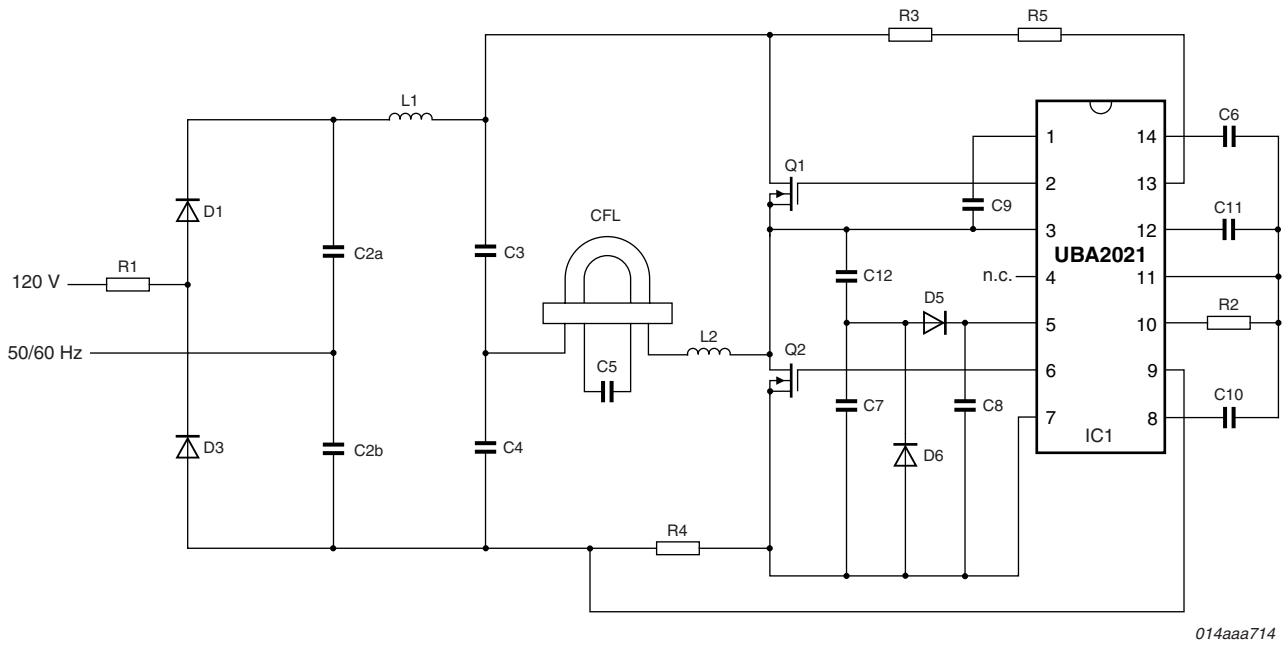


Fig 12. Voltage doubler for 100 V (AC)/120 V (AC) mains

The circuit is a derivative of the 230 V version, described in the main part of this application note (see Figure 2. The complete half-bridge section is a copy of this 230 V version, only the input circuit (formed by R1, D1, D3, C2a en C2b) differs. In this 100 V/120 V version, the input circuit is used as a voltage doubler circuit. In comparison to the 230 V version, C2a and C2b are twice the capacitance value of the original C2, but

half the voltage rating (in the original circuit C2 is 3.3 μF/400 V, here C2a and C2b are 6.8 μF/200 V). The fusible resistor R1 is reduced from 47 Ω (PR02 type) to 22 Ω (PR02 type). All other components are of the same value.

With this approach the impact on the total cost of ownership is major (decrease of total cost of ownership) when manufacturing both the 230 V and 100 V/120 V versions.

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