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Report nr. : RNR-T45-96-B-773
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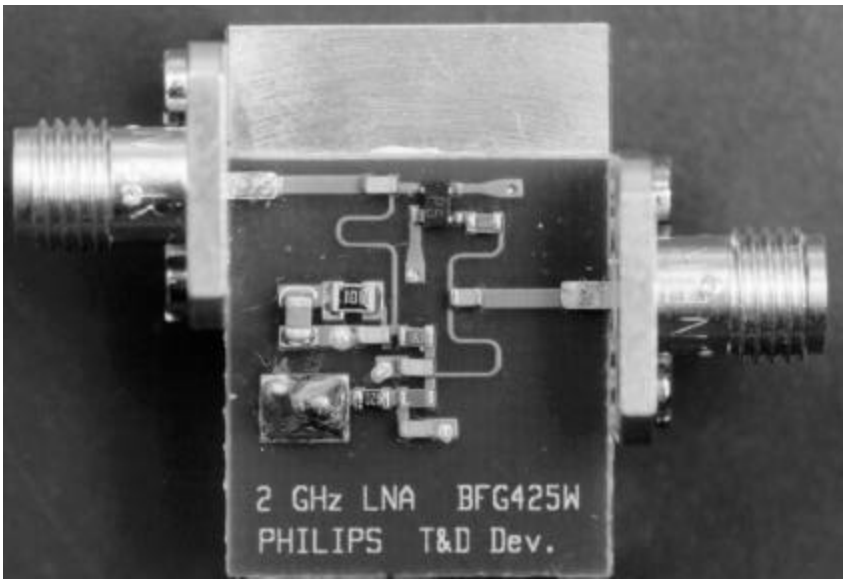
Date : 14-Nov-1996

2GHz LOW NOISE AMPLIFIER WITH THE BFG425W



Abstract:
This application note contains an example of a Low Noise Amplifier with the new BFG425W Double Poly RF-transistor. The LNA is designed for a frequency f=2GHz. At 2GHz: Gain~16dB@5mA,
NF~1.8dB@5mA,
$IP3_{input}$~2dBm@5mA.

Appendix I: Schematic of the circuit
Appendix II: Used components & materials
Appendix III: Simulation LNA-PCB
Appendix IV: Measurements LNA-PCB

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Introduction:
With the new Philips silicon bipolar double poly BFG400W series, it is possible to design low noise amplifiers for high frequency applications with a low current and a low supply voltage. These amplifiers are well suited for the new generation low voltage high frequency wireless applications. In this note a first study of such an amplifier will be given. This amplifier is designed for a working frequency of 2GHz.

Designing the circuit:
The circuit is designed to show the following performance:

transistor: BFG425W

V_{ce}=2V, I_c=2...10mA, V_{SUP}<5V
freq=2GHz
Gain~16dB@5mA
NF~1.8dB@5mA
$IP3_{input}$~2dBm@5mA
VSWRi<1:2
VSWRo<1:2

In the simulations the effect of extra RF-noise caused by the SMA-connectors was omitted, so in the practical situation the NF is ~0.1dB higher. This LNA is not optimised for the highest IP3 and Noise Figure. The IP3 can be optimised by:

I. an extra series RC-decoupling of the base to the ground
II. increasing I_C

With the solution I. two extra components are necessary, and with solution II, the Noise Figure of the LNA increases and the optimum source impedance also.

The in- and outputmatching is realised with a LC-combination. Also extra emitter-inductance on both emitter-leads (µ-strips) are used to improve the matching and the Noise Figure.

Designing the layout:
A lay-out has been designed with HP-MDS. Appendix II contains the printlayout.

Simulations:
Appendix III contains HP-MDS simulations of the LNA.

Measurements:
Appendix IV contains measurement-results of the LNA.

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Appendix I: Schematic of the circuit

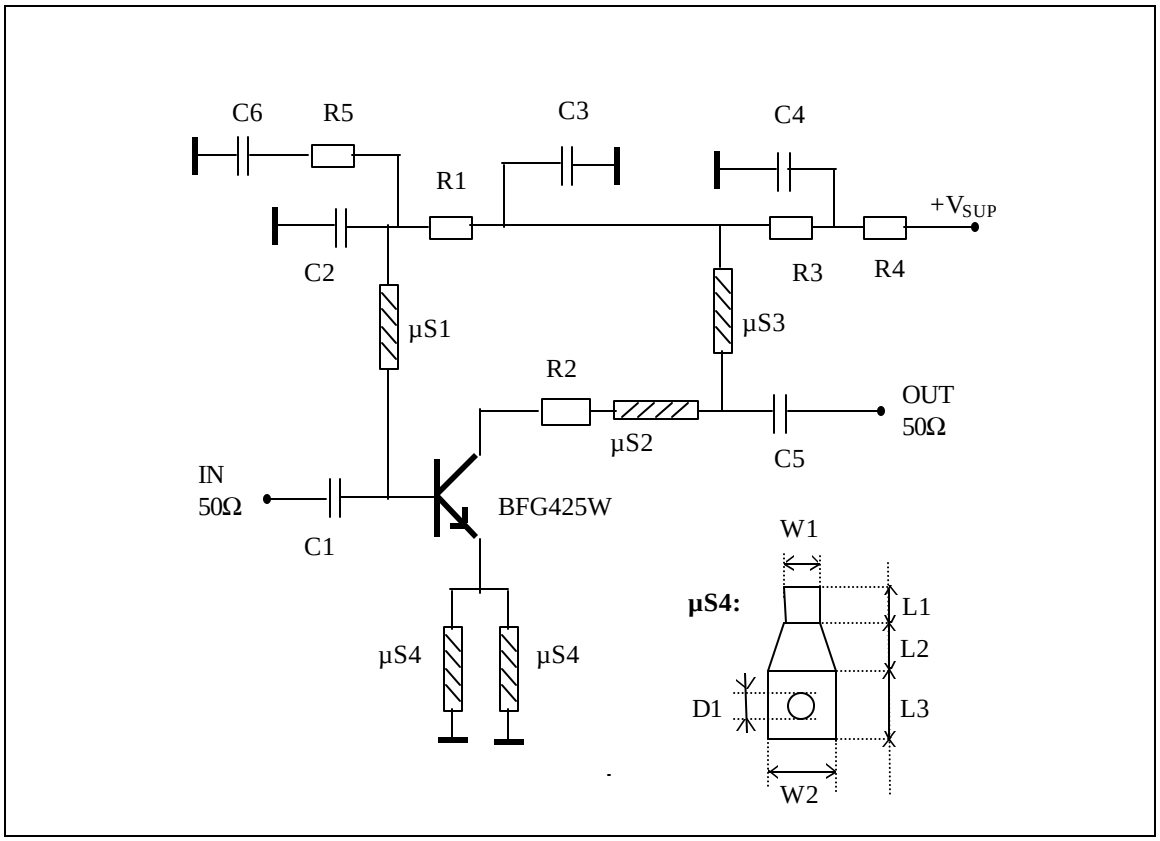

Figure 1: LNA circuit

2 GHz LNA Component list:

Component:	Value:	Comment:
R1	15 KΩ	Bias.
R2	0 Ω	Omitted.
R3	22 Ω	RF-block.
R4	82 Ω	Cancelling H_{FE}-spread.
R5	100 Ω	To improve IP3-performance
C1	4.7 pF	Input match.
C2	5.6 pF	2GHz short.
C3	5.6 pF	2GHz short.
C4	1 nF	RF-short
C5	2.7 pF	Output match.
C6	100 nH	To improve IP3-performance
µs1	8.9 x 0.25mm	µ-stripline Z_0~95Ω (PCB: ε_r ~4.6, H=0.5mm)
µs2	3.9 x 0.25mm	µ-stripline Z_0~95Ω (PCB: ε_r ~4.6, H=0.5mm)
µs3	6.6 x 0.25mm	µ-stripline Z_0~95Ω (PCB: ε_r ~4.6, H=0.5mm)
µs4	(next table)	Emitter induction: µ-stripline + via

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µS4 Emitter induction (µ-stripline + via):

Name	Dimension	Description
L1	1.0mm	length µ-stripline; Z_0~48Ω (PCB: ε_r ~4.6, H=0.5mm)
L2	1.0mm	length interconnect stripline and via-hole area
L3	1.0mm	length via-hole area
W1	0.5mm	width µ-stripline
W2	1.0mm	width via-hole area
D1	0.4mm	diameter of via-hole

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Appendix II: Used components & materials

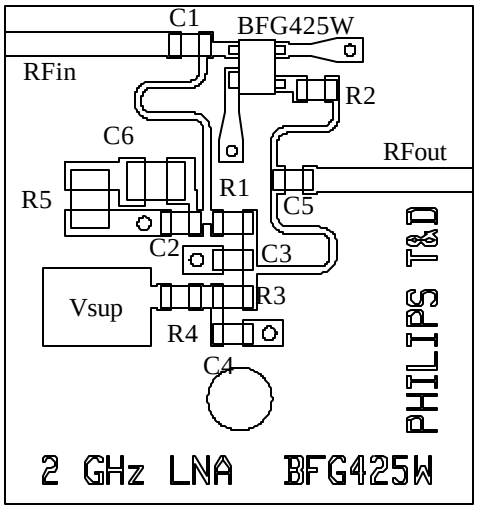

Figure 2: Printlayout

2GHz LNA Component list:

Component:	Value:	size:
R1	15 KΩ	0603 Philips
R2	0 Ω	0603 Philips
R3	22 Ω	0603 Philips
R4	82 Ω	0603 Philips
R5	100 Ω	**0805** Philips
C1	4.7 pF	0603 Philips
C2	5.6 pF	0603 Philips
C3	5.6 pF	0603 Philips
C4	1 nF	0603 Philips
C5	2.7 pF	0603 Philips
C6	100 nF	**0805** Philips
PCB	ε_r ~4.6, H=0.5mm	FR4

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Appendix III: Simulation LNA-PCB

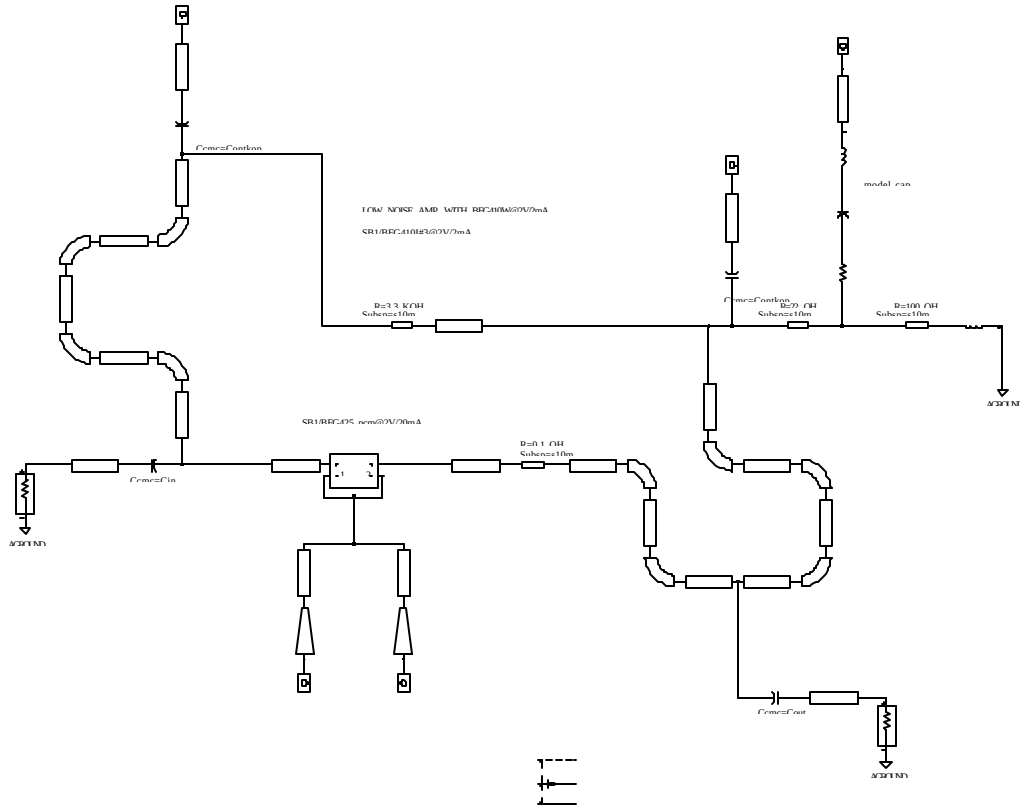

Figure 3: HP-MDS simulation circuit (Spice model and S_par 2-port model)

Results Simulations: f=2GHz

	SPICE MODEL	SPICE MODEL	SPICE MODEL		S_PAR MODEL	S_PAR MODEL
I_C [mA]	$\|S_{21}\|^2$ [dB]	IP3_B [dBm]	NF [dB]			NF [dB]
		input, Δf= 100KHz	note 1.			note 1.
2	14.3	-1.3	1.7		14.3	1.5
3	15.0	+0.6	1.7			
5	15.6	+3.8	1.9			
6	15.8	+6.1	2.0			
8	16.1	+7.1	2.2			
10	16.3	+8.5	2.4		16.3	2.0

note 1: There is a difference in Noise Figure between the Spice model and de S_par 2-port model. The latter uses measured S- and Noise-parameters.The difference in Noise Figure between both models can be explained by the fact that the Spice model is not extracted for Noise.

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Appendix IV: Measurements LNA-PCB

Results Measurements: f=2GHz

I_C [mA]	$\|S_{21}\|^2$ [dB]	IP3_A [dBm]	IP3_B [dBm]	NF [dB]
V_{CE} ~ 2.5V		input, Δf= 100KHz	input, Δf= 100KHz	
		note 1.	note 1.	
2	14.4	-10.9	-2.3	1.5
3	15.9	-3.4	-0.4	1.7
5	16.3	-0.9	1.8	1.8
6	16.6	1.0	2.6	1.9
8	16.9	3.9	5.6	2.1
10	17.1	6.5	6.7	2.3

note 1: IP3_A: IP3 without LF-decoupling at base
IP3_B: IP3 with LF-decoupling (R5 and C6) at base

At low currents, the IP3 can be improved by using a low frequency decouple network at the base of the bipolar transistor (figure 1: R5 and C6). The improvement with the IP3 optimising circuit is 8dBm at low current (I_C=3mA). As the current is increased, the effect of IP3 improvement decreases.