

74LVC2G00

Dual 2-input NAND gate

Rev. 10 — 30 November 2011

Product data sheet

1. General description

The 74LVC2G00 provides a 2-input NAND gate function.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant outputs for interfacing with 5 V logic
- High noise immunity
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V)
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C



3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC2G00DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G00DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G00GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC2G00GF	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	SOT1089
74LVC2G00GD	-40 °C to +125 °C	XSON8U	plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 × 2 × 0.5 mm	SOT996-2
74LVC2G00GM	-40 °C to +125 °C	XQFN8U	plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 × 1.6 × 0.5 mm	SOT902-1
74LVC2G00GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	SOT1116
74LVC2G00GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203

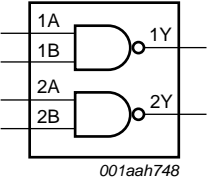
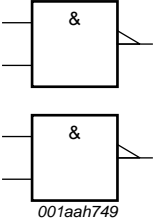
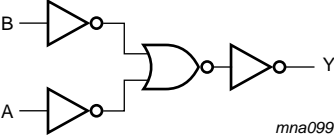
4. Marking

Table 2. Marking codes

Type number	Marking code ^[1]
74LVC2G00DP	V2G00
74LVC2G00DC	V00
74LVC2G00GT	V00
74LVC2G00GF	VA
74LVC2G00GD	V00
74LVC2G00GM	V00
74LVC2G00GN	VA
74LVC2G00GS	VA

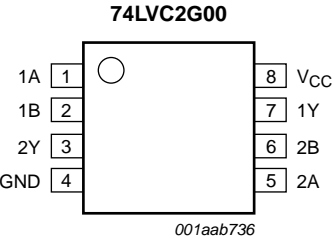
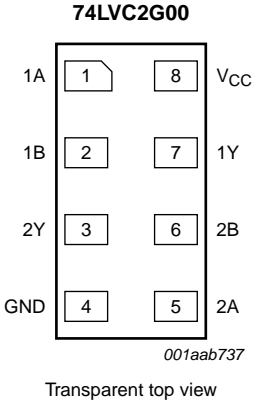
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

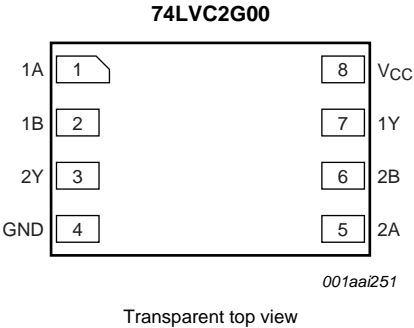
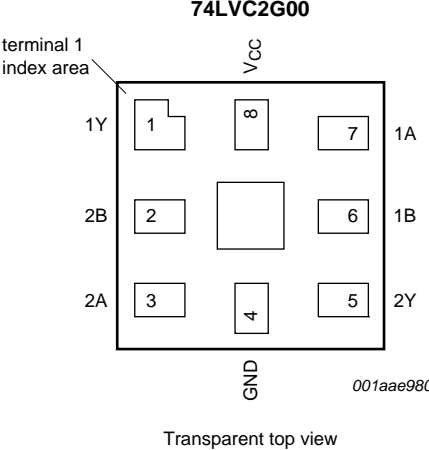
5. Functional diagram

 <p>001aah748</p>	 <p>001aah749</p>	 <p>mna099</p>
<p>Fig 1. Logic symbol</p>	<p>Fig 2. IEC logic symbol</p>	<p>Fig 3. Logic diagram (one gate)</p>

6. Pinning information

6.1 Pinning

 <p>001aab736</p>	 <p>001aab737</p> <p>Transparent top view</p>
<p>Fig 4. Pin configuration SOT505-2 and SOT765-1</p>	<p>Fig 5. Pin configuration SOT833-1, SOT1089, SOT1116 and SOT1203</p>

 <p>001aaiz51</p> <p>Transparent top view</p>	 <p>001aae980</p> <p>Transparent top view</p>
<p>Fig 6. Pin configuration SOT996-2</p>	<p>Fig 7. Pin configuration SOT902-1</p>

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT505-2, SOT765-1, SOT833-1, SOT1089, SOT996-2, SOT1116 and SOT1203	SOT902-1	
1A, 2A	1, 5	7, 3	data input
1B, 2B	2, 6	6, 2	data input
GND	4	4	ground (0 V)
1Y, 2Y	7, 3	1, 5	data output
V _{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table^[1]

Input		Output
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
V _I	input voltage		^[1] -0.5	+6.5	V
V _O	output voltage	Active mode	^[1] -0.5	V _{CC} + 0.5	V
		Power-down mode	^{[1][2]} -0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V or V _O > V _{CC}	-	±50	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	^[3] -	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

For XSON8, XSON8U and XQFN8U packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}$ [1]						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = -100\ \mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA}; V_{CC} = 1.65\text{ V}$	1.2	1.53	-	V
		$I_O = -8\text{ mA}; V_{CC} = 2.3\text{ V}$	1.9	2.13	-	V
		$I_O = -12\text{ mA}; V_{CC} = 2.7\text{ V}$	2.2	2.50	-	V
		$I_O = -24\text{ mA}; V_{CC} = 3.0\text{ V}$	2.3	2.60	-	V
		$I_O = -32\text{ mA}; V_{CC} = 4.5\text{ V}$	3.8	4.10	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = 100\ \mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 1.65\text{ V}$	-	0.08	0.45	V
		$I_O = 8\text{ mA}; V_{CC} = 2.3\text{ V}$	-	0.14	0.3	V
		$I_O = 12\text{ mA}; V_{CC} = 2.7\text{ V}$	-	0.19	0.4	V
		$I_O = 24\text{ mA}; V_{CC} = 3.0\text{ V}$	-	0.37	0.55	V
		$I_O = 32\text{ mA}; V_{CC} = 4.5\text{ V}$	-	0.43	0.55	V
I_I	input leakage current	$V_I = 5.5\text{ V or GND}; V_{CC} = 0\text{ V to }5.5\text{ V}$	-	± 0.1	± 5	μA
I_{OFF}	power-off leakage current	$V_I\text{ or }V_O = 5.5\text{ V}; V_{CC} = 0\text{ V}$	-	± 0.1	± 10	μA

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	$V_I = 5.5$ V or GND; $V_{CC} = 1.65$ V to 5.5 V; $I_O = 0$ A	-	0.1	10	μ A
ΔI_{CC}	additional supply current	per pin; $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 2.3$ V to 5.5 V	-	5	500	μ A
C_I	input capacitance		-	2.5	-	pF
$T_{amb} = -40$ °C to $+125$ °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
		$V_{CC} = 4.5$ V to 5.5 V	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	$0.3 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100$ μ A; $V_{CC} = 1.65$ V to 5.5 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -4$ mA; $V_{CC} = 1.65$ V	0.95	-	-	V
		$I_O = -8$ mA; $V_{CC} = 2.3$ V	1.7	-	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	1.9	-	-	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V	2.0	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100$ μ A; $V_{CC} = 1.65$ V to 5.5 V	-	-	0.1	V
		$I_O = 4$ mA; $V_{CC} = 1.65$ V	-	-	0.70	V
		$I_O = 8$ mA; $V_{CC} = 2.3$ V	-	-	0.45	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	-	0.60	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V	-	-	0.80	V
I_I	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 0$ V to 5.5 V	-	-	± 20	μ A
		V_I or $V_O = 5.5$ V; $V_{CC} = 0$ V	-	-	± 20	μ A
I_{OFF}	power-off leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 1.65$ V to 5.5 V; $I_O = 0$ A	-	-	40	μ A
ΔI_{CC}	additional supply current	per pin; $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 2.3$ V to 5.5 V	-	-	5000	μ A

[1] All typical values are measured at $T_{amb} = 25$ °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground 0 V); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nA, nB to nY; see Figure 8 ^[2]						
		V _{CC} = 1.65 V to 1.95 V	1.2	3.5	8.6	1.2	10.8	ns
		V _{CC} = 2.3 V to 2.7 V	0.7	2.3	4.8	0.7	6.0	ns
		V _{CC} = 2.7 V	0.7	3.0	5.6	0.7	7.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.7	2.2	4.3	0.7	5.4	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.8	3.3	0.5	4.2	ns
C _{PD}	power dissipation capacitance	per gate; V _I = GND to V _{CC} ^[3]	-	14	-	-	-	pF

[1] Typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

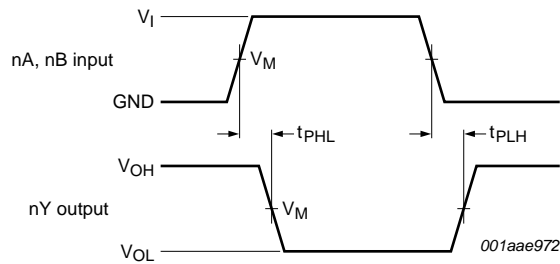
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

∑(C_L × V_{CC}² × f_o) = sum of outputs.

12. Waveforms



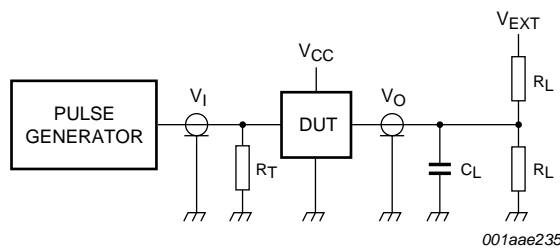
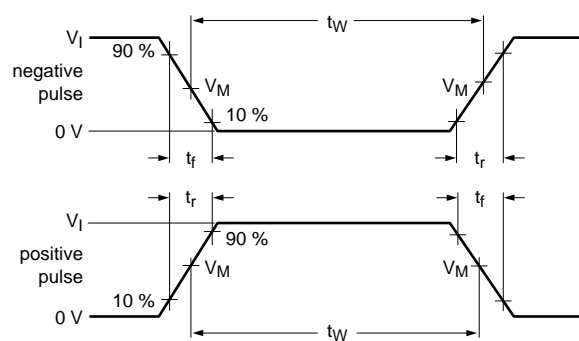
Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. Input (nA, nB) to output (nY) propagation delays

Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Fig 9. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load	V_{EXT}
V_{CC}	V_I	C_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	t_r, t_f	R_L
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF
2.7 V	2.7 V	≤ 2.0 ns	50 pF
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

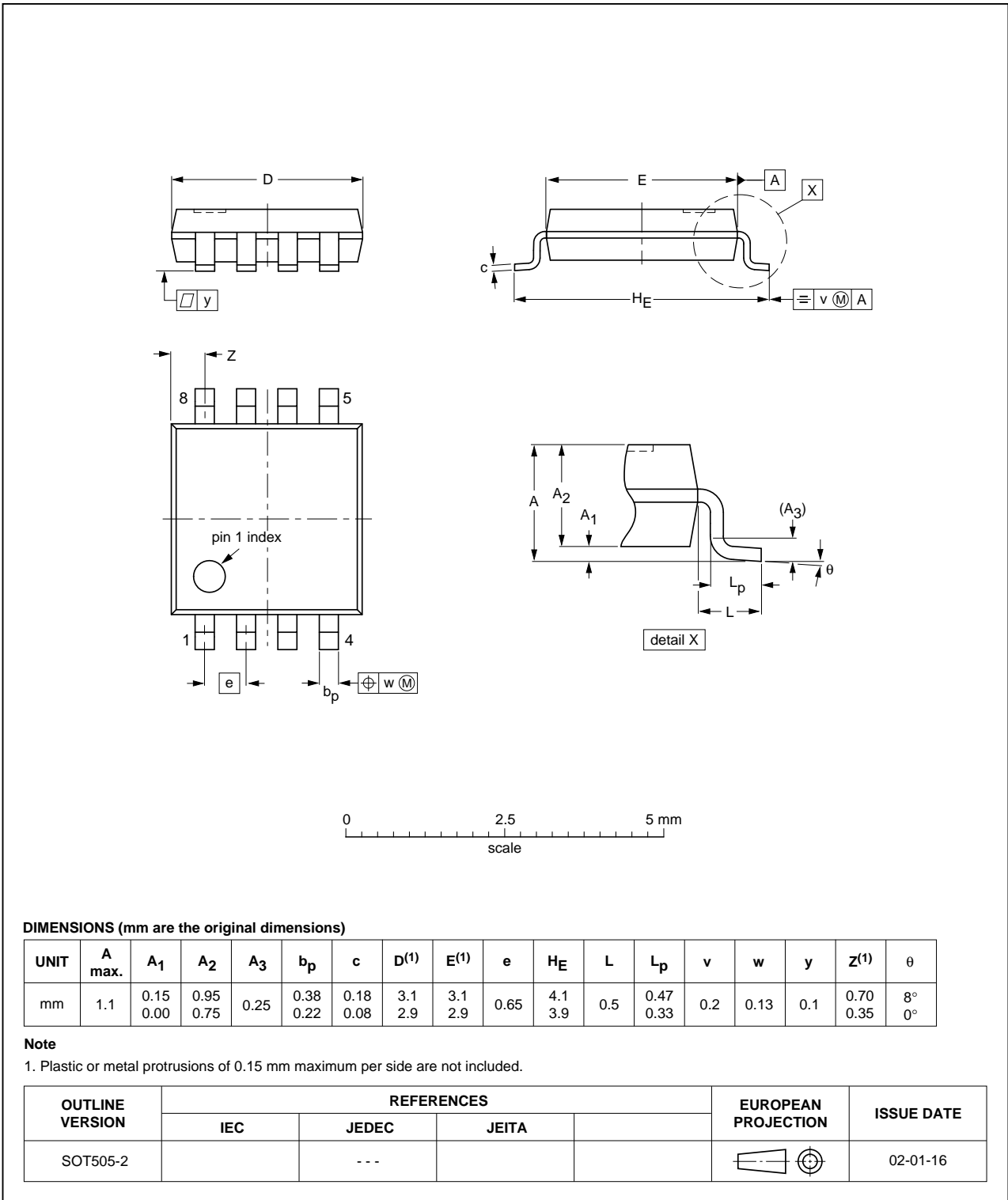


Fig 10. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

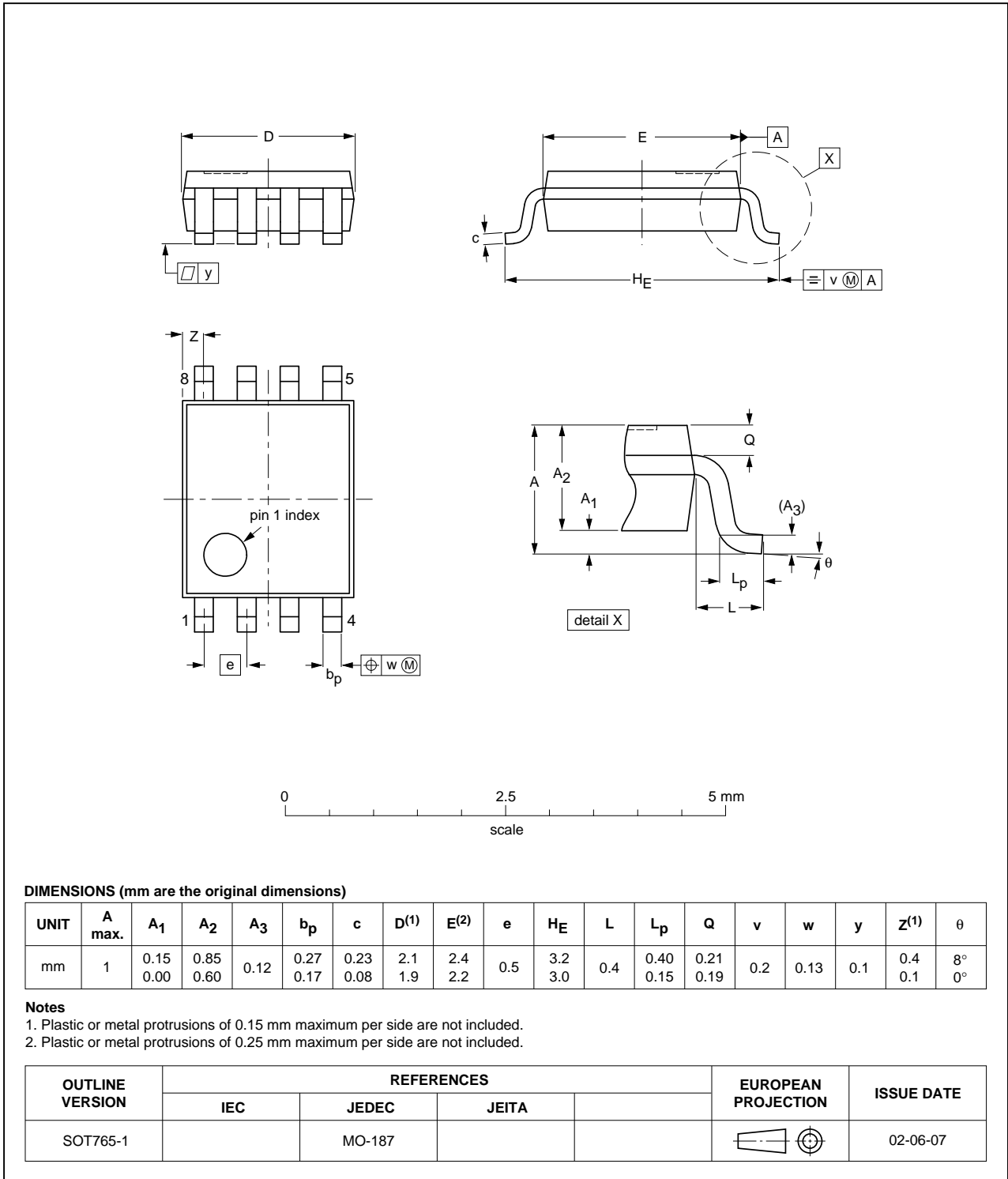


Fig 11. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

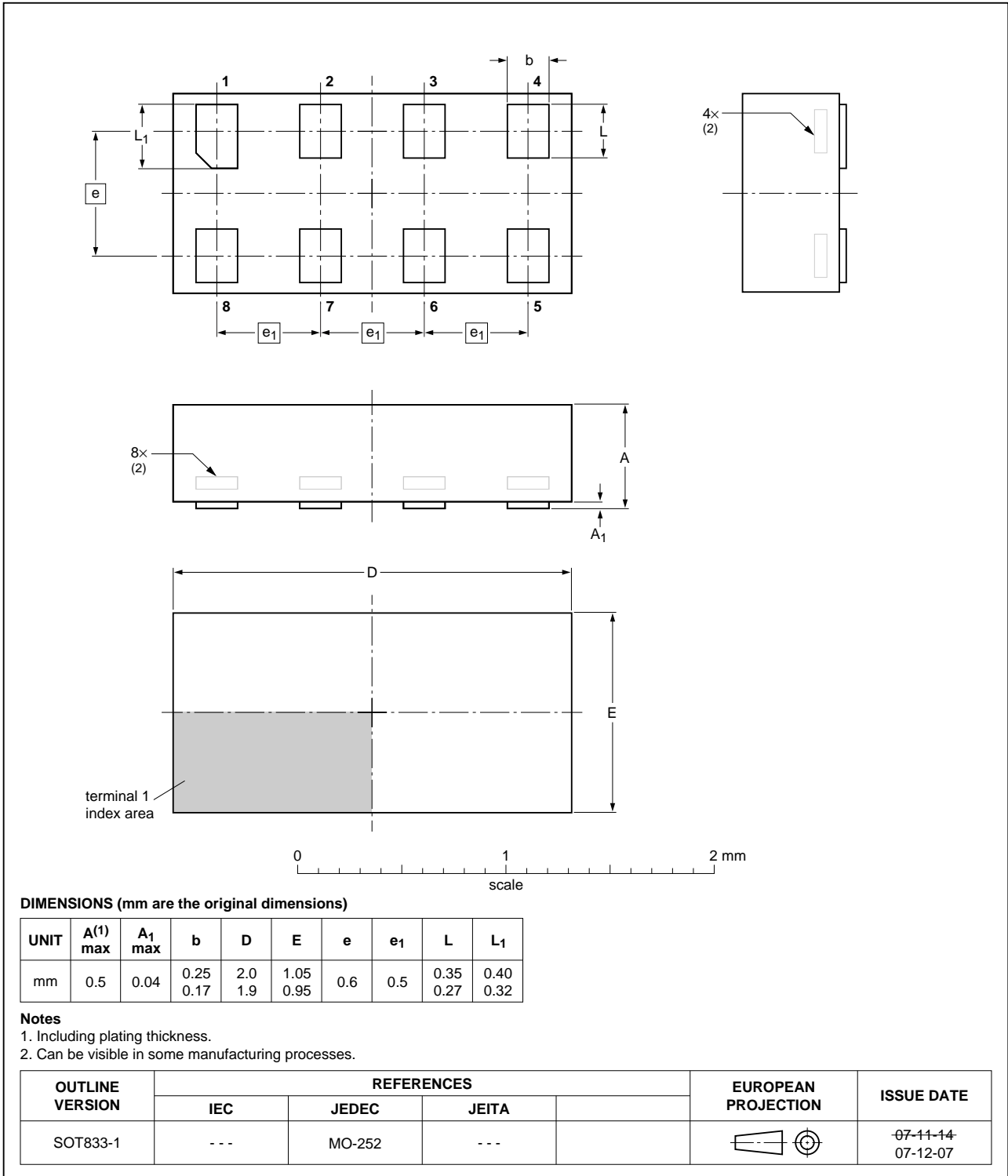


Fig 12. Package outline SOT833-1 (XSON8)

**XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1 x 0.5 mm**

SOT1089

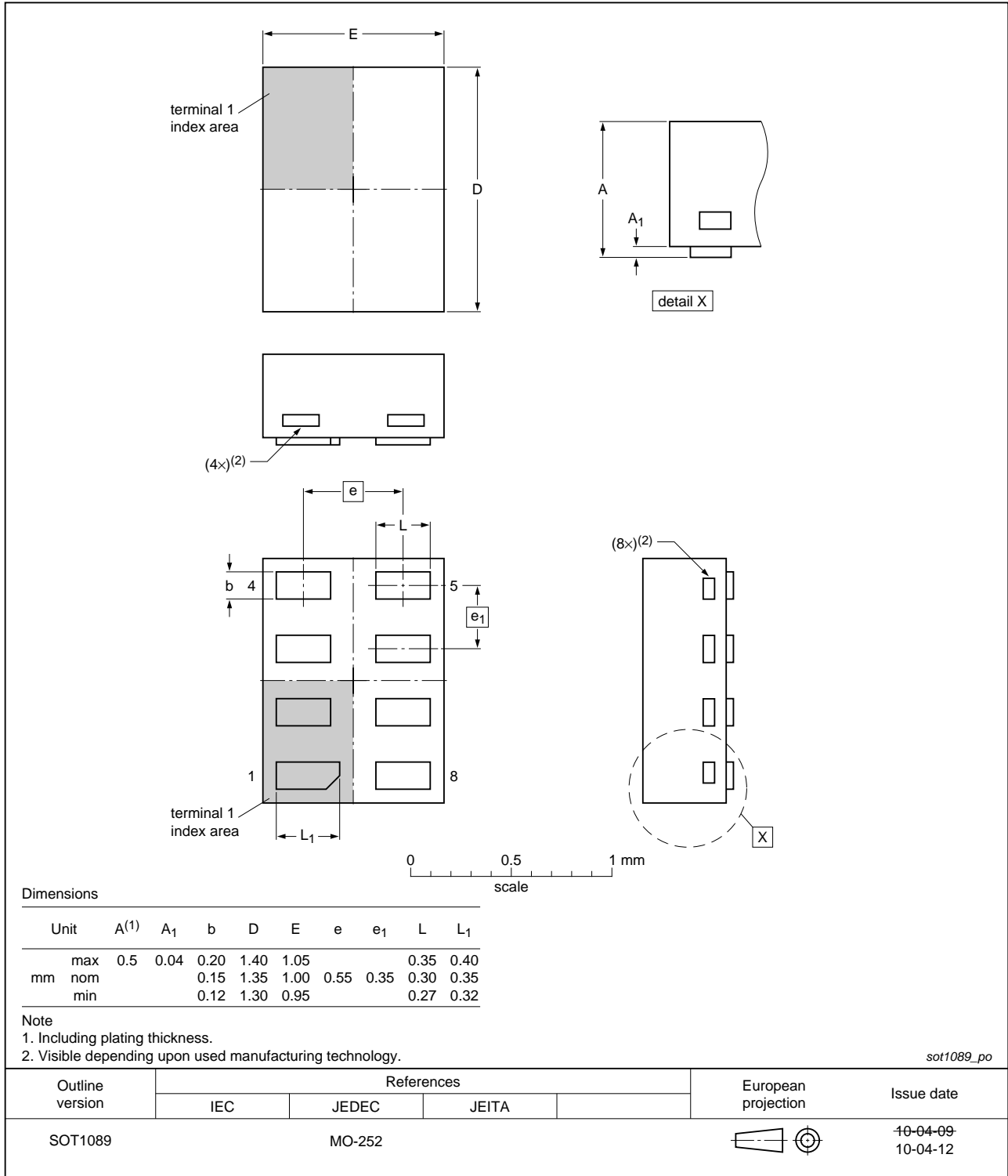


Fig 13. Package outline SOT1089 (XSON8)

XSON8U: plastic extremely thin small outline package; no leads;
8 terminals; UTLP based; body 3 x 2 x 0.5 mm

SOT996-2

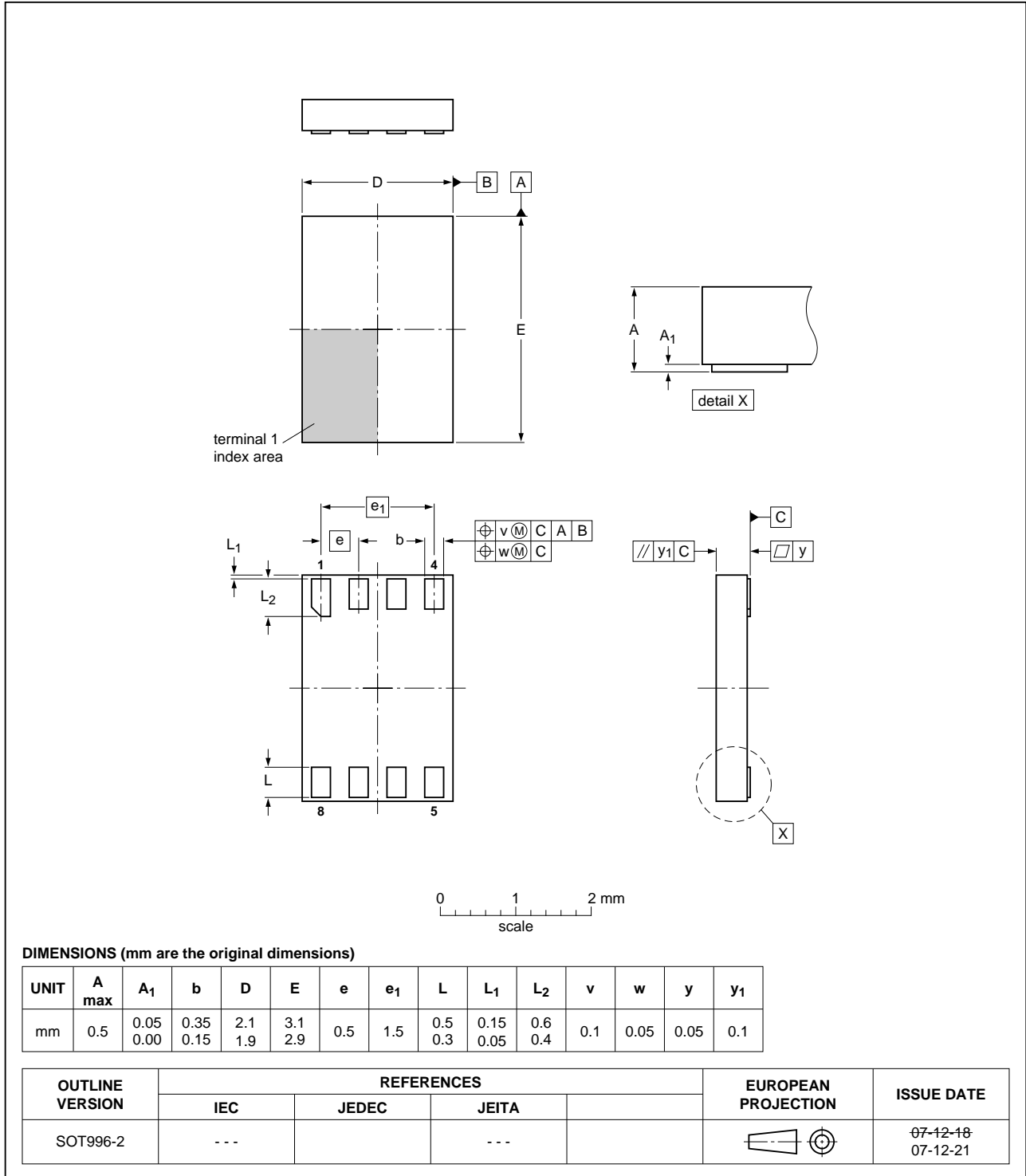


Fig 14. Package outline SOT996-2 (XSON8U)

XQFN8U: plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm

SOT902-1

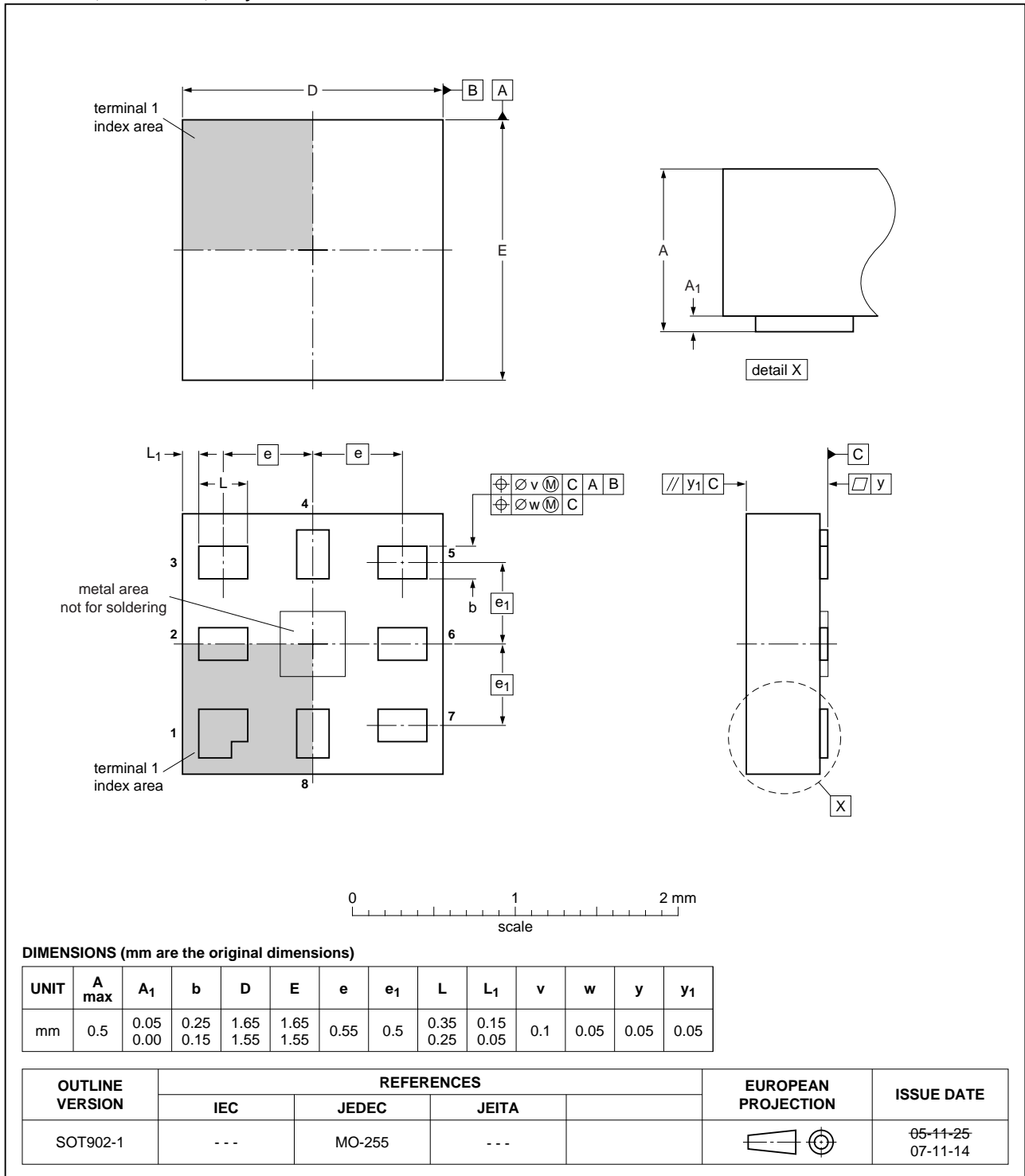


Fig 15. Package outline SOT902-1 (XQFN8U)

**XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.2 x 1.0 x 0.35 mm**

SOT1116

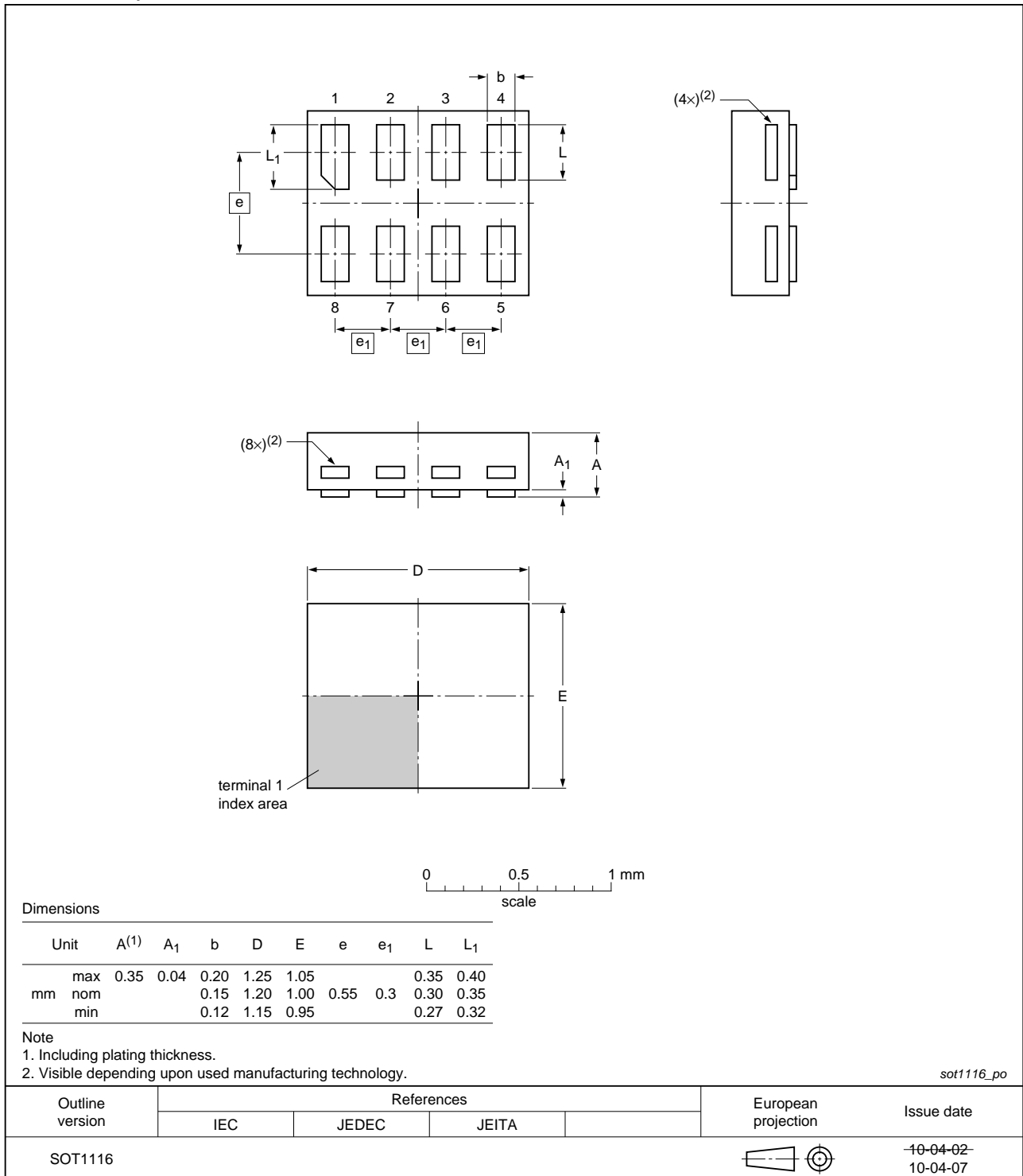


Fig 16. Package outline SOT1116 (XSON8)

**XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm**

SOT1203

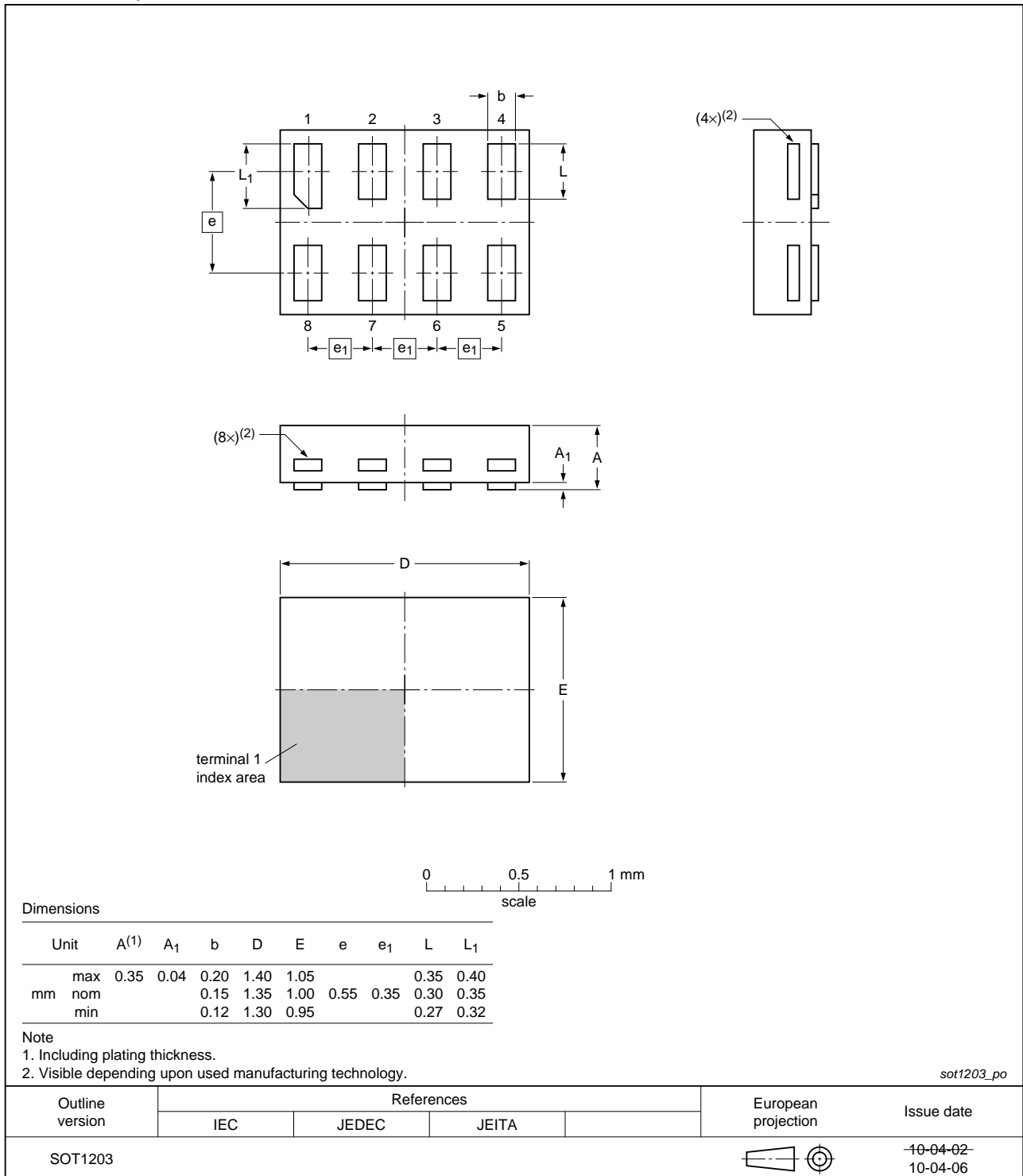


Fig 17. Package outline SOT1203 (XSON8)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G00 v.10	20111130	Product data sheet	-	74LVC2G00 v.9
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74LVC2G00 v.9	20100608	Product data sheet	-	74LVC2G00 v.8
74LVC2G00 v.8	20091026	Product data sheet	-	74LVC2G00 v.7
74LVC2G00 v.7	20080610	Product data sheet	-	74LVC2G00 v.6
74LVC2G00 v.6	20080220	Product data sheet	-	74LVC2G00 v.5
74LVC2G00 v.5	20070904	Product data sheet	-	74LVC2G00 v.4
74LVC2G00 v.4	20060515	Product data sheet	-	74LVC2G00 v.3
74LVC2G00 v.3	20050201	Product specification	-	74LVC2G00 v.2
74LVC2G00 v.2	20040923	Product specification	-	74LVC2G00 v.1
74LVC2G00 v.1	20031117	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Marking	2
5	Functional diagram	3
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	4
7	Functional description	4
8	Limiting values	4
9	Recommended operating conditions	5
10	Static characteristics	5
11	Dynamic characteristics	7
12	Waveforms	7
13	Package outline	9
14	Abbreviations	17
15	Revision history	17
16	Legal information	18
16.1	Data sheet status	18
16.2	Definitions	18
16.3	Disclaimers	18
16.4	Trademarks	19
17	Contact information	19
18	Contents	20

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 30 November 2011

Document identifier: 74LVC2G00