

ADC1443D series

Dual channel 14-bit ADC; 125, 160 or 200 Msps;
JESD204B-compliant CGVxpress serial outputs

Rev. 1 — 28 September 2011

Objective data sheet

1. General description

The ADC1443D is a dual channel 14-bit Analog-to-Digital Converter (ADC) with JESD204B-compliant CGVxpress interface optimized for high dynamic performance and low power consumption at sample rates up to 200 Msps. Pipelined architecture and output error correction ensure the ADC1443D is accurate enough to guarantee zero missing codes over the entire operating range.

Supplied from a single 1.8 V source, the ADC1443D has serial outputs compliant with the JESD204B standard over a configurable number of lanes (1 or 2). Multiple Device Synchronization (MDS) allows sample-accurate synchronization of the data outputs of multiple ADC devices. MDS, which is a unique feature of the CGV and CGVxpress technology of NXP Semiconductors, guarantees a maximum skew of one clock period between as many as 16 output lanes from up to eight ADC1443D devices.

An integrated Serial Peripheral Interface (SPI) allows easy configuration of the ADC. The device also includes a programmable full-scale to allow a flexible input voltage range of 1 V (p-p) to 2 V (p-p).

With excellent dynamic performance from the baseband to input frequencies of up to 250 MHz or more, the ADC1443D is ideal for use in undersampled multi-carrier, multi-standard communication system applications. Using a pipelined architecture, an output error correction scheme ensures the ADC1443D is accurate enough to guarantee zero missing codes over the entire operating range.

The ADC1443D200 is available in an HLQFN56 package (8 mm × 8 mm outline). It is supported with customer demo boards. This device is also available in a 12-bit resolution variant with a choice of maximum sampling frequency (125, 160 or 200 Msps).

2. Features and benefits

- Dual channel 14-bit resolution ADC
- Sampling rate up to 200 Msps
- JESD204B Device Subclass 0, 1 and 2 compliant with harmonic clocking and deterministic latency support
- ADC Multiple Device Synchronization (MDS), CGVxpress feature
- Single 1.8 V supply
- SNR = 72.5 dBFS (typical); $f_s = 185$ Msps; $f_i = 190$ MHz
- SFDR = 86 dBc (typical); $f_s = 185$ Msps; $f_i = 190$ MHz
- IMD3 = 88 dBc (typical); $f_s = 185$ Msps; $f_{i1} = 188.5$ MHz; $f_{i2} = 191.5$ MHz
- Analog input bandwidth of 1 GHz (typical)
- Typical power dissipation = 1.0 W; $f_s = 200$ Msps



- Two JESD204B serial output lanes, up to 5 Gsps typical
- Flexible input voltage range from 1 V (p-p) to 2 V (p-p) by 1 dB steps
- Clock input divider from 1 to 8 supports harmonic clocking
- Duty Cycle Stabilizer (DCS)
- Offset binary and two's complement output data
- Pin to pin compatible with ADC1413D series
- Power-down and sleep modes
- Industrial temperature range from -40 °C to +85 °C
- Serial Peripheral Interface (SPI) for configuration control and status monitoring
- HLQFN56 package; 8 mm × 8 mm

3. Applications

- Wireless infrastructure: LTE, TD-LTE, WiMAX, MC-GSM, CDMA, WCDMA, TD-SCDMA
- Software defined radio
- Medical non-invasive scanners
- Scientific particle detectors
- Microwave backhaul transceivers
- Aerospace and defense communications and radar systems
- Industrial signal analysis instruments
- General-purpose high-speed applications

4. Ordering information

Table 1. Ordering information

Type number	f _s (Msps)	Package		
		Name	Description	Version
ADC1443D200HD	200	HLQFN56	plastic thermal enhanced low profile quad flat package; no leads; 56 terminals; resin based; body 8 × 8 × 1.35 mm	SOT935-2
ADC1443D160HD	160	HLQFN56	plastic thermal enhanced low profile quad flat package; no leads; 56 terminals; resin based; body 8 × 8 × 1.35 mm	SOT935-2
ADC1443D125HD	125	HLQFN56	plastic thermal enhanced low profile quad flat package; no leads; 56 terminals; resin based; body 8 × 8 × 1.35 mm	SOT935-2

5. Block diagram

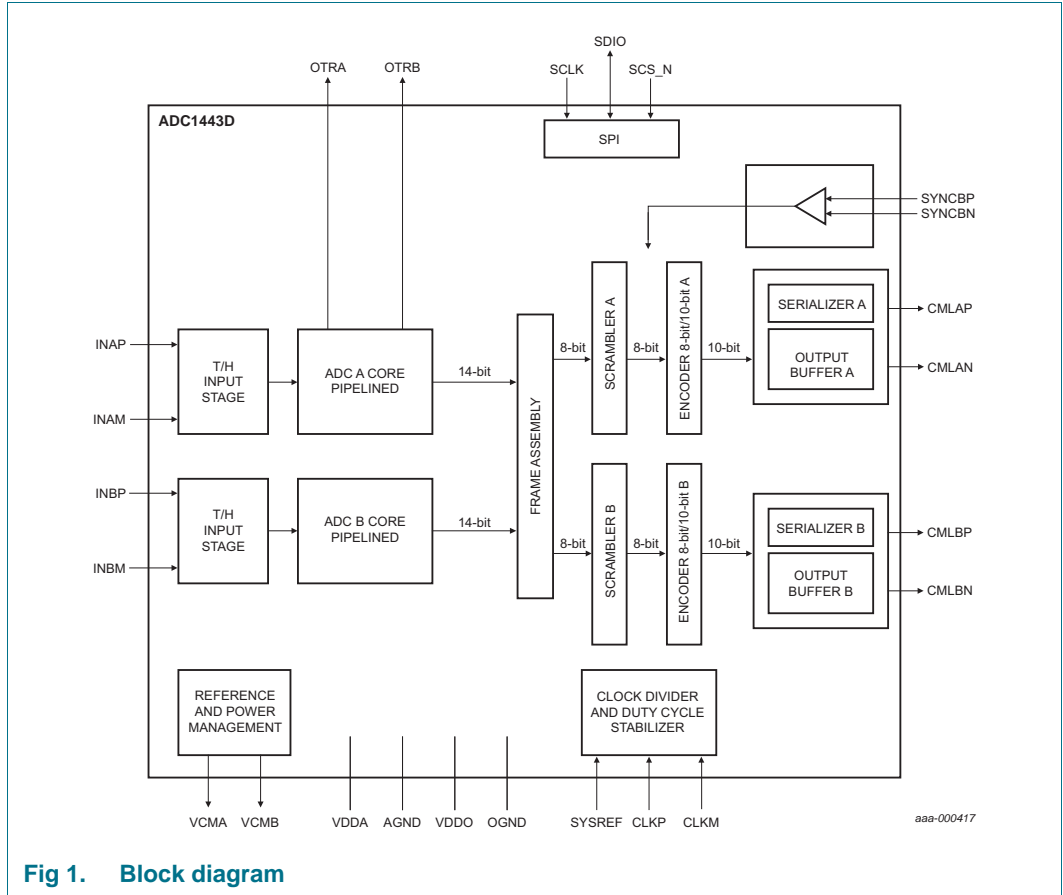


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

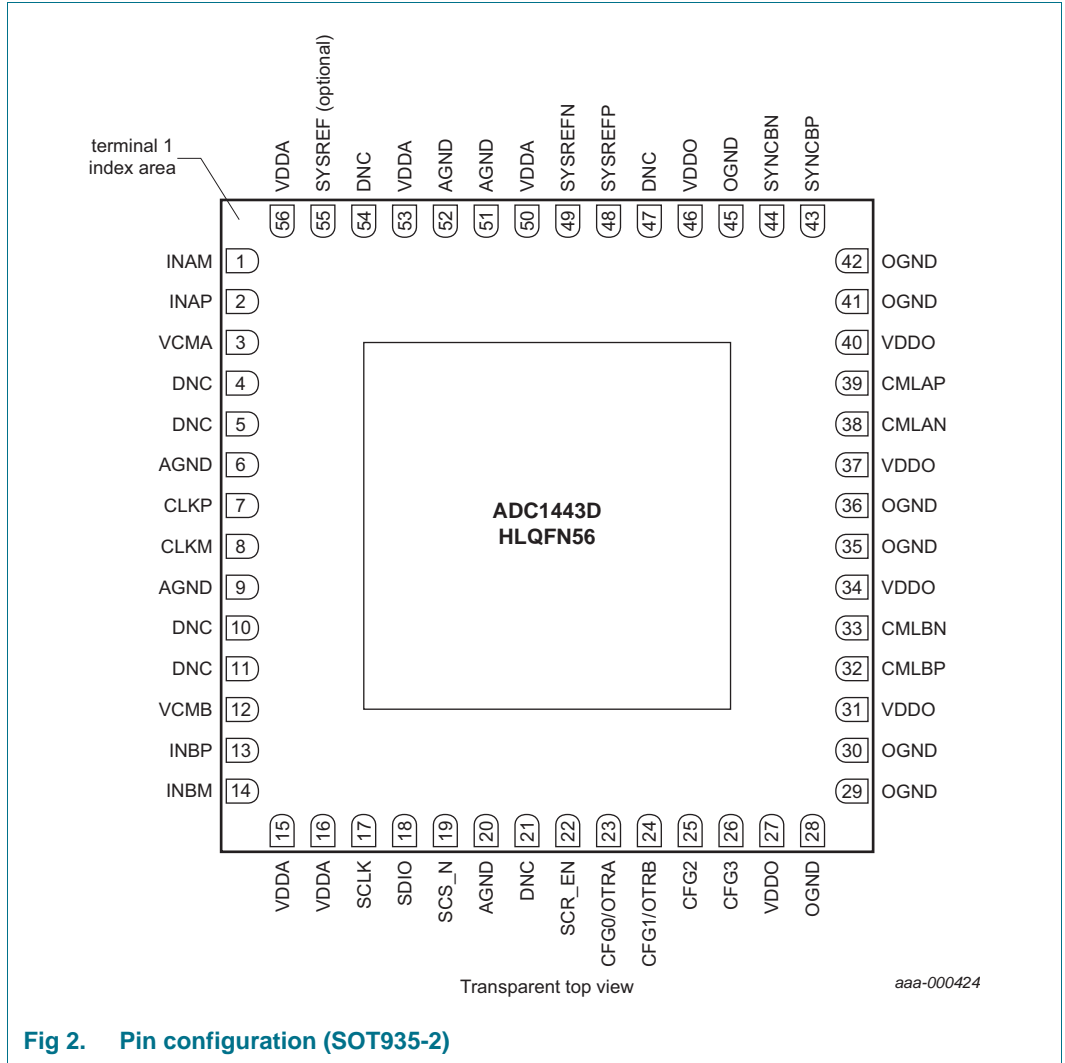


Fig 2. Pin configuration (SOT935-2)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type ^[1]	Description
INAM	1	I	channel A complementary analog input
INAP	2	I	channel A analog input
VCMA	3	O	channel A output common voltage
DNC	4	-	do not connect
DNC	5	-	do not connect
AGND	6	G	analog ground
CLKP	7	I	clock input
CLKN	8	I	complementary clock input
AGND	9	G	analog ground
DNC	10	-	do not connect
DNC	11	-	do not connect
VCMB	12	O	channel B output common voltage
INBP	13	I	channel B analog input
INBM	14	I	channel B complementary analog input
VDDA	15	P	analog power supply
VDDA	16	P	analog power supply
SCLK	17	I	SPI clock
SDIO	18	I/O	SPI data IO
SCS_N	19	I	SPI chip select
AGND	20	G	analog ground
DNC	21	-	do not connect
SCR_EN	22	I	scrambler enable
CFG0/OTRA	23	I/O	configuration pin 0/OuT of Range A (OTRA)
CFG1/OTRB	24	I/O	configuration pin 1/OuT of Range B (OTRB)
CFG2	25	I/O	configuration pin 2
CFG3	26	I/O	configuration pin 3
VDDO	27	P	digital output power supply
OGND	28	G	digital output ground
OGND	29	G	digital output ground
OGND	30	G	digital output ground
VDDO	31	P	digital output power supply
CMLBP	32	O	channel B output
CMLBN	33	O	channel B complementary output
VDDO	34	P	digital output power supply
OGND	35	G	digital output ground
OGND	36	G	digital output ground
VDDO	37	P	digital output power supply
CMLAN	38	O	channel A complementary output
CMLAP	39	O	channel A output

Table 2. Pin description ...continued

Symbol	Pin	Type ^[1]	Description
VDDO	40	P	digital output power supply
OGND	41	G	digital output ground
OGND	42	G	digital output ground
SYNCBP	43	I	synchronization from Field-Programmable Gate Array (FPGA)
SYNCBN	44	I	complementary synchronization from FPGA
AGND	45	G	analog ground
VDDA	46	P	analog power supply
DNC	47	-	do not connect
SYSREFP	48	I	positive clock synchronization
SYSREFN	49	I	negative clock synchronization
VDDA	50	P	analog power supply
AGND	51	G	analog ground
AGND	52	G	analog ground
VDDA	53	P	analog power supply
DNC	54	-	do not connect
SYSREF	55	I	single-ended ADC clock synchronization
VDDA	56	P	analog power supply

[1] P: power supply; G: ground; I: input; O: output; I/O: input/output.

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage		-0.3	+2.1	V
V_{DDO}	output supply voltage		-0.3	+2.1	V
ΔV_{DD}	supply voltage difference	$V_{DDA} - V_{DDO}$	<tbid>	<tbid>	V
V_I	input voltage	pins INP, INM, CLKP, CLKM, SYSREFP, and SYSREFN; referenced to AGND	-0.3	$V_{DDA} + 0.3$	V
		pins SCS_N, SDIO, SCLK, CFG, SCR_EN, SYNCBP, and SYNCBN; referenced to OGND	-0.3	$V_{DDO} + 0.3$	V
V_O	output voltage	pin VCM; referenced to AGND	-0.3	$V_{DDA} + 0.3$	V
		pins OTR, CMLP, and CMLN; referenced to OGND	-0.3	$V_{DDO} + 0.3$	V
T_{stg}	storage temperature		-55	+125	°C
T_{amb}	ambient temperature		-40	+85	°C
T_j	junction temperature		-	125	°C

8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1] <tbid>	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1] <tbid>	K/W

[1] In compliance with JEDEC test board, in free air.

9. Static characteristics

Table 5. Static characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DDA}	analog supply voltage		1.7	1.8	1.9	V
V_{DDO}	output supply voltage		1.7	1.8	1.9	V
I_{DDA}	analog supply current	$f_s = 200$ Msps; $f_i = 190$ MHz	-	<tbid>	<tbid>	mA
I_{DDO}	output supply current	$f_s = 200$ Msps; $f_i = 190$ MHz	-	<tbid>	<tbid>	mA

Table 5. Static characteristics^[1] ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P _{tot}	total power dissipation	f _i = 190 MHz				
		ADC1443D125	-	0.85	<td>	W
		ADC1443D160	-	0.95	<td>	W
		ADC1443D200	-	1.0	<td>	W
		Power-down mode	-	10	-	mW
		Sleep mode	-	130	-	mW
Clock inputs: pins CLKP and CLKM (AC-coupled; peak-to-peak)						
V _{i(clk)}	clock input voltage	LVPECL	-	±0.8	-	V
		LVDS	-	±0.35	-	V
		SINE differential	±0.2	±1.5	-	V
		LVCOS single	-	V _{DDA}	-	V
C _i	input capacitance		-	<td>	-	pF
Logic inputs						
I _{IL}	LOW-level input current		-	<td>	-	µA
I _{IH}	HIGH-level input current		-	<td>	-	µA
C _i	input capacitance		-	<td>	-	pF
pins SYSREFP, SYSREFN, SYNCBP, and SYNCBN						
V _{i(cm)}	common-mode input voltage		<td>	1.2	<td>	V
V _{i(dif)}	differential input voltage		-	0.35	-	V
pins SCS_N, SDIO, SCLK, SCR_EN and CFG						
V _{IL}	LOW-level input voltage		0	-	0.3V _{DDO}	V
V _{IH}	HIGH-level input voltage		0.7V _{DDO}	-	V _{DDO}	V
Logic output: pins OTR and SDIO						
V _{OL}	LOW-level output voltage		0	-	0.2V _{DDO}	V
V _{OH}	HIGH-level output voltage		0.8V _{DDO}	-	V _{DDO}	V
Digital outputs: pins CMLAP, CMLAN, CMLBP, and CMLBN						
V _{O(cm)}	common-mode output voltage		-	<td>	-	V
V _{O(dif)}	differential output voltage	default current	-	±400	-	mV
Analog inputs: pins INP and INM						
I _i	input current		-	±5	-	µA
R _i	input resistance	f _i = 190 MHz	-	<td>	-	Ω
C _i	input capacitance	f _i = 190 MHz	-	5	-	pF
V _{i(cm)}	common-mode input voltage	V _{INP} = V _{INM}	<td>	0.9	<td>	V
B _i	input bandwidth		-	1	-	GHz
V _{i(dif)}	differential input voltage	peak-to-peak; full-scale	1	-	2	V
Common-mode output voltage: pins VCMA and VCMB						
V _{O(cm)}	common-mode output voltage		-	0.9	-	V
I _{O(cm)}	common-mode output current	T _{amb} = 25 °C	-	-	4	mA
Accuracy						
INL	integral non-linearity	f _s = 200 Msps; f _i = 4.43 MHz	<td>	<td>	<td>	LSB

Table 5. Static characteristics^[1] ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DNL	differential non-linearity	$f_s = 200$ Msps; $f_i = 4.43$ MHz; guaranteed no missing codes	<td>	<td>	<td>	LSB
E_{offset}	offset error		-	<td>	-	mV
E_G	gain error	full-scale	-	<td>	-	%
$M_{G(\text{CTC})}$	channel-to-channel gain matching		-	<td>	-	%
Supply						
PSRR	power supply rejection ratio	<td> mV (p-p) on V_{DDA}	-	<td>	-	dB

[1] Typical values measured at $V_{\text{DDA}} = V_{\text{DDO}} = 1.8$ V; $T_{\text{amb}} = 25$ °C; minimum and maximum values are across the full temperature range $T_{\text{amb}} = -40$ °C to +85 °C at $V_{\text{DDA}} = V_{\text{DDO}} = 1.8$ V; $V_{\text{I(dif)}} = 2$ V; $V_{\text{INP}} - V_{\text{INM}} = -1$ dBFS; unless otherwise specified.

10. Dynamic characteristics

10.1 Dynamic characteristics

Table 6. Dynamic characteristics^[1]

Symbol	Parameter	Conditions	ADC1443D125 (f _s = 125 Msps)			ADC1443D160 (f _s = 154 Msps)			ADC1443D200 (f _s = 185 Msps)			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
α _{2H}	second harmonic level	f _i = 5 MHz	-	<td>	-	-	<td>	-	-	<td>	-	dBc
		f _i = 30 MHz	-	<td>	-	-	<td>	-	-	<td>	-	dBc
		f _i = 70 MHz	-	<td>	-	-	<td>	-	-	<td>	-	dBc
		f _i = 140 MHz	<td>	<td>	-	<td>	<td>	-	<td>	<td>	-	dBc
		f _i = 170 MHz	<td>	<td>	-	<td>	<td>	-	<td>	<td>	-	dBc
		f _i = 190 MHz	<td>	<td>	-	<td>	<td>	-	<td>	<td>	-	dBc
		f _i = 230 MHz	<td>	<td>	-	<td>	<td>	-	<td>	<td>	-	dBc
		f _i = 310 MHz	-	<td>	-	-	<td>	-	-	<td>	-	dBc
α _{3H}	third harmonic level	f _i = 5 MHz	-	<td>	-	-	<td>	-	-	<td>	-	dBc
		f _i = 30 MHz	-	<td>	-	-	<td>	-	-	<td>	-	dBc
		f _i = 70 MHz	-	<td>	-	-	<td>	-	-	<td>	-	dBc
		f _i = 140 MHz	<td>	<td>	-	<td>	<td>	-	<td>	<td>	-	dBc
		f _i = 170 MHz	<td>	<td>	-	<td>	<td>	-	<td>	<td>	-	dBc
		f _i = 190 MHz	<td>	<td>	-	<td>	<td>	-	<td>	<td>	-	dBc
		f _i = 230 MHz	<td>	<td>	-	<td>	<td>	-	<td>	<td>	-	dBc
		f _i = 310 MHz	-	<td>	-	-	<td>	-	-	<td>	-	dBc

Table 6. Dynamic characteristics^[1] ...continued

Symbol	Parameter	Conditions	ADC1443D125 (f _s = 125 Msps)			ADC1443D160 (f _s = 154 Msps)			ADC1443D200 (f _s = 185 Msps)			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SFDR	spurious-free dynamic range	-1 dBFS										
		f _i = 5 MHz	-	90	-	-	90	-	-	90	-	dBc
		f _i = 30 MHz	-	88	-	-	88	-	-	88	-	dBc
		f _i = 70 MHz	-	87	-	-	87	-	-	87	-	dBc
		f _i = 140 MHz	<tbid>	86	-	<tbid>	86	-	<tbid>	86	-	dBc
		f _i = 170 MHz	<tbid>	86	-	<tbid>	86	-	<tbid>	86	-	dBc
		f _i = 190 MHz	<tbid>	86	-	<tbid>	86	-	<tbid>	86	-	dBc
		f _i = 230 MHz	<tbid>	85	-	<tbid>	85	-	<tbid>	83	-	dBc
		f _i = 310 MHz	-	80	-	-	80	-	-	79	-	dBc
		-6 dBFS										
		f _i = 5 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _i = 30 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _i = 70 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _i = 140 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _i = 170 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _i = 190 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _i = 230 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _i = 310 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
THD	total harmonic distortion	f _i = 5 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _i = 30 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _i = 70 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _i = 140 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _i = 170 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _i = 190 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _i = 230 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _i = 310 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc

Table 6. Dynamic characteristics^[1] ...continued

Symbol	Parameter	Conditions	ADC1443D125 (f _s = 125 Msps)			ADC1443D160 (f _s = 154 Msps)			ADC1443D200 (f _s = 185 Msps)			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IMD3	third-order intermodulation distortion	f _{i1} = 3.5 MHz; f _{i2} = 6.5 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _{i1} = 28.5 MHz; f _{i2} = 31.5 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _{i1} = 68.5 MHz; f _{i2} = 71.5 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
		f _{i1} = 138.5 MHz; f _{i2} = 141.5 MHz	<tbid>	<tbid>	-	<tbid>	<tbid>	-	<tbid>	<tbid>	-	dBc
		f _{i1} = 168.5 MHz; f _{i2} = 171.5 MHz	<tbid>	88	-	<tbid>	88	-	<tbid>	88	-	dBc
		f _{i1} = 188.5 MHz; f _{i2} = 191.5 MHz	<tbid>	<tbid>	-	<tbid>	<tbid>	-	<tbid>	88	-	dBc
		f _{i1} = 228.5 MHz; f _{i2} = 231.5 MHz	<tbid>	<tbid>	-	<tbid>	<tbid>	-	<tbid>	<tbid>	-	dBc
		f _{i1} = 308.5 MHz; f _{i2} = 311.5 MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc
SNR	signal-to-noise ratio	f _i = 5 MHz	-	74	-	-	74	-	-	74	-	dBFS
		f _i = 30 MHz	-	74	-	-	74	-	-	74	-	dBFS
		f _i = 70 MHz	-	73.5	-	-	73.5	-	-	73.5	-	dBFS
		f _i = 140 MHz	<tbid>	73	-	<tbid>	73	-	<tbid>	73.5	-	dBFS
		f _i = 170 MHz	<tbid>	72.5	-	<tbid>	72.5	-	<tbid>	72.5	-	dBFS
		f _i = 190 MHz	<tbid>	72.5	-	<tbid>	72.5	-	<tbid>	72.5	-	dBFS
		f _i = 230 MHz	<tbid>	72	-	<tbid>	72	-	<tbid>	72	-	dBFS
		f _i = 310 MHz	-	71	-	-	71	-	-	71	-	dBFS

Table 6. Dynamic characteristics^[1] ...continued

Symbol	Parameter	Conditions	ADC1443D125 ($f_s = 125$ Msps)			ADC1443D160 ($f_s = 154$ Msps)			ADC1443D200 ($f_s = 185$ Msps)			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ENOB	effective number of bits	$f_i = 5$ MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	bit
		$f_i = 30$ MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	bit
		$f_i = 70$ MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	bit
		$f_i = 140$ MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	bit
		$f_i = 170$ MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	bit
		$f_i = 190$ MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	bit
		$f_i = 230$ MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	bit
		$f_i = 310$ MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	bit
$\alpha_{ct(ch)}$	channel crosstalk	$f_i = 140$ MHz	-	100	-	-	100	-	-	100	-	dBc
		$f_i = 230$ MHz	-	<tbid>	-	-	<tbid>	-	-	<tbid>	-	dBc

[1] Typical values measured at $V_{DDA} = V_{DDO} = 1.8$ V; $T_{amb} = 25$ °C; minimum and maximum values are across the full temperature range $T_{amb} = -40$ °C to $+85$ °C at $V_{DDA} = V_{DDO} = 1.8$ V; $V_{I(dif)} = 2$ V; $V_{INP} - V_{INM} = -1$ dBFS; unless otherwise specified.

10.2 Timing

10.2.1 Clock timing

Table 7. Clock and digital output timing characteristics^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{lat(data)}$	data latency time		-	<tbd>	-	clock cycles
t_{wake}	wake-up time	from Power-down mode	-	<tbd>	-	ns
		from Sleep mode	-	<tbd>	-	ns
		from high impedance	-	<tbd>	-	ns
Clock timing						
f_s	sampling rate	ADC1443D125	<tbd>	-	125	MHz
		ADC1443D160	<tbd>	-	160	MHz
		ADC1443D200	<tbd>	-	200	MHz
f_{clk}	clock frequency		<tbd>	-	1.2	GHz
δ_{clk}	clock duty cycle		30	-	70	%
$t_{d(s)}$	sampling delay time		-	<tbd>	-	ns

[1] Typical values measured at $V_{DDA} = V_{DDO} = 1.8\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; minimum and maximum values are across the full temperature range $T_{amb} = -40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$ at $V_{DDA} = V_{DDO} = 1.8\text{ V}$; $V_{I(dif)} = 2\text{ V}$; $V_{INP} - V_{INM} = -1\text{ dBFS}$; unless otherwise specified.

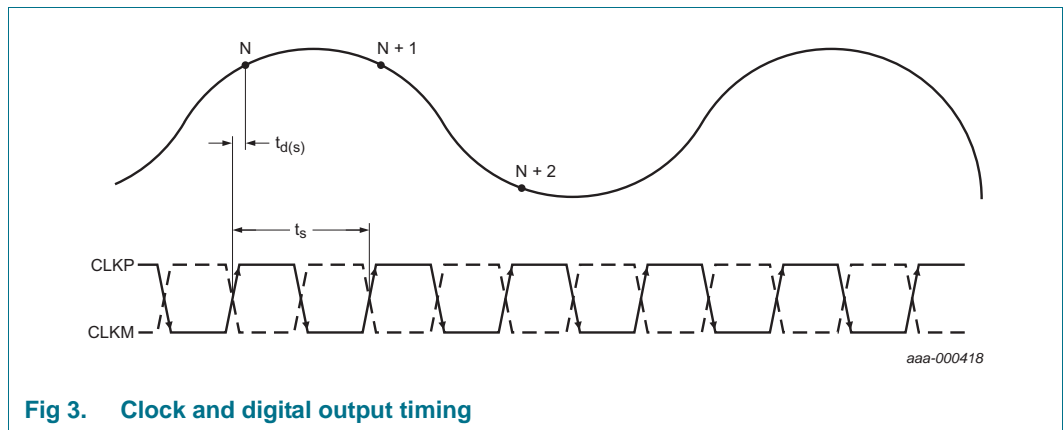


Fig 3. Clock and digital output timing

10.2.2 SYSREF timing

Table 8. SYSREF timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{su}	set-up time		<tbd>	-	-	ns
t_h	hold time		<tbd>	-	-	ns

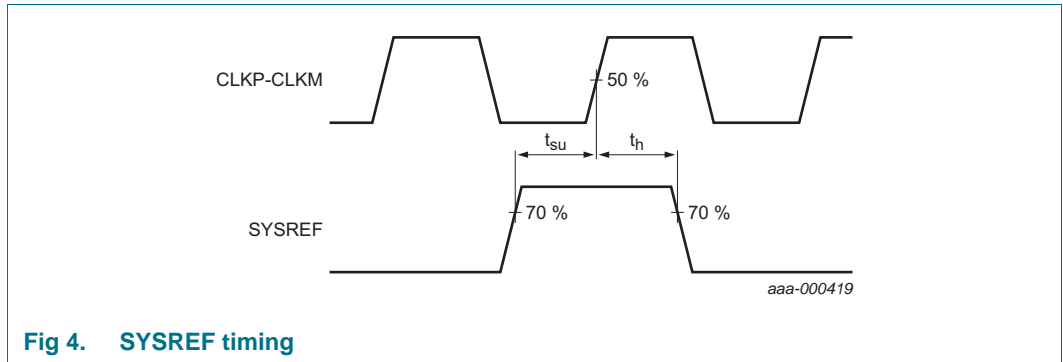


Fig 4. SYSREF timing

10.2.3 SPI timing

Table 9. SPI timing characteristics [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCLK)}$	SCLK pulse width		40	-	-	ns
$t_{w(SCLKH)}$	SCLK HIGH pulse width		16	-	-	ns
$t_{w(SCLKL)}$	SCLK LOW pulse width		16	-	-	ns
t_{su}	set-up time	SDIO to SCLK HIGH	5	-	-	ns
		SCS_N to SCLK HIGH	5	-	-	ns
t_h	hold time	SDIO to SCLK HIGH	2	-	-	ns
		SCS_N to SCLK HIGH	2	-	-	ns
f_{clk}	clock frequency		-	-	25	MHz

[1] Typical values measured at $V_{DDA} = V_{DDO} = 1.8\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; minimum and maximum values are across the full temperature range $T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ at $V_{DDA} = V_{DDO} = 1.8\text{ V}$

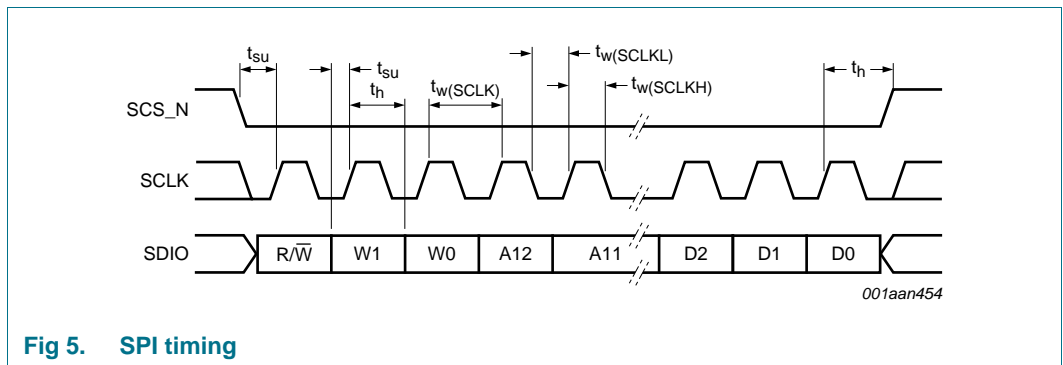


Fig 5. SPI timing

10.3 Typical dynamic performances

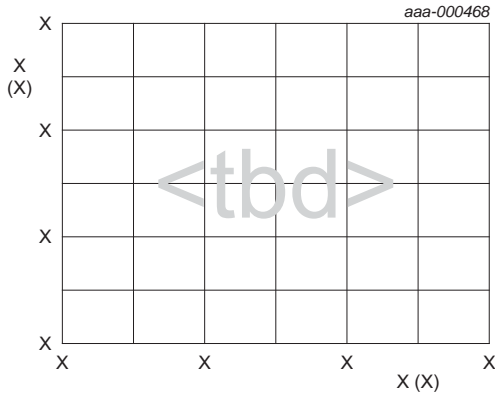


Fig 6. 1-tone FFT: -1 dBFS; $f_i = 30$ MHz; $f_s = 125$ Msps

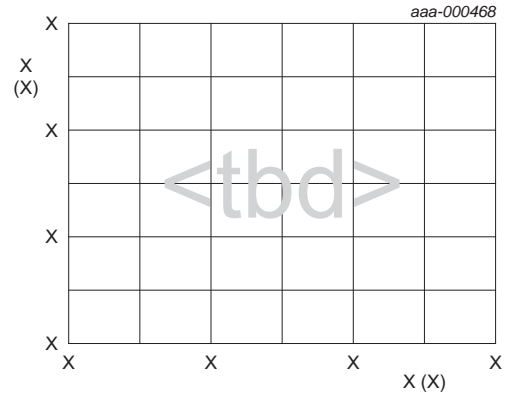


Fig 7. 1-tone FFT: -1 dBFS; $f_i = 190$ MHz; $f_s = 125$ Msps

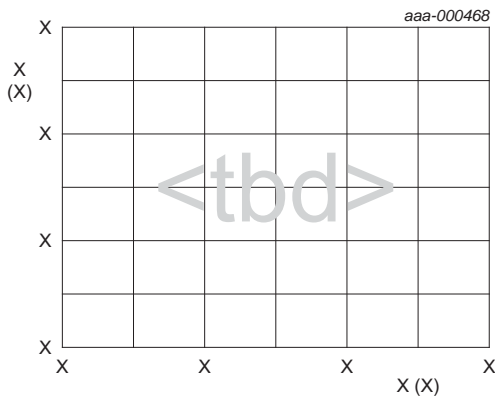


Fig 8. 1-tone FFT: -1 dBFS; $f_i = 30$ MHz; $f_s = 185$ Msps

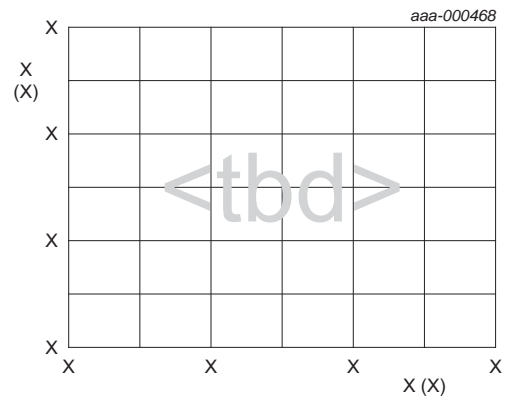


Fig 9. 1-tone FFT: -1 dBFS; $f_i = 190$ MHz; $f_s = 185$ Msps

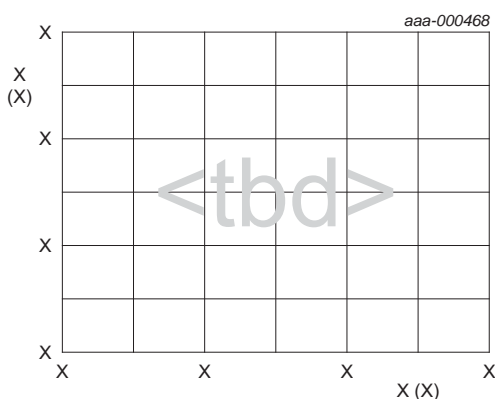


Fig 10. 2-tone FFT: -7 dBFS; $f_{i1} = 28.5$ MHz; $f_{i2} = 31.5$ MHz; $f_s = 185$ Msps

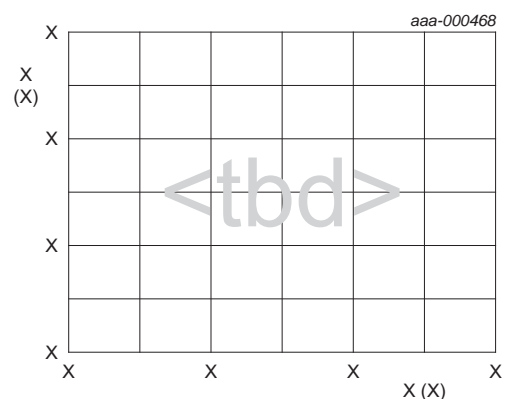


Fig 11. 2-tone FFT: -7 dBFS; $f_{i1} = 188.5$ MHz; $f_{i2} = 191.5$ MHz; $f_s = 185$ Msps

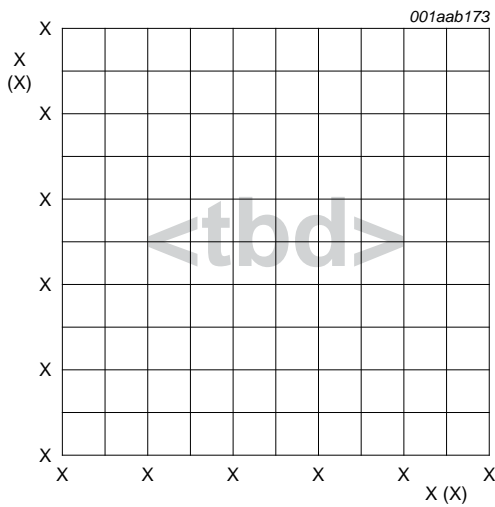


Fig 12. SNR as a function of sampling frequency:
-1 dBFS; $f_i = 190$ MHz

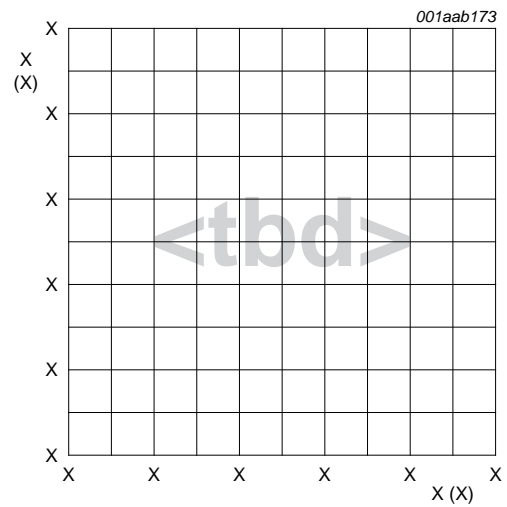


Fig 13. SNR as a function of input frequency:
-1 dBFS; $f_s = 185$ Msps

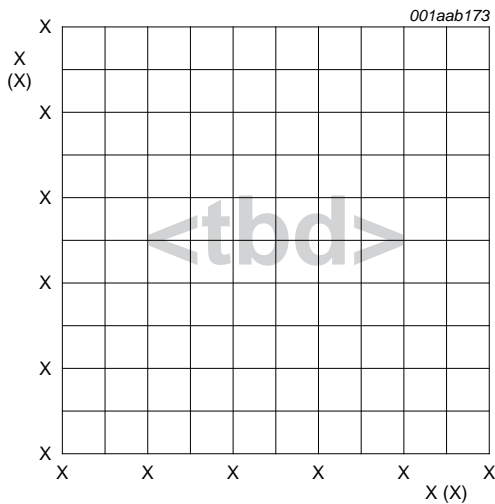


Fig 14. SNR as a function of input amplitude:
 $f_i = 190$ MHz; $f_s = 185$ Msps; $V_{I(dif)} = 2$ V

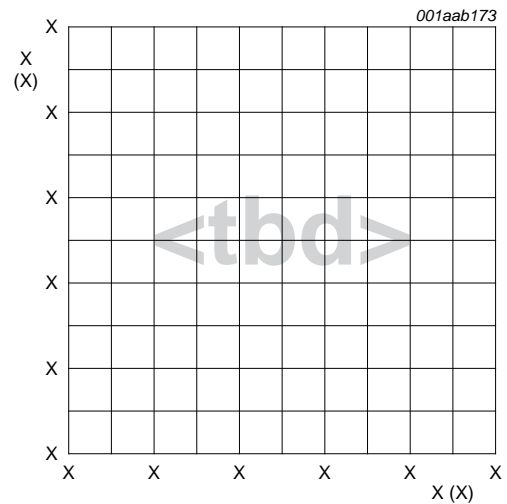


Fig 15. SNR as a function of full-scale amplitude:
-1 dBFS; $f_i = 190$ MHz; $f_s = 185$ Msps

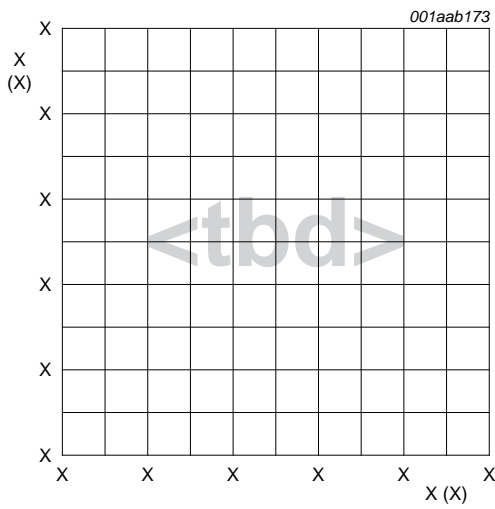


Fig 16. SFDR as a function of sampling frequency:
 -1 dBFS; $f_i = 190$ MHz

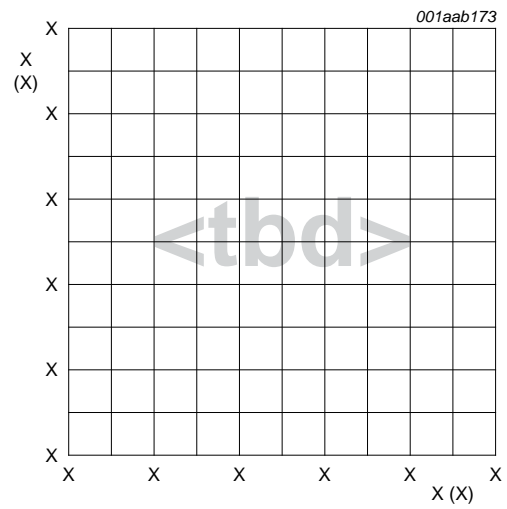


Fig 17. SFDR as a function of input frequency:
 -1 dBFS; $f_s = 185$ Msps

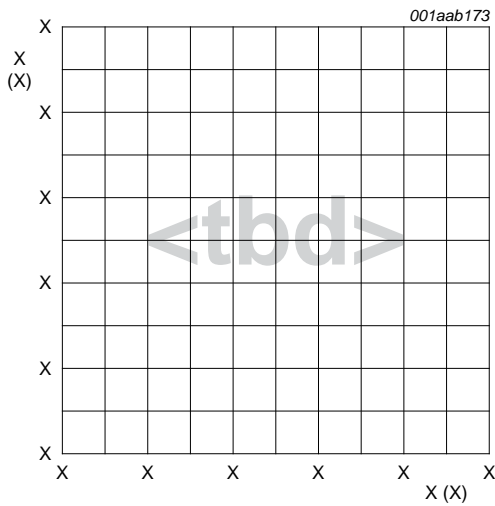


Fig 18. SFDR as a function of input amplitude:
 $f_i = 190$ MHz; $f_s = 185$ Msps; $V_{I(dif)} = 2$ V

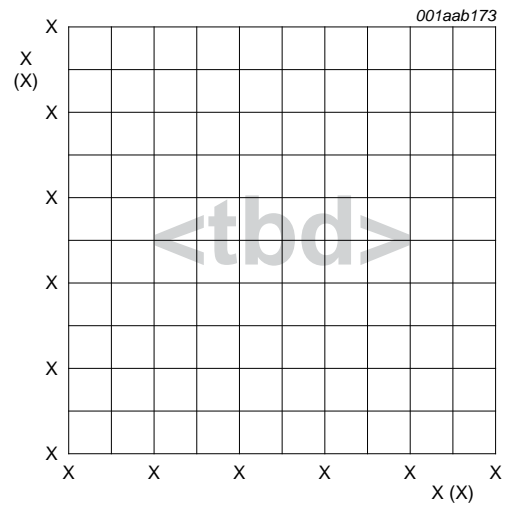


Fig 19. SFDR as a function of full-scale amplitude:
 -1 dBFS; $f_i = 190$ MHz; $f_s = 185$ Msps

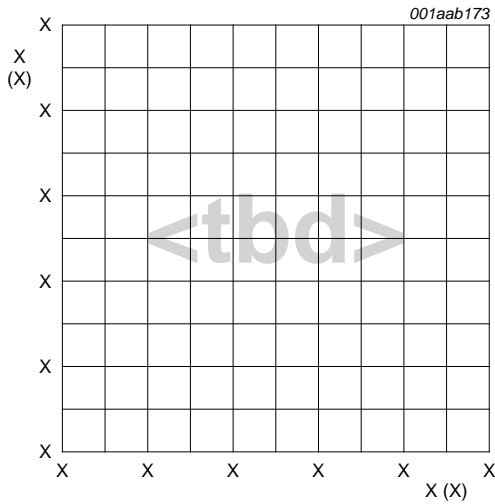


Fig 20. IMD3 as a function of sampling frequency:
-7 dBFS; $f_{i1} = 188.5$ MHz; $f_{i2} = 191.5$ MHz

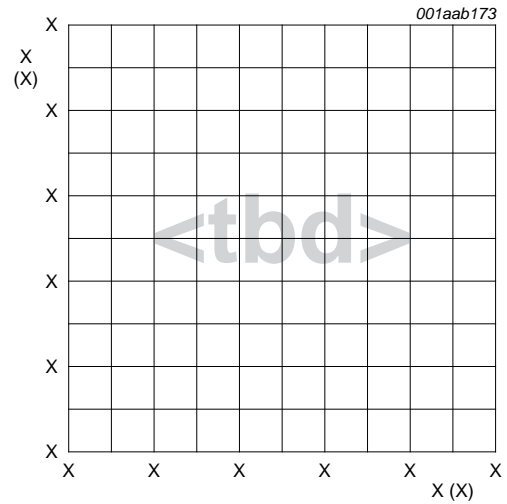


Fig 21. IMD3 as a function of input frequency:
-7 dBFS; $f_s = 185$ Msps; 3 MHz spacing

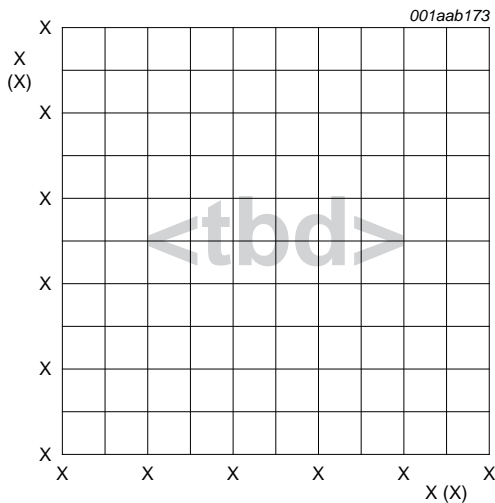


Fig 22. IMD3 as a function of input amplitude:
 $f_{i1} = 188.5$ MHz; $f_{i2} = 191.5$ MHz; $f_s = 185$ Msps;
 $V_{I(dif)} = 2$ V

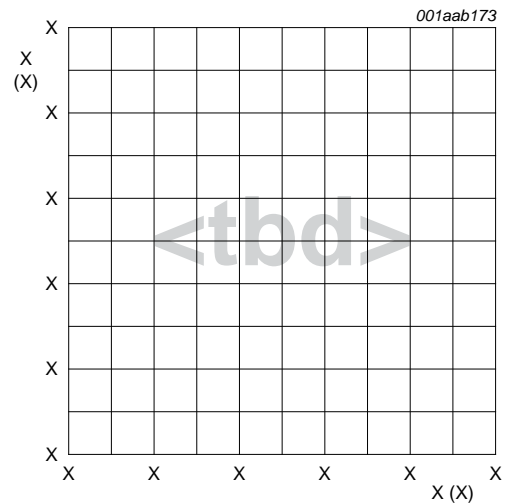


Fig 23. IMD3 as a function of full-scale amplitude:
-7 dBFS; $f_{i1} = 188.5$ MHz; $f_{i2} = 191.5$ MHz;
 $f_s = 185$ Msps

11. Application information

11.1 Analog inputs

11.1.1 Input stage

The analog input of the ADC1443D supports a differential or a single-ended input drive. Optimal performance is achieved using differential inputs with respect to the common-mode input voltage ($V_{I(cm)}$) on pins INP and INM.

The equivalent circuit of the sample and hold input stage, including ElectroStatic Discharge (ESD) protection and circuit and package parasitics, is shown in [Figure 24](#).

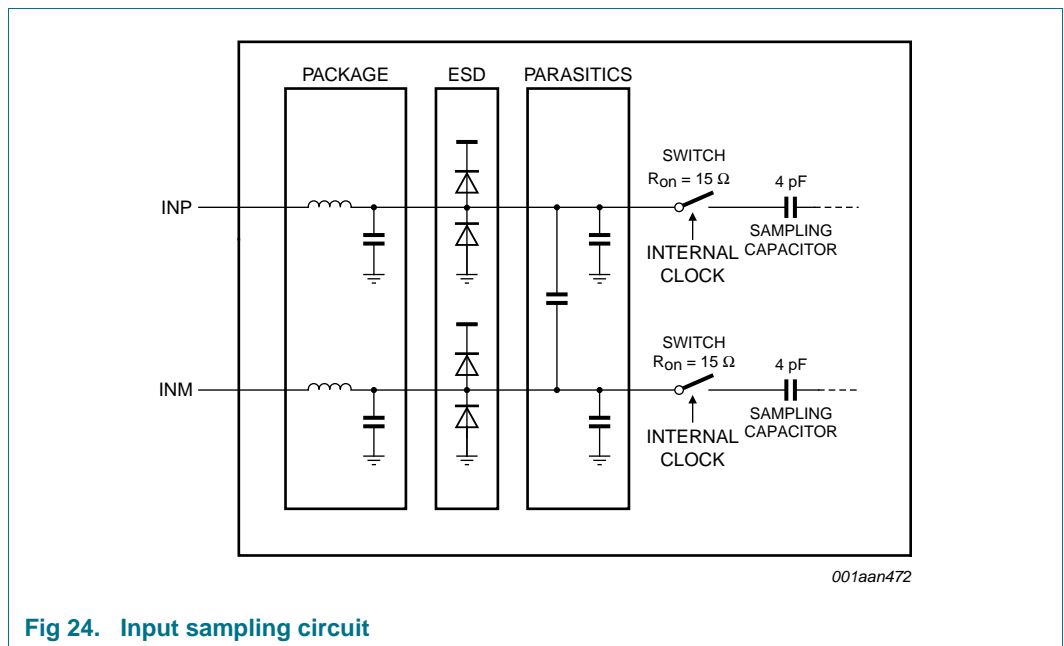


Fig 24. Input sampling circuit

The sample phase occurs when the internal sampling clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the sampling clock signal becomes LOW, the device enters the hold phase and the voltage information is transmitted to the ADC core.

11.1.2 Common-mode input voltage ($V_{I(cm)}$)

Set the common-mode input voltage ($V_{I(cm)}$) on pins INP and INM externally to 0.9 V for optimal performance.

11.1.3 Pin VCM

When the input stage is AC-coupled, pin VCM can be used to set the common-mode reference for the analog inputs, for instance, via a transformer middle point. Connect a 0.1 μ F filter capacitor between pin VCM and ground to ensure a low-noise common-mode output voltage.

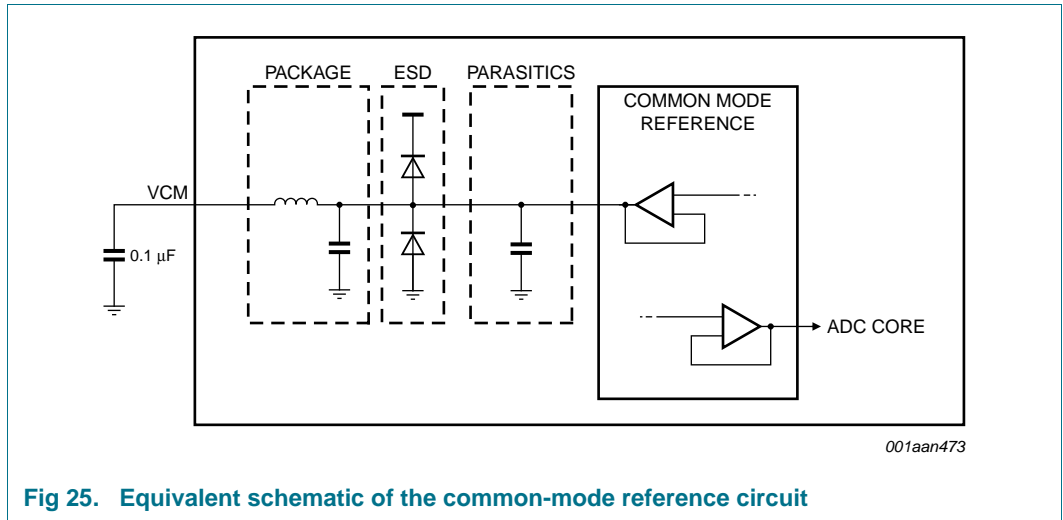


Fig 25. Equivalent schematic of the common-mode reference circuit

11.1.4 Programmable full-scale

The full-scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) by programming internal reference gain between 0 dB and -6 dB in 1 dB steps. The full-scale range can be set independently via bits INTREF[2:0] of the SPI local registers (see [Table 10](#) and [Table 24](#)).

Table 10. Reference gain control
Default values are shown highlighted.

INTREF[2:0]	Level (dB)	Full-scale (V (p-p))
000	0	2
001	-1	1.78
010	-2	1.59
011	-3	1.42
100	-4	1.26
101	-5	1.12
110	-6	1
111	reserved	x

11.1.5 Anti-kickback circuitry

An anti-kickback circuitry (RC-filter in [Figure 26](#)) is required to counteract the effects of the charge injection generated by the sampling capacitance.

The RC-filter is also used to filter noise from the signal before it reaches the sampling stage. It is recommended that the capacitor has a value that maximizes noise attenuation without degrading the settling time excessively.

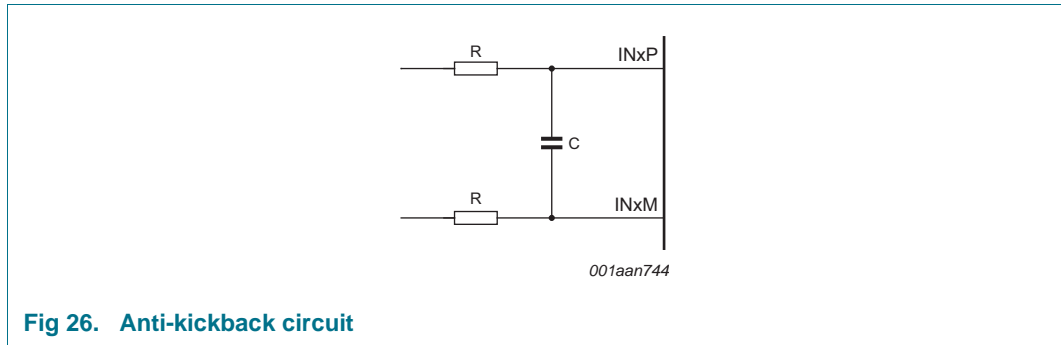


Fig 26. Anti-kickback circuit

The input frequency determines the component values. Select values that do not affect the input bandwidth.

Table 11. RC coupling versus input frequency; typical values

Input frequency range (MHz)	R (Ω)	C (pF)
0 to 50	<tbd>	<tbd>
50 to 100	<tbd>	<tbd>
100 to 200	<tbd>	<tbd>
200 to 300	<tbd>	<tbd>

11.1.6 Transformer

The input frequency determines the configuration of the transformer circuit. The configuration shown in Figure 27 is suitable for a baseband application.

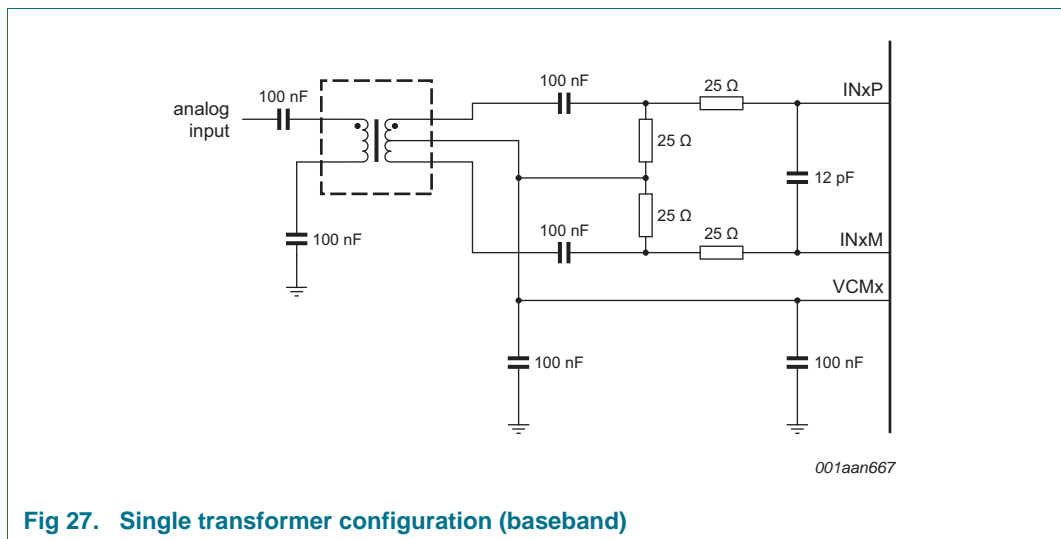
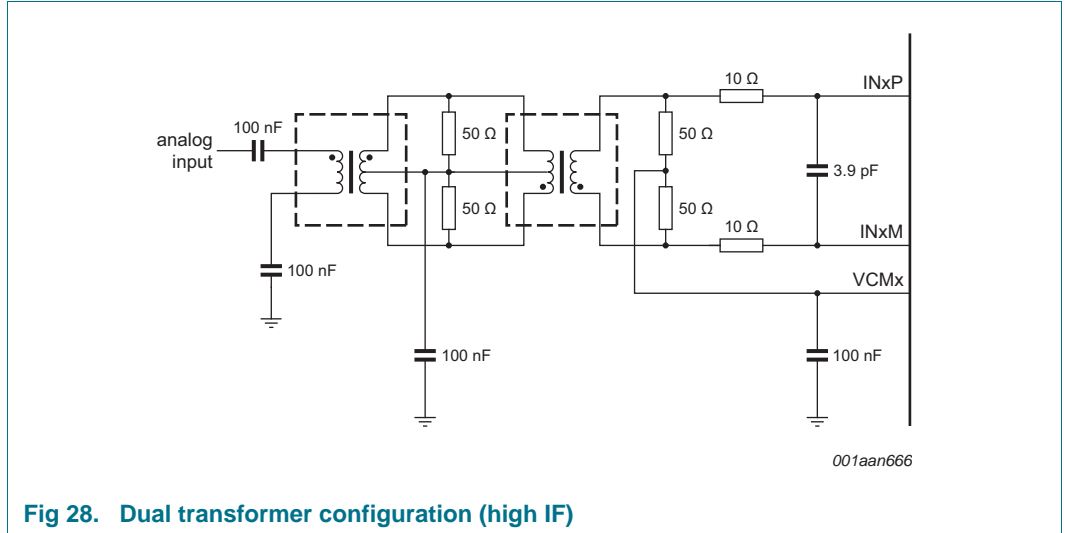


Fig 27. Single transformer configuration (baseband)

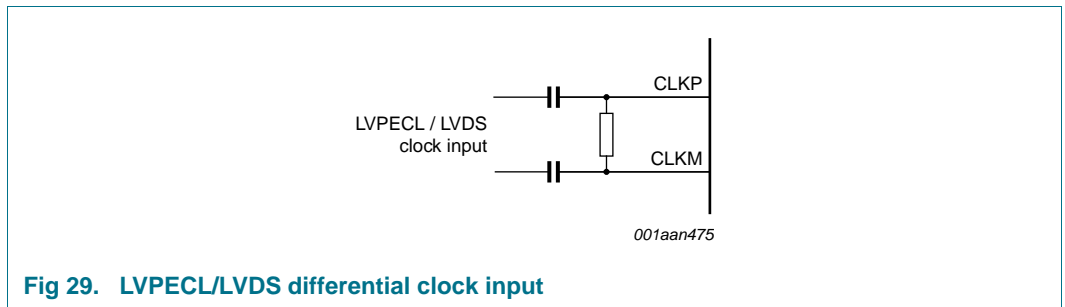
The configuration shown in [Figure 28](#) is recommended for high-frequency applications. In both cases, the choice of transformer is a compromise between cost and performance.

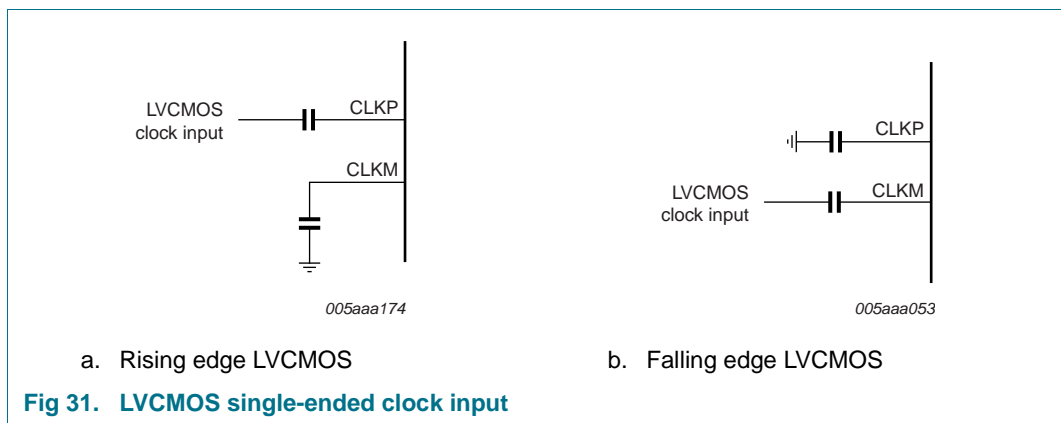
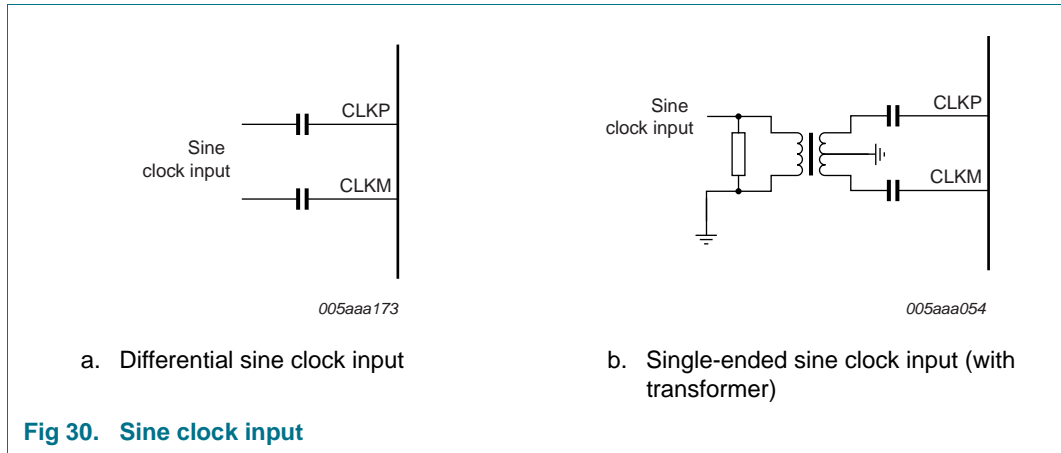


11.2 Clock input

11.2.1 Drive modes

The ADC1443D series can be driven differentially (LVPECL, LVDS or SINE). It can also be driven by a single-ended LVCMOS signal connected to either pin CLKP or pin CLKM (connect the complementary pin to ground using a capacitor). The LVPECL is recommended for an optimal performance.





Single-ended or differential clock inputs can be selected via bit DIFF_SE of SPI. If single-ended is enabled, the input pin (pin CLKM or pin CLKP) is selected using control bit SE_SEL (see [Table 23](#)).

11.2.2 Equivalent input circuit

Figure 32 shows the equivalent circuit of the input clock buffer. The input signal must be AC-coupled and the common-mode voltage of the differential input stage is set via internal 5 kΩ resistors.

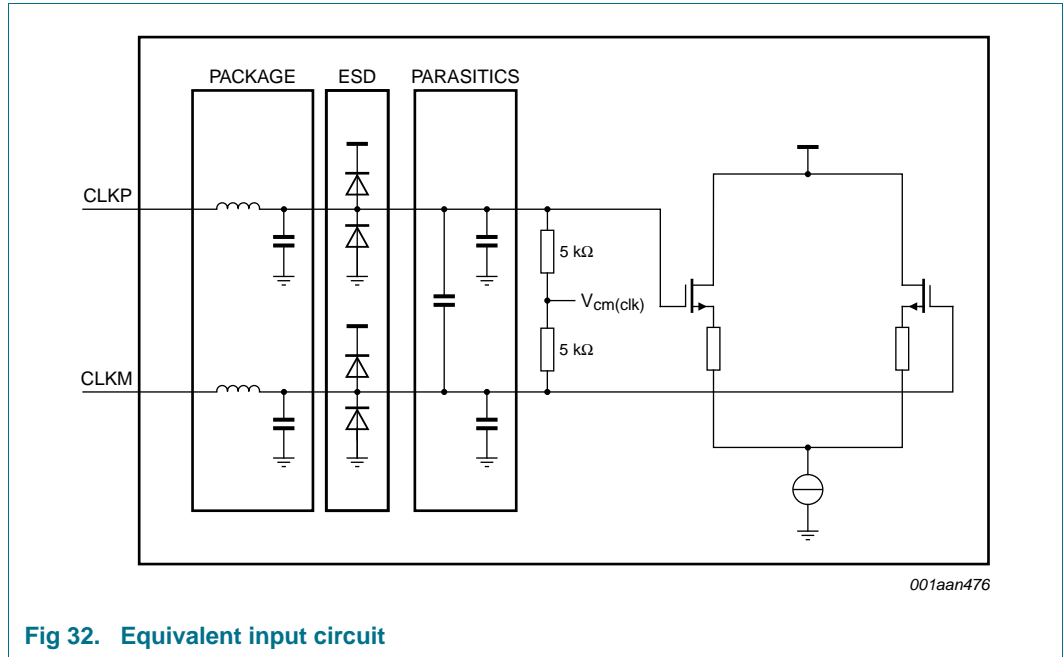


Fig 32. Equivalent input circuit

11.2.3 Clock input divider

The ADC1443D contains an input clock divider that divides the incoming clock (clock frequency f_{clk}) by a factor of 1 to 8. It outputs the sampling clock (sampling frequency f_s) (see bits CLK_DIV[1:0] in Table 23). This feature delivers a higher clock frequency with better jitter performance, leading to a better SNR result once acquisition has been performed.

11.2.4 Multi-device synchronization (pins SYSREF, SYSREFN and SYSREFP)

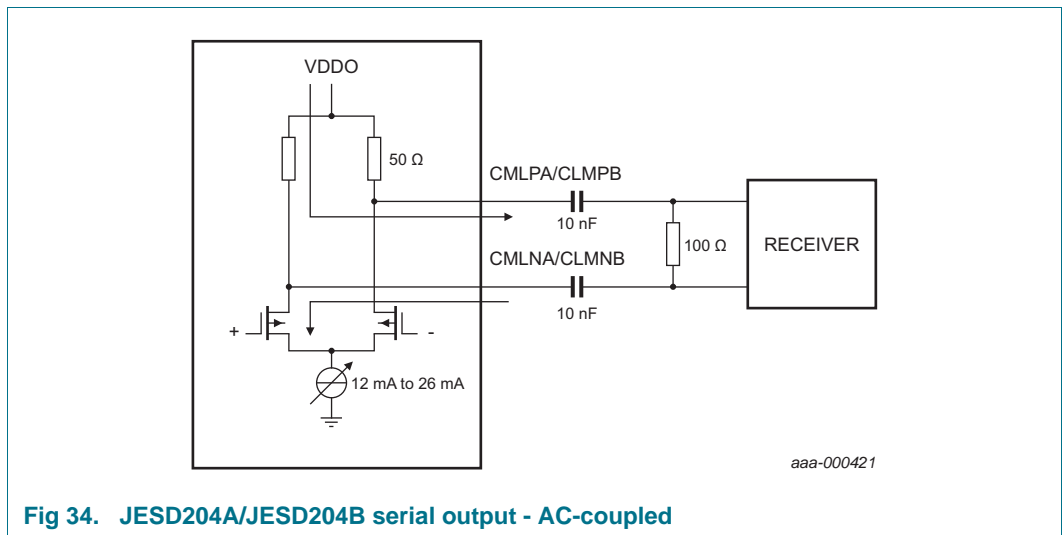
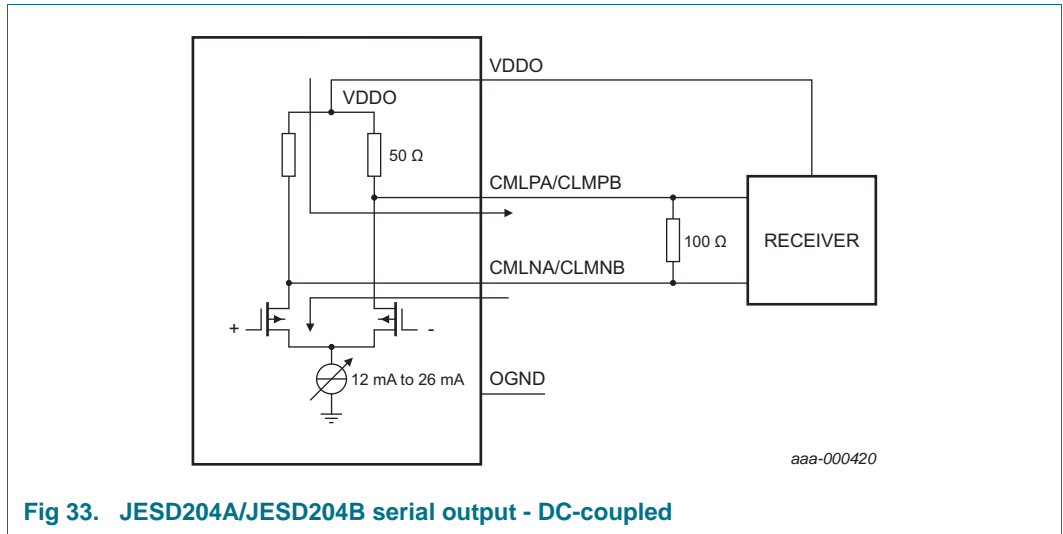
The multi-device synchronization can be controlled with a single-ended or a differential SYSREF signal.

A high level on SYSREF resets the clock divider phase registers. In a multi-device application and when the clock divider factor is higher than 1, the ADC1443D synchronization aligns all sampling clock edges (see Table 8 and Figure 4).

11.3 Digital outputs

11.3.1 Digital output buffers

The JESD204A/JESD204B standard specifies that both the receiver and the transmitter must be provided by the same supply if they are connected in DC-coupling.



11.3.2 JESD204A/JESD204B serializer

11.3.2.1 Digital JESD204A/JESD204B formatter

The block placed after the ADC cores is used to implement all functionalities of the JESD204A/JESD204B standard. This ensures signal integrity and guarantees the clock and the data recovery at the receiver side.

The block is highly parameterized and can be configured in various ways depending on the sampling frequency and the number of lanes used.

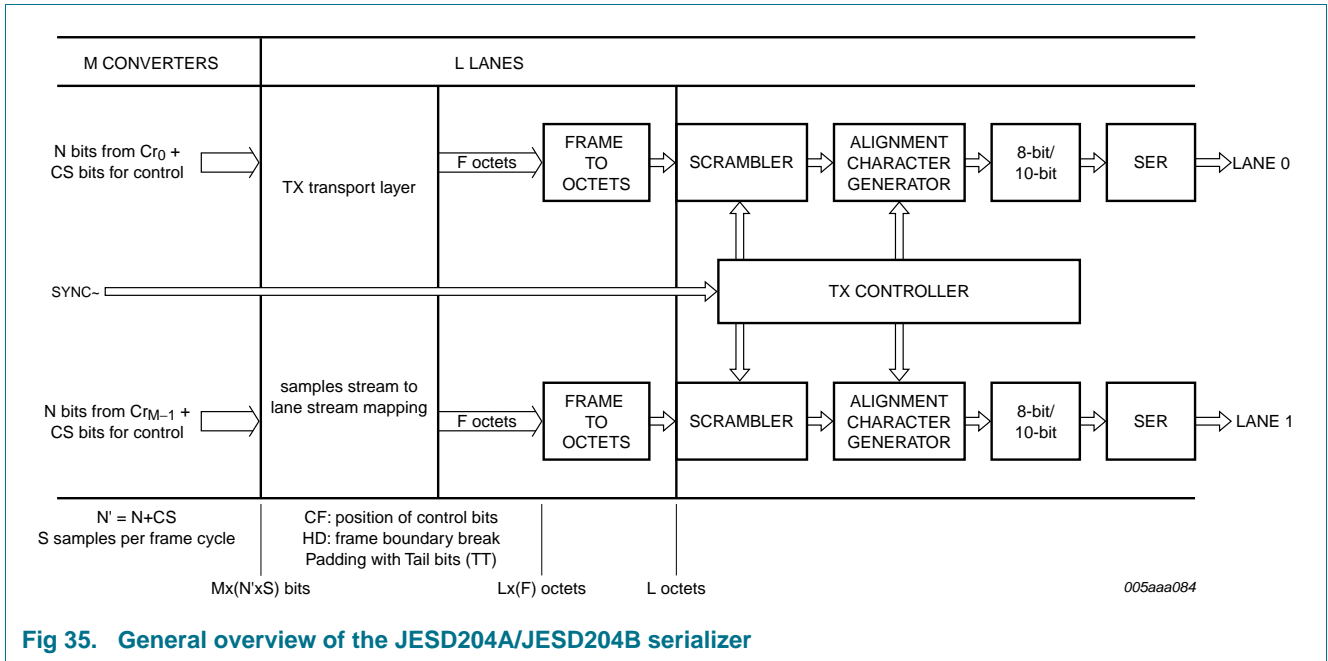


Fig 35. General overview of the JESD204A/JESD204B serializer

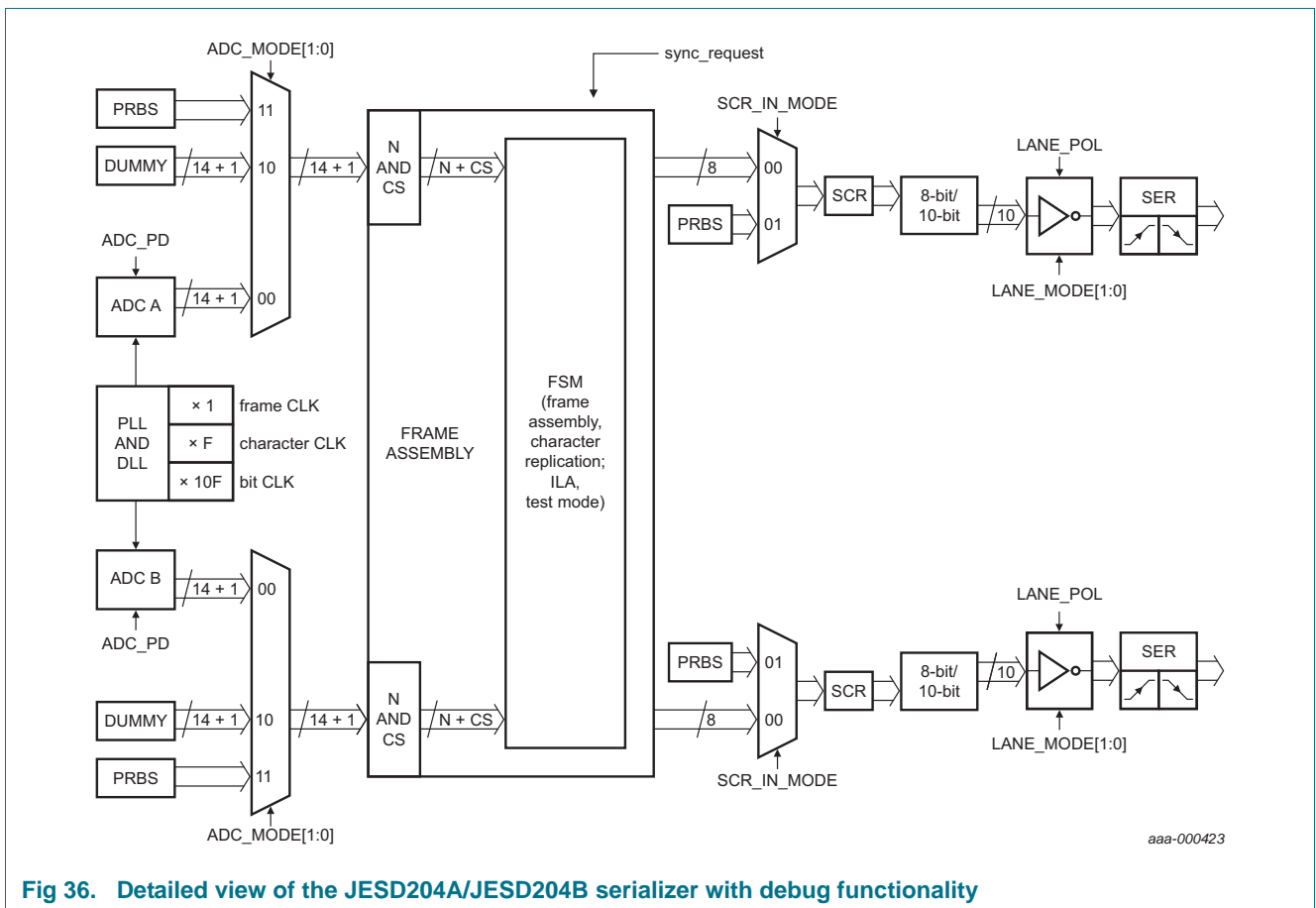


Fig 36. Detailed view of the JESD204A/JESD204B serializer with debug functionality

11.3.3 OuT-of-Range (OTR)

An out-of-range signal is provided on pins OTRA and OTRAB.

The latency of OTR is 31 clock cycles. The OTR response can be speeded up by enabling fast OTR using SPI local registers (bit FAST_OTR in [Table 31](#)). In this mode, the latency of OTR is reduced to only <td> clock cycles. The fast OTR detection threshold (below full-scale) can be programmed using the SPI local registers (bits FAST_OTR_DET[2:0] in [Table 31](#)).

Table 12. Fast OTR register threshold

FAST_OTR_DET[2:0]	Detection level (dB)
000	-18.06
001	-14.54
010	-12.04
011	-8.52
100	-6.02
101	-4.08
110	-2.5
111	-1.16

11.3.4 Digital offset

By default, the ADC1443D delivers an output code that corresponds to the analog input. However, it is possible to add a digital offset to the output code using the SPI local registers (bits DIG_OFFSET[5:0] in see [Table 13](#) and [Table 27](#)). The digital offset adjustment is coded in two's complement.

Table 13. Digital offset adjustment

Default values are shown highlighted.

DIG_OFFSET[5:0]	Digital offset adjustment (LSB)
10 0000	-32
10 0001	-31
...	...
11 1111	-1
00 0000	0
00 0001	+1
...	...
01 1110	+30
01 1111	+31

11.3.5 Test patterns

The ADC1443D can be configured to transmit one of a number of predefined test patterns using the SPI local registers (bits TEST_PAT_SEL[2:0] in [Table 14](#) and [Table 28](#)). The selected test pattern is transmitted regardless of the analog input.

Table 14. Digital test pattern selection

Default values are shown highlighted.

TEST_PAT_SEL[2:0]	Digital test pattern
000	Off
001	Mid code
010	Min code
011	Max code
100	Toggle '1111..1111'/'0000..0000'
101	Custom test pattern
110	'1010..1010'
111	'0101..0101'

A custom test pattern can be defined using the SPI local registers (bits TEST_PAT_USER[13:6] in [Table 29](#) and bits TEST_PAT_USER[5:0] in [Table 30](#)).

11.3.6 Output data format selection

The ADC1443D output data format can be selected (offset binary, two's complement or gray code) using the SPI local registers (bits DATA_FORMAT[1:0] in [Table 26](#)).

11.3.7 Output codes versus input voltage

Table 15. Output codes

$V_{INP} - V_{INM}$	Offset binary	Two's complement	Gray code	OTR
< -1	00 0000 0000 0000	10 0000 0000 0000	00 0000 0000 0000	1
-1	00 0000 0000 0000	10 0000 0000 0000	00 0000 0000 0000	0
-0.99987793	00 0000 0000 0001	10 0000 0000 0001	00 0000 0000 0001	0
-0.99975586	00 0000 0000 0010	00 0000 0000 0010	00 0000 0000 0011	0
...	0
-0.00024414	01 1111 1111 1110	11 1111 1111 1110	01 0000 0000 0001	0
-0.00012207	01 1111 1111 1111	11 1111 1111 1111	01 0000 0000 0000	0
+0.00012207	10 0000 0000 0000	00 0000 0000 0000	11 0000 0000 0000	0
+0.0.00024414	10 0000 0000 0001	00 0000 0000 0001	11 0000 0000 0001	0
...	0
+0.99975586	11 1111 1111 1101	01 1111 1111 1101	10 0000 0000 0011	0
+0.99987793	11 1111 1111 1110	01 1111 1111 1110	10 0000 0000 0001	0
+1	11 1111 1111 1111	01 1111 1111 1111	10 0000 0000 0000	0
> +1	11 1111 1111 1111	01 1111 1111 1111	10 0000 0000 0000	1

11.4 Configuration pins (CFG0, CFG1, CFG2, CFG3)

The configuration pins are only active as inputs at start-up. The values on those pins are read once to set up the device. Then the pins become outputs (OTRA and OTRB) and any change in the configuration is applied by SPI.

Table 16. JESD204A/JESD204B configuration table

CFG_SETUP[3:0]	ADC A	ADC B	Lane 0	Lane 1	F ^[1]	HD ^[1]	K ^[1]	M ^[1]	L ^[1]	Comment	CS ^[1]	CF ^[1]	S ^[1]	
0	0000	ON	ON	ON	2	0	9	2	2	(F × K) ≥ 17	1	0	1	
1	0001	ON	ON	ON	OFF	4	0	5	2	1	(F × K) ≥ 17	1	0	1
2	0010	ON	ON	OFF	ON	4	0	5	2	1	(F × K) ≥ 17	1	0	1
3	0011									reserved				
4	0100									reserved				
5	0101	ON	OFF	ON	OFF	2	0	9	1	1	(F × K) ≥ 17	1	0	1
6	0110	ON	OFF	OFF	ON	2	0	9	1	1	(F × K) ≥ 17	1	0	1
7	0111	OFF	ON	ON	OFF	2	0	9	1	1	(F × K) ≥ 17	1	0	1
8	1000	OFF	ON	OFF	ON	2	0	9	1	1	(F × K) ≥ 17	1	0	1
9	1001									reserved				
10	1010									reserved				
11	1011									reserved				
12	1100									reserved				
13	1101									reserved				
14	1110									reserved				
15	1111	OFF	OFF	OFF	OFF	2	0	9	2	2	chip power-down	1	0	1

[1] F: Octets per frame clock cycle
 HD: High-density mode
 K: Frame per multi-frame
 M: Converters per device
 L: Lane per converter device
 CS: Number of control bits per conversion sample
 CF: Control words per frame clock cycle and link
 S: Number of samples transmitted per single converter per frame cycle

11.5 Serial Peripheral Interface (SPI)

11.5.1 Register description

The ADC1443D serial interface is a synchronous serial communications port, which allows easy interfacing with many commonly used microprocessors. It provides access to the registers controlling the operation of the chip.

The register bits are either global or local functions:

- A global function operates over the full IC behavior. A local function operates on one or several previously selected channels only. If a channel is selected, the next WRITE command in the local registers applies to the selected channel. The WRITE command has no impact on channels that are not selected. This makes it possible to apply different configurations on each channel by first selecting a specific channel and then all the related settings.
- Select only one channel during a READ operation of the local registers. If several channels are selected, the READ operation occurs on the channel A.

Programming all registers at the same time is required:

- The IC allows the storage of a set of settings for the addresses 06h to 23h, which enables the configuration of all registers simultaneously by setting bit TRANSFER to HIGH (see [Table 32](#)). This bit is autoclearing. This function can be disabled using SPI (bit TRANS_DIS in [Table 32](#)). The registers are then updated at each WRITE operation.
- The transfer function does not apply to a READ operation.

The SPI interface is configured as a 3-wire type: pin SDIO is the bidirectional pin, pin SCLK is the serial clock input and SCS_N is the chip select pin.

A LOW level on pin SCS_N initiates each READ/WRITE operation. A minimum of 3 bytes is transmitted (two instruction bytes and at least 1 DATA byte; see [Table 18](#)).

Table 17. Instruction bytes for the SPI

Bit:	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Description	R/ \overline{W}	W1	W0	A12	A11	A10	A9	A8
	A7	A6	A5	A4	A3	A2	A1	A0

- Bit R/ \overline{W} indicates whether it is a READ (when HIGH) or a WRITE (when LOW) operation.
- Bits W1 and W0 indicate the number of bytes to be transferred after both instruction bytes (see [Table 18](#)).

Table 18. Number of data bytes transferred

W1	W0	Number of bytes transferred
0	0	1 byte
0	1	2 bytes
1	0	3 bytes
1	1	4 or more bytes

- Bits A12 to A0 indicate the address of the register being accessed. If it concerns a multiple byte transfer, this address is the first register accessed. An address counter is increased to access subsequent addresses.

The steps for a data transfer are:

1. Communication starts with the first rising edge on pin SCLK after a falling edge on pin SCS_N.
2. The first phase is the transfer of the 2-byte instruction.
3. The second phase is the transfer of the data. Its length varies, but it is always a multiple of 8 bits. The MSB is always sent first (for instruction and data bytes).
4. A rising edge on pin SCS_N indicates the end on data transmission.

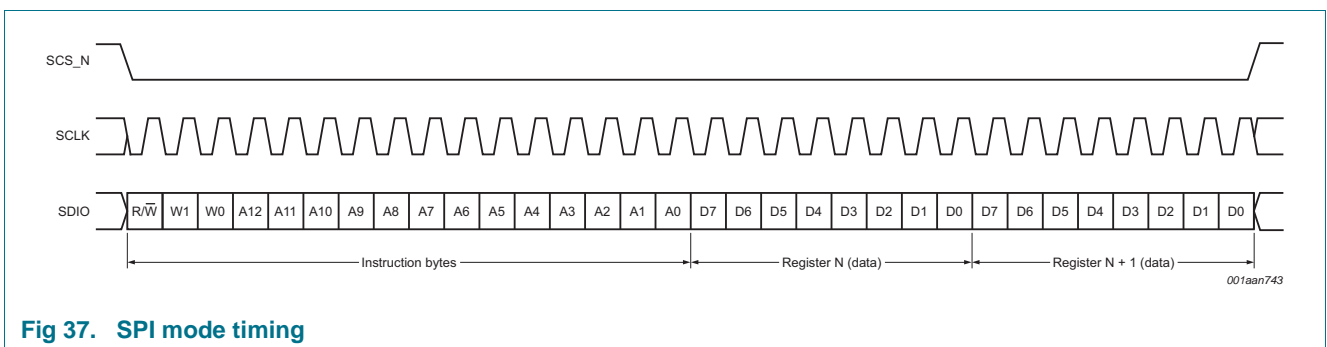


Fig 37. SPI mode timing

11.5.2 Register allocation map

Table 19 shows an overview of all registers.

Table 19. Register allocation map

Addr. (hex)	Register name	R/W	Bit definition								Default	
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
ADC control registers												
0000h	CHIP_RESET	R/W	SW_RST[7:0]								0000	00h
0001h	CHIP_ID	R	CHIP_ID[7:0] ^[1]								0100	43h
0005h	CHIP_RESET	R/W	SW_RST	-	-	-	-	-	-	-	0000	00h
0006h	OP_MODE	R/W	-	-	-	-	-	-	OP_MODE[1:0] ^[3]		0000	00h
0007h	CLK_CFG	R/W	-	-	-	SE_SEL	DIFF_SE	CLK_DIV[2:0]			0000	00h
0008h	INTERNAL_REF	R/W	-	-	-	-	-	INTREF[2:0]			0000	00h
0009h	CHANNEL_SEL	R/W	-	-	-	-	-	-	ADC_B	ADC_A	0000	0Fh
0011h	OUTPUT_CFG	R/W	-	-	-	-	-	DATA_SWAP	DATA_FORMAT[1:0]		0000	00h
0013h	DIG_OFFSET	R/W	DIG_OFFSET[5:0]						-	-	0000	00h
0014h	TEST_CFG_1	R/W	-	-	-	-	-	TEST_PAT_SEL[2:0]			0000	00h
0015h	TEST_CFG_2	R/W	TEST_PAT_USER[13:6]						-	-	0000	00h
0016h	TEST_CFG_3	R/W	TEST_PAT_USER[5:0]						-	-	0000	00h
0017h	OTR_CFG	R/W	-	-	-	-	-	FAST_OTR	FAST_OTR_DET[2:0]		0001	14h
00FFh	TRANS_CFG	R/W	TRANS_DIS	TRANSFER	-	-	-	-	-	-	0000	00h

Table 19. Register allocation map ...continued

Addr. (hex)	Register name	R/W	Bit definition								Default	
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
JESD204A/JESD204B control												
0800h	IP_DIGITAL_ID	R/W	1	0	1	0	IP_DIG_ID[3]	IP_DIG_ID[2]	IP_DIG_ID[1]	IP_DIG_ID[0]	1010 0000	
0801h	IP_STATUS	R/W	RXSYNC_ERR_FLG	RES_BONDING[2:0]			-	-	POR_TST	PLL_INL	0000 0000	
0802h	IP_RESET	R/W	SW_RST	-	-	-	FSM_SW_RST	-	-	-	0000 0000	
0803h	IP_CFG_SETUP	R/W	-	-	-	-	CFG_STP[3:0]			0000 ****		
0805h	IP_CTRL1	R/W	ADC_DIR_SCSB	TRISTATE_CFG_PATH	SYNC_POL	SYNC_SE	EN_RSSYNC_ERR	REV_SCR_IN	REV_ENC_IN	REV_SER_IN	0000 0000	
0806h	IP_CTRL2	R/W	SCR_CLK_DIS	PRECOMP_CLK_DIS	MDSSYNC_CLK_DIS	MDSDATA_CLK_DIS	LANE_MAP[1:0]		SWP_LANE_1_2	SWP_ADC_0_1	0000 ****	
0807h	IP_CTRL3	R/W	MDS_EN	SYNC_LAT[2:0]			DATA_LAT[3:0]			0000 0000		
0808h	IP_SYSREF_TOUT	R/W	SYSREF_TO[7:0]								0000 0000	
0809h	IP_SCR1	R/W	LSB_INIT[7:0]								0000 0000	
080Ah	IP_SCR2	R/W	MSB_INIT[7:0]								1111 1111	
080Bh	IP_PRBS_CTRL	R/W	-	-	-	-	-	PRBS_ON_SYNC	PRBS_TYPE[1:0]		0000 0000	
080Ch	IP_PLL_CTRL1	R/W	CK_DET_CUR[1:0]		ICP_INT[1:0]		PLL_REF_SEL	PLL_INL_BYP	PLL_TST_EN	PLL_PD	0000 00**	
080Dh	IP_PLL_CTRL2	R/W	PLL_CAL_CNTR[7:3]					PLL_P[2:0]			1000 0000	
0816h	IP_DEBUG_OUT1	R/W	-	-	-	-	-	-	PAT_OUT[9:8]		0000 0010	
0817h	IP_DEBUG_OUT2	R/W	PAT_OUT[7:0]								1010 1010	
0818h	IP_DEBUG_IN1	R/W	PAT_IN[15:8]								1010 1010	

Table 19. Register allocation map ...continued

Addr. (hex)	Register name	R/W	Bit definition								Default	
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
0819h	IP_DEBUG_IN2	R/W	PAT_IN[7:0]								0000	0010
081Ah	IP_SPARE_DEBUG	R/W	SPARE_DBG[7:5]			SYNC_TAP_EN	SYNC_TAP_SEL[3:0]					
0860h	OUTBUF01_CTRL	R/W	CTRL_SPARE[2:0]			PREEMPH_CTRL[2:0]		PREEMPH_PD	FULL_PD	0000	0000	
0861h	OUTBUF02_CTRL	R/W	CTRL_SPARE[2:0]			PREEMPH_CTRL[2:0]		PREEMPH_PD	FULL_PD	0000	0000	
0862h	OUTBUF03_CTRL	R/W	CTRL_SPARE[2:0]			PREEMPH_CTRL[2:0]		PREEMPH_PD	FULL_PD	0000	0000	
0863h	OUTBUF04_CTRL	R/W	CTRL_SPARE[2:0]			PREEMPH_CTRL[2:0]		PREEMPH_PD	FULL_PD	0000	0000	
086Ah	OUTBUF01_SWING	R/W	SWING_SPARE[2:0]			SWING[4:0]				0000	01**	
086Bh	OUTBUF02_SWING	R/W	SWING_SPARE[2:0]			SWING[4:0]				0000	01**	
086Ch	OUTBUF03_SWING	R/W	SWING_SPARE[2:0]			SWING[4:0]				0000	01**	
086Dh	OUTBUF04_SWING	R/W	SWING_SPARE[2:0]			SWING[4:0]				0000	01**	
0871h	LANE0_0_CTRL	R/W	LANE_LAT[2:0]			LANE_MODE[1:0]	LANE_POL	LANE_CLK_POS_EDGE	LANE_PD	0000	000*	
0872h	LANE1_0_CTRL	R/W	LANE_LAT[2:0]			LANE_MODE[1:0]	LANE_POL	LANE_CLK_POS_EDGE	LANE_PD	0000	000*	
0890h	ADCA_0_CTRL	R/W	-	-	ADC_MODE[1:0]	-	-	-	ADC_PD	0000	0000	
0891h	ADCB_0_CTRL	R/W	-	-	ADC_MODE[1:0]	-	-	-	ADC_PD	0000	0000	

[1] The READ-ONLY and RESERVED registers.

[2] The registers influenced by the TRANSFER function.

[3] The LOCAL registers.

11.5.3 Detailed register description

The tables in this section contain detailed descriptions of the registers.

11.5.3.1 ADC control registers

Table 20. CHIP_RESET register (address 0000h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	SW_RST	R/W	-	resets global and local registers for any value "1" written at any bit (autoclear).

Table 21. CHIP_RESET register (address 0005h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	SW_RST	R/W	0	resets global and local registers no reset
			1	performs a reset to the default values (autoclear)
6 to 0	-	-	-	not used

Table 22. OP_MODE register (address 0006h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 2	-	-	-	not used
1 to 0	OP_MODE[1:0] ^[1]	R/W	00	operating mode for the selected channel normal (power-up)
			01	power-down
			10	sleep
			11	not used

[1] Local register.

Table 23. CLK_CFG register (address 0007h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	-	-	-	not used
4	SE_SEL	R/W	0	single-ended clock input pin selection CLKP
			1	CLKM
3	DIFF_SE	R/W	0	differential/single-ended clock input selection fully differential
			1	single-ended

Table 23. CLK_CFG register (address 0007h) bit description ...continued

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
2 to 0	CLK_DIV[1:0]	R/W		clock divider selection
			000	divide by 1
			001	divide by 2
			010	divide by 3
			011	divide by 4
			100	divide by 5
			101	divide by 6
			110	divide by 7
			111	divide by 8

Table 24. INTERNAL_REF register (address 0008h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 3	-	-	-	not used
2 to 0	INTREF[2:0] ^[1]	R/W	-	see Table 10

[1] Local register

Table 25. CHANNEL_SEL register (address 0009h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 2	-	-	-	not used
1	ADC_B	R/W		channel B selection for next SPI operation in local registers
			0	not selected
			1	selected
0	ADC_A	R/W		channel A selection for next SPI operation in local registers
			0	not selected
			1	selected

Table 26. OUTPUT_CFG register (address 0011h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 3	-	-	-	not used
2	DATA_SWAP ^[1]	R/W		output data bits swapped
			0	no swapping
			1	MSBs swapped with LSBs

Table 26. OUTPUT_CFG register (address 0011h) bit description ...continued

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
1 to 0	DATA_FORMAT[1:0] ^[1]	R/W		output data format
			00	offset binary
			01	two's complement
			10	gray code
			11	offset binary

[1] Local register

Table 27. DIG_OFFSET register (address 0013h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 2	DIG_OFFSET[7:0] ^[1]	R/W	-	see Table 13
1 to 0	-	-	-	not used

[1] Local register

Table 28. TEST_CFG_1 register (address 0014h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 3	-	-	-	not used
2 to 0	TEST_PAT_SEL[2:0] ^[1]	R/W	-	see Table 14

[1] Local register

Table 29. TEST_CFG_2 register (address 0015h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	TEST_PAT_USER[13:6] ^[1]	R/W	-	custom digital test pattern (bits 13 to 6)

[1] Local register

Table 30. TEST_CFG_3 register (address 0016h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 2	TEST_PAT_USER[5:0] ^[1]	R/W	-	custom digital test pattern (bits 7 to 0)
1 to 0	-	-	-	not used

[1] Local register

Table 31. OTR_CFG register (address 0017h) bit description*Default settings are shown highlighted.*

Bit	Symbol	Access	Value	Description
7 to 4	-	-	-	not used
3	FAST_OTR ^[1]	R/W	0 1	Selection OTR full-scale/ fast OTR OTR full-scale fast OTR
2 to 0	FAST_OTR_DET[3:0] ^[1]	R/W	-	

[1] Local register

Table 32. TRANS_CFG register (address 00FFh) bit description*Default settings are shown highlighted.*

Bit	Symbol	Access	Value	Description
7	TRANS_DIS	R/W	0 1	disable transfer function transfer function active registers updated on a WRITE command
6	TRANSFER	R/W	0 1	updates the registers with the written settings settings are stored registers updated (autoclear)
5 to 0	-	-	-	not used

11.5.3.2 JESD204A/JESD204B control registers

Table 33. IP_DIGITAL_ID register (address 0800h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	-	-	1010	not used
3 to 0	IP_DIG_ID[3:0]	R/W	****	

Table 34. IP_STATUS register (address 0801h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	RXSYNC_ERR_FLG	R/W	0	
6 to 4	RES_BONDING[2:0]	R/W	000	
3 to 2	-	-	0	not used
1	POR_TST	R/W	0	power-on reset
0	PLL_INLOCK	R/W	0	

Table 35. IP_RESET register (address 0802h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	SW_RST	R/W	0	initiates a software reset of the JEDEC204A/JESD204B unit
6 to 4	-	-	000	not used
3	FSM_SW_RST	R/W	0	initiates a software reset of the internal state machine of JEDEC204A/JESD204B unit
2 to 0	-	-	000	not used

Table 36. IP_CFG_SETUP register (address 0803h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	-	-	0000	not used
3 to 0	CFG_SETUP[3:0]	R/W	****	

Table 37. IP_CTRL1 register (address 0805h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	ADC_DIRECT_SCSB	R/W	0	
6	TRISTATE_CFG_PATH	R/W	0 (1 > 0)	
5	SYNC_POL	R/W	0	synchronization polarity
4	SYNC_SE	R/W	0	
3	EN_RSSYNC_ERR	R/W	1	
2	REV_SCR_IN	R/W	0	
1	REV_ENC_IN	R/W	0	
0	REV_SER_IN	R/W	1	

Table 38. IP_CTRL2 register (address 0806h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	SCR_CLK_DIS	R/W	0	
6	PRECOMP_CLK_DIS	R/W	0	
5	MDSSYNC_CLK_DIS	R/W	0	
4	MDSDATA_CLK_DIS	R/W	0	
3 to 2	LANE_MAPPING[1:0]	R/W	**	
1	SWP_LANE_1_2	R/W	*	
0	SWP_ADC_0_1	R/W	*	

Table 39. IP_CTRL3 register (address 0807h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	MDS_EN	R/W	0	
6 to 4	SYNC_LATENCY[2:0]	R/W	000	
3 to 0	DATA_LATENCY[3:0]	R/W	0000	

Table 40. IP_SYSREF_TIME_OUT register (address 0808h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	SYSREF_TO[7:0]	R/W	0000 0000	

Table 41. IP_SCRAMBLER1 register (address 0809h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	LSB_INIT[7:0]	R/W	0000 0000	

Table 42. IP_SCRAMBLER2 register (address 080Ah) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	MSB_INIT[7:0]	R/W	1111 1111	

Table 43. IP_PRBS_CTRL register (address 080Bh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 3	-	-	00000	not used
2	PRBS_ON_SYNC	R/W	0	
1 to 0	PRBS_TYPE[1:0]	R/W	00	

Table 44. IP_PLL_CTRL1 register (address 080Ch) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	CK_DET_CUR[1:0]	R/W	00	
5 to 4	ICP_INT[1:0]	R/W	00	
3	PLL_REF_SEL	R/W	0	

Table 44. IP_PLL_CTRL1 register (address 080Ch) bit description ...continued

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
2	PLL_INLOCK_BYPASS	R/W	0	
1	PLL_TST_EN	R/W	*	
0	PLL_PD	R/W	*	

Table 45. IP_PLL_CTRL2 register (address 080Dh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 3	PLL_CAL_CNTR[7:3]	R/W	10000	
2 to 0	PLL_P[2:0]	R/W	000	

Table 46. IP_DEBUG_OUT1 register (address 0816h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 2	-	-	000000	not used
1 to 0	PATTERN_OUT[9:8]	R/W	10	

Table 47. IP_DEBUG_OUT2 register (address 0817h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	PATTERN_OUT[7:0]	R/W	1010 1010	

Table 48. IP_DEBUG_IN1 register (address 0818h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	PATTERN_IN[15:8]	R/W	1010 1010	

Table 49. IP_DEBUG_IN2 register (address 0819h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	PATTERN_IN[7:0]	R/W	0000 0010	

Table 50. IP_SPARE_DEBUG register (address 081Ah) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	SPARE_DEBUG[7:5]	R/W	<td>	
4	SYNC_TAP_EN	R/W	<td>	
3 to 0	SYNC_TAP_SEL[3:0]	R/W	<td>	

Table 51. IP_OUTBUF01_CTRL register (address 0860h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	CTRL_SPARE[2:0]	R/W	000	
4 to 2	PREEMPH_CTRL[2:0]	R/W	000	
1	PREEMPH_PD	R/W	0	
0	FULL_PD	R/W	0	

Table 52. IP_OUTBUF02_CTRL register (address 0861h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	CTRL_SPARE[2:0]	R/W	000	
4 to 2	PREEMPH_CTRL[2:0]	R/W	000	
1	PREEMPH_PD	R/W	0	
0	FULL_PD	R/W	0	

Table 53. IP_OUTBUF03_CTRL register (address 0862h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	CTRL_SPARE[2:0]	R/W	000	
4 to 2	PREEMPH_CTRL[2:0]	R/W	000	
1	PREEMPH_PD	R/W	0	
0	FULL_PD	R/W	0	

Table 54. IP_OUTBUF04_CTRL register (address 0863h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	CTRL_SPARE[2:0]	R/W	000	
4 to 2	PREEMPH_CTRL[2:0]	R/W	000	
1	PREEMPH_PD	R/W	0	
0	FULL_PD	R/W	0	

Table 55. IP_OUTBUF01_SWING register (address 086Ah) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	SWING_SPARE[2:0]	R/W	000	
4 to 0	SWING[4:0]	R/W	001**	

Table 56. IP_OUTBUF02_SWING register (address 086Bh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	SWING_SPARE[2:0]	R/W	000	
4 to 0	SWING[4:0]	R/W	001**	

Table 57. IP_OUTBUF03_SWING register (address 086Ch) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	SWING_SPARE[2:0]	R/W	000	
4 to 0	SWING[4:0]	R/W	001**	

Table 58. IP_OUTBUF04_SWING register (address 086Dh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	SWING_SPARE[2:0]	R/W	000	
4 to 0	SWING[4:0]	R/W	001**	

Table 59. IP_LANE0_0_CTRL register (address 0871h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	LANE_LATENCY[2:0]	R/W	000	
4 to 3	LANE_MODE[1:0]	R/W	00	
2	LANE_POL	R/W	0	
1	LANE_CLK_POS_EDGE	R/W	0	
0	LANE_PD	R/W	*	

Table 60. IP_LANE1_0_CTRL register (address 0872h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	LANE_LATENCY[2:0]	R/W	000	
4 to 3	LANE_MODE[1:0]	R/W	00	
2	LANE_POL	R/W	0	
1	LANE_CLK_POS_EDGE	R/W	0	
0	LANE_PD	R/W	*	

Table 61. IP_ADCA_0_CTRL register (address 0890h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	-	-	00	not used
5 to 4	ADC_MODE[1:0]	R/W	00	
3 to 1	-	-	000	not used
0	ADC_PD	R/W	0	

Table 62. IP_ADCB_0_CTRL register (address 0891h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	-	-	00	not used
5 to 4	ADC_MODE[1:0]	R/W	00	
3 to 1	-	-	000	not used
0	ADC_PD	R/W	0	

12. Package outline

HLQFN56R: plastic thermal enhanced low profile quad flat package; no leads; 56 terminals; resin based; body 8 x 8 x 1.35 mm

SOT935-2

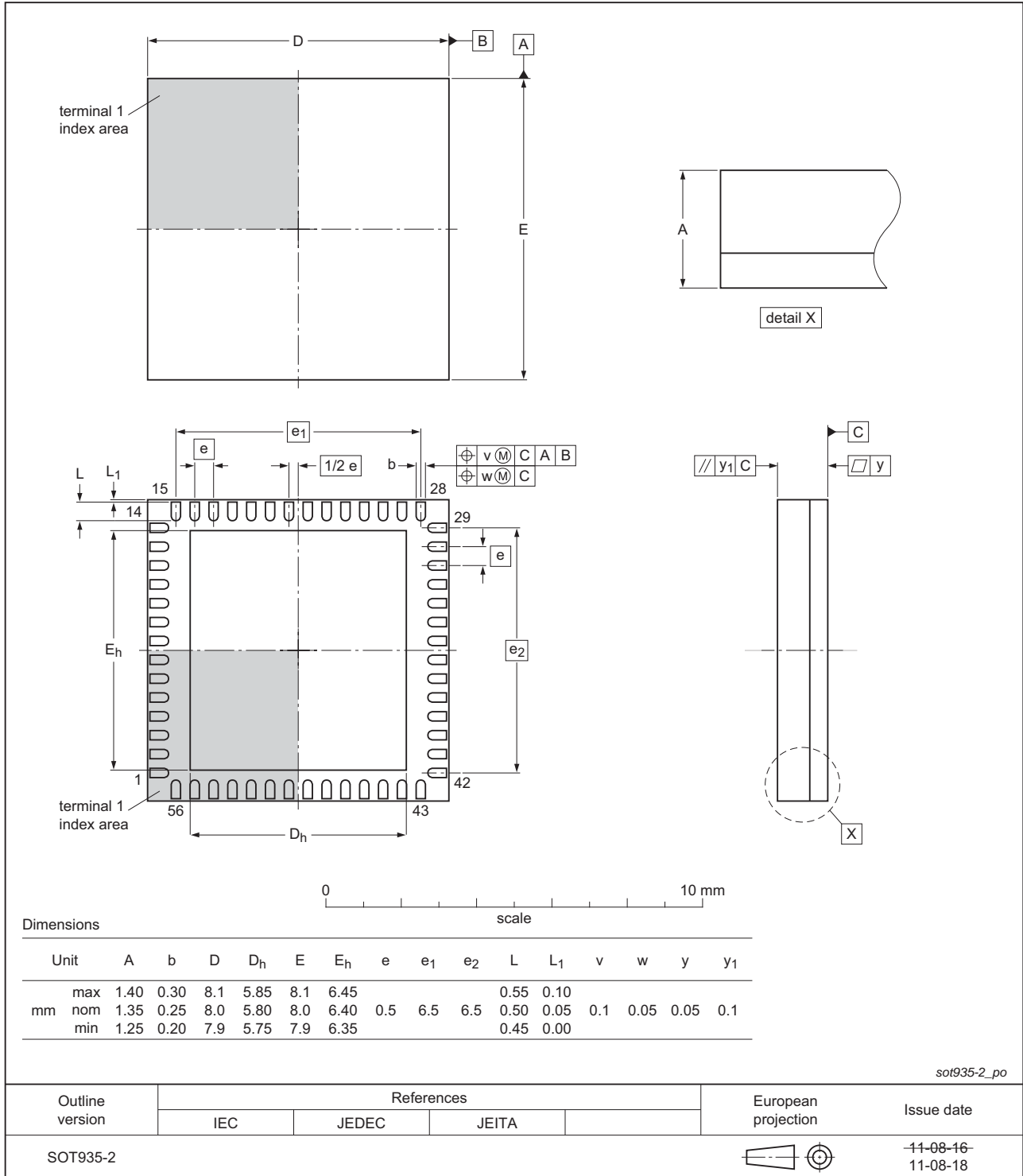


Fig 38. Package outline SOT935-2 (HLQFN56)

13. Abbreviations

Table 63. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
CDMA	Code Division Multiple Access
DAV	DAta Valid
ESD	ElectroStatic Discharge
FFT	Fast Fourier Transform
GSM	Global System for Mobile communications
IMD3	third order InterMoDulation product
LSB	Least Significant Bit
LTE	Long-Term Evolution
LVDS DDR	Low Voltage Differential Signaling Double Data Rate
LVPECL	Low-Voltage Positive Emitter-Coupled Logic
MIMO	Multiple Input Multiple Output
MSB	Most Significant Bit
OTR	OuT-of-Range
SFDR	Spurious-Free Dynamic Range
SPI	Serial Peripheral Interface
SNR	Signal-to-Noise Ratio
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
WCDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide interoperability for Microwave Access

14. Revision history

Table 64. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ADC1443D_SER v.1.1	20110928	Objective data sheet	-	ADC1443D_SER v.1
Modifications:	<ul style="list-style-type: none"> • Section 1 “General description” has been updated. • Section 2 “Features and benefits” has been updated. • Section 3 “Applications” has been updated. • Table 5 has been updated. 			
ADC1443D_SER v.1	20110901	Objective data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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17. Contents

1	General description	1	11.5.3	Detailed register description	36
2	Features and benefits	1	11.5.3.1	ADC control registers	36
3	Applications	2	11.5.3.2	JESD204A/JESD204B control registers	40
4	Ordering information	2	12	Package outline	45
5	Block diagram	3	13	Abbreviations	46
6	Pinning information	4	14	Revision history	47
6.1	Pinning	4	15	Legal information	48
6.2	Pin description	5	15.1	Data sheet status	48
7	Limiting values	7	15.2	Definitions	48
8	Thermal characteristics	7	15.3	Disclaimers	48
9	Static characteristics	7	15.4	Trademarks	49
10	Dynamic characteristics	10	16	Contact information	49
10.1	Dynamic characteristics	10	17	Contents	50
10.2	Timing	14			
10.2.1	Clock timing	14			
10.2.2	SYSREF timing	14			
10.2.3	SPI timing	15			
10.3	Typical dynamic performances	16			
11	Application information	20			
11.1	Analog inputs	20			
11.1.1	Input stage	20			
11.1.2	Common-mode input voltage ($V_{I(cm)}$)	20			
11.1.3	Pin VCM	20			
11.1.4	Programmable full-scale	21			
11.1.5	Anti-kickback circuitry	21			
11.1.6	Transformer	22			
11.2	Clock input	23			
11.2.1	Drive modes	23			
11.2.2	Equivalent input circuit	25			
11.2.3	Clock input divider	25			
11.2.4	Multi-device synchronization (pins SYSREF, SYSREFN and SYSREFP)	25			
11.3	Digital outputs	25			
11.3.1	Digital output buffers	25			
11.3.2	JESD204A/JESD204B serializer	26			
11.3.2.1	Digital JESD204A/JESD204B formatter	26			
11.3.3	OuT-of-Range (OTR)	28			
11.3.4	Digital offset	28			
11.3.5	Test patterns	29			
11.3.6	Output data format selection	29			
11.3.7	Output codes versus input voltage	29			
11.4	Configuration pins (CFG0, CFG1, CFG2, CFG3)	30			
11.5	Serial Peripheral Interface (SPI)	31			
11.5.1	Register description	31			
11.5.2	Register allocation map	33			

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