

BLF3G21-6

UHF power LDMOS transistor

Rev. 01 — 25 June 2008

Product data sheet

1. Product profile

1.1 General description

6 W LDMOS power transistor for base station applications at frequencies from HF to 2200 MHz

Table 1. Typical class-AB RF performance

$I_{Dq} = 90 \text{ mA}$; $T_h = 25^\circ\text{C}$ in a common source test circuit.

Mode of operation	f (MHz)	P_L (W)	G_p (dB)	η_D (%)	IMD3 (dB)	$P_{L(1dB)}$ (W)
CW	2000	7	12.5	43	-	7
Two-tone	2000	6	15.5	39	-32	-
		< 2	15.8	-	< -50	-

Table 2. Typical class-A RF performance

$I_{Dq} = 200 \text{ mA}$; $T_h = 25^\circ\text{C}$ in a modified PHS test fixture.

Mode of operation	f (MHz)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR _{600k} (dBc)
PHS	1880 to 1920	2	16	20	-75

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

- Excellent back-off linearity
- Typical PHS performance at a supply voltage of 26 V and I_{Dq} of 200 mA:
 - ◆ Average output power = 2 W
 - ◆ Power gain = 16 dB
 - ◆ Efficiency = 20 %
 - ◆ ACPR_{600k} = -75 dBc
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (HF to 2200 MHz)

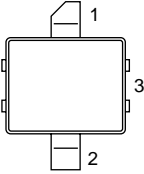
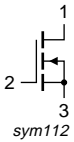
- No internal matching for broadband operation
- ESD protection

1.3 Applications

- RF power amplifiers for GSM, PHS, EDGE, CDMA and W-CDMA base stations and multicarrier applications in the HF to 2200 MHz frequency range
- Broadcast drivers

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source		

[1] Connected to flange.

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
BLF3G21-6	-	ceramic surface-mounted package; 2 leads	SOT538A

4. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	±13	V
I_D	drain current		-	2.3	A
T_{stg}	storage temperature		-65	+200	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_h = 25\text{ °C}; P_{L(AV)} = 15\text{ W}$	[1] 10	K/W

[1] Thermal resistance is determined under specified RF operating conditions.

6. Characteristics

Table 7. Characteristics

$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.13\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 13\text{ mA}$	2.0	2.6	3.0	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	1	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 6\text{ V};$ $V_{DS} = 10\text{ V}$	1.85	2.3	-	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 15\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 0.5\text{ A}$	-	0.6	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 9\text{ V}; I_D = 0.5\text{ A}$	-	1.6	2.07	Ω
C_{rs}	feedback capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V};$ $f = 1\text{ MHz}$	-	0.3	-	pF

7. Application information

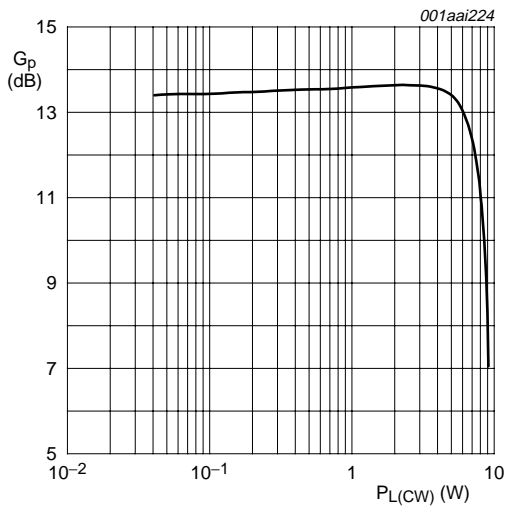
Table 8. Application information

$V_{DS} = 26\text{ V}; T_h = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Mode of operation: Two-tone CW (100 kHz tone spacing); $f = 2000\text{ MHz}; I_{Dq} = 90\text{ mA}$						
G_p	power gain	$P_{L(PEP)} = 6\text{ W}$	14	15.5	-	dB
RL_{in}	input return loss	$P_{L(PEP)} = 6\text{ W}$	-	-7	-3	dB
η_D	drain efficiency	$P_{L(PEP)} = 6\text{ W}$	35	39	-	%
IMD3	third order intermodulation distortion	$P_{L(PEP)} = 6\text{ W}$	-	-32	-29	dBc
		$P_{L(PEP)} < 2\text{ W}$	-	< -50	-	dBc
Mode of operation: one-tone CW; $f = 2000\text{ MHz}; I_{Dq} = 90\text{ mA}$						
G_p	power gain	$P_L = P_{L(1dB)} = 7\text{ W}$	-	12.5	-	dB
η_D	drain efficiency	$P_L = P_{L(1dB)} = 7\text{ W}$	-	43	-	%
Mode of operation: PHS; $f = 1900\text{ MHz}; I_{Dq} = 200\text{ mA}$						
G_p	power gain	$P_{L(AV)} = 2\text{ W}$	-	16	-	dB
η_D	drain efficiency	$P_{L(AV)} = 2\text{ W}$	-	20	-	%
$ACPR_{600k}$	adjacent channel power ratio (600 kHz)	$P_{L(AV)} = 2\text{ W}$	-	-75	-	dBc

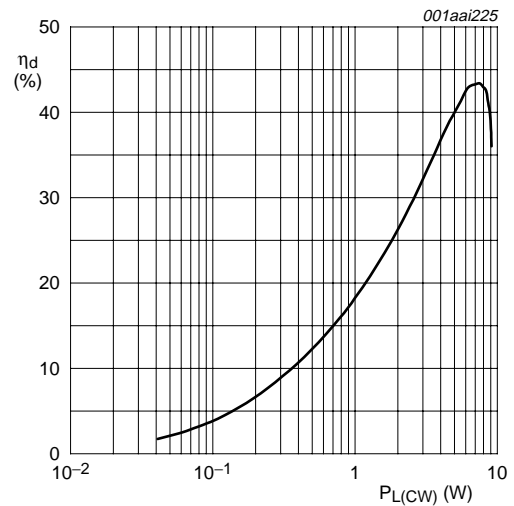
7.1 Ruggedness in class-AB operation

The BLF3G21-6 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 26\text{ V}$; $f = 2200\text{ MHz}$ at rated load power.



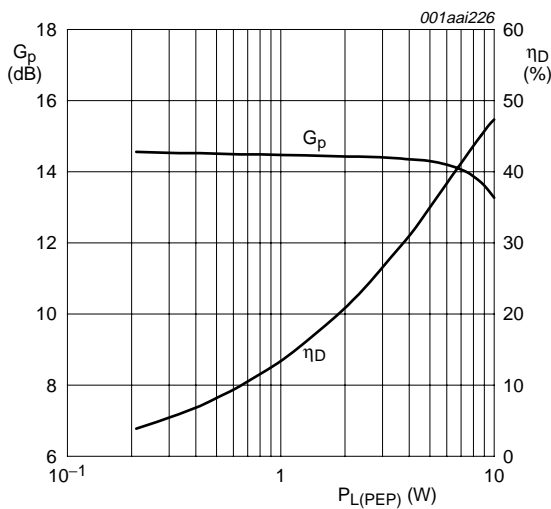
$V_{DS} = 26\text{ V}$; $I_{DQ} = 90\text{ mA}$; $T_h = 25\text{ }^\circ\text{C}$; $f = 2000\text{ MHz}$.

Fig 1. Power gain as a function of CW load power; typical values



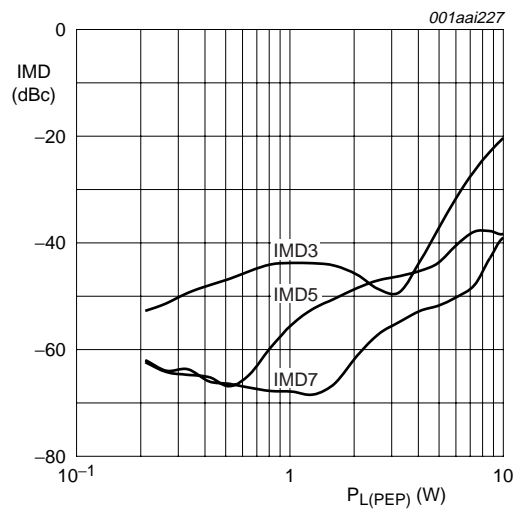
$V_{DS} = 26\text{ V}$; $I_{DQ} = 90\text{ mA}$; $T_h = 25\text{ }^\circ\text{C}$; $f = 2000\text{ MHz}$.

Fig 2. Drain efficiency as a function of CW load power; typical values



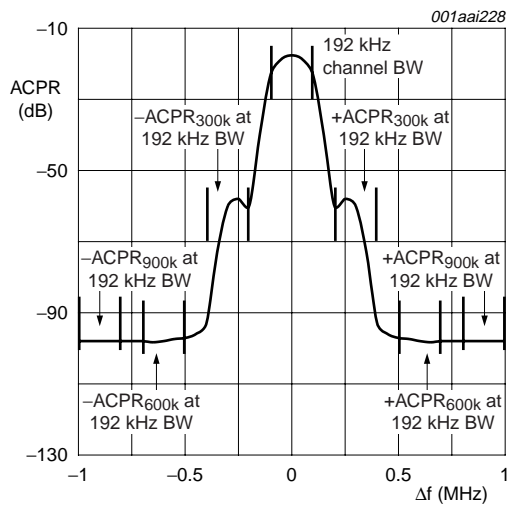
$V_{DS} = 26\text{ V}$; $I_{DQ} = 90\text{ mA}$; $T_h \leq 25\text{ }^\circ\text{C}$; $f_1 = 2000\text{ MHz}$; $f_2 = 2000.1\text{ MHz}$.

Fig 3. Two-tone power gain and drain efficiency as a function of peak envelope load power; typical values



$V_{DS} = 26\text{ V}$; $I_{DQ} = 90\text{ mA}$; $T_h \leq 25\text{ }^\circ\text{C}$; $f_1 = 2000\text{ MHz}$; $f_2 = 2000.1\text{ MHz}$.

Fig 4. Two-tone intermodulation distortion as a function of peak envelope load power; typical values



$V_{DS} = 26\text{ V}$; $I_{Dq} = 200\text{ mA}$; $T_h \leq 25\text{ }^\circ\text{C}$; $f_c = 1900\text{ MHz}$; $P_{L(AV)} = 2\text{ W}$.

Fig 5. ACPR performance under PHS conditions, measured in application board.

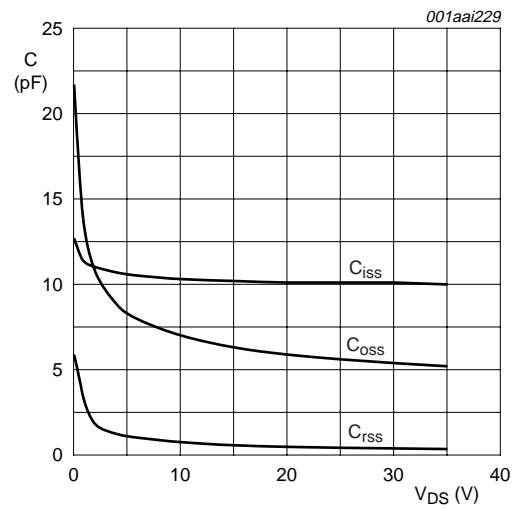
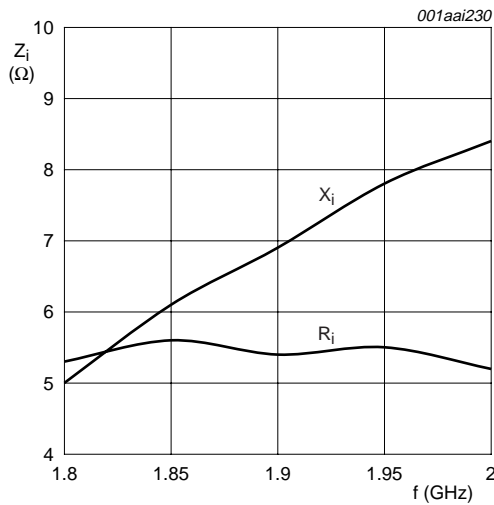
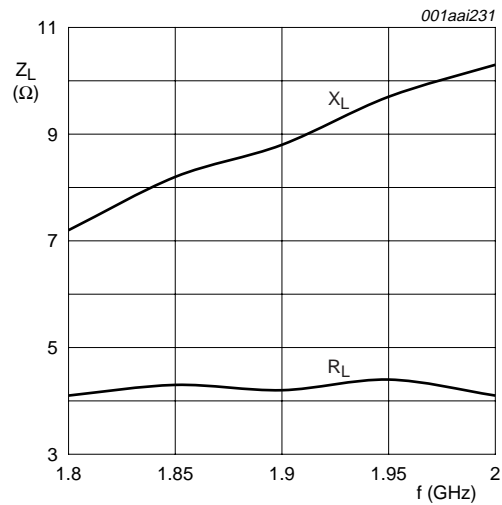


Fig 6. C_{iss} , C_{rss} and C_{oss} as function of drain supply voltage; typical values.



$V_{DS} = 26\text{ V}$; $I_{Dq} = 90\text{ mA}$; $P_L = 45\text{ W}$; $T_h \leq 25\text{ }^\circ\text{C}$.

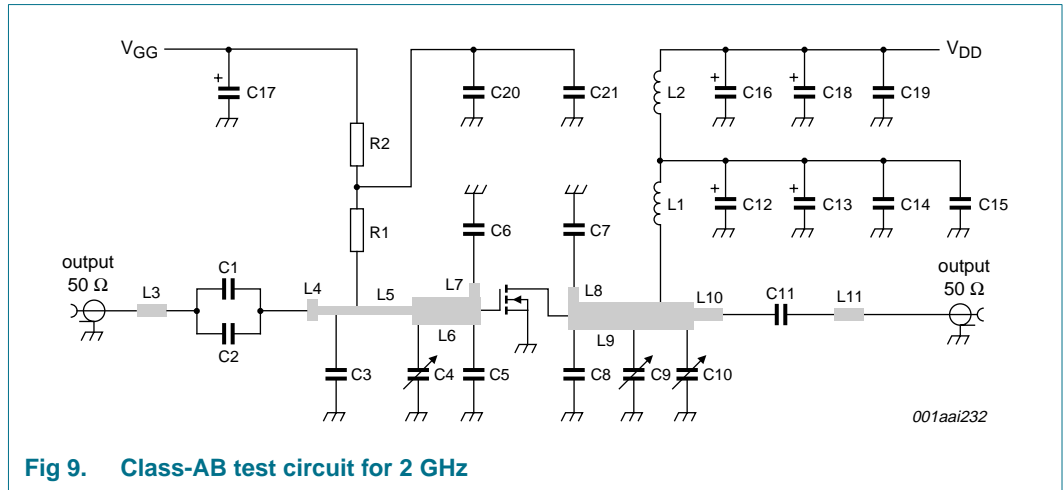
Fig 7. Input impedance as a function of frequency (series components); typical values

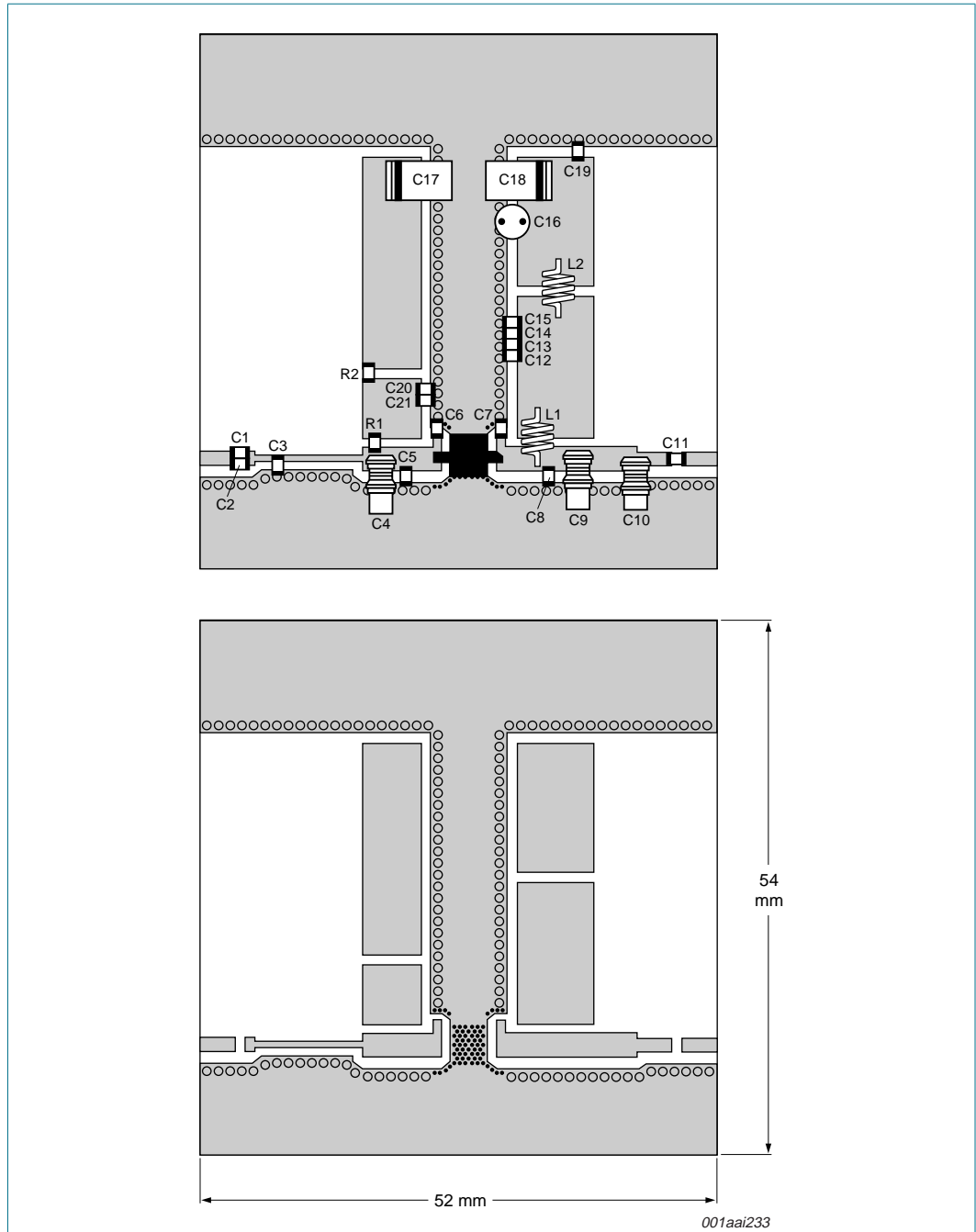


$V_{DS} = 26\text{ V}$; $I_{Dq} = 90\text{ mA}$; $P_L = 45\text{ W}$; $T_h \leq 25\text{ }^\circ\text{C}$.

Fig 8. Load impedance as a function of frequency (series components); typical values

8. Test information





Dimensions in mm.

The components are situated on one side of the copper-clad Printed-Circuit Board (PCB) with Teflon dielectric ($\epsilon_r = 2.2$); thickness = 0.51 mm.

The other side is unetched and serves as a ground plane.

See [Table 9](#) for list of components.

Fig 10. Component layout for 2 GHz class-AB test circuit

Table 9. List of components (see Figure 9 and Figure 10)

Component	Description	Value	Remarks
C1, C2, C11	multilayer ceramic chip capacitor	[1] 6.8 pF	
C4, C10	Tekelec variable capacitor; type 37281	0.4 pF to 2.5 pF	
C6	multilayer ceramic chip capacitor	[1] 2.7 pF	
C7	multilayer ceramic chip capacitor	[1] 2.0 pF	
C8	multilayer ceramic chip capacitor	[1] 0.2 nF	
C9	Tekelec variable capacitor; type 37281	0.6 pF to 4.5 pF	
C12	multilayer ceramic chip capacitor	[1] 10 pF	
C13	multilayer ceramic chip capacitor	[1] 51 pF	
C14	multilayer ceramic chip capacitor	[1] 120 pF	
C15	multilayer ceramic chip capacitor	100 nF	
C16	electrolytic capacitor	100 μ F; 63 V	
C17, C18	tantalum SMD capacitor	10 μ F; 35 V	
C19	multilayer ceramic chip capacitor	[2] 1 nF	
C20	multilayer ceramic chip capacitor	[1] 22 pF	
C21	multilayer ceramic chip capacitor	[1] 560 pF	
L1, L2	3 turns enamelled copper wire	[3] D = 2 mm; d = 0.8 mm; length = 3 mm	
L3	stripline	[3] 50 Ω	(L \times W) 3.5 mm \times 1.5 mm
L3	stripline	[3] 34.3 Ω	(L \times W) 1.0 mm \times 1.5 mm
L4	stripline	[3] 50 Ω	(L \times W) 11.0 mm \times 0.8 mm
L5	stripline	[3] 34.3 Ω	(L \times W) 8.0 mm \times 3.0 mm
L6	stripline	[3] 23.6 Ω	(L \times W) 1.5 mm \times 1.0 mm
L7, L8	stripline	[3] 5.6 Ω	(L \times W) 14.4 mm \times 3.0 mm
L9	stripline	[3] 3.5 Ω	(L \times W) 3.5 mm \times 1.5 mm
L10, L11	stripline	[3] 31.9 Ω	(L \times W) 12.0 mm \times 1.9 mm
R1	SMD resistor	470 Ω	
R2	SMD resistor	1 k Ω	

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

[3] The striplines are on a double copper-clad Printed-Circuit Board (PCB) with Rogers 5880 dielectric ($\epsilon_r = 2.2$); thickness = 0.51 mm.

9. Package outline

Ceramic surface-mounted package; 2 leads

SOT538A

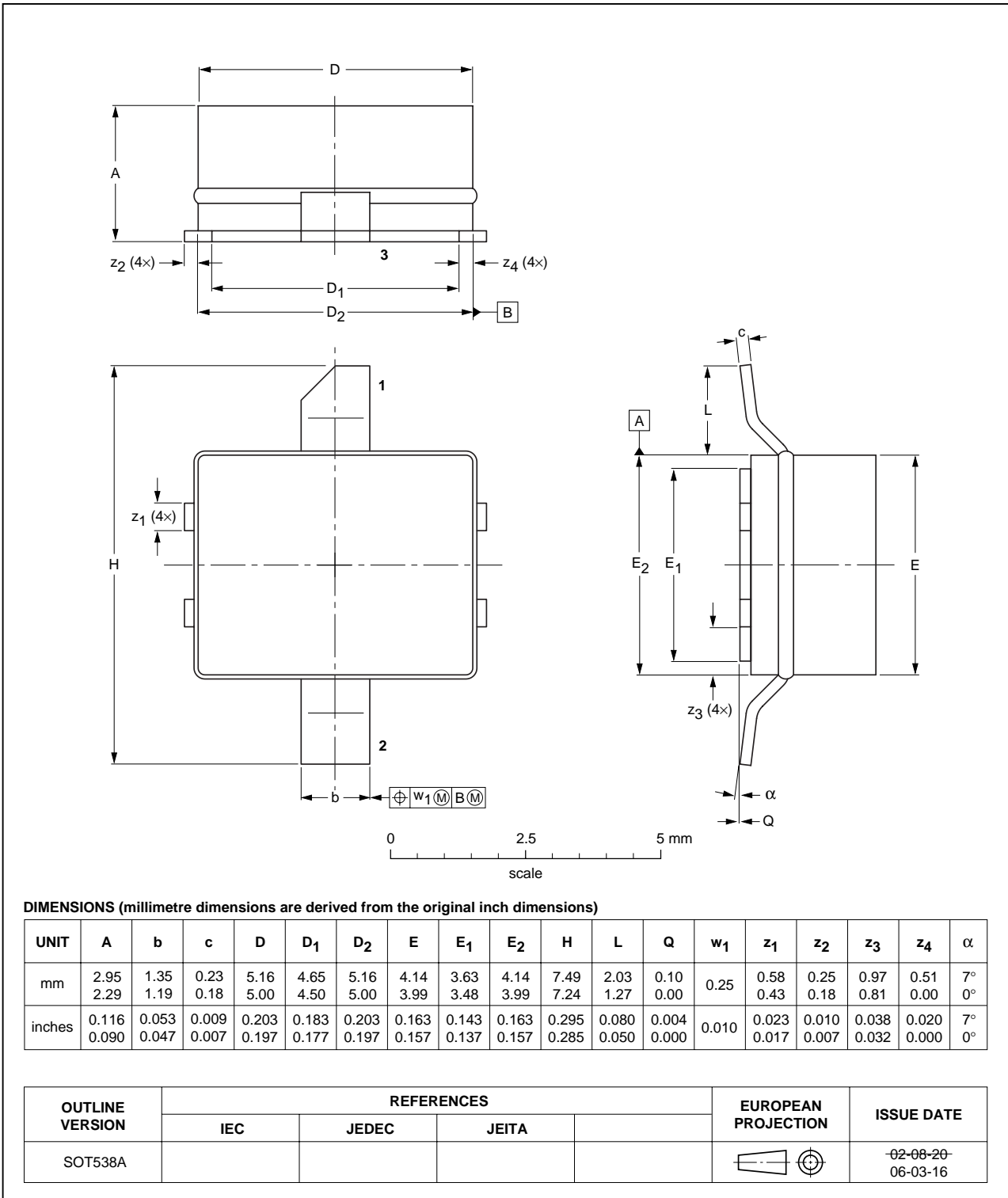


Fig 11. Package outline SOT538A

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDMA	Code Division Multiple Access
EDGE	Enhanced Data rates for GSM Evolution
GSM	Global System for Mobile communications
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PHS	Personal Handy-phone System
RF	Radio Frequency
SMD	Surface Mount Device
UHF	Ultra High Frequency
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF3G21-6_1	20080625	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

1 Product profile 1

1.1 General description 1

1.2 Features 1

1.3 Applications 2

2 Pinning information 2

3 Ordering information 2

4 Limiting values 2

5 Thermal characteristics 3

6 Characteristics 3

7 Application information 3

7.1 Ruggedness in class-AB operation 4

8 Test information 6

9 Package outline 9

10 Abbreviations 10

11 Revision history 10

12 Legal information 11

12.1 Data sheet status 11

12.2 Definitions 11

12.3 Disclaimers 11

12.4 Trademarks 11

13 Contact information 11

14 Contents 12

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