

BLF6G20-45; BLF6G20S-45

Power LDMOS transistor

Rev. 02 — 25 August 2008

Product data sheet

1. Product profile

1.1 General description

45 W LDMOS power transistor for base station applications at frequencies from 1800 MHz to 2000 MHz.

Table 1. Typical performance

RF performance at $T_{case} = 25\text{ }^{\circ}\text{C}$ in a common source class-AB production test circuit.

Mode of operation	f (MHz)	V _{DS} (V)	P _{L(AV)} (W)	G _p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA	1805 to 1880	28	2.5	19.2	14	-50 ^[1]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing 5 MHz.

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

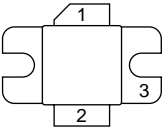
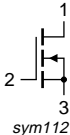
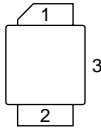
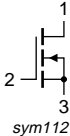
- Typical 2-carrier W-CDMA performance at frequencies of 1805 MHz and 1880 MHz, a supply voltage of 28 V and an I_{Dq} of 360 mA:
 - ◆ Average output power = 2.5 W
 - ◆ Power gain = 19.2 dB (typ)
 - ◆ Efficiency = 14 %
 - ◆ ACPR = -50 dBc
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1800 MHz to 2000 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 1800 MHz to 2000 MHz frequency range.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF6G20-45 (SOT608A)			
1	drain		
2	gate		
3	source		
BLF6G20S-45 (SOT608B)			
1	drain		
2	gate		
3	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF6G20-45	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT608A
BLF6G20S-45	-	ceramic earless flanged package; 2 leads	SOT608B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
I_D	drain current		-	13	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_{L(AV)} = 12.5\text{ W}$	1.7	K/W

6. Characteristics

Table 6. Characteristics

$T_j = 25\text{ °C}$ per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.5\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 72\text{ mA}$	1.4	1.9	2.4	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}; I_D = 300\text{ mA}$	1.70	2.30	2.79	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	1.5	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	12.5	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	150	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 3.6\text{ A}$	-	5	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 2.5\text{ A}$	-	0.2	-	Ω

7. Application information

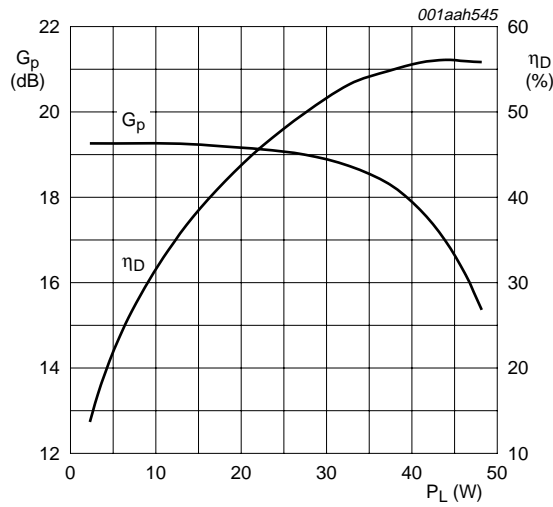
Table 7. Application information

Mode of operation: 2-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1 to 64 PDPCH; $f_1 = 1802.5\text{ MHz}; f_2 = 1807.5\text{ MHz}; f_3 = 1872.5\text{ MHz}; f_4 = 1877.5\text{ MHz};$ RF performance at $V_{DS} = 28\text{ V}; I_{Dq} = 360\text{ mA}; T_{case} = 25\text{ °C};$ unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)} = 2.5\text{ W}$	18.3	19.2	20.8	dB
RL_{in}	input return loss	$P_{L(AV)} = 2.5\text{ W}$	-	-10	-6.5	dB
η_D	drain efficiency	$P_{L(AV)} = 2.5\text{ W}$	12	14	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 2.5\text{ W}$	-	-50	-46	dBc

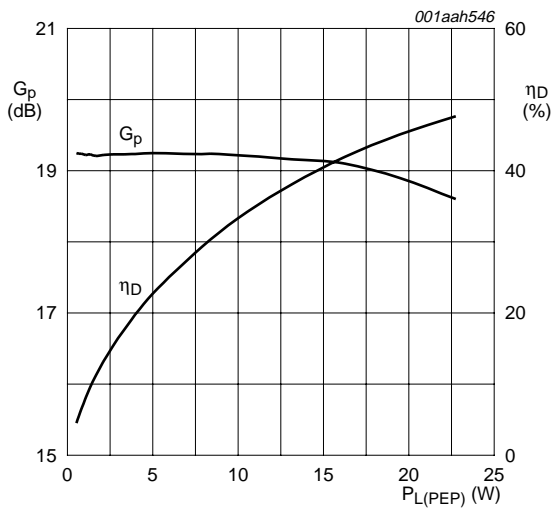
7.1 Ruggedness in class-AB operation

The BLF6G20-45 and BLF6G20S-45 are capable of withstanding a load mismatch corresponding to $VSWR = 10 : 1$ through all phases under the following conditions: $V_{DS} = 28\text{ V}; I_{Dq} = 360\text{ mA}; P_L = 45\text{ W (CW)}; f = 1880\text{ MHz}.$



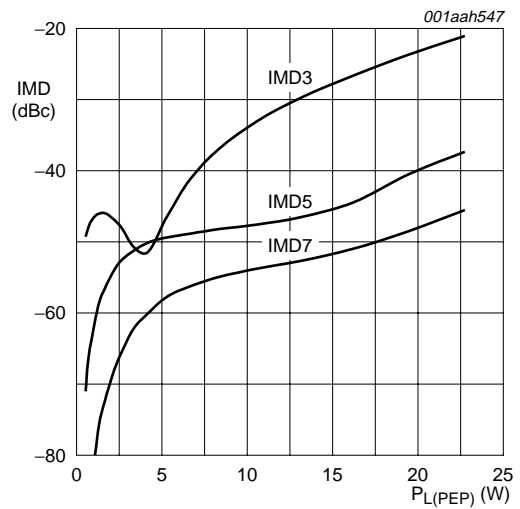
$V_{DS} = 28$ V; $I_{Dq} = 360$ mA; $f = 1842$ MHz.

Fig 1. One-tone CW power gain and drain efficiency as functions of load power; typical values



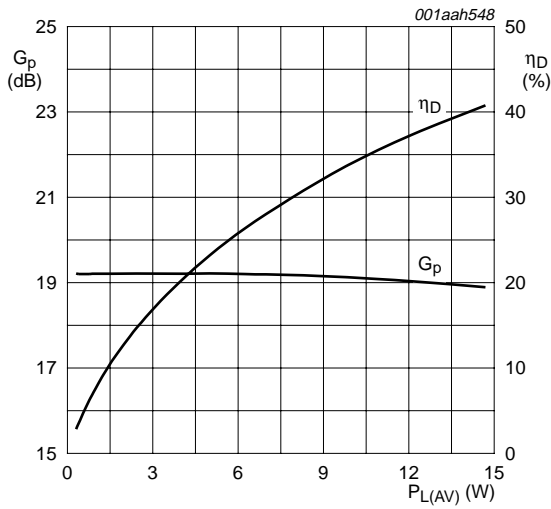
$V_{DS} = 28$ V; $I_{Dq} = 360$ mA; $f_1 = 1843$ MHz; $f_2 = 1843.1$ MHz.

Fig 2. Two-tone CW power gain and drain efficiency as functions of peak envelope load power; typical values



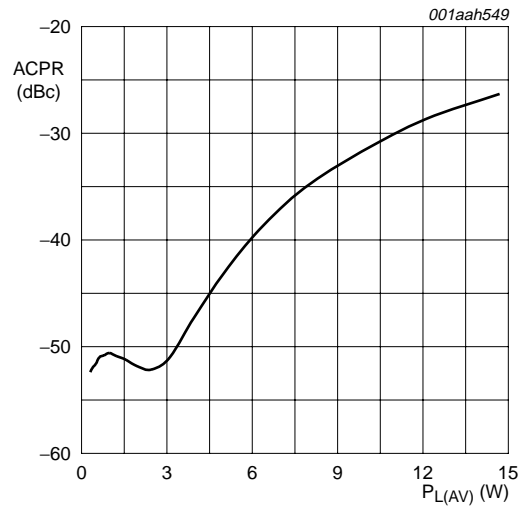
$V_{DS} = 28$ V; $I_{Dq} = 360$ mA; $f_1 = 1843$ MHz; $f_2 = 1843.1$ MHz.

Fig 3. Two-tone CW intermodulation distortion as a function of peak envelope load power; typical values



$V_{DS} = 28\text{ V}$; $I_{DQ} = 360\text{ mA}$; $f_1 = 1840.5\text{ MHz}$; $f_2 = 1845.5\text{ MHz}$; carrier spacing 5 MHz.

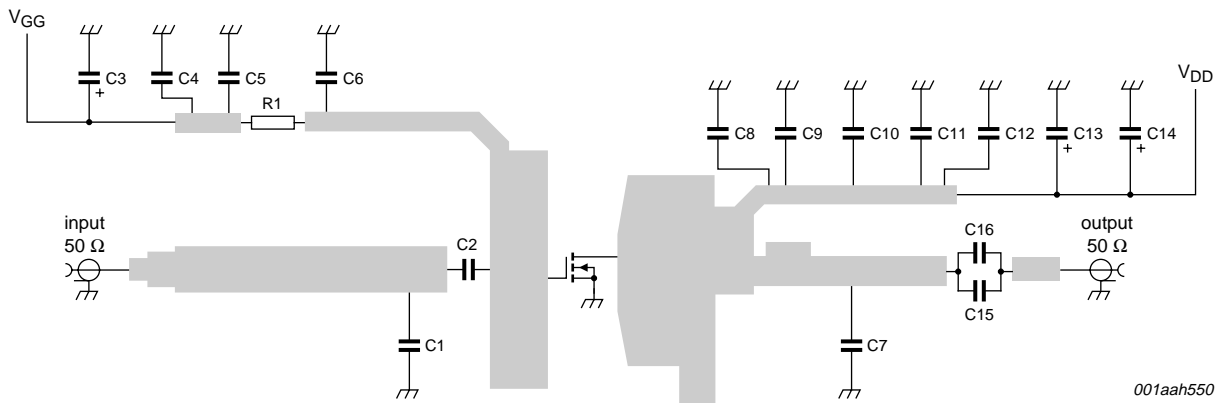
Fig 4. 2-carrier W-CDMA power gain and drain efficiency as functions of average load power; typical values



$V_{DS} = 28\text{ V}$; $I_{DQ} = 360\text{ mA}$; $f_1 = 1840.5\text{ MHz}$; $f_2 = 1845.5\text{ MHz}$; carrier spacing 5 MHz.

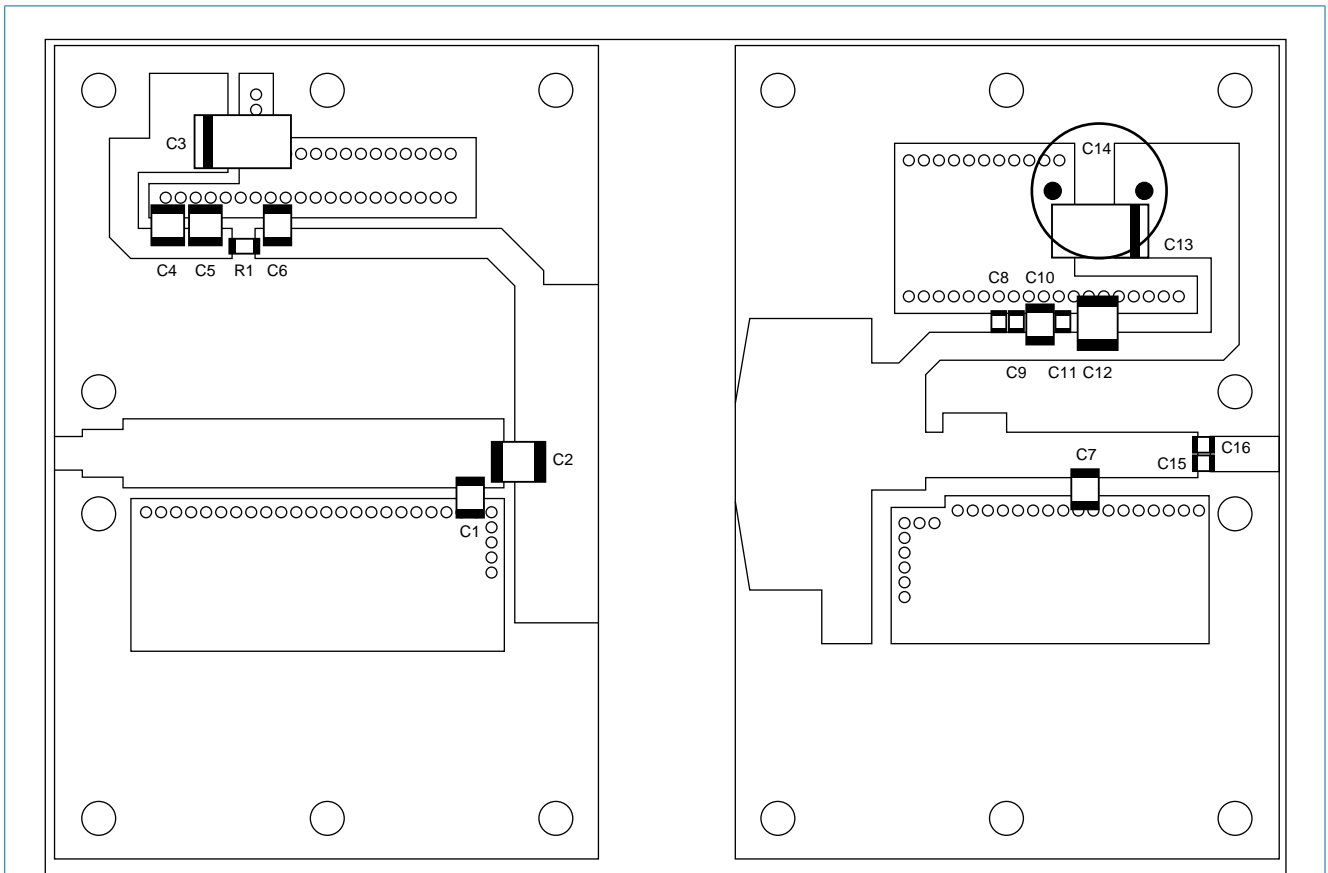
Fig 5. 2-carrier W-CDMA adjacent power channel ratio as function of average load power; typical values

8. Test information



See [Table 8](#) for list of components.

Fig 6. Test circuit for operation at 1805 MHz and 1880 MHz



001aah551

Striplines are on a double copper-clad Rogers Duroid 5880 Printed-Circuit Board (PCB) ($\epsilon_r = 2.2$), thickness = 0.79 mm.
 See [Table 8](#) for list of components.

Fig 7. Component layout for 1805 MHz and 1880 MHz test circuit

Table 8. List of components

For test circuit, see [Figure 6](#) and [Figure 7](#).

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	0.7 pF	[1]
C2	multilayer ceramic chip capacitor	3.9 pF	[1]
C3, C13	tantalum capacitor	10 μ F	
C4, C5	multilayer ceramic chip capacitor	1.5 μ F	
C6, C10	multilayer ceramic chip capacitor	10 pF	[1]
C7	multilayer ceramic chip capacitor	1.2 pF	[1]
C8, C9	multilayer ceramic chip capacitor	100 nF	
C11	multilayer ceramic chip capacitor	220 nF	
C12	multilayer ceramic chip capacitor	4.7 μ F	
C14	Philips electrolytic capacitor	220 μ F, 63 V	
C15, C16	multilayer ceramic chip capacitor	6.8 pF	[2]
R1	Philips chip resistor	5.6 Ω	

[1] American technical ceramics type 100B or capacitor of same quality.

[2] American technical ceramics type 100A or capacitor of same quality.

9. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT608A

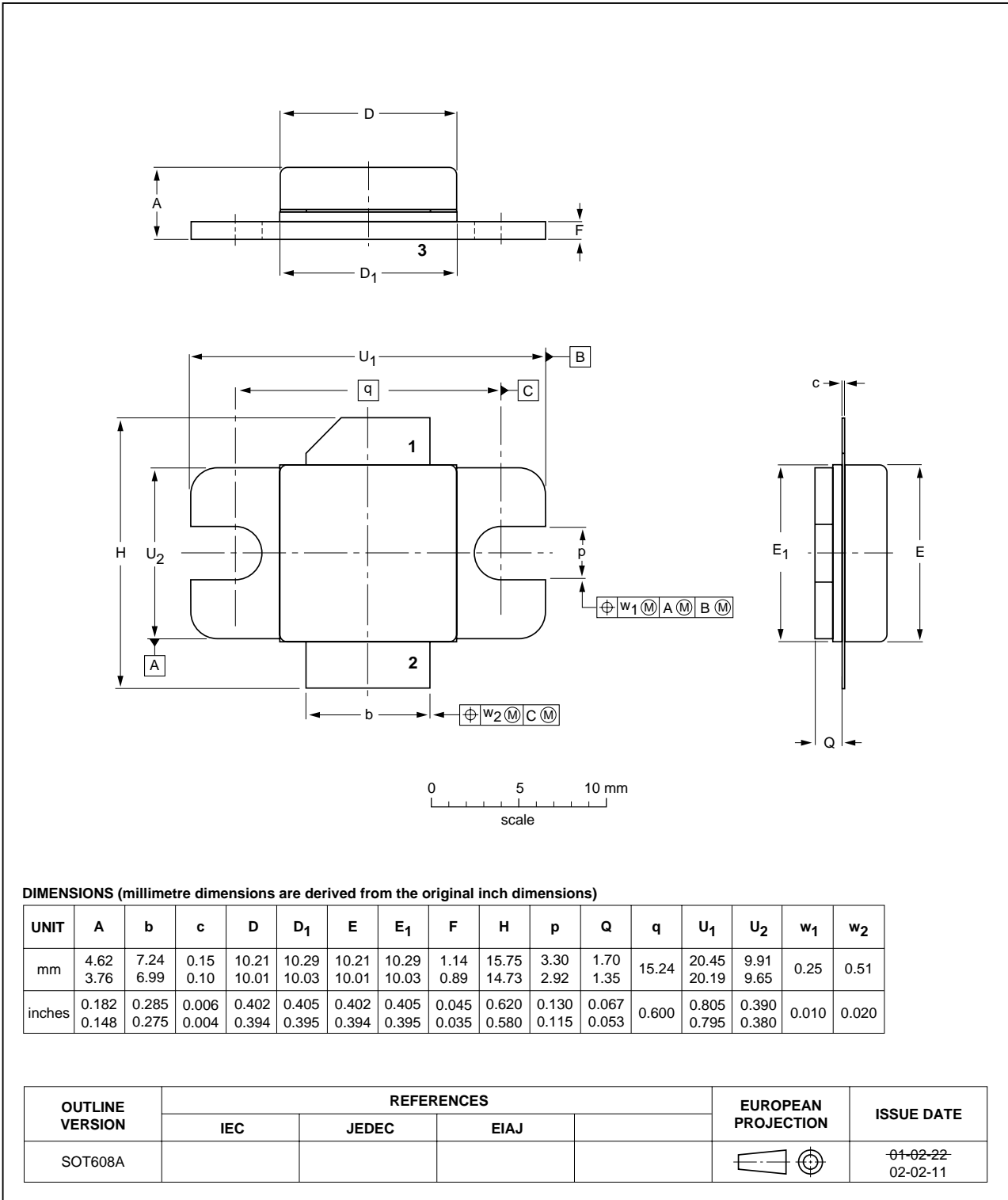


Fig 8. Package outline SOT608A

Ceramic earless flanged package; 2 leads

SOT608B

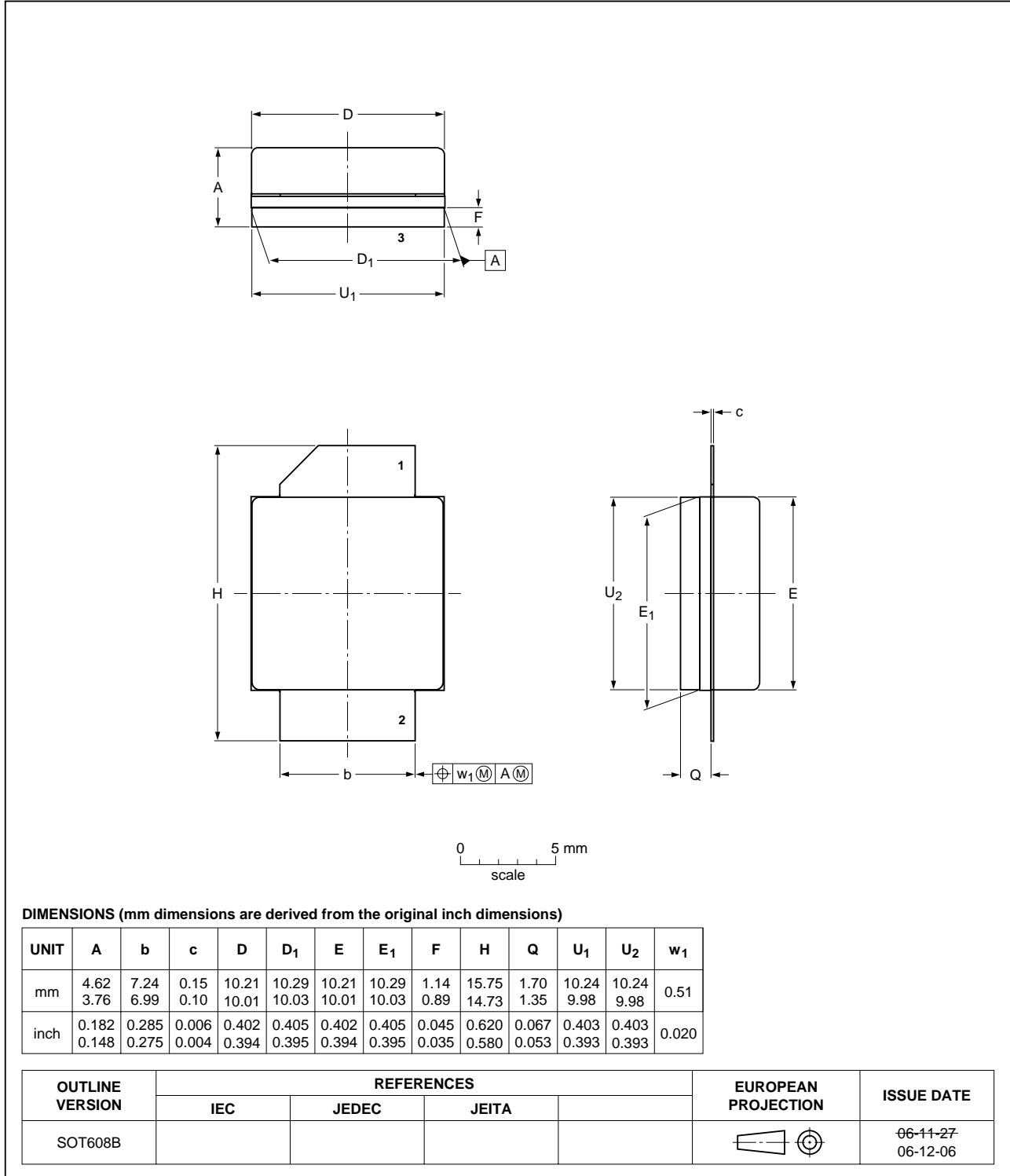


Fig 9. Package outline SOT608B

10. Abbreviations

Table 9. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
IMD	InterModulation Distortion
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PAR	Peak-to-Average power Ratio
PDPCH	transmission Power of the Dedicated Physical CHannel
RF	Radio Frequency
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G20-45_BLF6G20S-45_2	20080825	Product data sheet	-	BLF6G20-45_1
Modifications:				
			<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP semiconductors. Legal texts have been adapted to the new company name where appropriate. The document now describes both the eared and earless version of this product: BLF6G20-45 and BLF6G20S-45 respectively. 	
BLF6G20-45_1	20060220	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

12.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

13. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

14. Contents

1	Product profile	1
1.1	General description	1
1.2	Features	1
1.3	Applications	2
2	Pinning information	2
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	3
6	Characteristics	3
7	Application information	3
7.1	Ruggedness in class-AB operation	3
8	Test information	5
9	Package outline	8
10	Abbreviations	10
11	Revision history	10
12	Legal information	11
12.1	Data sheet status	11
12.2	Definitions	11
12.3	Disclaimers	11
12.4	Trademarks	11
13	Contact information	11
14	Contents	12

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2008.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 25 August 2008

Document identifier: BLF6G20-45_BLF6G20S-45_2