BLL1214-250R

LDMOS L-band radar power transistor

Rev. 01 — 4 February 2010 **Product data sheet**

1. Product profile

1.1 General description

Silicon N-channel enhancement model LDMOS power transistor encapsulated in a 2-lead flange package (SOT502A) with a ceramic cap. The common source is connected to the flange.

Table 1. Test information

Typical RF performance at T_h = 25 °C; t_p = 1 ms; δ = 10 %; in a common source class-AB test circuit.

Mode of operation	f (GHz)	V_{DS} (V)	I_{Dq} (mA)	P_L (W)	G_p (dB)	η_D (%)	$P_{droop(pulse)}$ (dB)	t_r (ns)	t_f (ns)
pulsed RF	1.2 to 1.4	36	150	250	13	47	0.2	15	5

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

- Typical pulsed RF performance at a frequency of 1.2 GHz to 1.4 GHz, a supply voltage of 36 V, an I_{Dq} of 150 mA, a t_p of 1 ms with δ of 10 %:
  - Output power = 250 W
  - Power gain = 13 dB
  - Efficiency = 47 %
- High power gain
- Easy power control
- Excellent ruggedness
- Source on mounting base eliminates DC isolators, reducing common mode inductance.

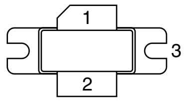
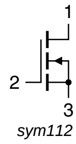
1.3 Applications

- L-band radar applications in the 1.2 GHz to 1.4 GHz frequency range

founded by Philips

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLL1214-250R	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	75	V
V_{GS}	gate-source voltage		–22	+22	V
P_{tot}	total power dissipation	$T_h \leq 70$ °C; $t_p = 1$ ms; $\delta = 10$ %	-	400	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-h)}$	transient thermal impedance from junction to heatsink	$T_h = 25$ °C		
		$t_p = 100$ μs; $\delta = 10$ %	0.17	K/W
		$t_p = 1$ ms; $\delta = 10$ %	0.32	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3 mA	75	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 300 mA	4	-	5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 36 V	-	-	1	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 9 V; V_{DS} = 10 V	45	-	-	A
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	-	1	μA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 10 A	-	9	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = 9 V; I_D = 10 A	-	60	-	mΩ

Table 7. RF characteristics

Mode of operation: pulsed RF; t_p = 1 ms; δ = 10 %; f = 1.2 GHz to 1.4 GHz; RF performance at V_{DS} = 36 V; I_{Dq} = 150 mA; T_h = 25 °C; $Z_{th(mb-h)}$ = 0.25 K/W; unless otherwise specified, in a common source class-AB circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_L	output power		-	250	-	W
V_{DS}	drain-source voltage	P_L = 250 W	-	36	-	V
G_p	power gain	P_L = 250 W	-	13	-	dB
η_D	drain efficiency	P_L = 250 W	-	47	-	%
$P_{droop(pulse)}$	pulse droop power	P_L = 250 W	-	0.2	-	dB
t_r	rise time	P_L = 250 W	-	15	-	ns
t_f	fall time	P_L = 250 W	-	5	-	ns

6.1 Ruggedness in class-AB operation

The BLL1214-250R is capable of withstanding a load mismatch corresponding to VSWR = 3 : 1 through all phases under the following conditions: V_{DS} = 36 V; f = 1.2 GHz to 1.4 GHz at rated load power.

7. Application information

7.1 Impedance information

Table 8. Typical impedance

Typical values unless otherwise specified.

f GHz	Z_S Ω	Z_L Ω
1.20	1.3 – j2.8	1.1 – j0.9
1.25	1.9 – j2.8	1.0 – j0.5
1.30	4.6 – j2.9	0.8 – j0.2
1.35	5.7 – j0.3	0.7 – j0.3
1.40	2.7 – j1.8	0.6 – j0.4

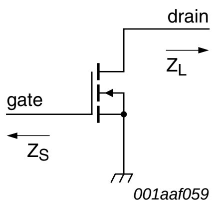


Fig 1. Definition of transistor impedance

7.2 Application circuit

Table 9. List of components

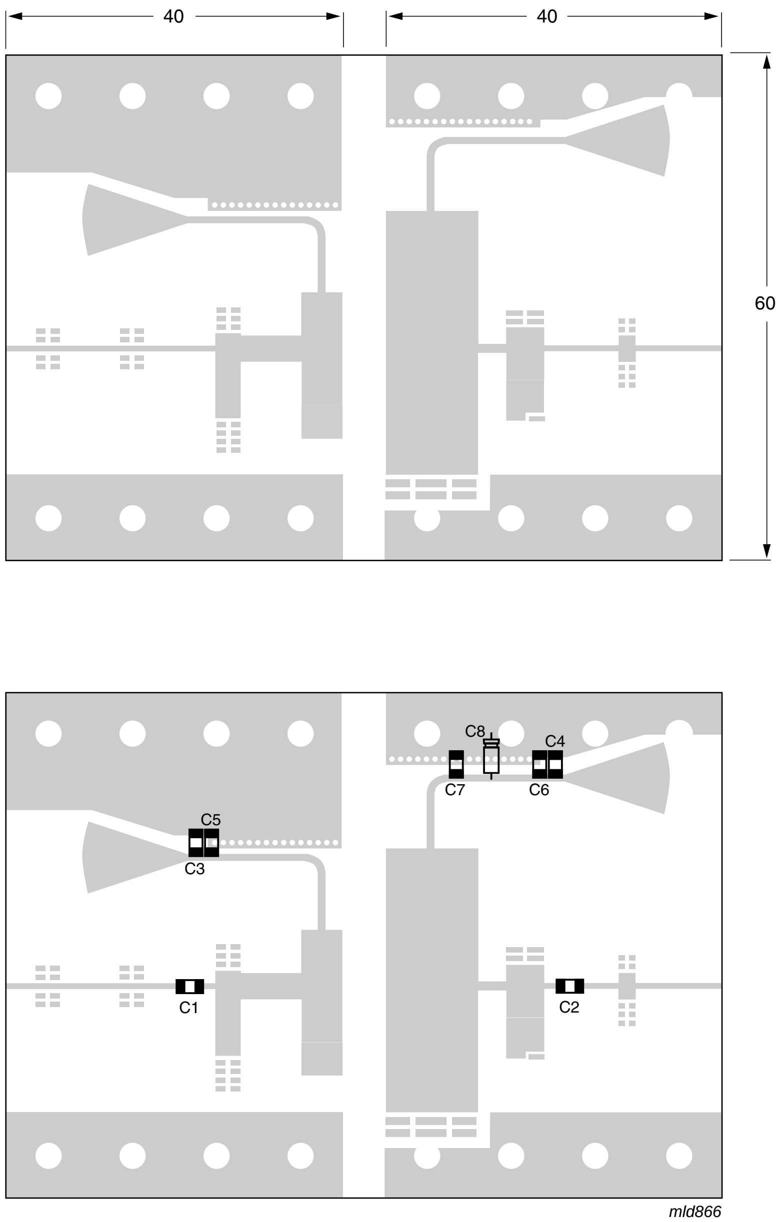
See Figure 2.

The components are situated in one side of the copper-clad Rodgers Duroid 6010 Printed-Circuit Board (PCB); ε_r = 10.2 F/m; thickness = 0.64 mm. The other side is unetched and serves as a ground plane.

Component	Description	Value	Remarks
C1, C3	multilayer ceramic chip capacitor	39 pF [1]	
C2, C4	multilayer ceramic chip capacitor	47 pF [1]	
C5, C6	multilayer ceramic chip capacitor	20 nF [2]	
C7	multilayer ceramic chip capacitor	36 pF [2]	
C8	electrolytic capacitor	100 μF; 100 V	

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 200B or capacitor of same quality.



See Table 9 for list of components.

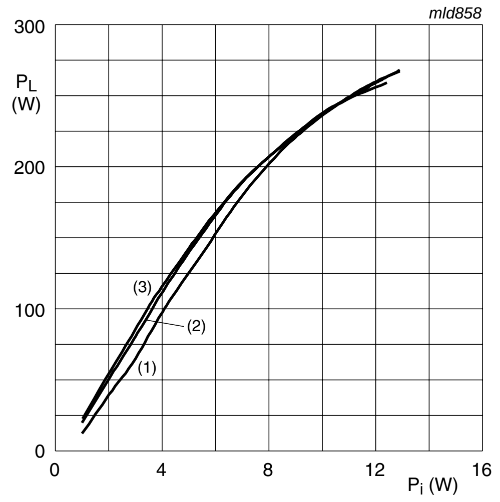
Dimensions in mm.

The components are situated in one side of the copper-clad Rodgers Duroid 6010 Printed-Circuit Board (PCB); ε_r = 10.2 F/m; thickness = 0.64 mm. The other side is unetched and serves as a ground plane.

Fig 2. Component layout

8. Test information

8.1 RF performance



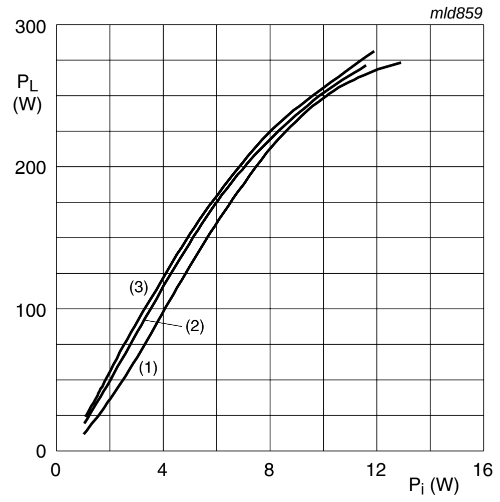
t_p = 1 ms; δ = 10 %.

(1) f = 1.2 GHz.

(2) f = 1.3 GHz.

(3) f = 1.4 GHz.

Fig 3. Output power as a function of input power; typical values



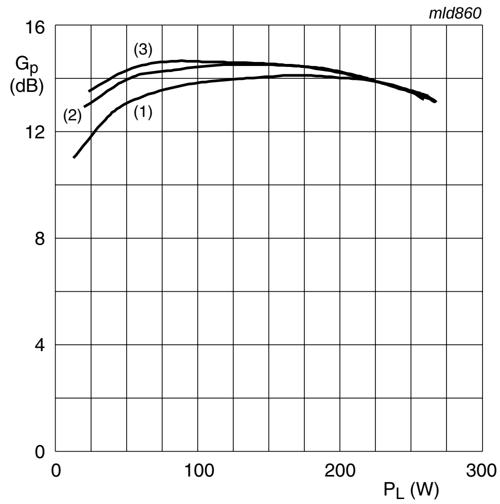
t_p = 100 μs; δ = 10 %.

(1) f = 1.2 GHz.

(2) f = 1.3 GHz.

(3) f = 1.4 GHz.

Fig 4. Output power as a function of input power; typical values



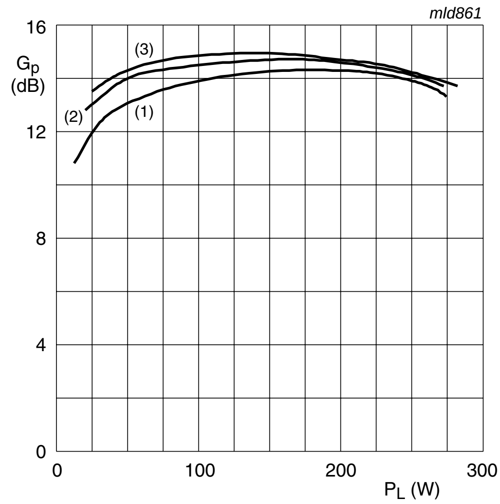
t_p = 1 ms; δ = 10 %.

(1) f = 1.2 GHz.

(2) f = 1.3 GHz.

(3) f = 1.4 GHz.

Fig 5. Power gain as a function of load power; typical values



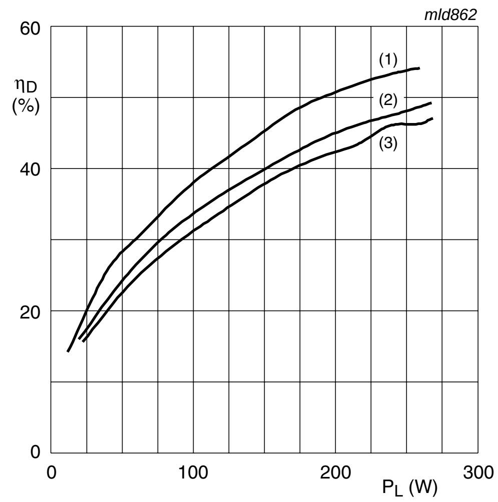
t_p = 100 μs; δ = 10 %.

(1) f = 1.2 GHz.

(2) f = 1.3 GHz.

(3) f = 1.4 GHz.

Fig 6. Power gain as a function of load power; typical values



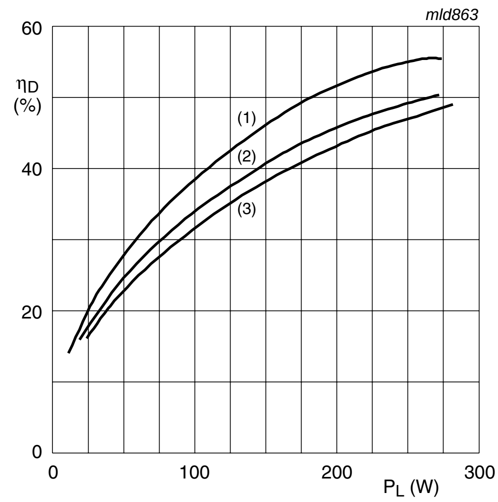
t_p = 1 ms; δ = 10 %.

(1) f = 1.2 GHz.

(2) f = 1.3 GHz.

(3) f = 1.4 GHz.

Fig 7. Drain efficiency as a function of load power; typical values



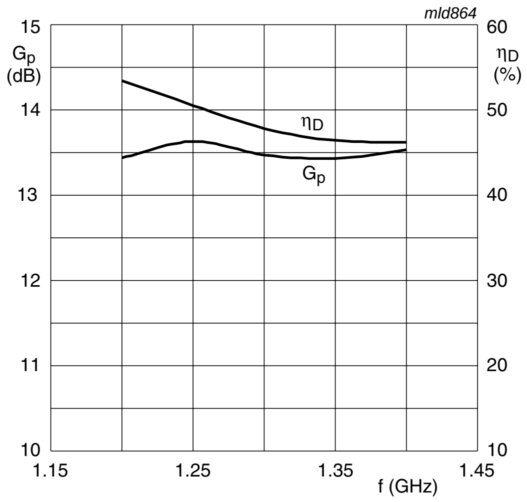
t_p = 100 μs; δ = 10 %.

(1) f = 1.2 GHz.

(2) f = 1.3 GHz.

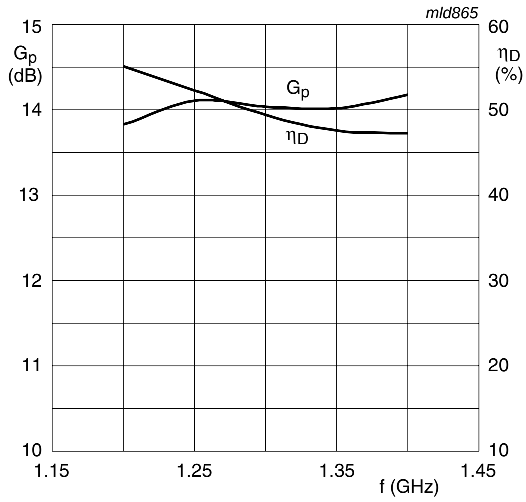
(3) f = 1.4 GHz.

Fig 8. Drain efficiency as a function of load power; typical values



t_p = 1 ms; δ = 10 %.

Fig 9. Power gain and drain efficiency as function of frequency; typical values

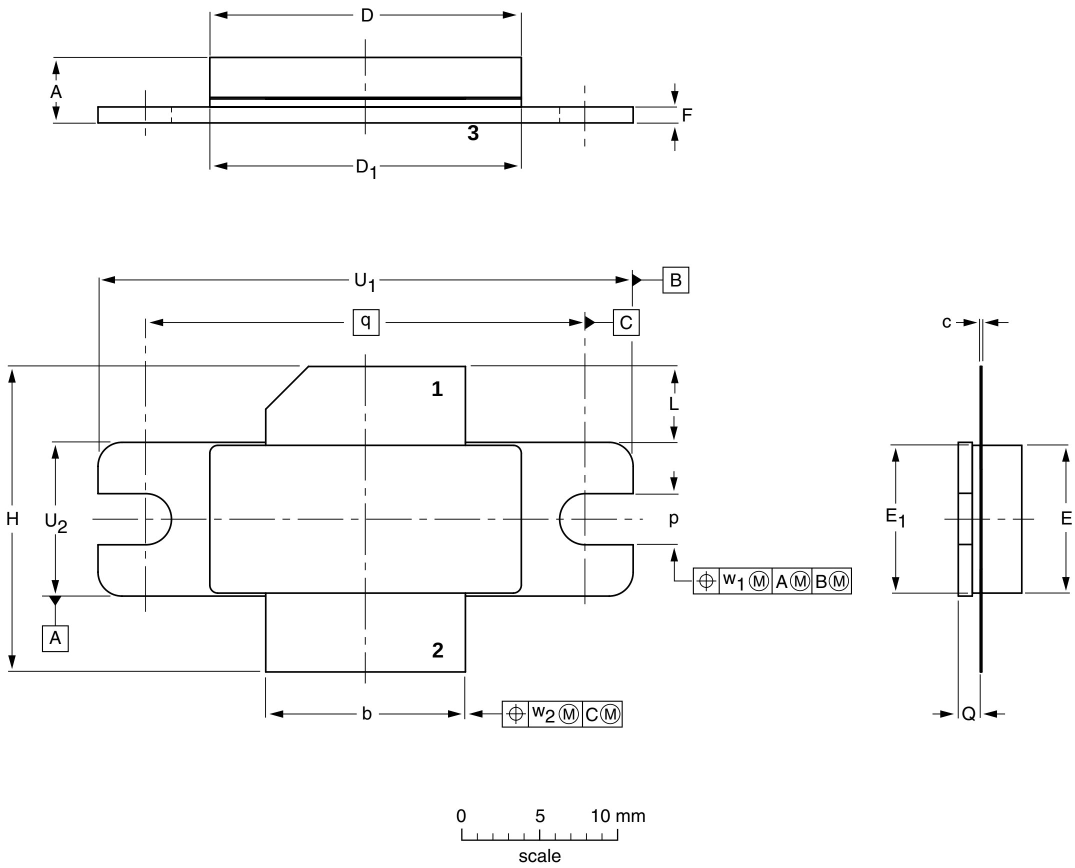


t_p = 100 μs; δ = 10 %.

Fig 10. Power gain and drain efficiency as function of frequency; typical values

9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~99-12-28~~ 03-01-10

Fig 11. Package outline SOT502A

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
DC	Direct Current
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
L-band	Long wave band
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLL1214-250R_1	20100204	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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