BLS6G2731-6G

LDMOS S-Band radar power transistor

Rev. 01 — 19 February 2009 **Product data sheet**

1. Product profile

1.1 General description

6 W LDMOS power transistor intended for radar applications in the 2.7 GHz to 3.1 GHz range.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C; t_p = 100 µs; δ = 10 %; I_{Dq} = 25 mA; in a class-AB production test circuit.

Mode of operation	f (GHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	t_r (ns)	t_f (ns)
pulsed RF	2.7 to 3.1	32	6	15	33	20	10

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

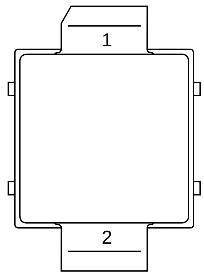
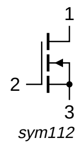
- Typical pulsed RF performance at a frequency of 2.7 GHz to 3.1 GHz, a supply voltage of 32 V, an I_{Dq} of 25 mA, a t_p of 100 µs and a δ of 10 %:
  - Output power = 6 W
  - Power gain = 15 dB
  - Efficiency = 33 %
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (2.7 GHz to 3.1 GHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

- S-Band power amplifiers for radar applications in the 2.7 GHz to 3.1 GHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
1	drain			
2	gate			
3	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLS6G2731-6G	-	eared flanged ceramic package; 2 mounting holes; 2 leads	SOT975C

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	60	V
V_{GS}	gate-source voltage	–0.5	+13	V
I_D	drain current	-	3.5	A
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 6 W		
		t_p = 100 μs; δ = 10 %	1.56	K/W
		t_p = 200 μs; δ = 10 %	1.95	K/W
		t_p = 300 μs; δ = 10 %	2.20	K/W
		t_p = 100 μs; δ = 20 %	2.00	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.18 mA	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 18 mA	1.4	1.8	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	2.7	-	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 0.9 A	0.81	-	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)}$ + 3.75 V; I_D = 0.63 A	328	-	1260	mΩ

7. Application information

Table 7. Application information

Mode of operation: pulsed RF; t_p = 100 μs; δ = 10 %; RF performance at V_{DS} = 32 V; I_{Dq} = 25 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	P_L = 6 W	-	-	32	V
G_p	power gain	P_L = 6 W	14	15	-	dB
η_D	drain efficiency	P_L = 6 W	30	33	-	%
t_r	rise time	P_L = 6 W	-	20	50	ns
t_f	fall time	P_L = 6 W	-	10	50	ns

Table 8. Typical impedance

f GHz	Z_S Ω	Z_L Ω
2.7	2.44 – j17.78	3.30 – j4.14
2.8	2.99 – j16.04	4.52 – j3.72
2.9	3.94 – j14.56	5.67 – j4.67
3.0	5.44 – j13.75	4.94 – j6.39
3.1	6.89 – j14.58	3.00 – j6.56

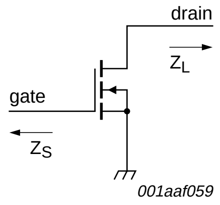
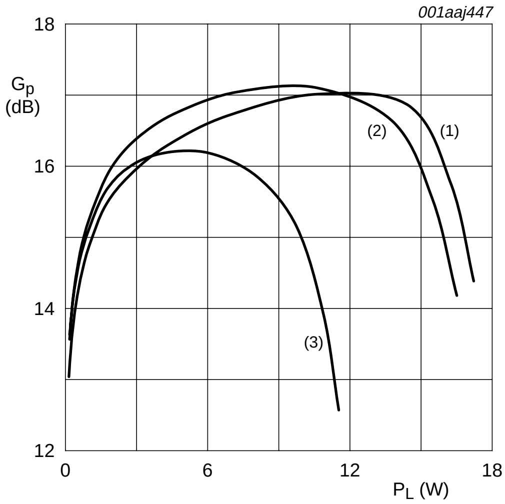


Fig 1. Definition of transistor impedance

7.1 Ruggedness in class-AB operation

The BLS6G2731-6G is capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 25 mA; P_L = 6 W; t_p = 100 μs; δ = 10 %.

7.2 Graphs



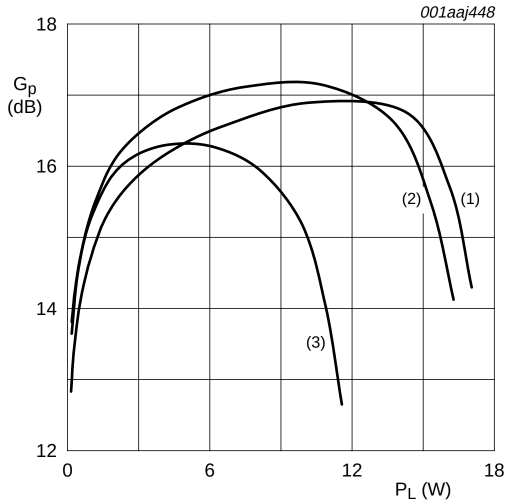
V_{DS} = 32 V; I_{Dq} = 25 mA; t_p = 300 μs; δ = 10 %.

(1) f = 2.7 GHz

(2) f = 2.9 GHz

(3) f = 3.1 GHz

Fig 2. Power gain as a function of load power; typical values



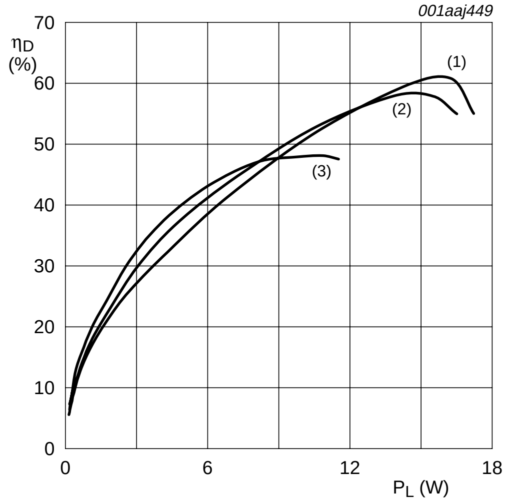
V_{DS} = 32 V; I_{Dq} = 25 mA; t_p = 100 μs; δ = 20 %.

(1) f = 2.7 GHz

(2) f = 2.9 GHz

(3) f = 3.1 GHz

Fig 3. Power gain as a function of load power; typical values



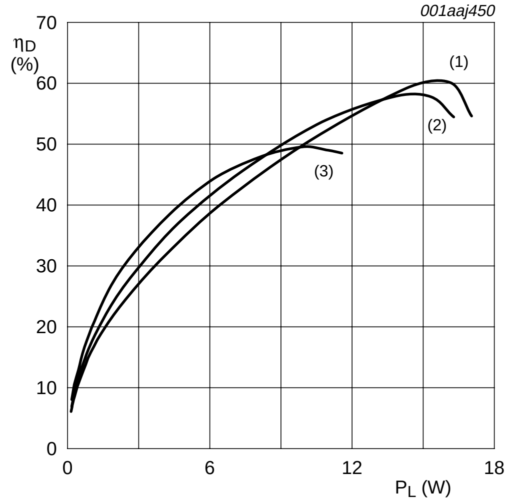
V_{DS} = 32 V; I_{Dq} = 25 mA; t_p = 300 μs; δ = 10 %.

(1) f = 2.7 GHz

(2) f = 2.9 GHz

(3) f = 3.1 GHz

Fig 4. Drain efficiency as a function of load power; typical values



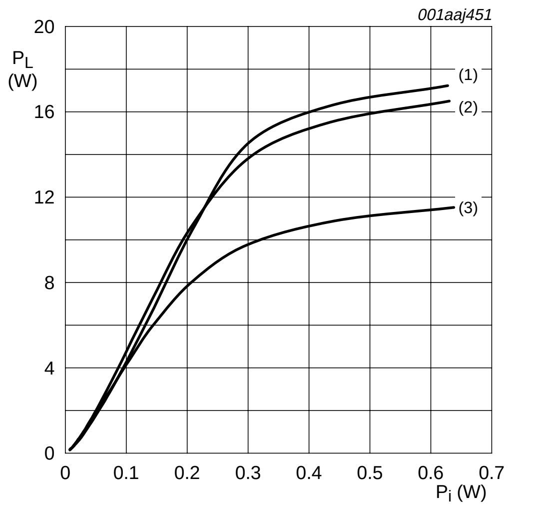
V_{DS} = 32 V; I_{Dq} = 25 mA; t_p = 100 μs; δ = 20 %.

(1) f = 2.7 GHz

(2) f = 2.9 GHz

(3) f = 3.1 GHz

Fig 5. Drain efficiency as a function of load power; typical values



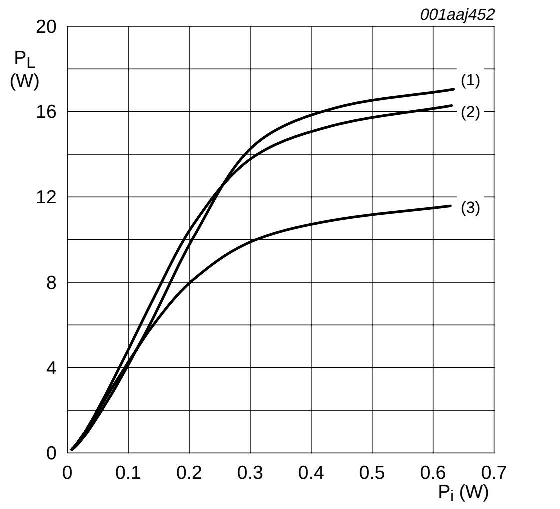
V_{DS} = 32 V; I_{Dq} = 25 mA; t_p = 300 µs; δ = 10 %.

(1) f = 2.7 GHz

(2) f = 2.9 GHz

(3) f = 3.1 GHz

Fig 6. Load power as a function of input power; typical values



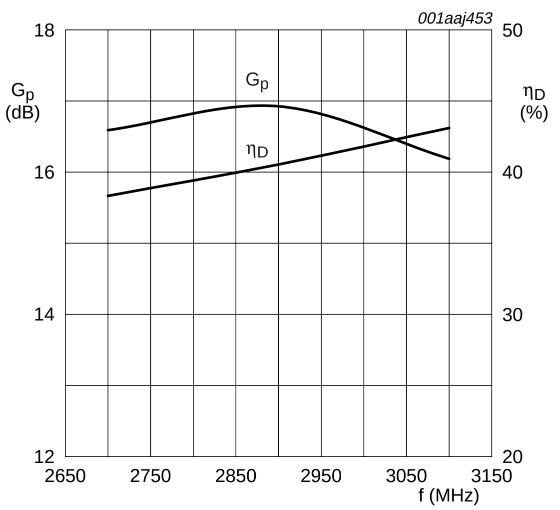
V_{DS} = 32 V; I_{Dq} = 25 mA; t_p = 100 µs; δ = 20 %.

(1) f = 2.7 GHz

(2) f = 2.9 GHz

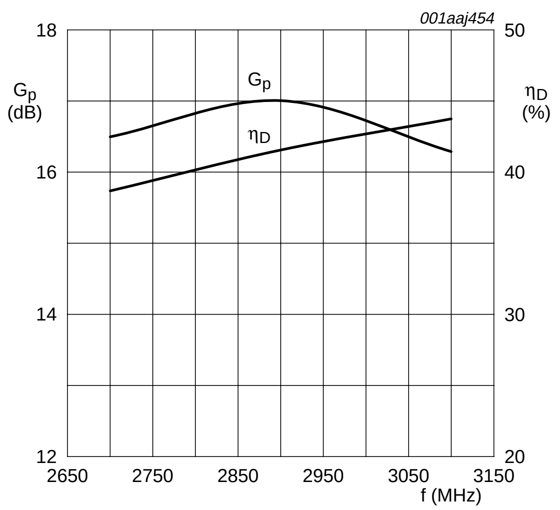
(3) f = 3.1 GHz

Fig 7. Load power as a function of input power; typical values



V_{DS} = 32 V; I_{Dq} = 25 mA; t_p = 300 µs; δ = 10 %.

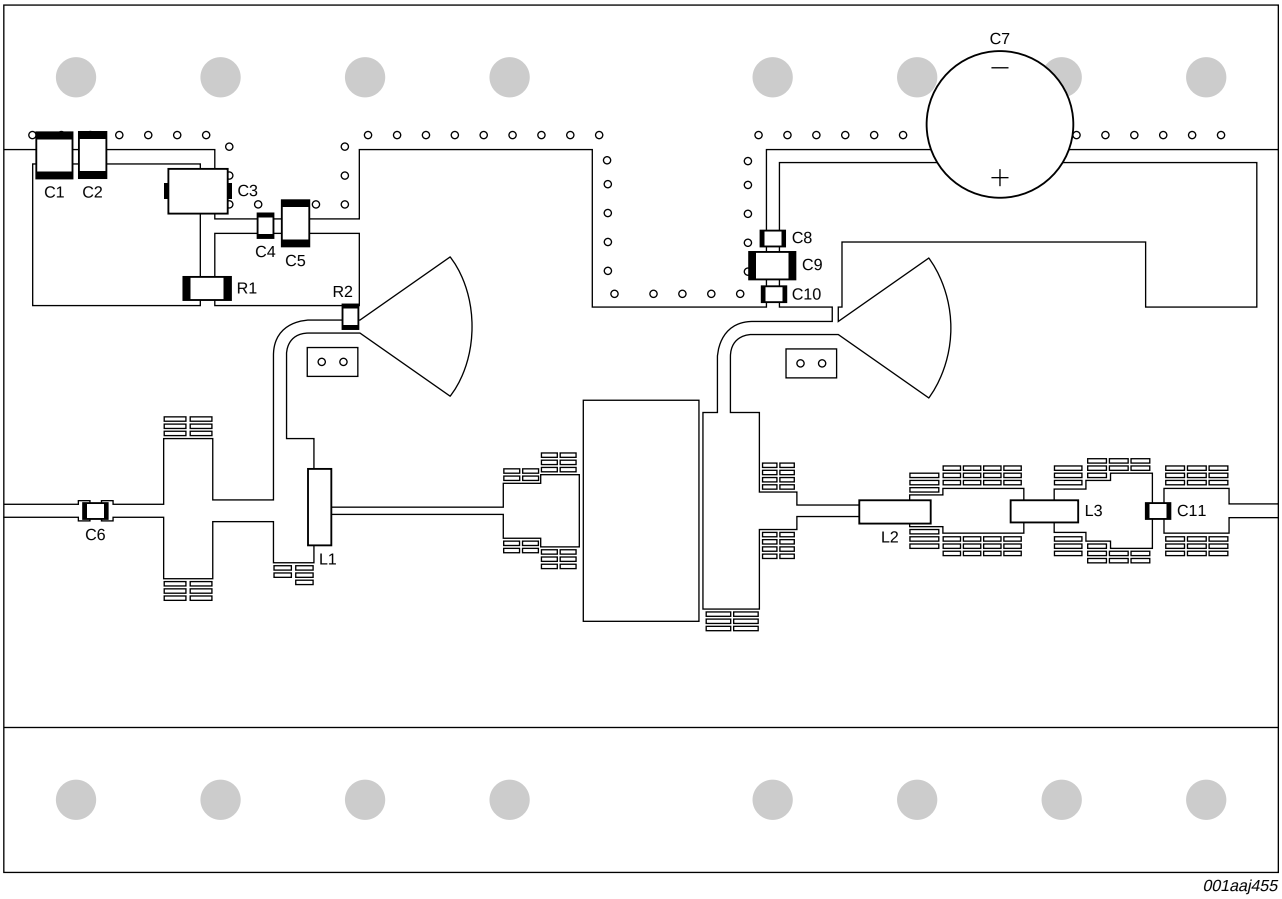
Fig 8. Power gain and drain efficiency as function of frequency; typical values



V_{DS} = 32 V; I_{Dq} = 25 mA; t_p = 100 µs; δ = 20 %.

Fig 9. Power gain and drain efficiency as function of frequency; typical values

8. Test information



Striplines are on a double copper-clad Duroid 6006 Printed-Circuit Board (PCB) with ε_r = 6.15 and thickness = 0.64 mm.

See Table 9 for list of components.

Fig 10. Component layout for 2700 MHz to 3100 MHz test circuit

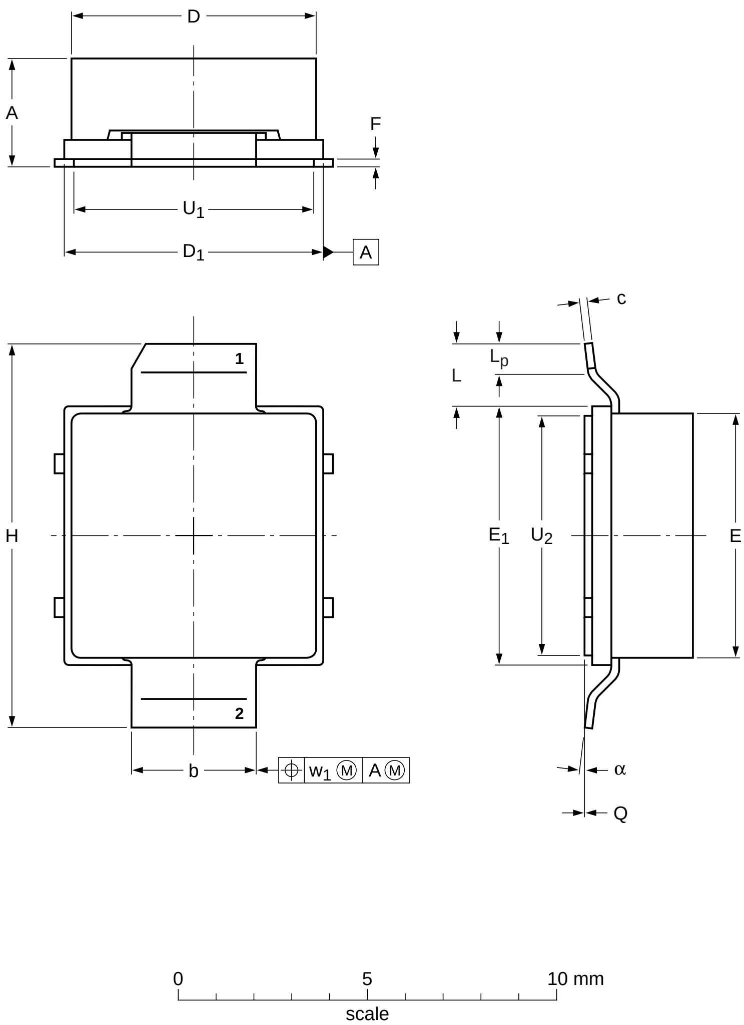
Table 9. List of components (see Figure 10)

Striplines are on a double copper-clad Duroid 6006 Printed-Circuit Board (PCB) with ε_r = 6.15 and thickness = 0.64 mm.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	20 nF	ATC 200B or equivalent
C2, C9	multilayer ceramic chip capacitor	100 pF	ATC 100B or equivalent
C3	multilayer ceramic chip capacitor	10 µF; 35 V	AVX TAJD106K035R or equivalent
C4, C8	multilayer ceramic chip capacitor	1 nF	ATC 700A or equivalent
C5, C10, C11	multilayer ceramic chip capacitor	20 pF	ATC 100A or equivalent
C6	multilayer ceramic chip capacitor	2.7 pF	ATC 100A or equivalent
C7	electrolytic capacitor	47 µF; 63 V	
R1	SMD resistor	56 Ω	
R2	SMD resistor	3.9 Ω	
L1, L2, L3	copper (Cu) strips	-	

9. Package outline

Earless flanged ceramic package; 2 leads **SOT975C**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	L_p	Q	U_1	U_2	w_1	α
mm	3.63 3.05	3.38 3.23	0.23 0.18	6.55 6.40	6.93 6.78	6.55 6.40	6.93 6.78	0.23 0.18	10.29 10.03	1.65	1.02 0.51	+0.05 −0.05	6.43 6.27	6.43 6.27	0.51	7° 0°
inches	0.143 0.120	0.133 0.127	0.009 0.007	0.258 0.252	0.273 0.267	0.258 0.252	0.273 0.267	0.009 0.007	0.405 0.395	0.065	0.040 0.020	+0.002 −0.002	0.253 0.247	0.253 0.247	0.020	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT975C						~~08-05-20~~ 08-07-10

Fig 11. Package outline SOT975C

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
RF	Radio Frequency
S-Band	Short wave Band
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLS6G2731-6G_1	20090219	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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