

BUK9MTT-65PBB

Dual TrenchPLUS FET Logic Level FET

Rev. 02 — 17 June 2010

Product data sheet

1. Product profile

1.1 General description

Dual N-channel enhancement mode field-effect power transistor in SO20. Device is manufactured using NXP High-Performance (HPA) TrenchPLUS technology, featuring very low on-state resistance, integrated current sensing transistors and over temperature protection diodes.

1.2 Features and benefits

- Integrated current sensors
- Integrated temperature sensors

1.3 Applications

- Lamp switching
- Motor drive systems
- Power distribution
- Solenoid drivers

1.4 Quick reference data

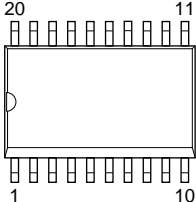
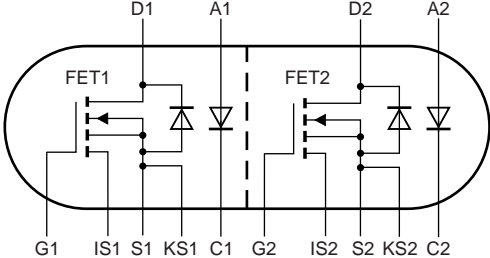
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FET1 and FET2 static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 3\text{ A}$; $T_j = 25\text{ °C}$; see Figure 13 ; see Figure 14	-	85	100	mΩ
I_D/I_{sense}	ratio of drain current to sense current	$T_j = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 15	900	1000	1100	A/A
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$	65	-	-	V



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G1	gate 1	 <p>SOT163-1 (SO20)</p>	 <p style="text-align: right;">003aaa745</p>
2	IS1	current sense 1		
3	D1	drain		
4	A1	anode 1		
5	C1	cathode 1		
6	G2	gate 2		
7	IS2	current sense 2		
8	D2	drain 2		
9	A2	anode 2		
10	C2	cathode 2		
11	D2	drain 2		
12	KS2	Kelvin source 2		
13	S2	source 2		
14	S2	source 2		
15	D2	drain 2		
16	D1	drain 1		
17	KS1	Kelvin source 1		
18	S1	source 1		
19	S1	source 1		
20	D1	drain 1		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9MTT-65PBB	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

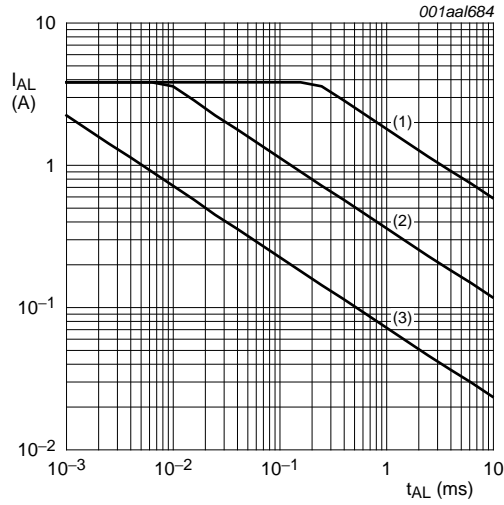
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

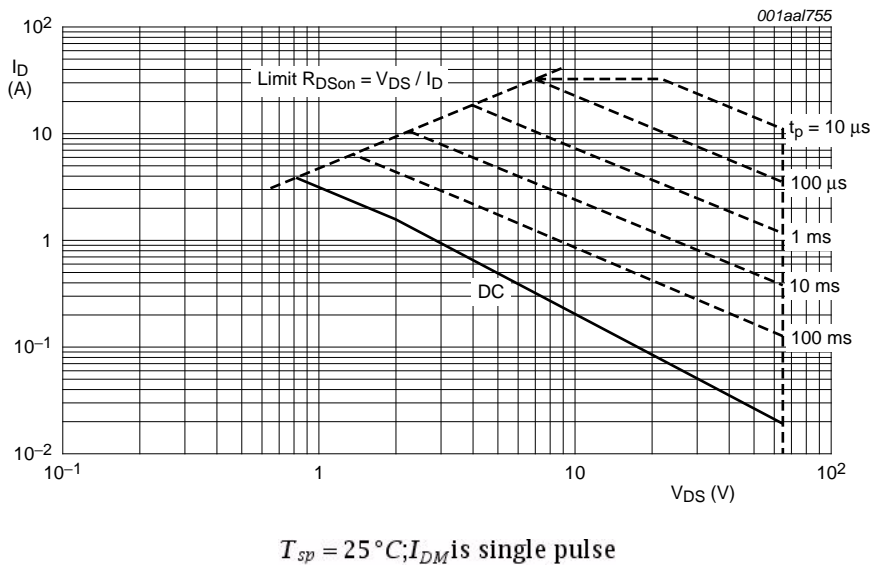
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FET1 and FET2						
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	65	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$; $25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	65	V
V_{GS}	gate-source voltage		-15	-	15	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{sp} = 25\text{ °C}$	[1][2]	-	3.8	A
		$V_{GS} = 5\text{ V}$; $T_{sp} = 100\text{ °C}$	[1][2]	-	2.4	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; single pulse; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 2	-	-	32.4	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$	-	-	3.15	W
T_{stg}	storage temperature		-55	-	150	°C
T_j	junction temperature		-55	-	150	°C
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage		-	-	100	V
FET1 and FET2 source-drain diode						
I_S	source current	$T_{sp} = 25\text{ °C}$	[1][3]	-	4.4	A
I_{SM}	peak source current	single pulse; $t_p \leq 10\text{ }\mu\text{s}$; $T_{sp} = 25\text{ °C}$	-	-	32.4	A
FET1 and FET2 avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 3.8\text{ A}$; $V_{sup} = 65\text{ V}$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; see Figure 1	[4][5][6]	-	0.036	mJ
FET1 and FET2 electrostatic discharge						
V_{ESD}	electrostatic discharge voltage	HBM; $C = 100\text{ pF}$; $R = 1.5\text{ k}\Omega$; all pins	-	-	0.15	kV
		HBM; $C = 100\text{ pF}$; $R = 1.5\text{ k}\Omega$; pins 8, 11 and 15 to pins 6, 7, 12, 13 and 14 shorted	-	-	4	kV
		HBM; $C = 100\text{ pF}$; $R = 1.5\text{ k}\Omega$; pins 3, 16 and 20 to pins 1, 2, 17, 18 and 19 shorted	-	-	4	kV

- [1] Single device conducting.
- [2] Continuous current is limited by package.
- [3] Current is limited by chip power dissipation rating.
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 150 °C.
- [5] Repetitive rating defined in avalanche rating figure.
- [6] Refer to application note AN10273 for further information.



- (1) Single-pulse; $T_j = 25\text{ }^\circ\text{C}$.
- (2) Single-pulse; $T_j = 150\text{ }^\circ\text{C}$.
- (3) Repetitive.

Fig 1. Single-Pulse and repetitive avalanche rating; avalanche current as a function of avalanche time. FET1 and FET2.



$T_{sp} = 25\text{ }^\circ\text{C}; I_{DM}$ is single pulse

Fig 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	FET1	-	-	40	K/W
		FET2	-	-	40	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; both channels conducting; zero heat sink area; see Figure 3 ; see Figure 4	-	73	-	K/W
		mounted on a printed-circuit board; both channels conducting; 200 mm ² copper heat sink area; see Figure 5 ; see Figure 4	-	60	-	K/W
		mounted on a printed-circuit board; both channels conducting; 400 mm ² copper heat sink area; see Figure 6 ; see Figure 4	-	51	-	K/W
		mounted on a printed-circuit board; one channel conducting; zero heat sink area; see Figure 3 ; see Figure 4	-	105	-	K/W
		mounted on a printed-circuit board; one channel conducting; 200 mm ² copper heat sink area; see Figure 5 ; see Figure 4	-	90	-	K/W
		mounted on a printed-circuit board; one channel conducting; 400 mm ² copper heat sink area; see Figure 6 ; see Figure 4	-	70	-	K/W

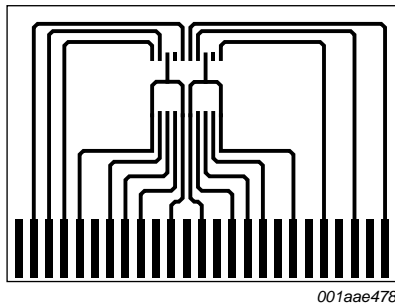
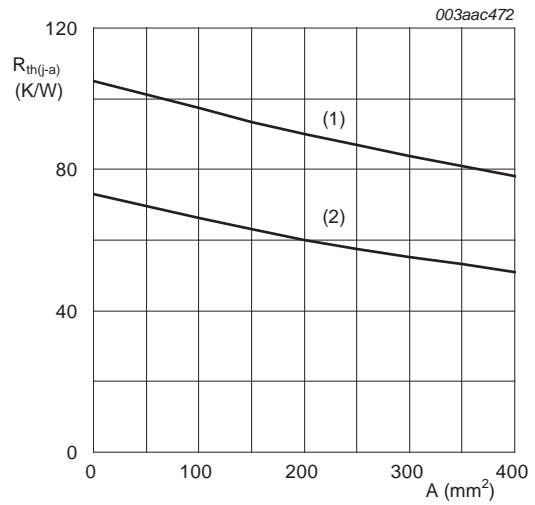


Fig 3. PCB used for thermal tests; zero heat sink area



(1) One channel conducting dissipating 500mW.
 (2) Both channels conducting each dissipating 500mW.
 Zero air flow

Fig 4. Thermal resistance from junction to ambient as a function of printed-circuit board (PCB) heat sink area

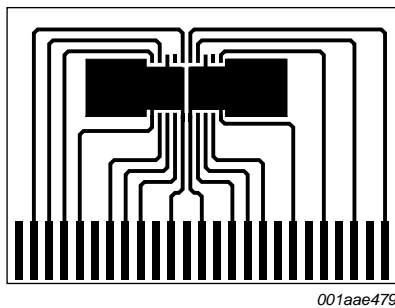


Fig 5. PCB used for thermal tests; heat sink area 200 mm²

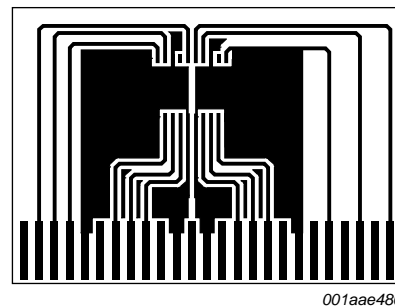


Fig 6. PCB used for thermal tests; heat sink area 400 mm²

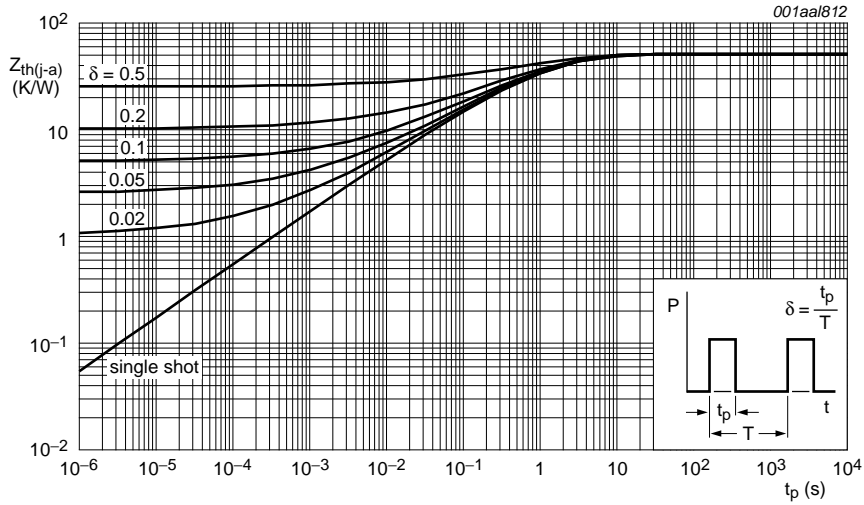


Fig 7. Transient thermal impedance from junction to ambient as a function of pulse duration

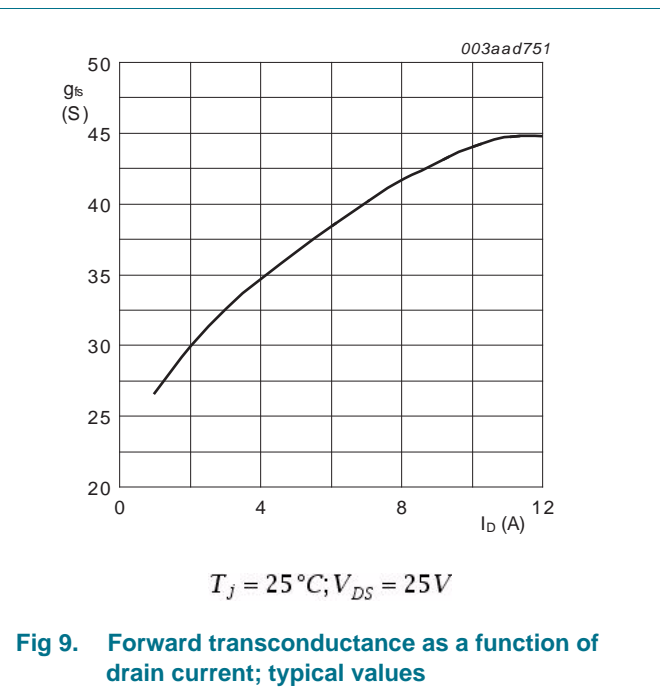
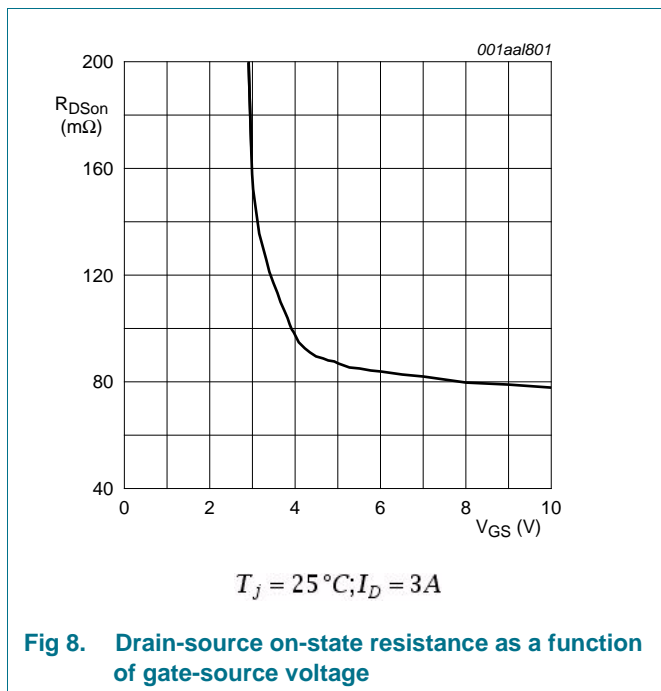
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FET1 and FET2 static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	65	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	59	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 11 ; see Figure 12	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ C$; see Figure 11 ; see Figure 12	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$; see Figure 11 ; see Figure 12	-	-	2.3	V
I_{DSS}	drain leakage current	$V_{DS} = 52 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.02	3	μA
		$V_{DS} = 52 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ C$	-	-	125	μA
I_{GSS}	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 15 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	300	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 3 \text{ A}; T_j = 25 \text{ }^\circ C$; see Figure 13 ; see Figure 14	-	-	111.5	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 3 \text{ A}; T_j = 25 \text{ }^\circ C$; see Figure 13 ; see Figure 14	-	85	100	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 3 \text{ A}; T_j = 150 \text{ }^\circ C$; see Figure 13 ; see Figure 14	-	-	214	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 3 \text{ A}; T_j = 25 \text{ }^\circ C$; see Figure 13 ; see Figure 14	-	-	90.4	m Ω
I_D/I_{sense}	ratio of drain current to sense current	$V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ C$; see Figure 15	900	1000	1100	A/A
$S_{F(TSD)}$	temperature sense diode temperature coefficient	$I_F = 250 \mu A; 25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$; see Figure 16	-5.4	-5.7	-6	mV/K

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{F(TSD)}$	temperature sense diode forward voltage	$I_F = 250 \mu A$; $T_j = 25 \text{ }^\circ C$; see Figure 16	2.855	2.9	2.945	V
FET1 and FET2 dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 3 A$; $V_{DS} = 52 V$; $V_{GS} = 5 V$; see Figure 17	-	6.3	-	nC
Q_{GS}	gate-source charge		-	1.47	-	nC
Q_{GD}	gate-drain charge		-	2.53	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 V$; $V_{DS} = 25 V$; $f = 1 \text{ MHz}$;	-	535	-	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^\circ C$; see Figure 18	-	85	-	pF
C_{rss}	reverse transfer capacitance		-	24.8	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 V$; $R_L = 3 \Omega$; $V_{GS} = 5 V$;	-	15	-	ns
t_r	rise time	$R_{G(ext)} = 10 \Omega$	-	15	-	ns
$t_{d(off)}$	turn-off delay time	$V_{DS} = 30 V$; $V_{GS} = 5 V$; $R_{G(ext)} = 10 \Omega$	-	43	-	ns
t_f	fall time	$V_{DS} = 30 V$; $R_L = 3 \Omega$; $V_{GS} = 5 V$;	-	35	-	ns
		$R_{G(ext)} = 10 \Omega$				
L_D	internal drain inductance	from pin to center of die	-	0.9	-	nH
L_S	internal source inductance	from source lead to source bonding pad	-	2	-	nH
FET1 and FET2 source-drain diode						
V_{SD}	source-drain voltage	$I_S = 3 A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$; see Figure 19	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 3 A$; $di_S/dt = -100 A/\mu s$;	-	44	-	ns
Q_r	recovered charge	$V_{GS} = -10 V$; $V_{DS} = 30 V$	-	0.092	-	nC



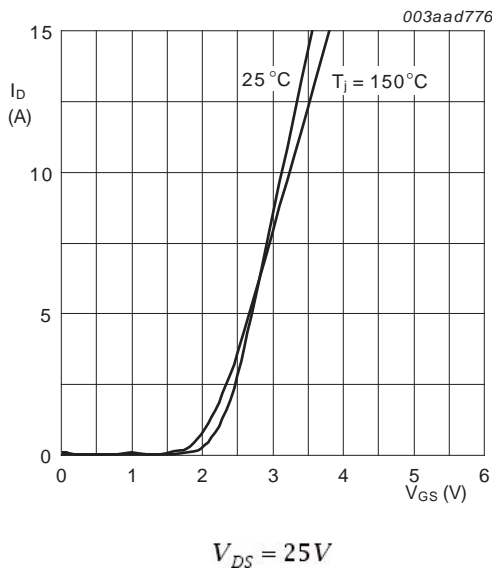


Fig 10. Transfer characteristics; drain current as a function of gate-source voltage

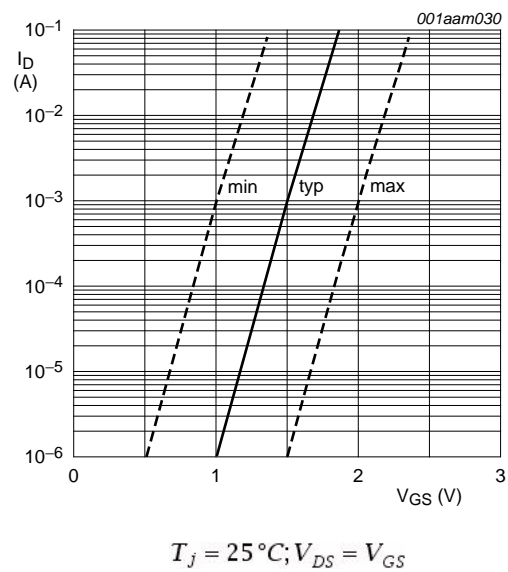


Fig 11. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2

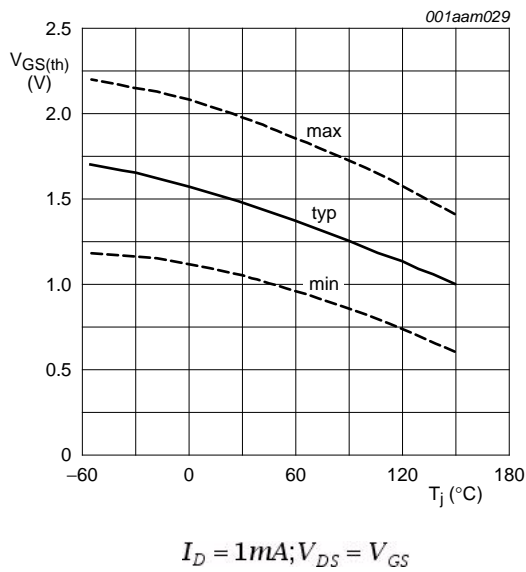


Fig 12. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2

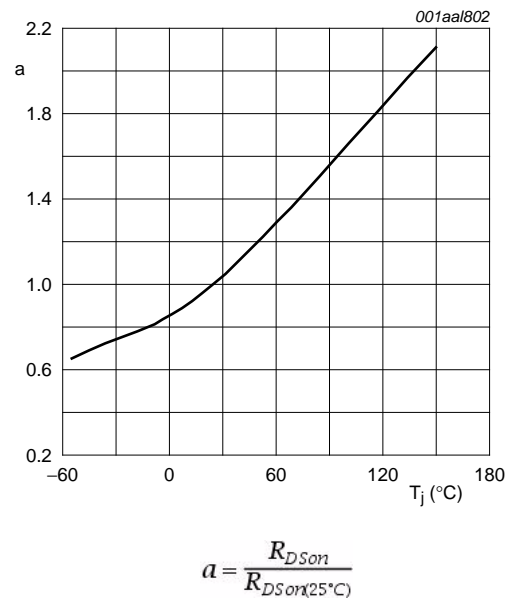
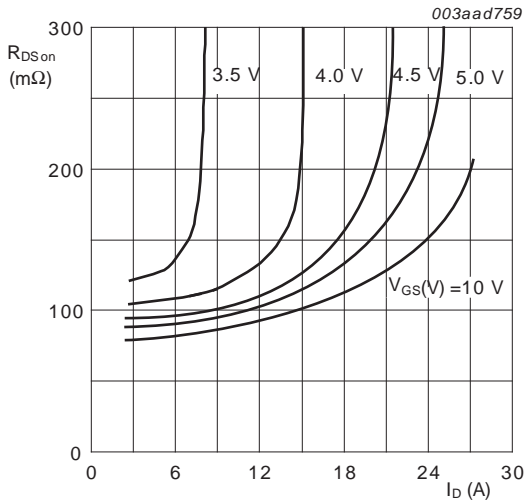
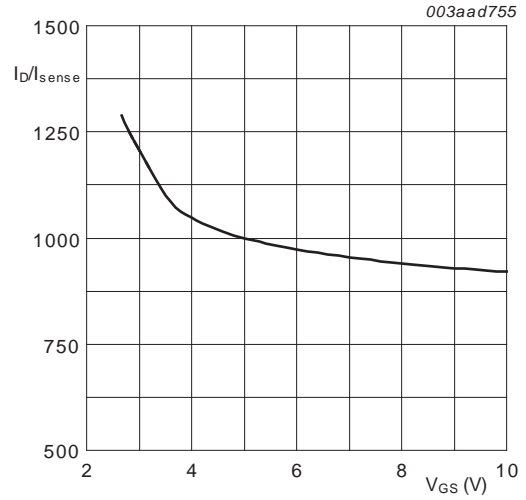


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2



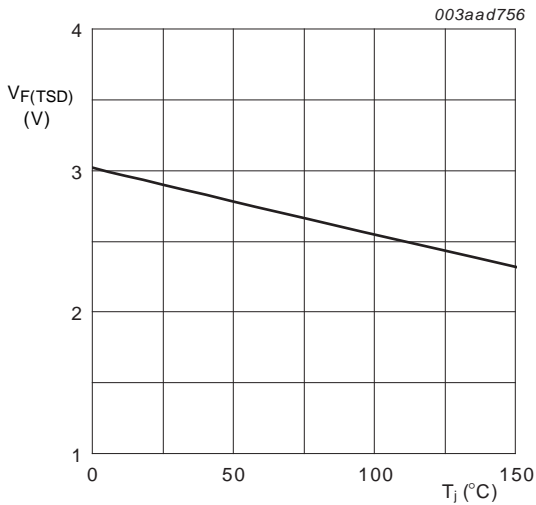
$T_j = 25^\circ\text{C}; t_p = 300\mu\text{s}$

Fig 14. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2



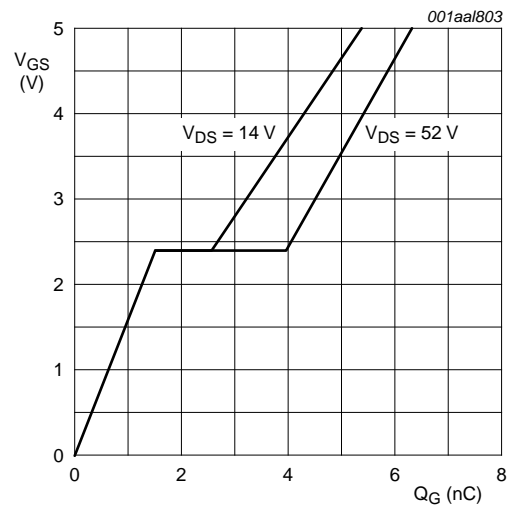
$T_j = 25^\circ\text{C}; I_D = 5\text{A}$

Fig 15. Ratio of drain current to sense current as a function of gate-source voltage; typical values, FET1 and FET2



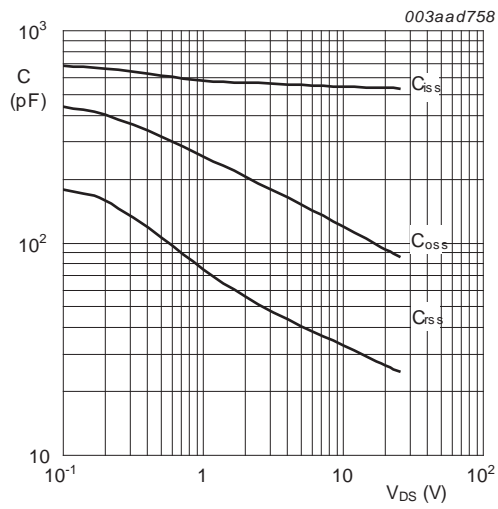
$I_F = 250\mu\text{A}$

Fig 16. Temperature sense diode forward voltage as a function of junction temperature; typical values, FET1 and FET2



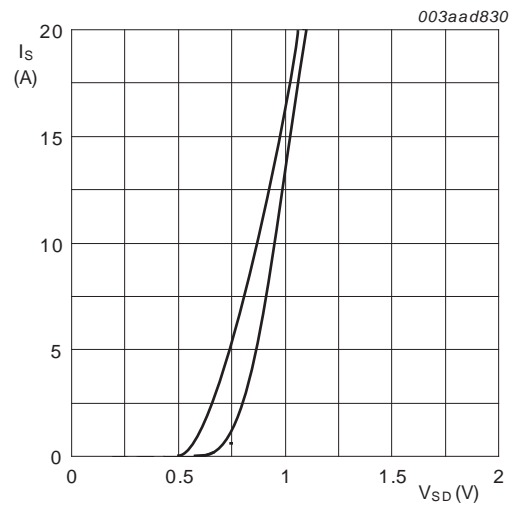
$T_j = 25^\circ\text{C}; I_D = 3\text{A}$

Fig 17. Gate-source voltage as a function of turn-on gate charge; typical values, FET1 and FET2



$V_{GS} = 0V; f = 1MHz$

Fig 18. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2



$V_{GS} = 0V$

Fig 19. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

7. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

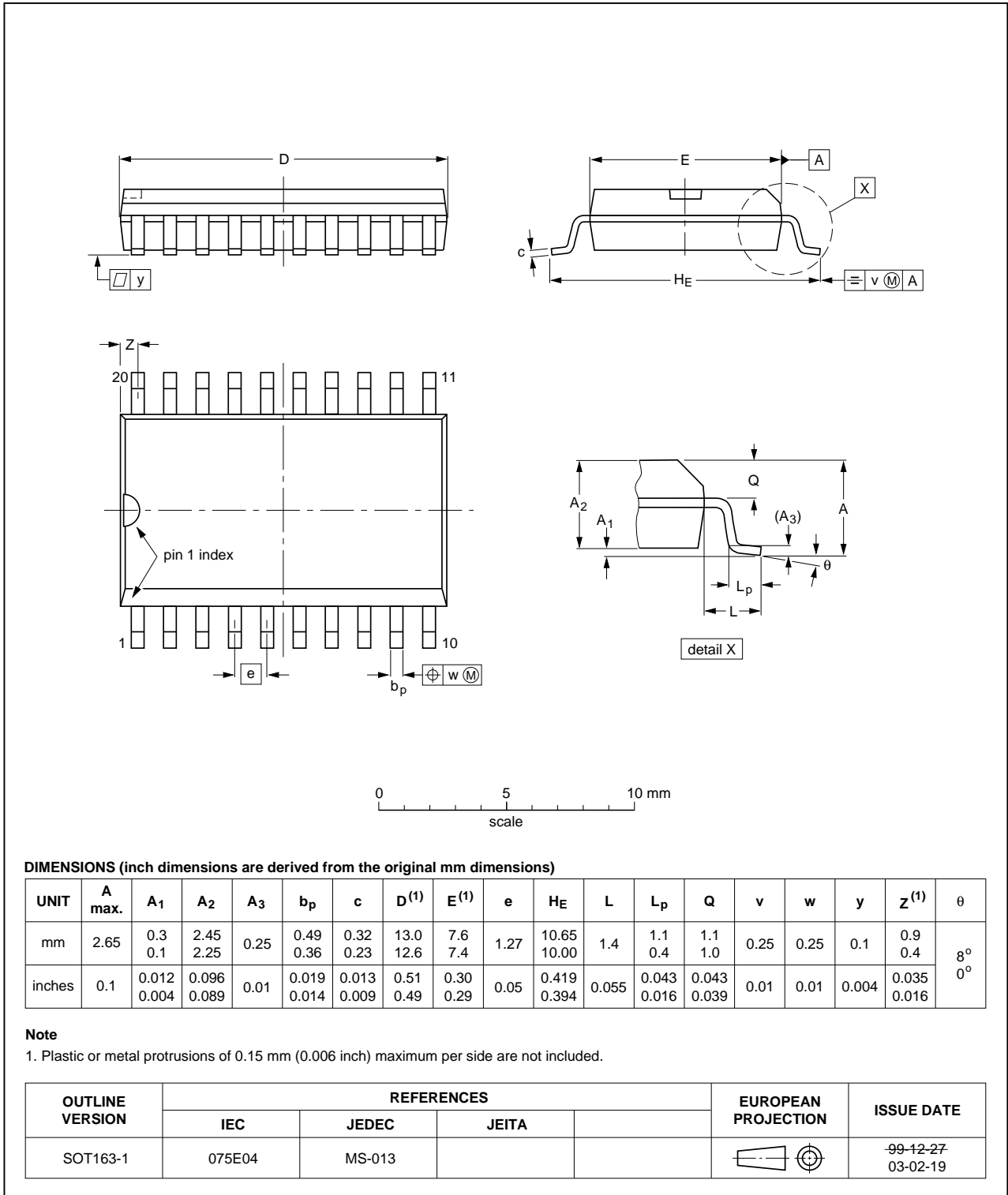


Fig 20. Package outline SOT163-1 (SO20)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9MTT-65PBB v.2	20100617	Product data sheet	-	BUK9MTT-65PBB v.1
Modifications:	• Status changed from objective to product.			
BUK9MTT-65PBB v.1	20100328	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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