

DAC1001D125

Dual 10-bit DAC, up to 125 Msps

Rev. 2 — 27 January 2012

Product data sheet

1. General description

The DAC1001D125 is a dual-port high-speed 2-channel CMOS Digital-to-Analog Converter (DAC), optimized for high dynamic performance with low power dissipation. Supporting an update rate of up to 125 Msps, the DAC1001D125 is suitable for Direct IF applications.

Separate write inputs allow data to be written to the two DAC ports independently of one another. Two separate clocks control the update rate of each DAC port.

The DAC1001D125 can interface two separate data ports or one single interleaved high-speed data port. In Interleaved mode, the input data stream is demultiplexed into its original I and Q data and latched. The I and Q data is then converted by the two DACs and updated at half the input data rate.

Each DAC port has a high-impedance differential current output, suitable for both single-ended and differential analog output configurations.

The DAC1001D125 is pin compatible with the AD9763, DAC2900 and DAC5652.

2. Features and benefits

- Dual 10-bit resolution
- 125 Msps update rate
- Single 3.3 V supply
- Dual-port or Interleaved data modes
- 1.8 V, 3.3 V and 5 V compatible digital inputs
- Internal and external reference
- 2 mA to 20 mA full-scale output current
- Typical 185 mW power dissipation
- 16 mW power-down
- SFDR: 80 dBc; $f_o = 1$ MHz; $f_s = 52$ Msps
- SFDR: 77 dBc; $f_o = 10.4$ MHz; $f_s = 78$ Msps
- SFDR: 72 dBc; $f_o = 1$ MHz; $f_s = 52$ Msps; -12 dBFS
- LQFP48 package
- Industrial temperature range of -40 °C to $+85$ °C

3. Applications

- Quadrature modulation
- Medical/test instrumentation
- Direct IF applications
- Direct digital frequency synthesis
- Arbitrary waveform generator



4. Ordering information

Table 1. Ordering information

| Type number | Package | | Version |
|---------------|---------|--|----------|
| | Name | Description | |
| DAC1001D125HL | LQFP48 | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |

5. Block diagram

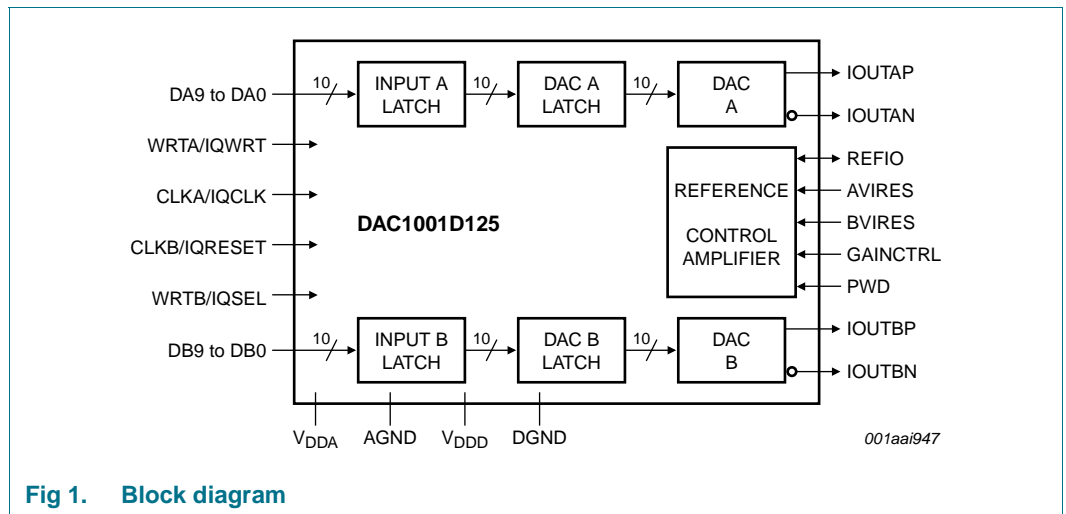


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

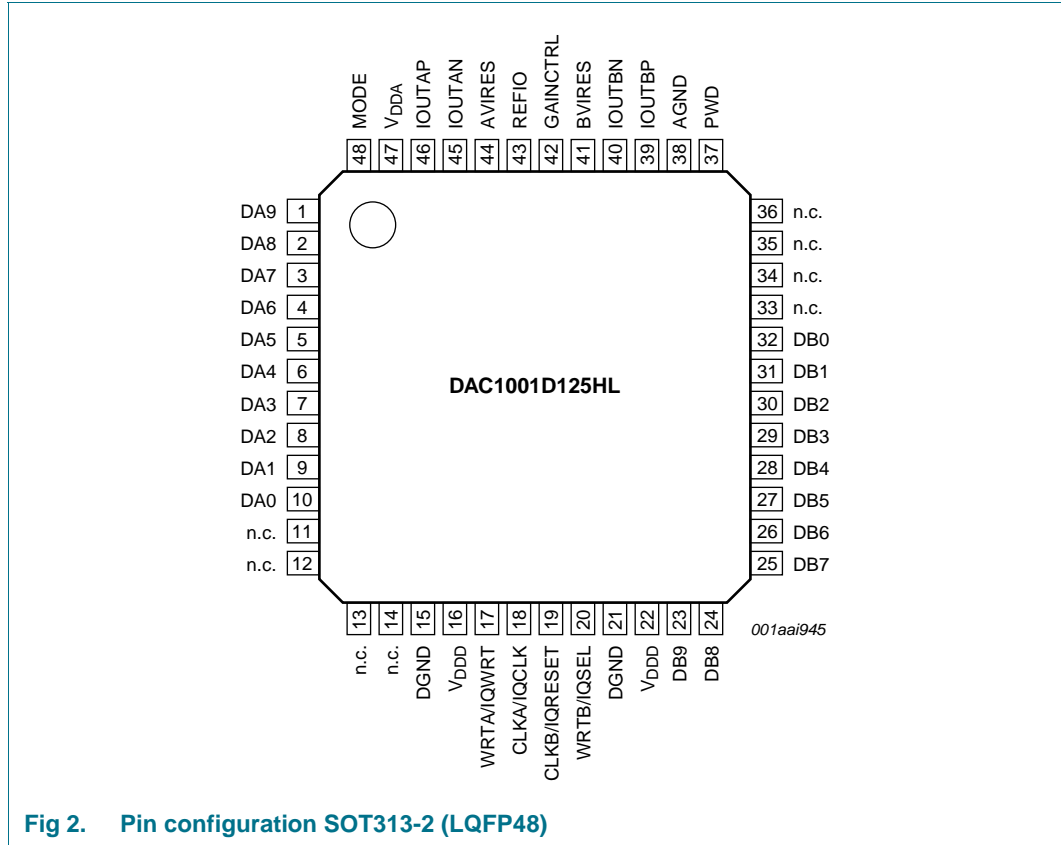


Fig 2. Pin configuration SOT313-2 (LQFP48)

6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Type ^[1] | Description |
|--------|-----|---------------------|-------------------------------|
| DA9 | 1 | I | DAC A, data input bit 9 (MSB) |
| DA8 | 2 | I | DAC A, data input bit 8 |
| DA7 | 3 | I | DAC A, data input bit 7 |
| DA6 | 4 | I | DAC A, data input bit 6 |
| DA5 | 5 | I | DAC A, data input bit 5 |
| DA4 | 6 | I | DAC A, data input bit 4 |
| DA3 | 7 | I | DAC A, data input bit 3 |
| DA2 | 8 | I | DAC A, data input bit 2 |
| DA1 | 9 | I | DAC A, data input bit 1 |
| DA0 | 10 | I | DAC A, data input bit 0 (LSB) |
| n.c. | 11 | | not connected |
| n.c. | 12 | | not connected |
| n.c. | 13 | | not connected |

Table 2. Pin description ...continued

| Symbol | Pin | Type ^[1] | Description |
|------------------|-----|---------------------|---|
| n.c. | 14 | | not connected |
| DGND | 15 | G | digital ground |
| V _{DD} | 16 | S | digital supply voltage |
| WRTA/IQWRT | 17 | I | input write port A/input write IQ in Interleaved mode |
| CLKA/IQCLK | 18 | I | input clock port A/input clock IQ in Interleaved mode |
| CLKB/IQRESET | 19 | I | input clock port B/reset IQ in Interleaved mode |
| WRTB/IQSEL | 20 | I | input write port B/select IQ in Interleaved mode |
| DGND | 21 | G | digital ground |
| V _{DD} | 22 | S | digital supply voltage |
| DB9 | 23 | I | DAC B, data input bit 9 (MSB) |
| DB8 | 24 | I | DAC B, data input bit 8 |
| DB7 | 25 | I | DAC B, data input bit 7 |
| DB6 | 26 | I | DAC B, data input bit 6 |
| DB5 | 27 | I | DAC B, data input bit 5 |
| DB4 | 28 | I | DAC B, data input bit 4 |
| DB3 | 29 | I | DAC B, data input bit 3 |
| DB2 | 30 | I | DAC B, data input bit 2 |
| DB1 | 31 | I | DAC B, data input bit 1 |
| DB0 | 32 | I | DAC B, data input bit 0 (LSB) |
| n.c. | 33 | | not connected |
| n.c. | 34 | | not connected |
| n.c. | 35 | | not connected |
| n.c. | 36 | | not connected |
| PWD | 37 | I | power-down mode |
| AGND | 38 | S | analog ground |
| IOUTBP | 39 | O | DAC B current output |
| IOUTBN | 40 | O | complementary DAC B current output |
| BVIRE | 41 | I | adjust DAC B for full-scale output current |
| GAINCTRL | 42 | I | gain control mode |
| REFIO | 43 | I/O | reference I/O |
| AVIRE | 44 | I | adjust DAC A for full-scale output current |
| IOUTAN | 45 | O | complementary DAC A current output |
| IOUTAP | 46 | O | DAC A current output |
| V _{DDA} | 47 | S | analog supply voltage |
| MODE | 48 | I | select between Dual-port or Interleaved mode |

[1] Type description: S = Supply; G = Ground; I = Input; O = Output; I/O = Input/Output.

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|---------------------------|---|----------|------------------------|------|
| V _{DDD} | digital supply voltage | | [1] -0.3 | +5.0 | V |
| V _{DDA} | analog supply voltage | | [1] -0.3 | +5.0 | V |
| ΔV _{DD} | supply voltage difference | between analog and digital supply voltage | -150 | +150 | mV |
| V _I | input voltage | digital inputs referenced to DGND | -0.3 | +5.5 | V |
| | | pins REFIO, AVIRES, BVIRES referenced to AGND | -0.3 | +5.5 | V |
| V _O | output voltage | pins IOUTAP, IOUTAN, IOUTBP and IOUTBN referenced to AGND | -0.3 | V _{DDA} + 0.3 | V |
| T _{stg} | storage temperature | | -55 | +150 | °C |
| T _{amb} | ambient temperature | | -40 | +85 | °C |
| T _j | junction temperature | | - | 125 | °C |

[1] All supplies are connected together.

8. Thermal characteristics

Table 4. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|----------------------|---|-------------|------|------|
| R _{th(j-a)} | thermal resistance from junction to ambient | in free air | 89.3 | K/W |
| R _{th(c-a)} | thermal resistance from case to ambient | in free air | 60.6 | K/W |

9. Characteristics

Table 5. Characteristics

V_{DDD} = V_{DDA} = 3.3 V; AGND and DGND connected together; I_{O(fs)} = 20 mA and T_{amb} = -40 °C to +85 °C; typical values measured at T_{amb} = 25 °C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|--------------------------------------|--|------|------|------------------|------|
| Supplies | | | | | | |
| V _{DDD} | digital supply voltage | | 3.0 | 3.3 | 3.65 | V |
| V _{DDA} | analog supply voltage | | 3.0 | 3.3 | 3.65 | V |
| I _{DDD} | digital supply current | f _s = 65 Msps, f _o = 1 MHz, V _{DD} = 3.0 V to 3.6 V | - | 6 | 7 | mA |
| I _{DDA} | analog supply current | f _s = 65 Msps, f _o = 1 MHz, V _{DD} = 3.0 V to 3.6 V | - | 50 | 65 | mA |
| P _{tot} | total power dissipation | f _s = 65 Msps, f _o = 1 MHz, V _{DD} = 3.0 V to 3.6 V | - | 185 | 260 | mW |
| P _{pd} | power dissipation in power-down mode | | - | 16.5 | - | mW |
| Digital inputs | | | | | | |
| V _{IL} | LOW-level input voltage | | DGND | - | 0.9 | V |
| V _{IH} | HIGH-level input voltage | | 1.3 | - | V _{DDD} | V |

Table 5. Characteristics ...continued

$V_{DDD} = V_{DDA} = 3.3\text{ V}$; AGND and DGND connected together; $I_{O(fs)} = 20\text{ mA}$ and $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$; typical values measured at $T_{amb} = 25\text{ °C}$.

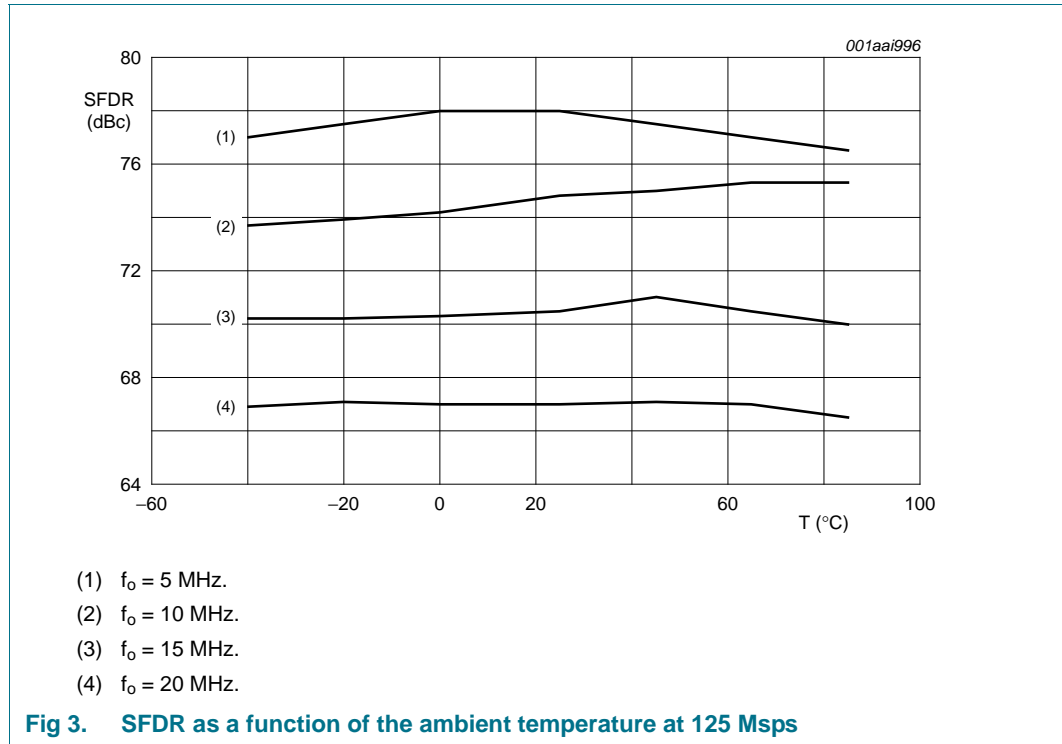
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|----------------------------|--|------------|------------|------------|---------------|
| I_{IL} | LOW-level input current | $V_{IL} = 0.9\text{ V}$ | - | 5 | - | μA |
| I_{IH} | HIGH-level input current | $V_{IH} = 1.3\text{ V}$ | - | 5 | - | μA |
| C_i | input capacitance | | [1] - | 5 | - | pF |
| Analog outputs: pins IOUTAP, IOUTAN, IOUTBP and IOUTBN | | | | | | |
| $I_{O(fs)}$ | full-scale output current | differential outputs | 2 | - | 20 | mA |
| V_O | output voltage | compliance range | -1 | - | +1.25 | V |
| R_o | output resistance | | [1] - | 150 | - | k Ω |
| C_o | output capacitance | | [1] - | 3 | - | pF |
| Reference voltage input/output: pin REFIO | | | | | | |
| $V_{O(ref)}$ | reference output voltage | | [1] 1.21 | 1.26 | 1.31 | V |
| $I_{O(ref)}$ | reference output current | | - | 100 | - | nA |
| V_i | input voltage | compliance range | 1.0 | - | 1.26 | V |
| R_i | input resistance | | - | 1 | - | M Ω |
| Input timing; see Figure 18 | | | | | | |
| f_s | sampling frequency | | - | - | 125 | Msps |
| $t_{w(WRT)}$ | WRT pulse width | pins WRTA, WRTB | 2 | - | - | ns |
| $t_{w(CLK)}$ | CLK pulse width | pins CLKA, CLKB | 2 | - | - | ns |
| $t_{h(i)}$ | input hold time | | 1 | - | - | ns |
| $t_{su(i)}$ | input set-up time | | 1.8 | - | - | ns |
| Output timing: pins IOUTAP, IOUTAN, IOUTBP and IOUTBN | | | | | | |
| t_d | delay time | | - | 1 | - | ns |
| t_t | transition time | rising or falling transition (10 % to 90 % or 90 % to 10 %) | [1] - | 0.6 | - | ns |
| t_s | settling time | $\pm 1\text{ LSB}$ | [1] - | 16 | - | ns |
| Static linearity | | | | | | |
| INL | integral non-linearity | 25 °C | ± 0.1 | ± 0.13 | ± 0.18 | LSB |
| | | -40 °C to +85 °C | ± 0.08 | - | ± 0.18 | LSB |
| DNL | differential non-linearity | -40 °C to +85 °C | ± 0.03 | ± 0.05 | ± 0.07 | LSB |
| Static accuracy (relative to full-scale) with GAINCTRL = 0 | | | | | | |
| E_{offset} | offset error | | -0.02 | - | +0.02 | % |
| E_G | gain error | with external reference | -1.9 | ± 1.5 | +2.5 | % |
| | | with internal reference | -2.9 | ± 2.1 | +2.9 | % |
| ΔG | gain mismatch | between DAC A and DAC B | -0.5 | ± 0.5 | +0.5 | % |

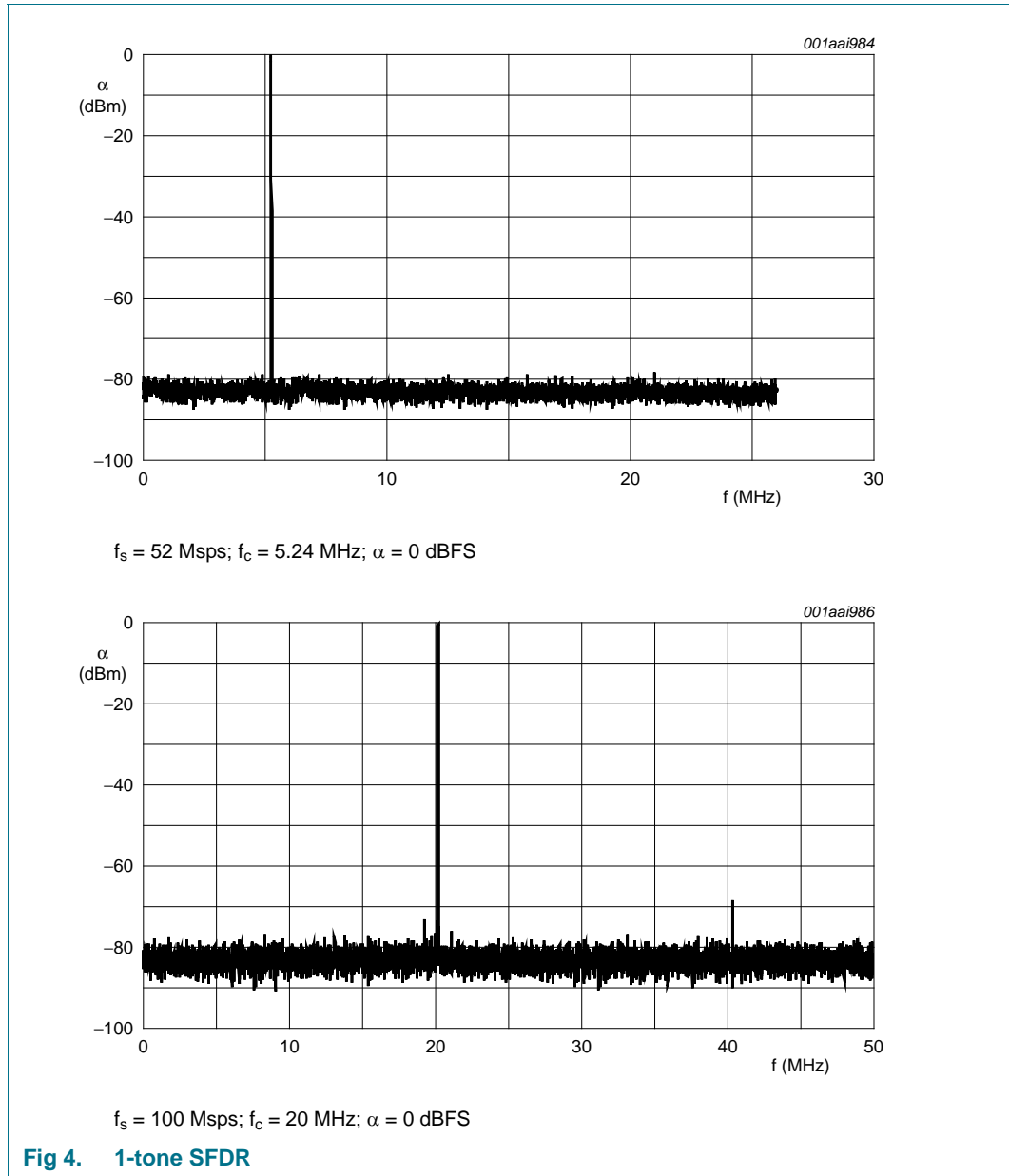
Table 5. Characteristics ...continued

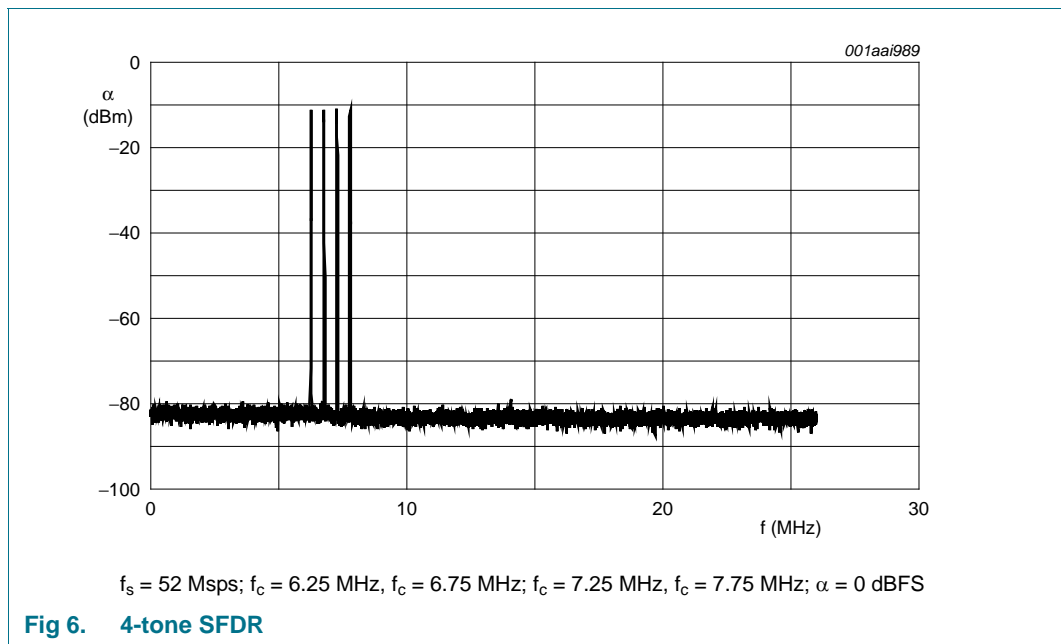
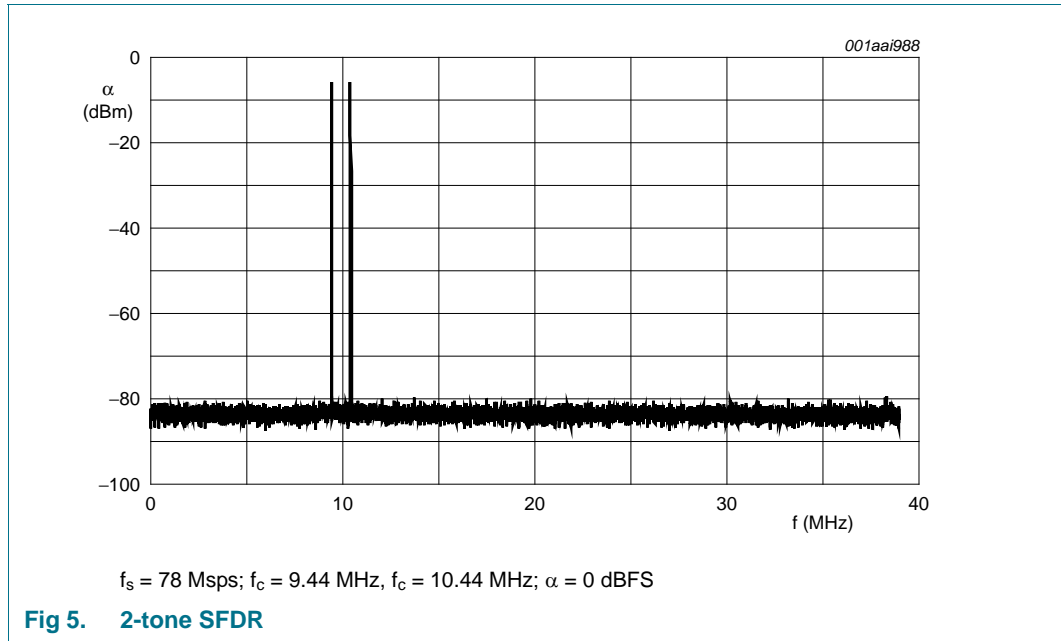
$V_{DD} = V_{DDA} = 3.3\text{ V}$; AGND and DGND connected together; $I_{O(fs)} = 20\text{ mA}$ and $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$; typical values measured at $T_{amb} = 25\text{ °C}$.

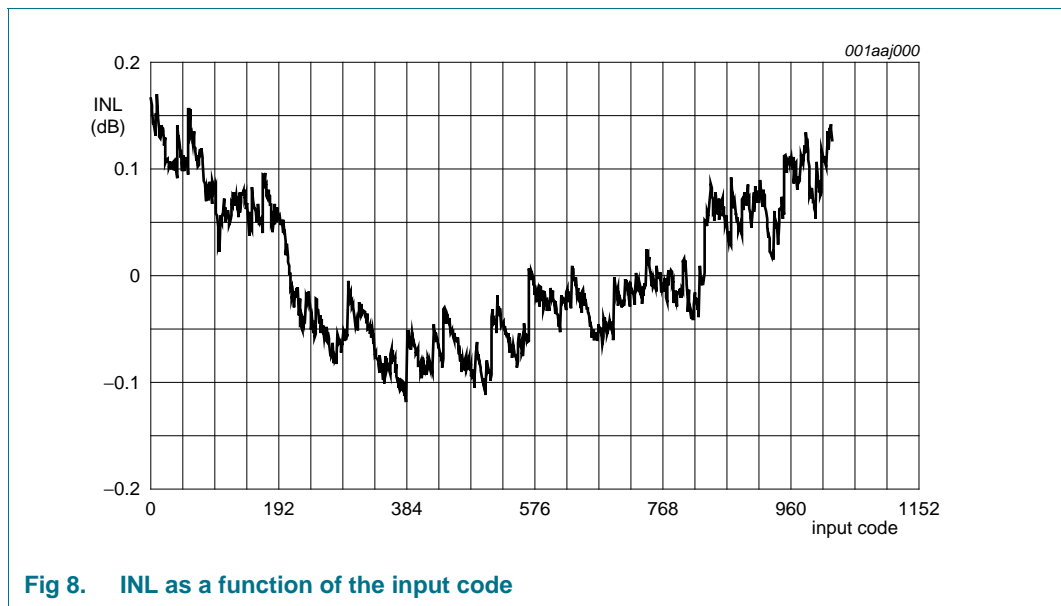
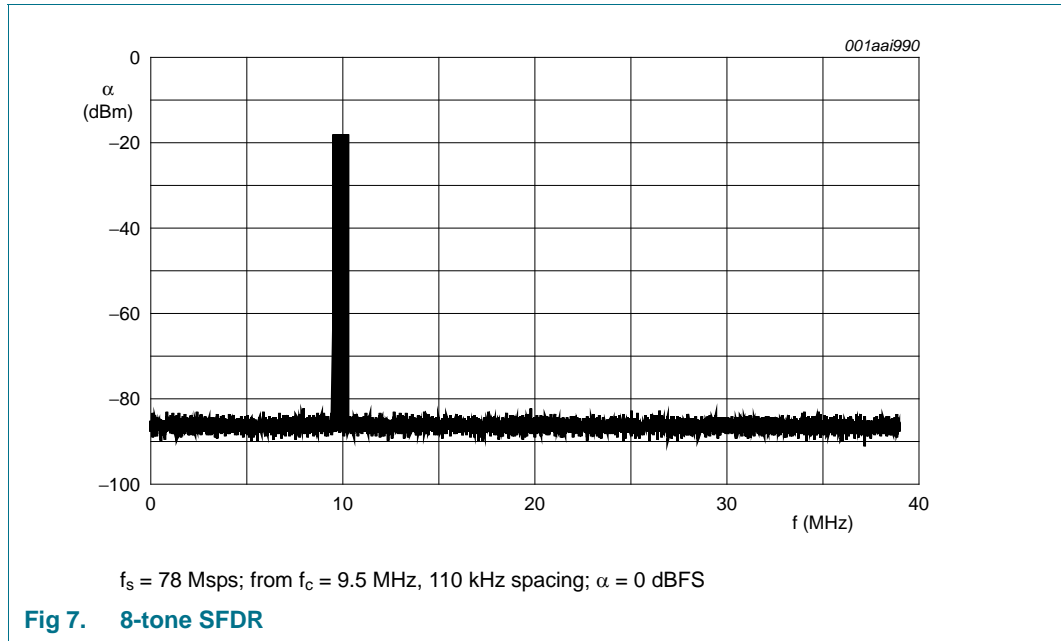
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|----------------------------|-----------------------------|--|-----|--------|-----|--------|--|
| Dynamic performance | | | | | | | |
| SFDR | spurious free dynamic range | B = Nyquist | | | | | |
| | | $f_s = 52\text{ Msps}$; $f_o = 1\text{ MHz}$ | | | | | |
| | | 0 dBFS | - | 80 | - | dBc | |
| | | -6 dBFS | - | 78 | - | dBc | |
| | | -12 dBFS | - | 72 | - | dBc | |
| | | $f_s = 52\text{ Msps}$; 0 dBFS | | | | | |
| | | $f_o = 5.24\text{ MHz}$ | - | 78 | - | dBc | |
| | | $f_s = 78\text{ Msps}$; 0 dBFS | | | | | |
| | | $f_o = 10.4\text{ MHz}$ | - | 77 | - | dBc | |
| | | $f_o = 15.7\text{ MHz}$ | - | 70 | - | dBc | |
| | | $f_s = 100\text{ Msps}$; 0 dBFS | | | | | |
| | | $f_o = 5.04\text{ MHz}$ | - | 76 | - | dBc | |
| | | $f_o = 20.2\text{ MHz}$ | 60 | 68 | - | dBc | |
| | | $f_s = 125\text{ Msps}$; 0 dBFS | | | | | |
| | | $f_o = 20.1\text{ MHz}$ | - | 67 | - | dBc | |
| | | Within a Window | | | | | |
| THD | total harmonic distortion | $f_s = 52\text{ Msps}$; $f_o = 1\text{ MHz}$; 2 MHz span | - | 87 | - | dBc | |
| | | $f_s = 52\text{ Msps}$; $f_o = 5.24\text{ MHz}$; 10 MHz span | - | 85 | - | dBc | |
| | | $f_s = 78\text{ Msps}$; $f_o = 5.26\text{ MHz}$; 10 MHz span | - | 88 | - | dBc | |
| | | $f_s = 125\text{ Msps}$; $f_o = 5.04\text{ MHz}$; 10 MHz span | 78 | 88 | - | dBc | |
| | | $f_s = 52\text{ Msps}$; $f_o = 1\text{ MHz}$ | - | -77 | - | dBc | |
| MTPR | multitone power ratio | $f_s = 78\text{ Msps}$; $f_o = 5.26\text{ MHz}$ | - | -75 | - | dBc | |
| | | $f_s = 100\text{ Msps}$; $f_o = 5.04\text{ MHz}$ | - | -73 | - | dBc | |
| | | $f_s = 125\text{ Msps}$; $f_o = 20.1\text{ MHz}$ | - | -63 | -59 | dBc | |
| | | $f_s = 65\text{ Msps}$; 2 MHz < f_o < 2.99 MHz; 8 tones at 110 kHz spacing at 0 dB full-scale | - | 80 | - | dBc | |
| NSD | noise spectral density | $f_s = 100\text{ Msps}$; $f_o = 5.04\text{ MHz}$ | - | -148.5 | - | dBm/Hz | |
| α_{cs} | channel separation | $f_s = 78\text{ Msps}$; $f_o = 10.4\text{ MHz}$ | - | 88.0 | - | dBc | |
| | | $f_s = 125\text{ Msps}$; $f_o = 20.1\text{ MHz}$ | - | 83.5 | - | dBc | |

[1] Guaranteed by design.









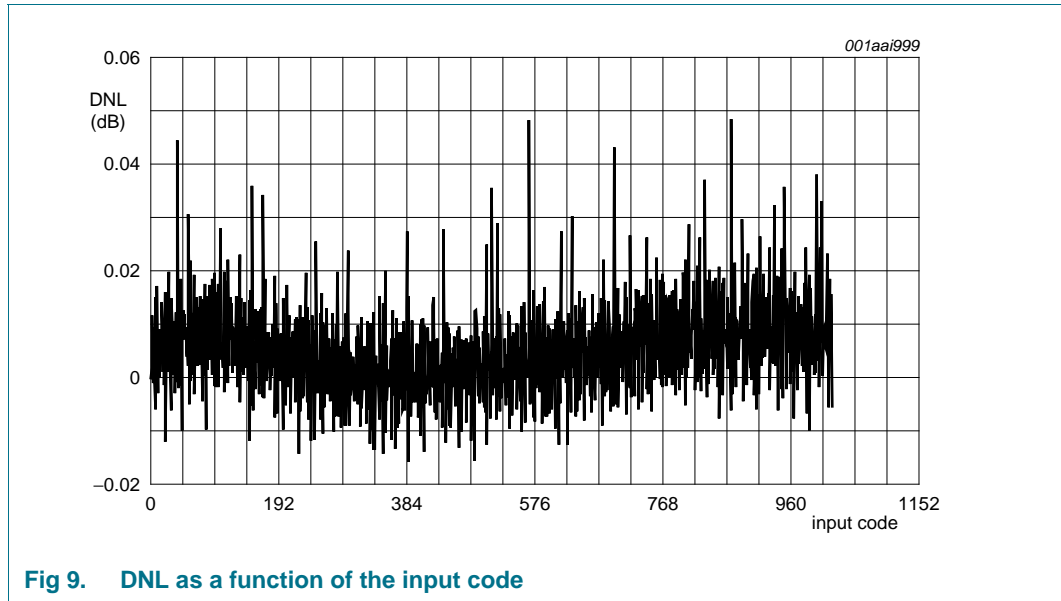


Fig 9. DNL as a function of the input code

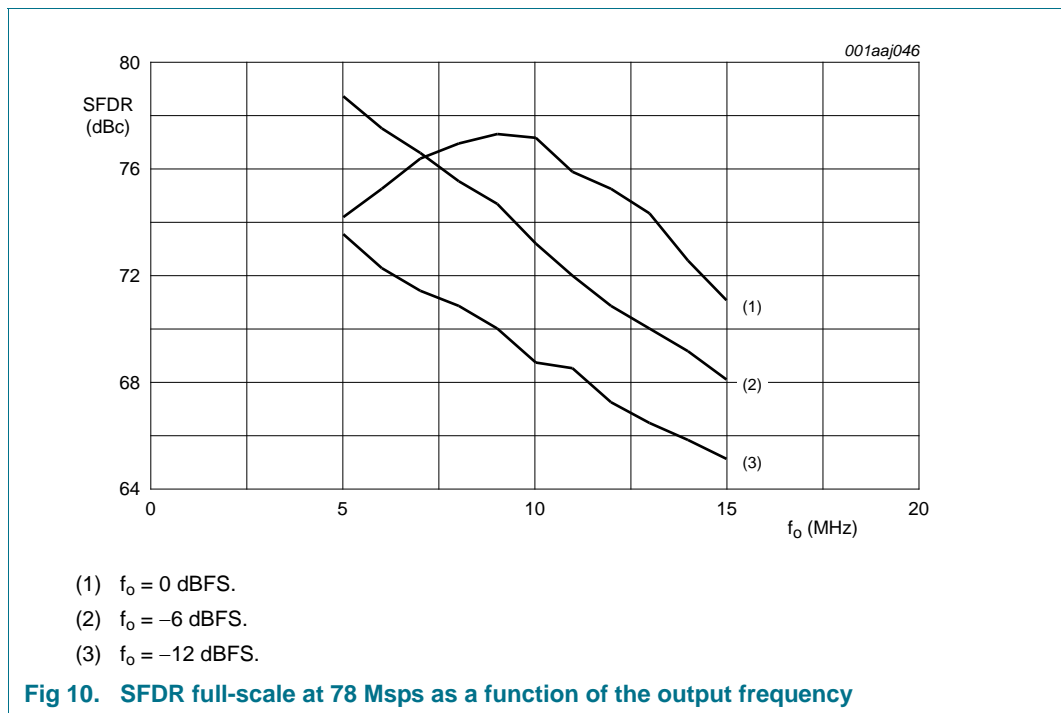
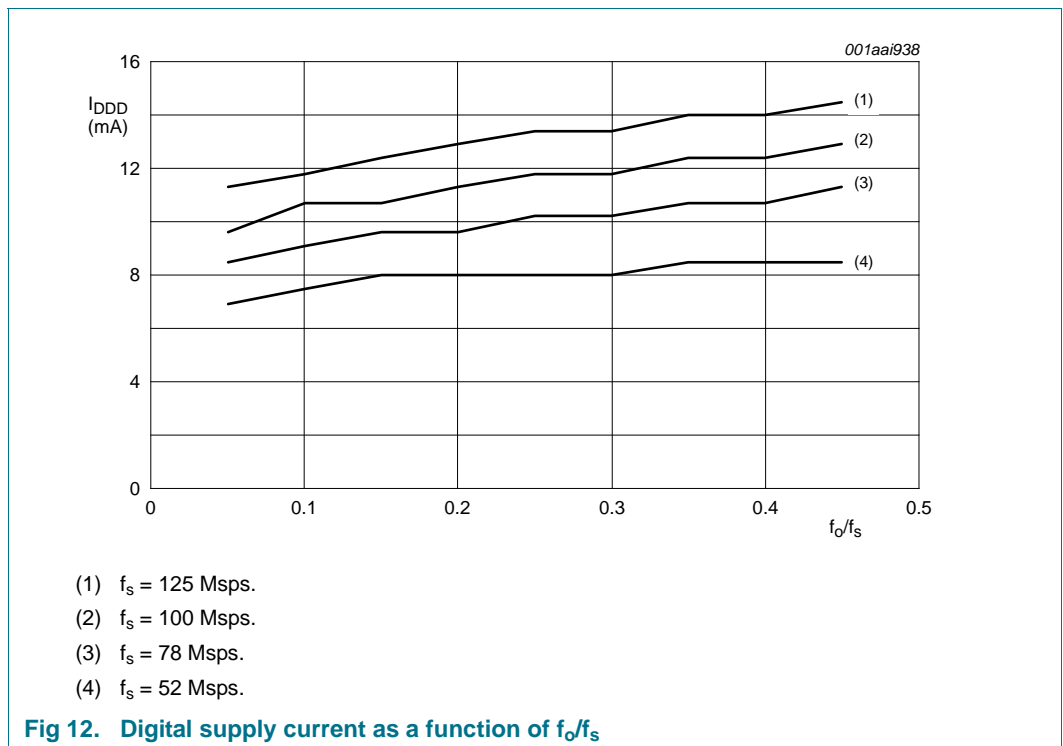
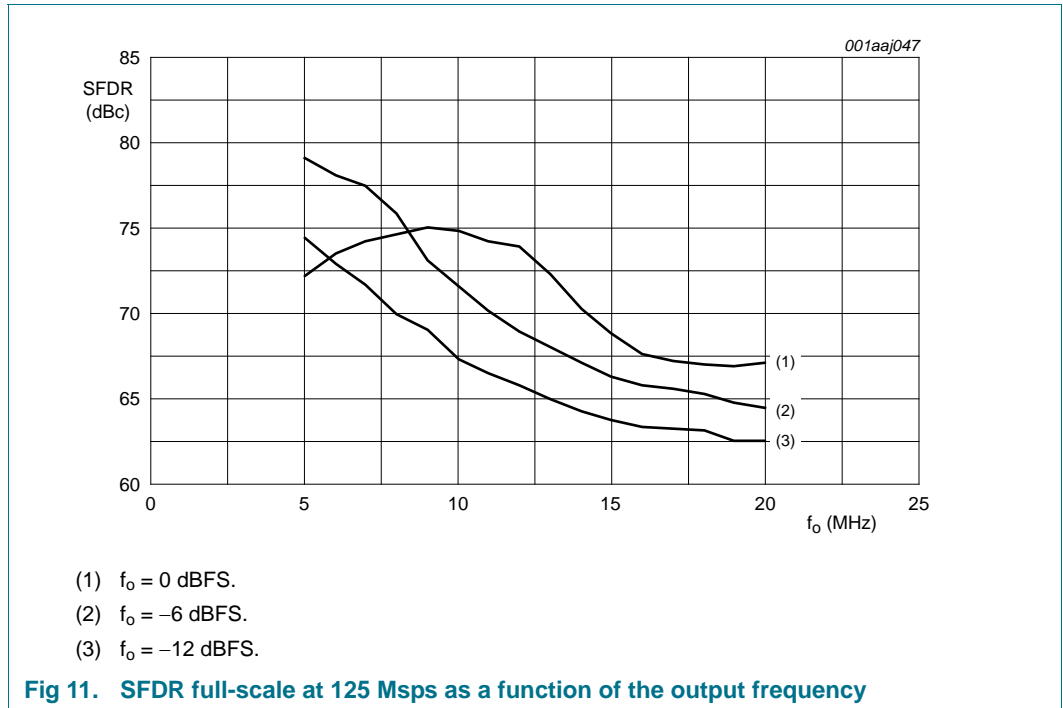
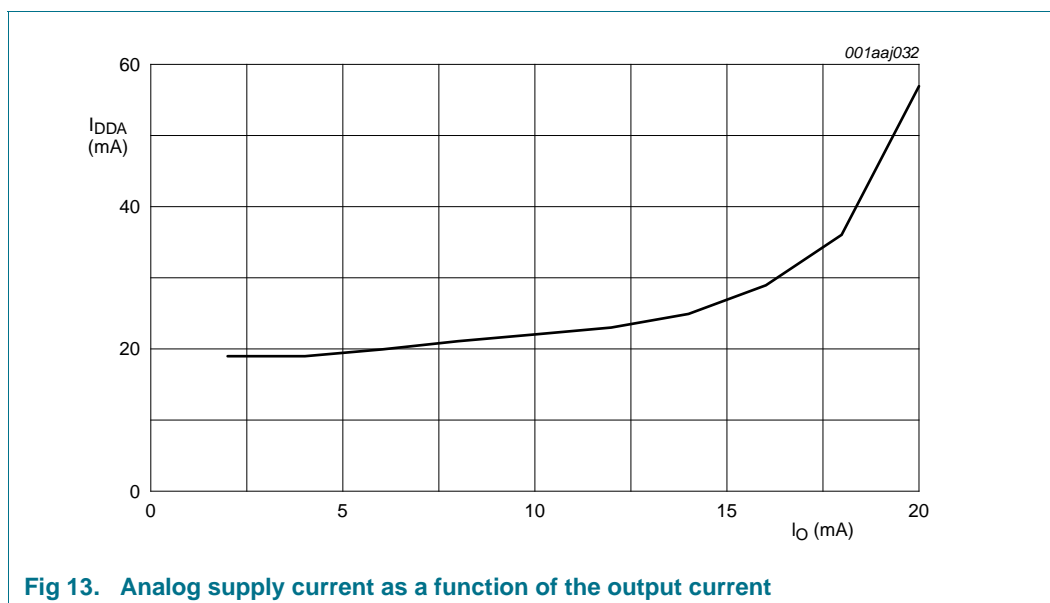


Fig 10. SFDR full-scale at 78 Mps as a function of the output frequency





10. Application information

10.1 General description

The DAC1001D125 is a dual 10-bit DAC operating up to 125 Msp/s. Each DAC consists of a segmented architecture, comprising a 7-bit thermometer sub-DAC and a 3-bit binary weighted sub-DAC.

Two modes are available for the digital input depending on the status of the pin MODE. In Dual-port mode, each DAC uses its own data input line at the same frequency as the update rate. In Interleaved mode, both DACs use the same data input line at twice the update rate.

Each DAC generates on pins IOU_{TAP}/IOU_{TAN} and IOU_{TBP}/IOU_{TBN} two complementary current outputs. This provides a full-scale output current ($I_{O(fs)}$), up to 20 mA. A single common or two independent full-scale current controls can be selected for both channels using pin GAIN_{CTRL}. An internal reference is available for the reference current, which is externally adjustable using pin REF_{IO}.

The DAC1001D125 operates at 3.3 V and has separate digital and analog power supplies. Pin PWD is used to power-down the device. The digital input is 1.8 V compliant, 3.3 V compliant and 5 V tolerant.

10.2 Input data

The DAC1001D125 input follows a straight binary coding where DA₉ and DB₉ are the Most Significant Bits (MSB) and DA₀ and DB₀ are the Least Significant Bits (LSB).

The setting applied to pin MODE defines whether the DAC1001D125 operates in Dual-port mode or in Interleaved mode (see [Table 6](#)).

Table 6. Mode selection

| Mode | Function | DA9 to DA0 | DB9 to DB0 | Pin 17 | Pin 18 | Pin 19 | Pin 20 |
|------|------------------|------------|------------|--------|--------|---------|--------|
| 0 | Interleaved mode | active | off | IQWRT | IQCLK | IQRESET | IQSEL |
| 1 | Dual-port mode | active | active | WRTA | CLKA | CLKB | WRTB |

10.2.1 Dual-port mode

The data and clock circuit for Dual-port mode operation is shown in [Figure 14](#).

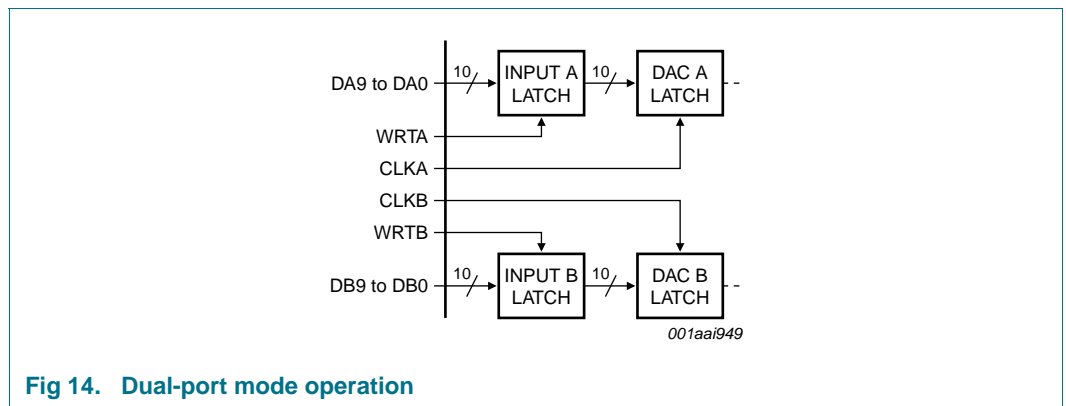


Fig 14. Dual-port mode operation

Each DAC has its own independent data and clock inputs. The data enters the input latch on the rising edge of the WRTA/WRTB signal and is transferred to the DAC latch. The output is updated on the rising edge of the CLKA/CLKB signal.

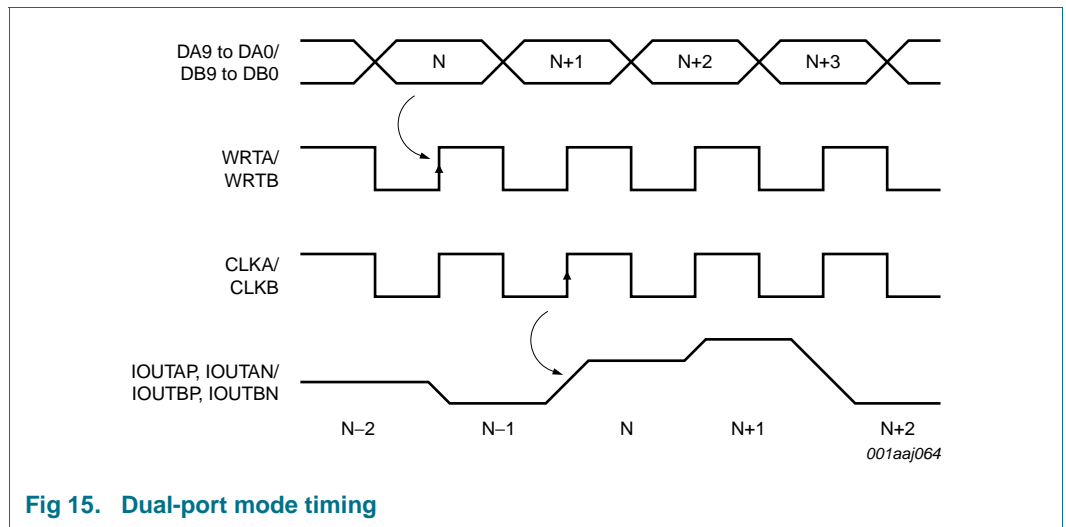


Fig 15. Dual-port mode timing

10.2.2 Interleaved mode

The data and clock circuit for Interleaved mode operation is illustrated in Figure 16.

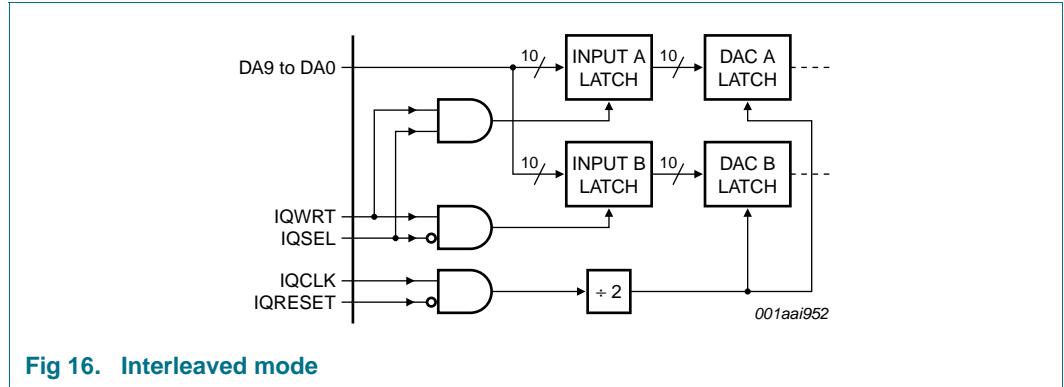


Fig 16. Interleaved mode

In Interleaved mode, both DACs use the same data and clock inputs at twice the update rate. Data enters the latch on the rising edge of IQWRT. The data is sent to either latch A or latch B, depending on the value of IQSEL. The IQSEL transition must occur when IQWRT and IQCLK are LOW.

The IQCLK is divided by 2 internally and the data is transferred to the DAC latch. It is updated on its rising edge. When IQRESET is HIGH, IQCLK is disabled, see Figure 17.

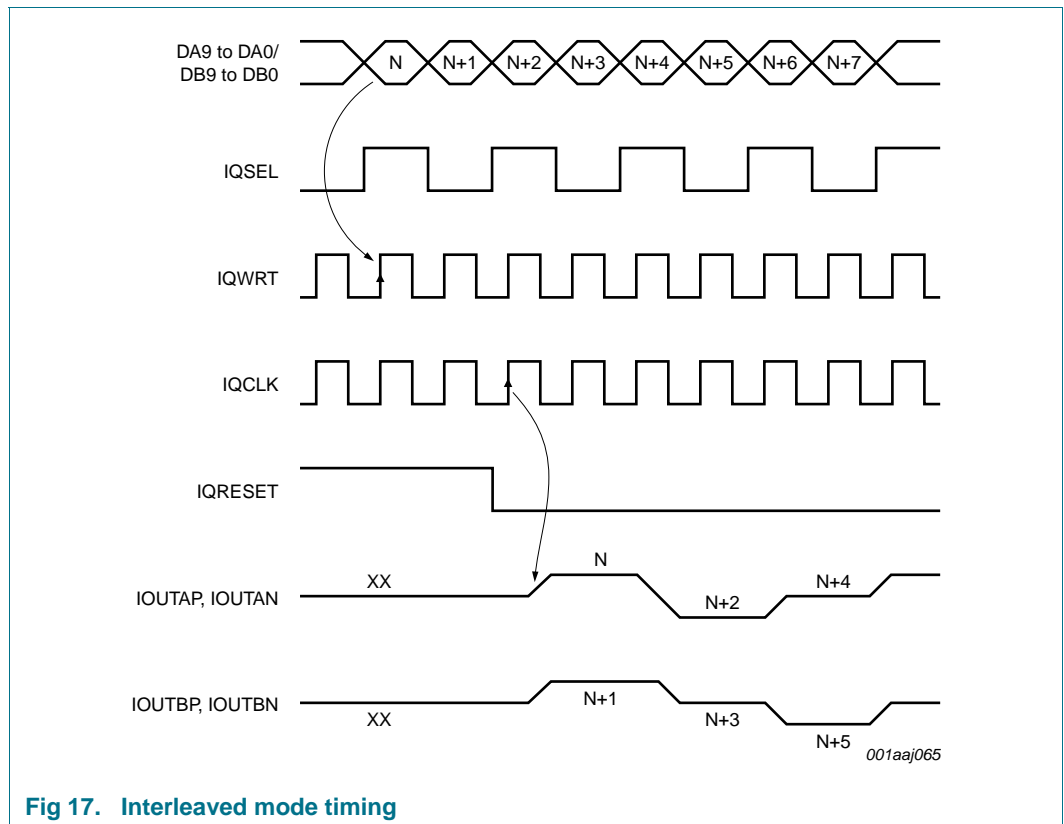


Fig 17. Interleaved mode timing

10.3 Timing

The DAC1001D125 can operate at an update rate of 125 Msps, which generates an input data rate of 125 MHz in Dual-port mode and 250 MHz in Interleaved mode. The timing of the DAC1001D125 is shown in [Figure 18](#).

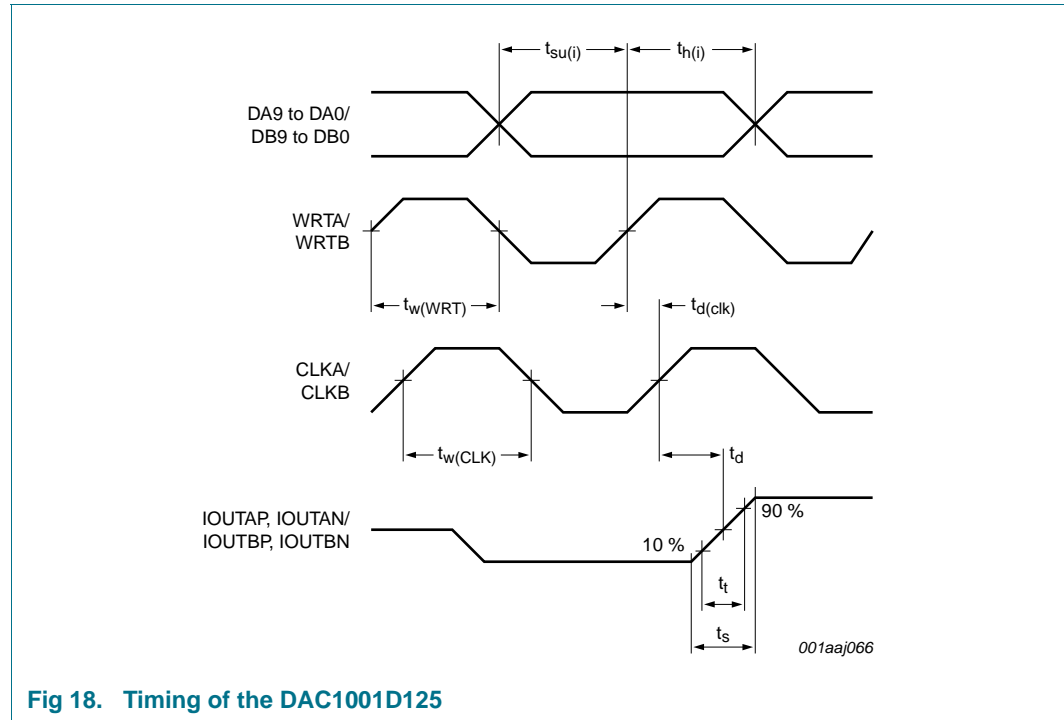


Fig 18. Timing of the DAC1001D125

The typical performances are measured at 50 % duty cycle but any timing within the limits of the characteristics will not alter the performance.

- A configuration resulting in the same timing for the signals WRTA/WRTB and CLKA/CLKB, can be achieved either by synchronizing them or by connecting them together.
- The rising edge of the CLKA/CLKB signal can also be placed in a range from half a period in front of the rising edge of the WRTA/WRTB signal to half a period minus 1 ns after the rising edge of the WRTA/WRTB signal.

A typical set-up time of 0 ns and a hold time of 0.6 ns enable the DAC1001D125 to be easily integrated into any application.

10.4 DAC transfer function

The full-scale output current for each DAC is the sum of the two complementary current outputs:

$$I_{O(fs)} = I_{IOUTP} + I_{IOUTN} \tag{1}$$

The output current depends on the digital input data:

$$I_{IOUTP} = I_{O(fs)} \times \left(\frac{DATA}{1024} \right) \quad I_{IOUTN} = I_{O(fs)} \times \left(\frac{(1023 - DATA)}{1024} \right)$$

Table 7 shows the output current as a function of the input data, when $I_{O(fs)} = 20 \text{ mA}$.

Table 7. DAC transfer function

| Data | DA9/DB9 to DA0/DB0 | IOUTAP/IOUTBP | IOUTAN/IOUTBN |
|-------|--------------------|---------------|---------------|
| 0 | 00 0000 0000 | 0 mA | 20 mA |
| ... | ... | ... | ... |
| 8192 | 10 0000 0000 | 10 mA | 10 mA |
| ... | ... | ... | ... |
| 16383 | 11 1111 1111 | 20 mA | 0 mA |

10.5 Full-scale current adjustment

The DAC1001D125 integrates one 1.25 V reference and two current sources to adjust the full-scale current in both DACs.

The internal reference configuration is shown in Figure 19.

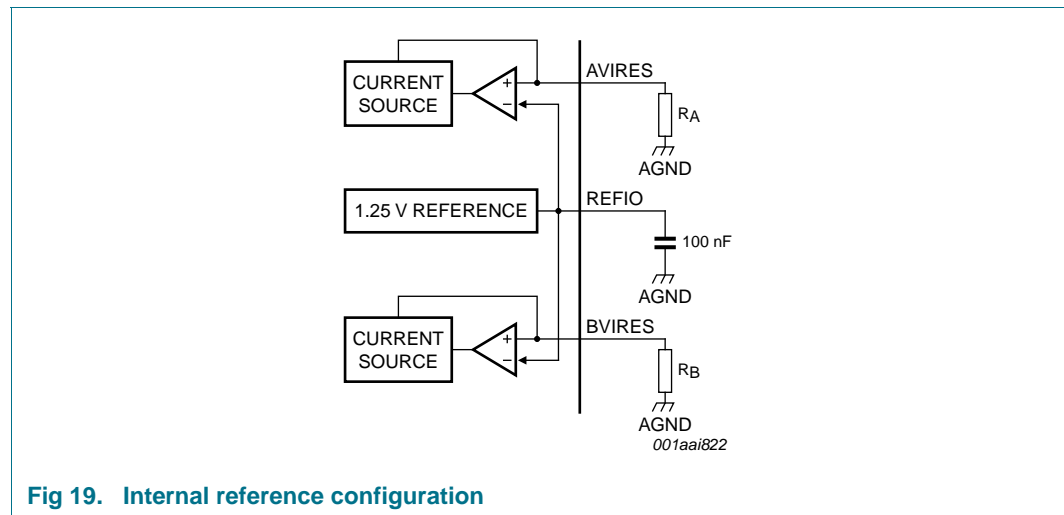


Fig 19. Internal reference configuration

The bias current is generated by the output of the internal regulator connected to the inverting input of the internal operational amplifiers. The external resistors R_A and R_B are connected to pins AVIRES and BVIRES, respectively. This configuration is optimal for temperature drift compensation because the band gap can be matched with the voltage on the feedback resistors.

The relationship between full-scale output current ($I_{O(fs)}$) at the output of channel A or channel B and the resistor is:

$$I_{O(fs)} = \frac{24V_{REFIO}}{R_A} \tag{2}$$

The output current of the two DACs is typically fixed to 20 mA when both resistors R_A and R_B are set to 1.5 kΩ. The operational range of DAC1001D125 is from 2 mA to 20 mA.

It is recommended to decouple pin REFIO with a 100 nF capacitor.

An external reference can also be used for applications requiring higher accuracy or precise current adjustment. Due to the high input impedance of pin REFIO, applying an external source disables the band gap.

10.6 Gain control

Table 8 shows how to select the different gain control modes.

Table 8. Gain control

| GAINCTRL | Mode | DAC A full-scale control | DAC B full-scale control |
|----------|--------------------------|--------------------------|--------------------------|
| 0 | independent gain control | AVIRES | BVIRES |
| 1 | common gain control | AVIRES | AVIRES |

In independent gain mode, both full-scale currents can be adjusted independently using resistors R_A on pin AVIRES and R_B on pin BVIRES.

In Common gain mode, the full-scale current is adjusted with resistor R_A on pin AVIRES and divided by two in both DACs.

10.7 Analog outputs

See Figure 20 for the analog output circuit of one DAC. This circuit consists of a parallel combination of PMOS current sources and associated switches for each segment.

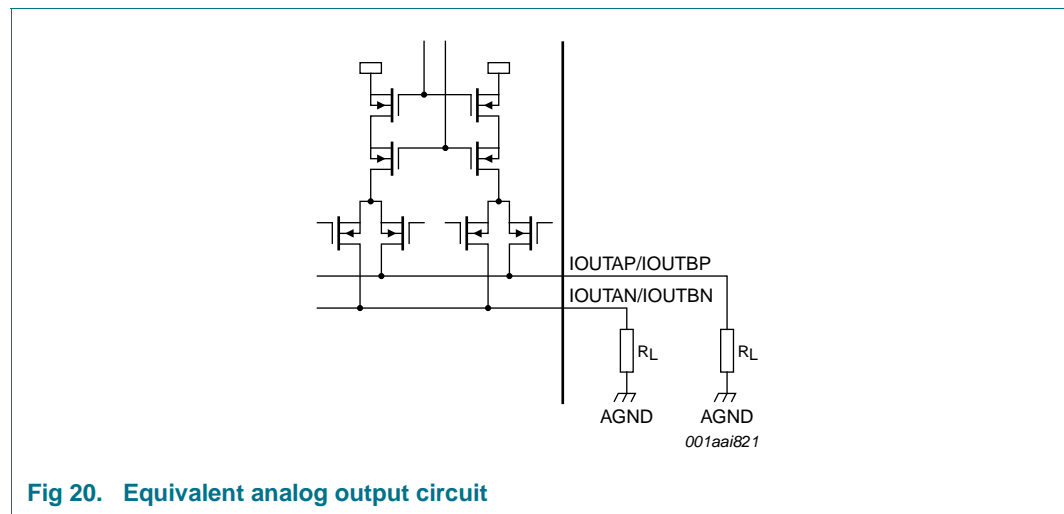


Fig 20. Equivalent analog output circuit

Cascode source configuration enables the output impedance of the source to be increased, thus improving the dynamic performance by reducing distortion.

The DAC1001D125 can be used either with:

- a differential output, coupled to a transformer (or operational amplifier) to reduce even-order harmonics and noise
- or a single-ended output for applications requiring unipolar voltage.

The typical configuration is to use 1 V p-p level on each output IOUTAP/IOUTBP and IOUTAN/IOUTBN but several combinations can be used as far as they respect the voltage compliance range.

10.7.1 Differential output using transformer

The use of a differentially coupled transformer output (see Figure 21) provides optimum distortion performance. In addition, it helps to match the impedance and provides electrical isolation.

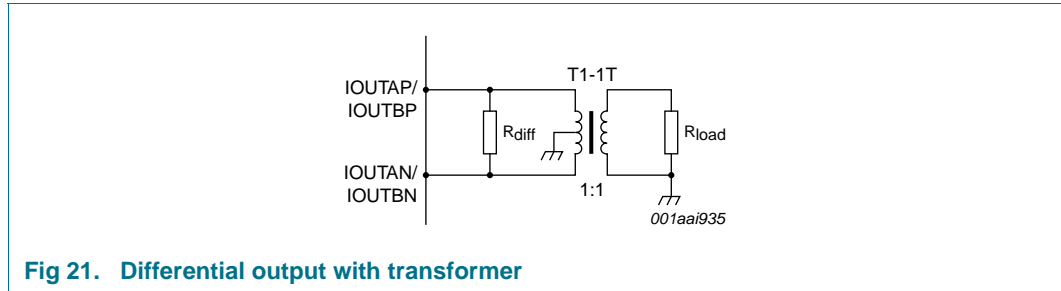


Fig 21. Differential output with transformer

The center tap is grounded to allow the DC current flow to/from both outputs. If the center tap is open, the differential resistor must be replaced by two resistors connected to ground.

10.7.2 Single-ended output

Using a single load resistor on one current output will provide an unipolar output range, typically from 0 V to 0.5 V with a 20 mA full-scale current at a 50 Ω load.

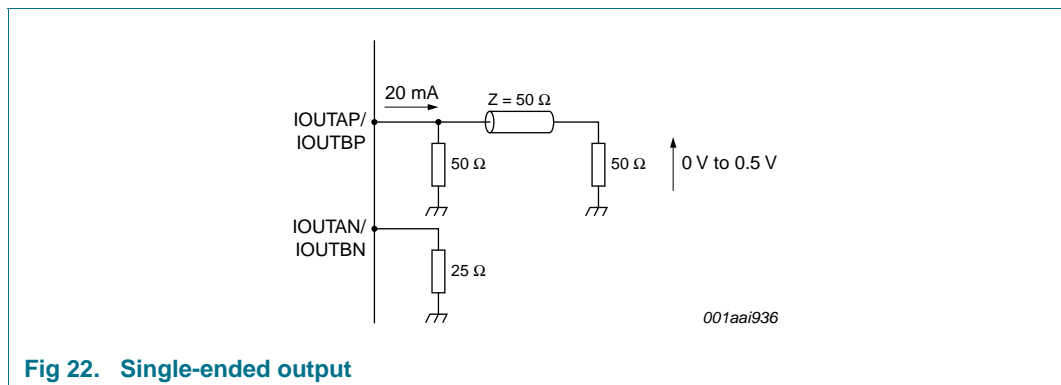


Fig 22. Single-ended output

The resistor on the other current output is 25 Ω.

10.8 Power-down function

The DAC1001D125 has a power-down function to reduce the power consumption when it is not active.

Table 9. Power-down

| PWD | Device function | Power dissipation (typ) |
|-----|-----------------|-------------------------|
| 0 | active | 185 mW |
| 1 | not active | 16.5 mW |

10.9 Alternative parts

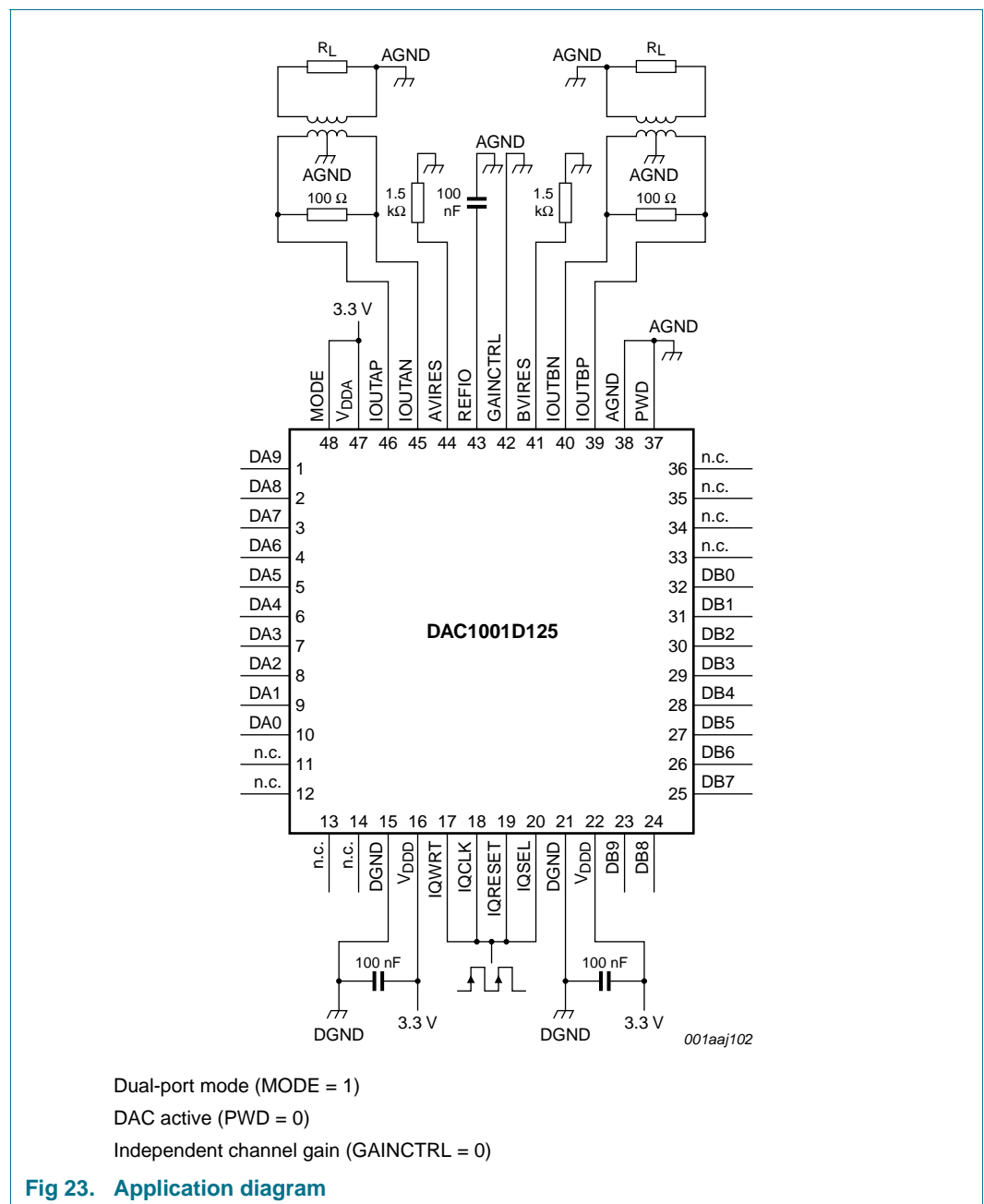
The following alternative parts are also available.

Table 10. Alternative parts

Pin compatible

| Type number | Description | Sampling frequency |
|-------------|-----------------|--------------------|
| DAC1401D125 | dual 14-bit DAC | up to 125 Msps |
| DAC1201D125 | dual 12-bit DAC | up to 125 Msps |

10.10 Application diagram



11. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

SOT313-2

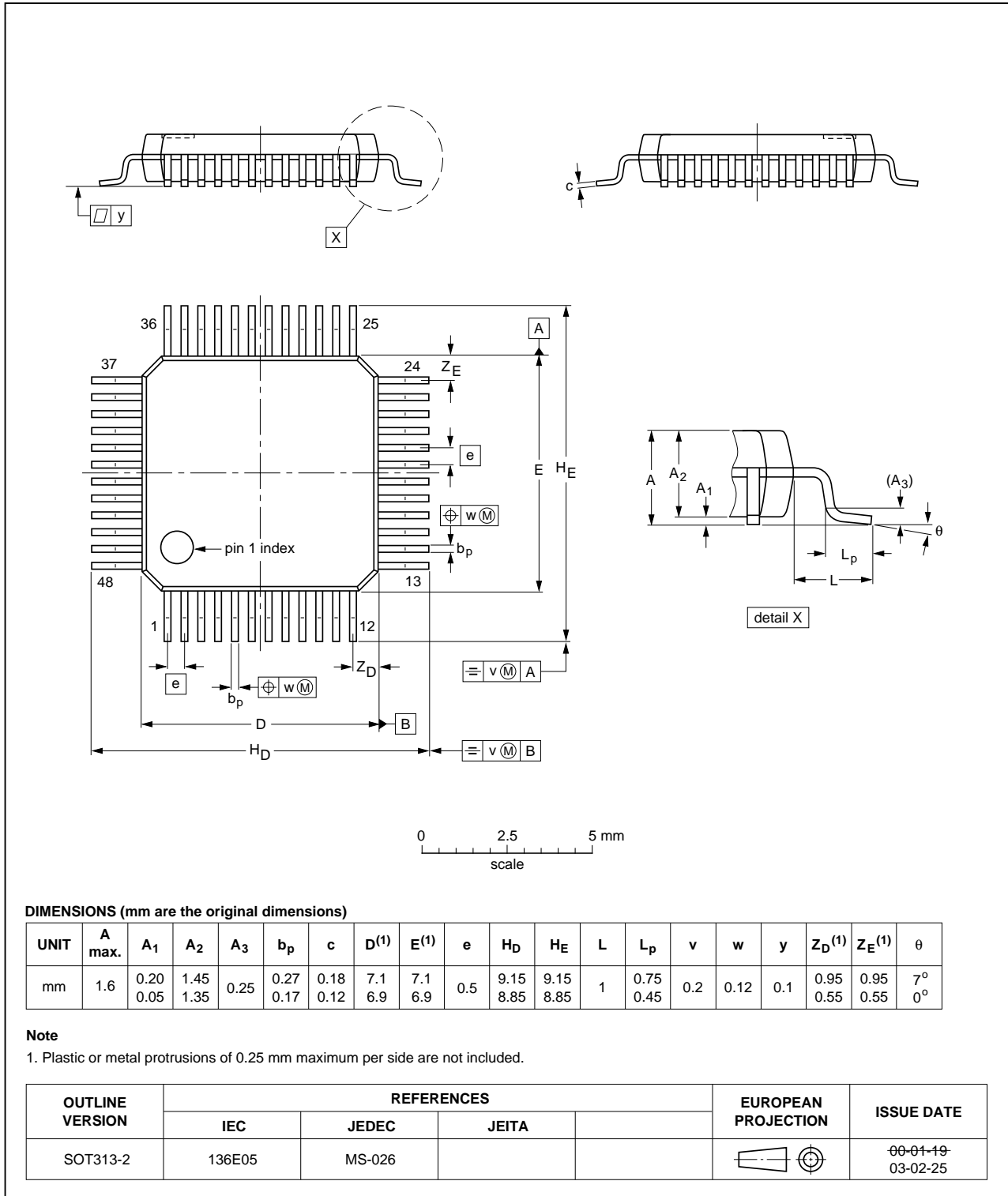


Fig 24. Package outline SOT313-2 (LQFP48)

12. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|------------------------------------|
| BW | BandWidth |
| dBFS | deciBel Full Scale |
| DDS | Direct Digital frequency Synthesis |
| IF | Intermediate Frequency |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| SFDR | Spurious-Free Dynamic Range |

13. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|--------------|--------------------|---|-----------------|
| DAC1001D125 v.2 | 20120127 | Product data sheet | - | DAC1001D125 v.1 |
| Modifications: | | | | |
| | | | <ul style="list-style-type: none">• Table 4 “Thermal characteristics” has been updated.• Section 10.6 “Gain control” has been updated. | |
| DAC1001D125 v.1 | 20081124 | Product data sheet | - | - |

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14.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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