



SA56004X

± 1 °C accurate, SMBus-compatible, 8-pin, remote/local digital temperature sensor with overtemperature alarms

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Product data sheet

1. General description

The NXP Semiconductors SA56004X is an SMBus compatible, 11-bit remote/local digital temperature sensor with overtemperature alarms. The remote channel of the SA56004X monitors a diode junction, such as a substrate PNP of a microprocessor or a diode connected transistor such as the 2N3904 (NPN) or 2N3906 (PNP). With factory trimming, remote sensor accuracy of ± 1 °C is achieved.

Undertemperature and overtemperature alert thresholds can be programmed to cause the $\overline{\text{ALERT}}$ output to indicate when the on-chip or remote temperature is out of range. This output may be used as a system interrupt or SMBus alert. The $\overline{\text{T_CRIT}}$ output is activated when the on-chip or remote temperature measurement rises above the programmed T_CRIT threshold register value. This output may be used to activate a cooling fan, send a warning or trigger a system shutdown. To further enhance system reliability, the SA56004X employs an SMBus time-out protocol. The SA56004X has a unique device architecture.

The SA56004X is available in the SO8, TSSOP8 and HVSON8 packages. SA56004X has 8 factory-programmed device address options. The SA56004X is pin-compatible with the LM86, MAX6657/8, and ADM1032.

2. Features

- Accurately senses temperature of remote microprocessor thermal diodes or diode connected transistors within ± 1 °C
- On-chip local temperature sensing within ± 2 °C
- Temperature range of -40 °C to $+125$ °C
- 11-bit, 0.125 °C resolution
- 8 different device addresses are available for server applications. The SA56004ED with marking code 56004E, and SA56004EDP with marking code 6004E are address compatible with the National LM86, the MAX6657/8 and the ADM1032.
- Offset registers available for adjusting the remote temperature accuracy
- Programmable under/overtemperature alarms: $\overline{\text{ALERT}}$ and $\overline{\text{T_CRIT}}$
- SMBus 2.0 compatible interface, supports TIMEOUT
- Operating voltage range: 3.0 V to 3.6 V
- I²C-bus Standard-mode and Fast-mode compatible
- SO8, TSSOP8 and HVSON8 packages
- Programmable conversion rate (0.0625 Hz to 26 Hz)
- Undervoltage lockout prevents erroneous temperature readings
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA

3. Applications

- System thermal management in laptops, desktops, servers and workstations
- Computers and office electronic equipment
- Electronic test equipment and instrumentation
- HVAC
- Industrial controllers and embedded systems

4. Ordering information

Table 1. Ordering information

Type number ^[1]	Package		Version
	Name	Description	
SA56004AD	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
SA56004BD			
SA56004CD			
SA56004DD			
SA56004ED			
SA56004FD			
SA56004GD			
SA56004HD			
SA56004ADP			
SA56004BDP			
SA56004ATK	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT782-1
SA56004ETK			
SA56004GDP			
SA56004HDP			

[1] There are 8 device slave address options, as described in [Table 2](#).

4.1 Ordering options

Table 2. Ordering options

Type number	Topside mark	Device slave address ^[1]
SA56004AD	56004A	1001 000
SA56004ADP	6004A	
SA56004ATK	6004A	
SA56004BD	56004B	1001 001
SA56004BDP	6004B	

Table 2. Ordering options ...continued

Type number	Topside mark	Device slave address ^[1]
SA56004CD	56004C	1001 010
SA56004CDP	6004C	
SA56004DD	56004D	1001 011
SA56004DDP	6004D	
SA56004ED ^[2]	56004E	1001 100
SA56004EDP ^[2]	6004E	
SA56004ETK ^[2]	6004E	
SA56004FD	56004F	1001 101
SA56004FDP	6004F	
SA56004FTK	6004F	
SA56004GD	56004G	1001 110
SA56004GDP	6004G	
SA56004HD	56004H	1001 111
SA56004HDP	6004H	

[1] The device slave address is factory programmed in OTP device address register.

[2] The SA56004ED/EDP/ETK has the bus address of the National LM86, MAX6657/8 and the ADM1032.

5. Block diagram

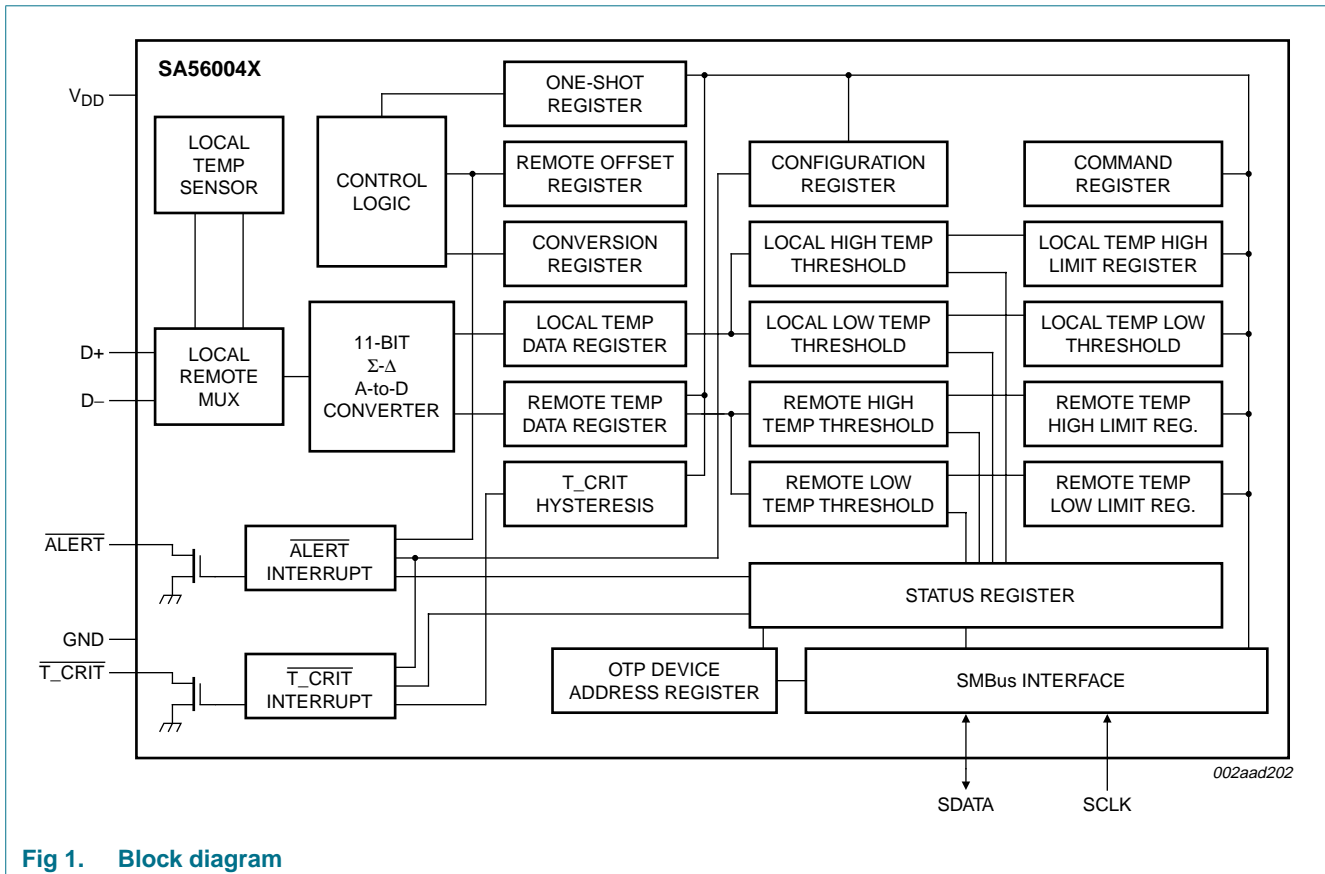
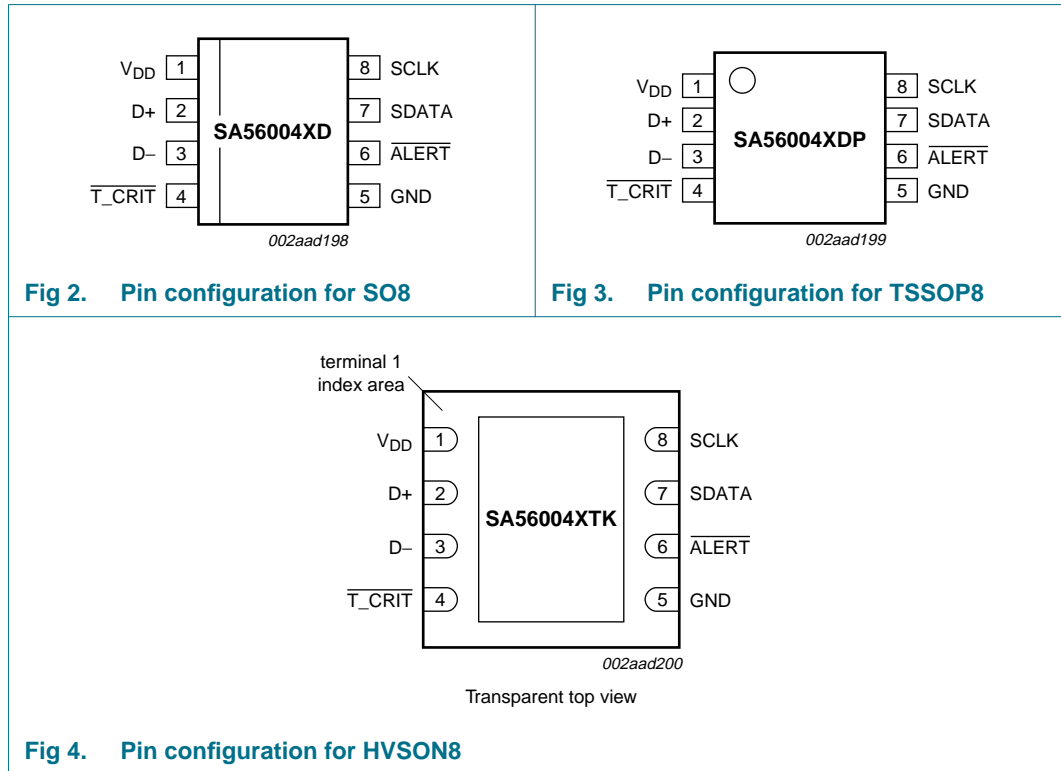


Fig 1. Block diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
V _{DD}	1	Positive supply voltage. DC voltage from 3.0 V to 5.5 V.
D+	2	Diode current source (anode).
D-	3	Diode sink current (cathode).
T _{CRIT}	4	T _{CRIT} alarm is open-drain, active LOW output which requires an external pull-up resistor. It functions as a system interrupt or power shutdown.
GND	5	Power supply ground.
ALERT	6	ALERT alarm is an open-drain, active LOW output which requires an external pull-up resistor. It functions as an interrupt indicating that the temperature of the on-chip or remote diode is above or below programmed overtemperature or undertemperature thresholds.
SDATA	7	SMBus/I ² C-bus bidirectional data line. This is an open-drain output which requires an external pull-up resistor.
SCLK	8	SMBus/I ² C-bus clock input which requires an external pull-up resistor.

7. Functional description

Refer to [Figure 1 “Block diagram”](#).

7.1 Serial bus interface

The SA56004X should be connected to a compatible two-wire serial interface System Management Bus (SMBus) as a slave device using the two device terminals SCLK and SDATA. The $\overline{\text{ALERT}}$ pin can optionally be used with the SMBus protocol to implement the ARA response. The controller will provide a clock signal to the device SCLK pin and write/read data to/from the device through the device SDATA pin. External pull-up resistors, about 10 k Ω each, are needed for these device pins due to open-drain circuitry.

Data of 8-bit digital byte or word are used for communication between the controller and the device using SMBus 2.0 protocols which are described more in [Section 7.10 “SMBus interface”](#). The operation of the device to the bus is described with details in the following sections.

7.2 Slave address

The SA56004X has a 7-bit slave address register which is factory programmed in OTP memory. Eight unique devices are available with different slave addresses as defined in [Table 2 “Ordering options”](#). Up to eight devices can reside on the same SMBus without conflict, provided that their addresses are unique.

7.3 Register overview

The SA56004X contains three types of SMBus addressable registers. These are read-only (R), write-only (W), and read-write (R/W). Attempting to write to any R-only register or read data from any W-only register will produce an invalid result. Some of the R/W registers have separate addresses for reading and writing operations.

The registers of the SA56004X serve four purposes:

- Control and configuration of the SA56004X
- Status reporting
- Temperature measurement storage
- ID and manufacturer test registers

[Table 4](#) describes the names, addresses, Power-On Reset (POR), and functions of each register. The data of the temperature-related registers is in 2's complement format in which the MSB is the sign bit. The 8-bit data of other registers is in 8-bit straight format.

Table 4. Register assignments

Register name	Command byte		POR state	Function	Bits	Access
	Read address	Write address				
LTHB	00h	n/a	0000 0000	local temperature high byte	8	R
RTHB	01h	n/a	0000 0000	remote temperature high byte	8	R
SR	02h	n/a	0000 0000	status register	8	R
CON	03h	09h	0000 0000	configuration register	8	R/W
CR	04h	0Ah	1000	conversion rate	4	R/W
LHS	05h	0Bh	0100 0110	local high setpoint	8	R/W
LLS	06h	0Ch	0000 0000	local low setpoint	8	R/W
RHSHB	07h	0Dh	0100 0110	remote high setpoint high byte	8	R/W
RLSHB	08h	0Eh	0000 0000	remote low setpoint high byte	8	R/W
One Shot	n/a	0Fh	-	writing register initiates a one shot conversion	0	W
RTLB	10h	n/a	0000 00	remote temperature low byte	6 (MSBs)	R
RTOHB	11h	11h	0000 0000	remote temperature offset high byte	8	R/W
RTOLB	12h	12h	000	remote temperature offset low byte	3 (MSBs)	R/W
RHSLB	13h	13h	000	remote high setpoint low byte	3 (MSBs)	R/W
RLSLB	14h	14h	000	remote low setpoint low byte	3 (MSBs)	R/W
RCS	19h	19h	0101 0101	remote T_CRIT setpoint	8	R/W
LCS	20h	20h	0101 0101	local T_CRIT setpoint	8	R/W
TH	21h	21h	0 1010	T_CRIT hysteresis	5	R/W
ATLB	22h	n/a	0000 0000	local temperature low byte	3 (MSBs)	R
AM	BFh	BFh	0	Alert mode	1	R/W
RMID	FEh	n/a	1010 0001	read manufacturer's ID	8	R
RDR	FFh	n/a	0000 0000	read stepping or die revision	8	R

7.4 Power-on reset

When power is applied to the SA56004X, the device will enter into its Power-On Reset (POR) state and its registers are reset to their default values. The configuration, status, and temperature-reading registers remain in these states until after the first conversion. As shown in [Table 4](#) this results in:

1. Command register set to 00h.
2. Local Temperature register (LTHB and LTLB) set to 0 °C.
3. Remote Diode Temperature register (RTHB and RTLB) set to 0 °C until the end of the first conversion.
4. Status register (SR) set to 00h.
5. Configuration register (CON) set to 00h; interrupt latches are cleared, the ALERT and T_CRIT output drivers are off and the $\overline{\text{ALERT}}$ and $\overline{\text{T_CRIT}}$ pins are pulled HIGH by the external pull-up resistors.
6. Local T_CRIT temperature setpoints (LCS) and Remote T_CRIT temperature setpoints (RCS) at 85 °C.
7. Local HIGH setpoint (LHS) and remote HIGH temperature setpoint (RHSHB) at 70 °C.

8. Local LOW setpoint (LLS) and Remote LOW temperature setpoints (RLSHB) at 0 °C.
9. Conversion Rate register (CR) is set to 8h; the default value of about 16 conversions/s.

7.5 Starting conversion

Upon POR, the RUN/STOP bit 6 of the configuration register is zero (default condition), then, the device will enter into its free-running operation mode in which the device A/D converter is enabled and the measurement function is activated. In this mode, the device cycles the measurements of the local and remote temperature automatically and periodically. The conversion rate is defined by the programmable conversion rate stored in the conversion rate register. It also performs comparison between readings and limits of the temperature in order to set the flags and interruption accordingly at the end of every conversion. Measured values are stored in the temp registers, results of the limit comparisons are reflected by the status of the flag bits in the status register and the interruption is reflected by the logical level of the $\overline{\text{ALERT}}$ and $\overline{\text{T_CRIT}}$ output. If the power-on temperature limit is not suitable, the temp limit values could be written into the limit registers during the busy-conversion duration of about 38 ms of the first conversion after power-up. Otherwise, the status register must be read and the configuration bit 7 must be reset in order to recover the device from interruption caused by the undesired temp limits.

7.6 Low power software standby mode

The device can be placed in a software standby mode by setting the RUN/STOP bit 6 in the configuration register HIGH (logic 1). In standby, the free-running oscillator is stopped, the supply current is less than 10 μA if there is no SMBus activity, all data in the registers is retained. However, the SMBus is still active and reading and writing registers can still be performed. A one-shot command will initiate a single conversion which has the same effect as any conversion that occurs when the device is in its free-running mode. To restore the device to free running mode, set the RUN/STOP bit 6 LOW (logic 0).

7.7 Temperature data format

The temperature data can only be read from the Local and Remote Temperature registers; the setpoint registers (e.g., T_CRIT, LOW, HIGH) are read/write.

Both local and remote temperature reading data is represented by an 11-bit, 2's complement word with the Least Significant Bit (LSB) = 0.125 °C. The temperature setpoint data for the remote channel is also represented by an 11-bit, 2's complement word with the LSB = 0.125 °C. The temperature setpoint data for both the local channel and the T_CRIT setpoints are represented by 8-bit, 2's complement words with the LSB = 1.0 °C. For 11-bit temp data, the data format is a left justified, 16-bit word available in two 8-bit registers (high byte and low byte). For 8-bit temp data, the data is available in a single 8-bit register (high byte only).

Table 5. Temperature data format

Temperature	Digital output	
	Binary	Hex
+125 °C	0111 1101 0000 0000	7D00h
+25 °C	0001 1001 0000 0000	1900h
+1 °C	0000 0001 0000 0000	0100h
+0.125 °C	0000 0000 0010 0000	0020h
0 °C	0000 0000 0000 0000	0000h
-0.125 °C	1111 1111 1110 0000	FFE0h
-1 °C	1111 1111 0000 0000	FF00h
-25 °C	1110 0111 0000 0000	E700h
-55 °C	1100 1001 0000 0000	C900h

7.8 SA56004X SMBus registers

7.8.1 Command register

The command register selects which register will be read or written to. Data for this register should be transmitted during the Command Byte of the SMBus write communication.

7.8.2 Local and remote temperature registers (LTHB, LTLB, RTHB, RTLB)

Table 6. LTHB, LTLB, RTHB, RTLB - Local and remote temperature registers

Byte	High byte (read only; address 00h, 01h)								Low byte (read only; address 10h)							
Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Value	sign	64	32	16	8	4	2	1	0.5	0.25	0.125	0	0	0	0	0

7.8.3 Configuration register (CON)

The configuration register is an 8-bit register with read address 03h and write address 09h. [Table 7](#) shows how the bits in this register are used.

Table 7. CON - Configuration register (read address 03h; write address 09h) bit assignments

Bit	Description	POR state
7	$\overline{\text{ALERT}}$ mask. The ALERT interrupt is enabled when this bit is LOW. The ALERT interrupt is disabled (masked) when this bit is HIGH.	0
6	$\overline{\text{RUN/STOP}}$. Standby or run mode control. Running mode is enabled when this bit is LOW. The SA56004X is in standby mode when this bit is HIGH.	0
5	Not defined; defaults to logic 0.	0
4	Remote $\overline{\text{T_CRIT}}$ mask. The $\overline{\text{T_CRIT}}$ output will be activated by a remote temperature that exceeds the remote T_CRIT setpoint when this bit is LOW. The $\overline{\text{T_CRIT}}$ output will not be activated under this condition when this bit is HIGH.	0
3	Not defined; defaults to logic 0.	0

Table 7. CON - Configuration register (read address 03h; write address 09h) bit assignments ...continued

Bit	Description	POR state
2	Local $\overline{T_CRIT}$ mask. The $\overline{T_CRIT}$ output will be activated by a local temperature that exceeds the local T_CRIT setpoint when this bit is LOW. The $\overline{T_CRIT}$ output will not be activated under this condition when this bit is HIGH.	0
1	Not defined; defaults to logic 0.	0
0	Fault queue. A single remote temperature measurement outside the HIGH, LOW or T_CRIT setpoints will trigger an outside limit condition resulting in setting the status bits and associated output pins when this bit is LOW. Three consecutive measurements outside of one of these setpoints are required to trigger an outside of limit condition when this bit is HIGH.	0

7.8.4 Status register (SR)

The contents of the status register reflect condition status resulting from all activities: comparison between temperature measurements and temperature limits, the status of A/D conversion, and the hardware condition of external diode to the device. Bit assignments are listed in [Table 8](#). This register is read-only and its address is 02h. Upon POR, all bits are set to zero.

Remark: Any one of the fault conditions, with the exceptions of Diode OPEN and A/D BUSY, introduces an Alert interrupt (see [Section 7.9.1.2](#)). Also, whenever a one-shot command is executed, the status byte should be read after the conversion is completed, which is about 38 ms (1 conversion time period) after the one-shot command is sent.

Table 8. SR - Status register (read-only address 02h) bit assignments

Bit	Name	Description
7	BUSY	When logic 1, A/D is busy converting. POR state = n/a.
6	LHIGH	When logic 1, indicates local HIGH temperature alarm. POR state = 0.
5	LLOW	When logic 1, indicates a local LOW temperature alarm. POR state = 0.
4	RHIGH	When logic 1, indicates a remote diode HIGH temperature alarm. POR state = 0.
3	RLOW	When logic 1, indicates a remote diode LOW temperature alarm. POR state = 0.
2	OPEN	When logic 1, indicates a remote diode disconnect. POR state = 0.
1	RCRIT	When logic 1, indicates a remote diode critical temperature alarm. POR state = 0.
0	LCRIT	When logic 1, indicates a local critical temperature alarm. POR state = 0.

7.8.5 Conversion rate register (CR)

The conversion rate register is used to store programmable conversion data, which defines the time interval between conversions in the standard free-running auto convert mode. Table 9 shows all applicable data values and rates for the SA56004X. Only the 4 LSBs of the register are used and the other bits are reserved for future use. The register is R/W using the read address 04h and write address 0Ah. The POR default conversion data is 08h.

Table 9. Conversion rate control byte (CR)

Data value	Conversion rate (Hz)
00h	0.06
01h	0.12
02h	0.25
03h	0.50
04h	1.0
05h	2
06h	4
07h	8
08h	16
09h	32
0Ah to FFh	n/a

7.8.6 Temperature limit registers

Table 10. LHS, RSHSB, RHSLB - Local and remote HIGH setpoint registers

Byte	High byte (read only address 05h, 07h; write address 0Bh, 0Dh) ^[1]								Low byte (read/write address 13h) ^[2]							
Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Value	sign	64	32	16	8	4	2	1	0.5	0.25	0.125	0	0	0	0	0

[1] POR default LHS = RSHSV = 46h (70 °C).

[2] POR default RHSLB = 00h.

Table 11. LLS, RLSHB, RLSLB - Local and remote LOW setpoint registers

Byte	High byte (read address 06h, 08h; write address 0Ch, 0Eh) ^[1]								Low byte (read/write address 14h) ^[2]							
Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Value	sign	64	32	16	8	4	2	1	0.5	0.25	0.125	0	0	0	0	0

[1] POR default LLS = RLSHV = 00h.

[2] POR default RLSLB = 00h (0 °C).

Table 12. LCS, RCS - Local and remote T_CRIT registers

Byte	Single high byte (read/write address 20h, 19h) ^[1]							
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	sign	64	32	16	8	4	2	1

[1] POR default LCS = RCS = 55h (85 °C).

Table 13. TH - T_CRIT hysteresis register

Byte	Single high byte (read/write address 21h) ^[1]							
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	-	-	-	16	8	4	2	1

[1] POR default TH = 0Ah (10 °C).

7.8.7 Programmable offset register (remote only)

Table 14. RTOHB, RTOLB - Remote temperature offset registers

Byte	High byte (read/write address 11h) ^[1]								Low byte (read/write address 12h) ^[2]							
Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Value	sign	64	32	16	8	4	2	1	0.5	0.25	0.125	0	0	0	0	0

[1] POR default RTOHB = RTOLB = 00h.

[2] POR default RTOLB = 00h.

7.8.8 ALERT mode register (AM)

Table 15. AM - ALERT mode register

Read and write address BFh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	0	0	0	0	0	0	0	ALERT mode

D[7:1] is not defined and defaults to logic 0.

D0: The $\overline{\text{ALERT}}$ output is in interrupt mode when this bit is LOW. The $\overline{\text{ALERT}}$ output is in comparator mode when this bit is HIGH.

7.8.9 Other registers

The **Manufacturers ID** register has a default value A1h (1010 0001) and a read address FEh.

The **Die Revision Code** register has a default value 00h (0000 0000) and read address FFh. This register will increment by 1 every time there is a revision to the die.

7.8.10 One-shot register

The one-shot register is used to initiate a single conversion and comparison cycle when the device is in the standby mode; upon completion of the single conversion cycle, the device returns to the standby mode. It is not a data register; it is the write operation that causes the one-shot conversion. The data written to this register is not stored; an FFh value will always be read from this register. To initiate a one-shot operation, send a standard write command with the command byte of 0Fh (One-Shot Write Address).

7.9 Interruption logic and functional description

7.9.1 $\overline{\text{ALERT}}$ output

The $\overline{\text{ALERT}}$ output is used to signal Alert interruptions from the device to the SMBus or other system interrupt handler and it is active LOW. Because this is an open-drain output, a pull-up resistor (typically 10 k Ω) to V_{DD} is required. Several slave devices can share a common interrupt line on the same SMBus.

The $\overline{\text{ALERT}}$ function is very versatile and accommodates three separate operating modes:

- Temperature comparator
- System interrupt based on temperature
- SMBus Alert Response Address (ARA) response.

The ARA and interrupt modes are different only in how the user interacts with the SA56004X.

At the end of every temperature reading, digital comparators determine if the readings are above the HIGH or T_CRIT setpoint or below the LOW setpoint register values. If so, the corresponding bit in the Status register is set. If the $\overline{\text{ALERT}}$ mask bit 7 of the Configuration register is not HIGH, then any bit set in the Status register other than the BUSY (D7) and OPEN (D2) will cause the $\overline{\text{ALERT}}$ output pin to be active LOW. An alert will be triggered after any conversion cycle that finds the temperature is out of the limits defined by the setpoint registers. In order to trigger an ALERT in all alert modes, the $\overline{\text{ALERT}}$ mask bit 7 of the Configuration register must be cleared (not HIGH).

7.9.1.1 $\overline{\text{ALERT}}$ output in comparator mode

When operating the SA56004X in a system that utilizes an SMBus controller not having an interrupt, the $\overline{\text{ALERT}}$ output may be operated as a temperature comparator. In this mode, when the condition that triggered the ALERT to be asserted is no longer present, the $\overline{\text{ALERT}}$ output is released as it goes HIGH. In order to use the $\overline{\text{ALERT}}$ output as a temperature comparator, bit D0 (the ALERT configure bit) in the ALERT Mode (AM) register must be set HIGH. This is not the POR default.

7.9.1.2 $\overline{\text{ALERT}}$ output in interrupt mode

In the interrupt mode, the $\overline{\text{ALERT}}$ output is used to provide an interrupt signal that remains asserted until the interrupt service routine has elapsed. In the interrupt operating mode, a read of the Status register will set the $\overline{\text{ALERT}}$ mask bit 7 of the Configuration register if any of the temperature alarm bits of the Status register is set, with exception of BUSY (D7) and OPEN (D2). This protocol prevents further $\overline{\text{ALERT}}$ output triggering until the master device has reset the $\overline{\text{ALERT}}$ mask bit at the end of the interrupt service routine. The Status register bits are cleared only upon a read of the Status register by the serial bus master (see [Figure 5](#)). In order for the $\overline{\text{ALERT}}$ output to be used as an interrupt, the ALERT Configure bit D0 of the ALERT Mode (AM) register must be set LOW (POR default).

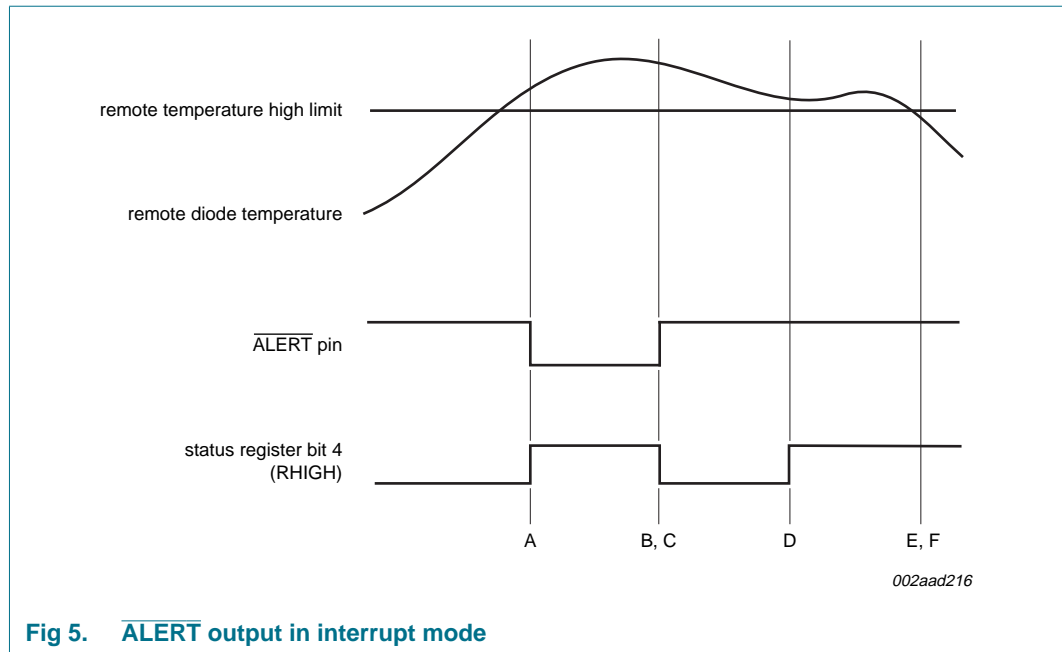


Fig 5. $\overline{\text{ALERT}}$ output in interrupt mode

The following events summarize the ALERT output interrupt mode of operation:

- Event A:** Master senses $\overline{\text{ALERT}}$ output being active-LOW.
- Event B:** Master reads the SA56004X Status register to determine what cause the $\overline{\text{ALERT}}$ interrupt.
- Event C:** SA56004X clears the Status register, resets the $\overline{\text{ALERT}}$ output HIGH, and sets the $\overline{\text{ALERT}}$ mask bit 7 in the Configuration register.
- Event D:** A new conversion result indicates the temperature is still above the high limit, however the $\overline{\text{ALERT}}$ pin is not activated due to the ALERT mask.
- Event E:** Master should correct the conditions that caused the $\overline{\text{ALERT}}$ output to be triggered. For instance, the fan is started, setpoint levels are adjusted.
- Event F:** Master resets the $\overline{\text{ALERT}}$ mask bit 7 in the Configuration register.

7.9.1.3 $\overline{\text{ALERT}}$ output in SMBus ALERT mode

When several slave devices share a common interrupt line, an SMBus alert line is implemented. The SA56004X is designed to accommodate the Alert interrupt detection capability of the SMBus 2.0 Alert Response Address (ARA) protocol, defined in *SMBus specification 2.0*. This procedure is designed to assist the master in resolving which slave device generated the interrupt and in servicing the interrupt while minimizing the time to restore the system to its proper operation. Basically, the SMBus provides Alert response interrupt pointers in order to identify slave devices which have caused the Alert interrupt. When the ARA command is received by all devices on the SMBus, the devices pulling the SMBus alert line LOW send their device addresses to the master; await an acknowledgement and then release the alert line. This requirement to disengage the SMBus alert line prevents locking up the alert line. The SA56004X complies with this ARA disengagement protocol by setting the $\overline{\text{ALERT}}$ mask bit 7 in the Configuration register at address 09h after successfully sending out its address in response to an ARA command and releasing the $\overline{\text{ALERT}}$ output. Once the mask bit is activated, the $\overline{\text{ALERT}}$ output will be disabled until enabled by software. In order to enable the $\overline{\text{ALERT}}$ the master must read the

Status register, at address 02h, during the interrupt service routine and then reset the $\overline{\text{ALERT}}$ mask bit 7 in the Configuration register to logic 0 at the end of the interrupt service routine (see [Figure 6](#)).

In order for the SA56004X to respond to the ARA command, the bit D0 in the ALERT mode register must be set LOW.

$\overline{\text{ALERT}}$ mask bit 7 and the ALERT mode bit D0 are both LOW for the POR default.

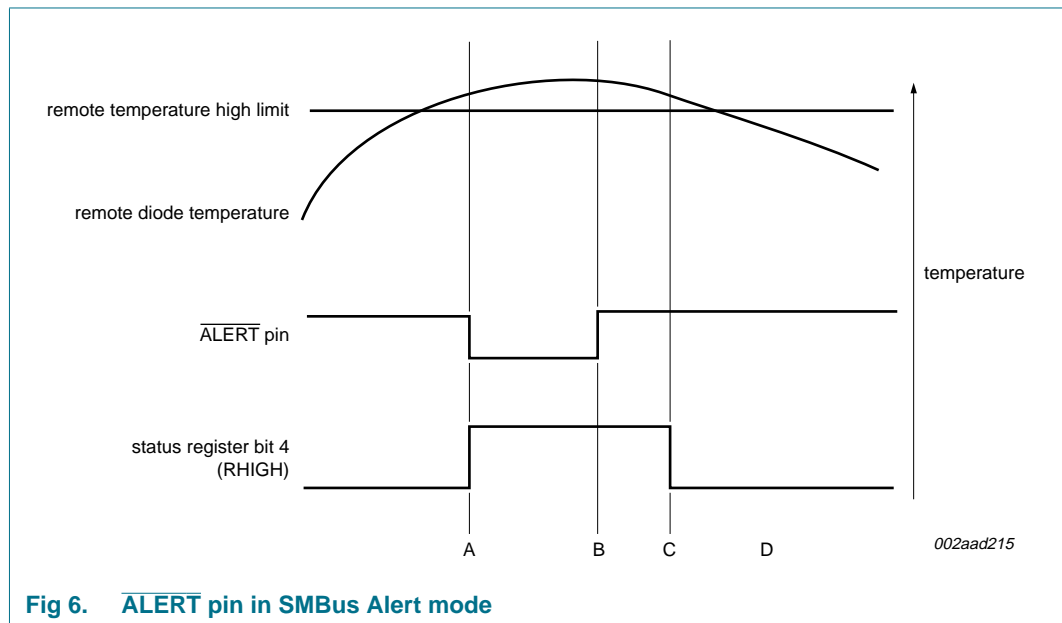


Fig 6. $\overline{\text{ALERT}}$ pin in SMBus Alert mode

The following events summarize the $\overline{\text{ALERT}}$ output interrupt operation in the SMBus Alert mode:

Event A: Master senses the ALERT line being LOW.

Event A to B: Master sends a read command using the common 7-bit Alert Response Address (ARA) of 0001100.

Event A to B: Alerting device(s) return ACK signal and their addresses using the I²C-bus Arbitration (the device with the lowest address value sends its address first. The master can repeat the alert reading process and work up through all the interrupts).

Event B: Upon the successful completion of returning address, the SA56004X resets its $\overline{\text{ALERT}}$ output (to OFF) and sets the $\overline{\text{ALERT}}$ mask bit 7 in its configuration register.

Event C: Master should read the device status register to identify and correct the conditions that caused the Alert interruption. The status register is reset.

Event D: Master resets the $\overline{\text{ALERT}}$ mask bit 7 in the configuration register to enable the device $\overline{\text{ALERT}}$ output interruption.

Remark: The bit assignment of the returned data from the ARA reading is listed in [Table 16](#). If none of the devices on the bus is alerted then the returned data from ARA reading will be FFh (1111 1111).

Table 16. ALERT response bit assignment

ALERT response bit	Device address bit	Function
7 (MSB)	ADD6	address bit 6 (MSB) of alerted device
6	ADD5	address bit 5 of alerted device
5	ADD4	address bit 4 of alerted device
4	ADD3	address bit 3 of alerted device
3	ADD2	address bit 2 of alerted device
2	ADD1	address bit 1 of alerted device
1	ADD0	address bit 0 of alerted device
0	1	always logic 1

7.9.2 T_CRIT output

The T_CRIT output is LOW when any temperature reading is greater than the preset limit in the corresponding critical temperature setpoint register. When one of the T_CRIT setpoint temperatures is exceeded, the appropriate status register bit, 1 (RCRIT) or 0 (LCRIT), is set.

After every local and remote temperature conversion the status register flags and the T_CRIT output are updated. Figure 7 is a timing diagram showing the relationship of T_CRIT output, Status bit 1 (RCRIT) and the remote critical temperature setpoint (RCS), and critical temperature hysteresis (TH) with remote temperature changes. Note that the T_CRIT output is de-activated only after the remote temperature is below the remote temperature setpoint, RCS minus the hysteresis, TH. In the interrupt mode only, the Status register flags are reset after the Status register is read.

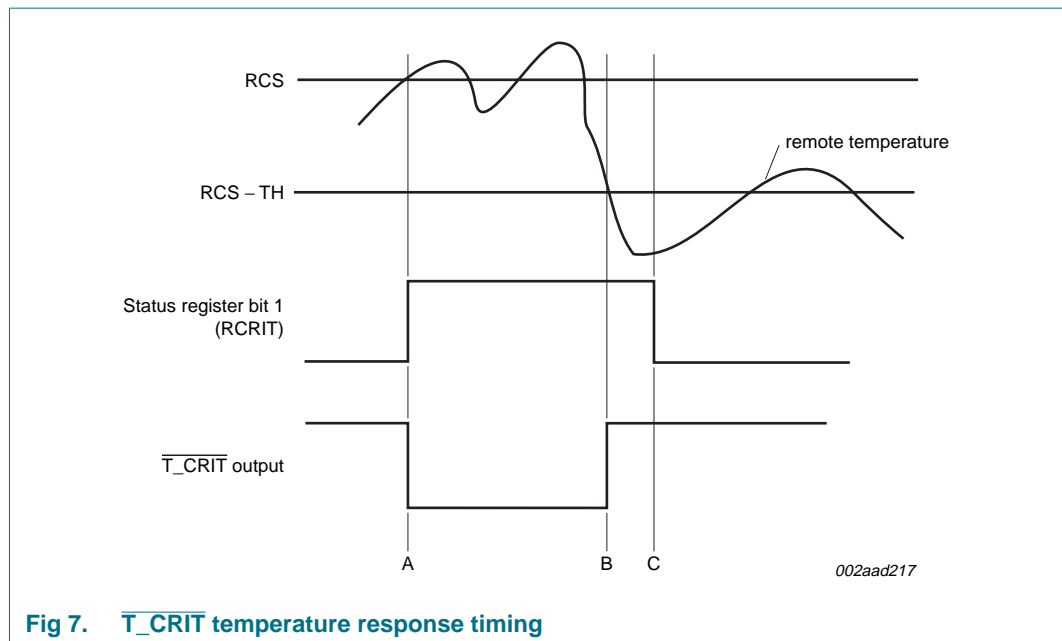


Fig 7. T_CRIT temperature response timing

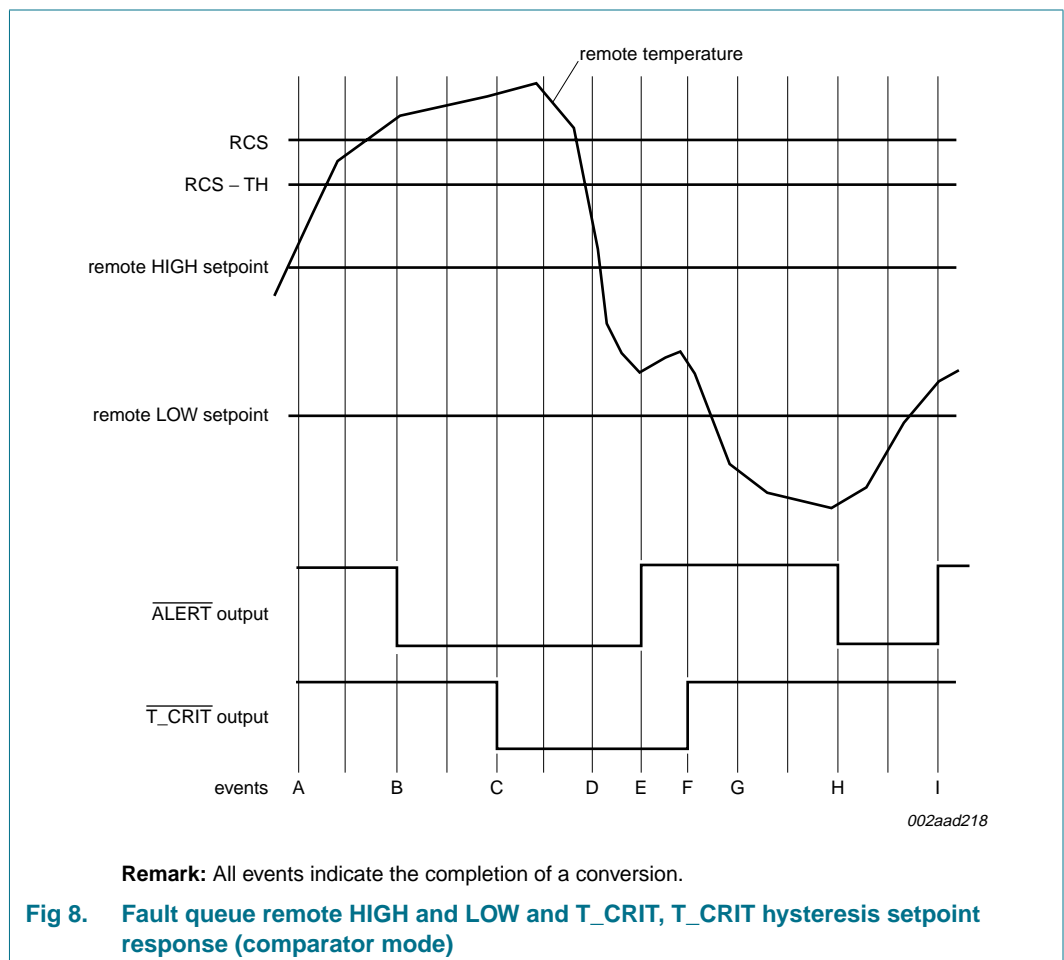
Event A: T_CRIT goes LOW and Status bit 1 (RCRIT) is set HIGH when Remote Temperature exceeds RCS, Remote T_CRIT Setpoint.

Event B: Remote Temperature goes below RCS - TH. T_CRIT is de-activated, but Status register remains unchanged.

Event C: The Status register bit 1 (RCRIT) is reset by a read of the Status register (in the interrupt mode).

7.9.3 Fault Queue

To suppress erroneous $\overline{\text{ALERT}}$ or $\overline{\text{T_CRIT}}$ triggering, the SA56004X implements a Fault Queue for both local and remote channel. The Fault Queue insures a temperature measurement is genuinely beyond a HIGH, LOW or T_CRIT setpoint by not triggering until three consecutive out-of-limit measurements have been made. The fault queue defaults OFF upon POR and may be activated by setting bit 0 in the Configuration register (address 09h) to logic 1.



Event A: The remote temperature has exceeded the Remote HIGH setpoint.

Event B: Three consecutive over limit measurements have been made exceeding the Remote HIGH setpoint; the $\overline{\text{ALERT}}$ output is activated (goes LOW). By now, the remote temp has exceeded the Remote T_CRIT setpoint (RCS).

Event C: Three consecutive over limit measurements have been made exceeding RCS; the $\overline{\text{T_CRIT}}$ output is activated (goes LOW).

Event D: The remote temperature falls below the RCS - TH setpoint.

Event E: The $\overline{\text{ALERT}}$ output is de-activated (goes HIGH) after a below_high_limit temperature measurement is completed.

Event F: Three consecutive measurements have been made with the remote temperature below the RCS – TH threshold; the $\overline{T_CRIT}$ output is de-activated (goes HIGH).

Event G: The remote temp falls below the Remote LOW setpoint.

Event H: Three consecutive measurements are made with the temp below the Remote LOW setpoint; \overline{ALERT} output is activated (goes LOW).

Event I: The \overline{ALERT} output is de-activated (goes HIGH) after a above_low_limit temperature measurement is completed.

7.9.4 Remote diode selection

To measure the remote temperature or the temperature of an externally attached diode, the device automatically forces two successive currents of about 160 μ A and 10 μ A at D+ pin. It measures the voltage (V_{BE}) between D+ and D–, detects the difference between the two V_{BE} voltages or the ΔV_{BE} and then converts the ΔV_{BE} into a temperature data using the basic PTAT voltage formula as shown in [Equation 1](#). The device typically takes about 38 ms to perform a measurement during each conversion period or cycle, which is selectable by programming the conversion rate register.

$$\Delta V_{BE} = n \times \frac{kT}{q} \times \ln\left(\frac{I_2}{I_1}\right) \tag{1}$$

Where:

n = diode ideality factor

k = Boltzmann’s constant

T = absolute temperature (°K) = 273 °C + T (°C)

q = electron charge

ln = natural logarithm

I₂, I₁ = two source currents

Because the device does not directly convert the sensed V_{BE} as in the old method of temperature measurement systems, the V_{BE} calibration is not required. Furthermore, the device remote temperature error is adjusted at the manufacturer to meet the specifications with the use of the reference diode-connected transistors such as the 2N3904/2N3906.

The diode type to be used in customer applications must have the characteristics as close to the 2N3904/2N3906 as possible in order to obtain optimal results. Finally, to prevent the effects of system noise on the measured V_{BE} signals, an external capacitor of about 2200 pF connected between the D+ and D– pins as well as the grounded-shield cable for the diode connection wires are recommended.

7.9.5 Diode fault detection

The SA56004X is designed with circuitry to detect the fault conditions of the remote diode. When the D+ pin is shorted to V_{DD} or floating, the Remote Temperature High Byte (RTHB) register is loaded with +127 °C, the Remote Temperature Low Byte (RTLB) register is loaded with 0 °C, and the OPEN bit (bit 2 of the Status register) is set. Under the above conditions of D+ shorted to V_{DD} or floating, if the Remote $\overline{T_CRIT}$ setpoint is set less than +127 °C, and T_CRIT Mask are disabled, then, the $\overline{T_CRIT}$ output pins will be pulled

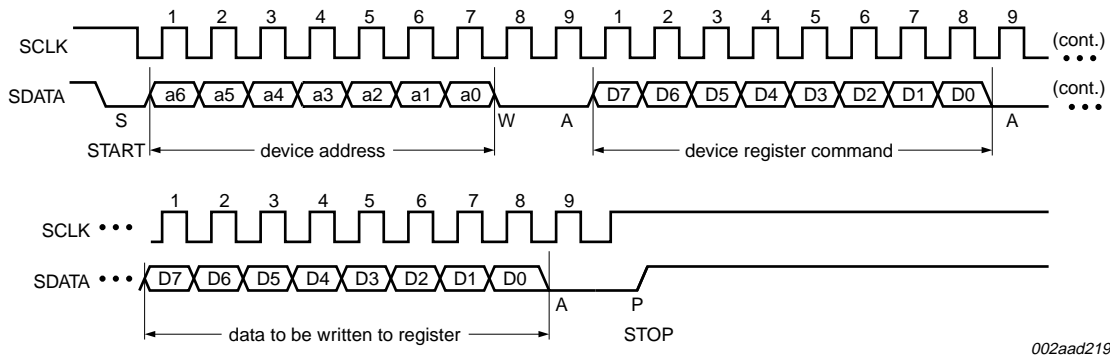
LOW. Furthermore, if the Remote HIGH Setpoint High Byte (RHS $\overline{\text{HB}}$) register is set to a value less than +127 °C and the Alert Mask is disabled, then the $\overline{\text{ALERT}}$ output will be pulled LOW. Note that the OPEN bit itself will not trigger an ALERT.

When the D+ pin is shorted to ground or to D-, the Remote Temperature High Byte (RTHB) register is loaded with -128 °C (1000 0000) and the OPEN (bit 2 in the Status register) will not be set. Since operating the SA56004X is beyond its normal limits, this temperature reading represents this shorted fault condition. If the value in the Remote Low Setpoint High Byte (RLSHB) register is more than -128 °C and the Alert Mask is disabled, the $\overline{\text{ALERT}}$ output will be pulled LOW.

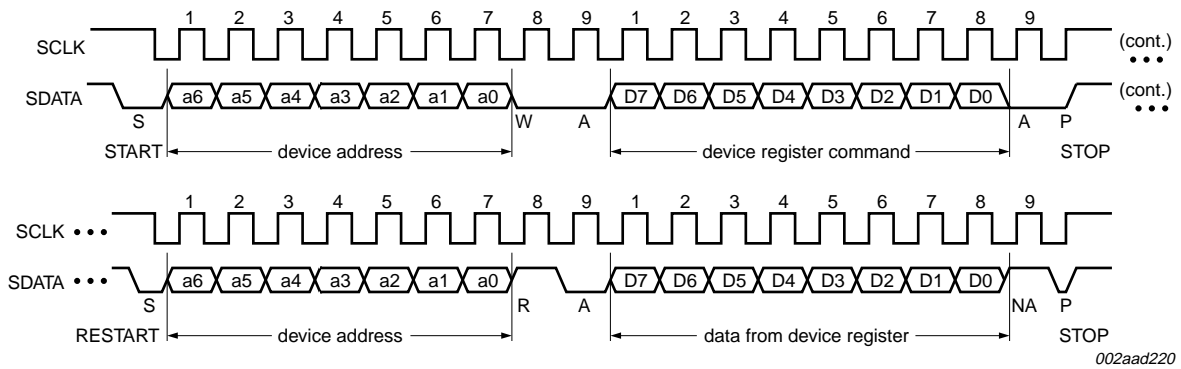
7.10 SMBus interface

The device can communicate over a standard two-wire serial interface System Management Bus (SMBus) or compatible I²C-bus using SCLK and SDATA. The device employs four standard SMBus protocols: Write Byte, Read Byte, Receive Byte, and Send Byte. Data formats of four protocols are shown in [Figure 9](#). The following key points of protocol are important:

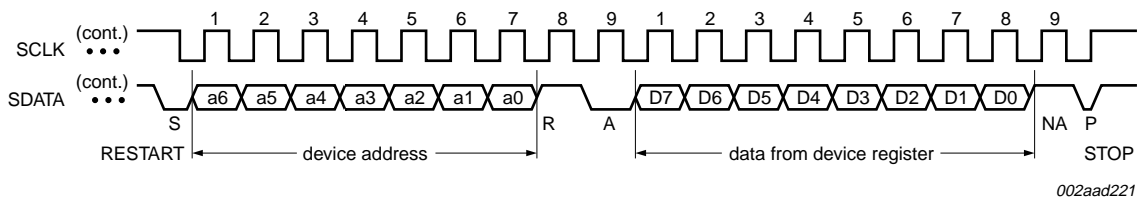
- The SMBus master initiates data transfer by establishing a START condition (S) and terminates data transfer by generating a STOP condition (P).
- Data is sent over the serial bus in sequences of 9 clock pulses according to each 8-bit data byte followed by 1-bit status of device acknowledgement (A).
- The 7-bit slave address is equivalent to factory-programmed address of the device.
- The command byte is equivalent to the address of the selected device register.
- The Receive Byte format is used for quicker transfer data from a device reading register that was previously selected.



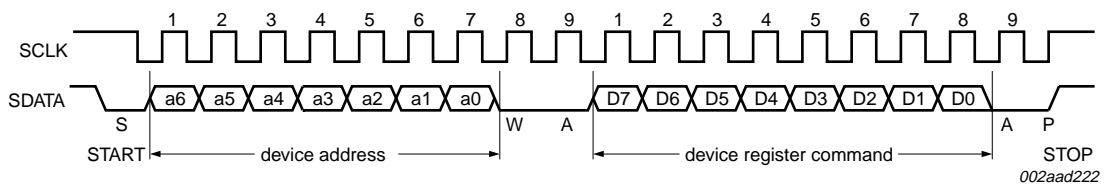
a. Write Byte format (to write a data byte to the device register)



b. Read Byte format (to read a data byte from the device register)



c. Receive Byte format (to read a data byte from already pointed register)



d. Send Byte format

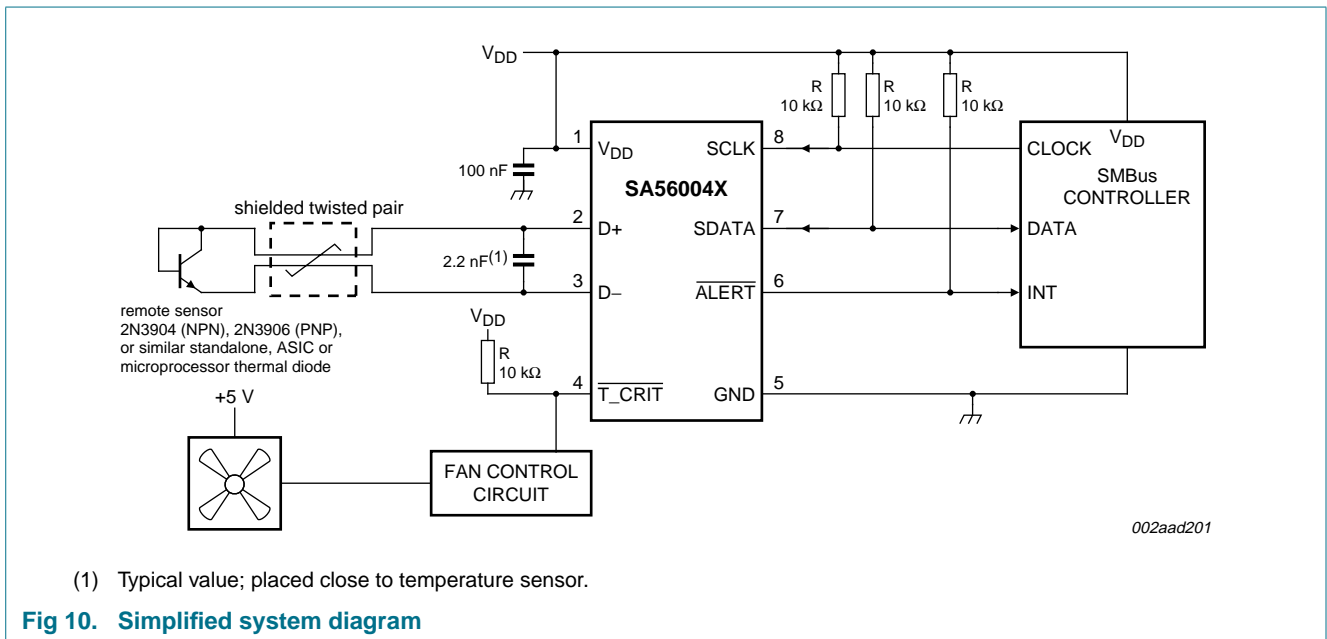
Fig 9. SMBus interface protocols

7.10.1 Serial interface reset

If the SMBus master attempts to reset the SA56004X while the SA56004X is controlling the data line and transmitting on the data line, the SA56004X must be returned to a known state in the communication protocol. This may be accomplished in two ways:

1. When the SDATA is LOW, the SA56004X SMBus state machine resets to the SMBus idle state if SCLK is held LOW for more than 35 ms (maximum TIMEOUT period). According to *SMBus specification 2.0*, all devices are required to time-out when the SCLK line is held LOW for 25 ms to 35 ms. Therefore, to insure a time-out of all devices on the bus, the SCLK line must be held LOW for at least 35 ms.
2. When the SDATA is HIGH, the master initiates an SMBus START. The SA56004X will respond properly to a SMBus START condition only during the data retrieving cycle. After the START, the SA56004X will expect an SMBus Address byte.

8. Simplified system diagram



9. Limiting values

Table 17. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

All voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.3	+6	V
	voltage at SDATA, SCLK, ALERT, T_CRIT		-0.3	+6	V
V _{D+}	voltage at positive diode input		-0.3	V _{DD} + 0.3	V
V _{D-}	voltage at negative diode input		-0.3	+0.8	V
I _{sink}	sink current	SDATA, SCLK, ALERT, T_CRIT	-1	+50	mA
I _{D+}	D+ input current		-1	+1	mA
V _{esd}	electrostatic discharge voltage	Human Body Model	[1] -	2000	V
		Machine Model	[1] -	200	V
T _{j(max)}	maximum junction temperature		-	+150	°C
T _{stg}	storage temperature		-65	+165	°C

[1] The D+ and D- pins are 1000 V HBM and 100 V MM due to the higher sensitivity of the analog pins that introduces a limitation to the circuit protection structure.

10. Characteristics

Table 18. Electrical characteristics

$V_{DD} = 3.0\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ °C to }+125\text{ °C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{ERRL}	local temperature error	T _{amb} = +60 °C to +100 °C	-2	±1	+2	°C
		T _{amb} = -40 °C to +125 °C	-3	-	+3	°C
T _{ERRR}	remote temperature error	T _{amb} = +25 °C to +85 °C; T _{RD} = +60 °C to +100 °C	-1	-	+1	°C
		T _{amb} = -40 °C to +85 °C; T _{RD} = -40 °C to +125 °C	-3	-	+3	°C
T _{RESR}	remote temperature resolution		-	11	-	bit
			-	0.125	-	°C
T _{RESL}	local temperature resolution		-	11	-	bit
			-	0.125	-	°C
T _{conv}	conversion period		-	38	-	ms
V _{DD}	supply voltage		[1] 3.0	-	5.5	V
I _{DD}	quiescent current	during conversion, 16 Hz conversion rate	-	500	-	µA
	shut-down current	SMBus inactive	-	10	-	µA
I _{RD}	remote diode source current	high setting: D+ – D– = +0.65 V	-	160	-	µA
		low setting	-	10	-	µA
UVL	UnderVoltage Lockout (UVL) threshold voltage[2]	V _{DD} input disables A/D conversion	[3] 2.6	-	2.95	V
	Power-On Reset (POR) threshold voltage	V _{DD} input falling edge	[4] 1.8	-	2.4	V
	local and remote $\overline{\text{ALERT}}$ high default temperature settings	default values set at power-up	-	+70	-	°C
	local and remote $\overline{\text{ALERT}}$ low default temperature settings	default values set at power-up	-	0	-	°C
	local and remote $\overline{\text{T_CRIT}}$ default temperature settings	default values set at power-up	-	+85	-	°C
	$\overline{\text{T_CRIT}}$ hysteresis	default value set at power-up	-	+10	-	°C
	$\overline{\text{ALERT}}$ and $\overline{\text{T_CRIT}}$ output saturation voltage	I _O = 6.0 mA	-	-	0.4	V

[1] The SA56004X is optimized for 3.3 V V_{DD} operation.

[2] Definition of Under Voltage Lockout (UVL): The value of V_{DD} below which the internal A/D converter is disabled. This is designed to be a minimum of 200 mV above the power-on reset. During the time that it is disabled, the temperature that is in the 'read temperature registers' will remain at the value that it was before the A/D was disabled. This is done to eliminate the possibility of reading unexpected false temperatures due to the A/D converter not working correctly due to low voltage. In case of power-up (rising V_{DD}), the reading that is stored in the 'read temperature registers' will be the default value of 0 °C. V_{DD} will rise to the value of the UVL, at which point the A/D will function correctly and the normal temperature will be read.

[3] V_{DD} (rising edge) voltage below which the A/D converter is disabled.

[4] V_{DD} (falling edge) voltage below which the logic is reset.

Table 19. SMBus interface characteristics

$V_{DD} = 3.0\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$; unless otherwise specified.

These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	SCLK, SDATA; $V_{DD} = 2.7\text{ V to }5.5\text{ V}$	2.2	-	-	V
V_{IL}	LOW-level input voltage	SCLK, SDATA; $V_{DD} = 2.7\text{ V to }5.5\text{ V}$	-	-	0.8	V
I_{OL}	LOW-level output current	ALERT, $\overline{T_CRIT}$; $V_{OL} = 0.4\text{ V}$	1.0	-	-	mA
		SDATA; $V_{OL} = 0.6\text{ V}$	6.0	-	-	mA
I_{OH}	LOW-level output current		-	-	1.0	μA
I_{IL}	LOW-level input current		-1.0	-	-	μA
I_{IH}	HIGH-level input current		-	-	1.0	μA
C_i	input capacitance	SCLK, SDATA	-	5	-	pF
SMBus digital switching characteristics^[1]						
f_{SCLK}	SCLK operating frequency		-	-	400	kHz
t_{LOW}	SCLK LOW time	10 % to 10 %	600	5000	-	ns
t_{HIGH}	SCLK HIGH time	90 % to 90 %	600	5000	-	ns
t_{BUF}	SMBus free time ^[2]		600	-	-	ns
$t_{HD;STA}$	hold time of START condition ^[3]	10 % of SDATA to 90 % of SCLK	600	-	-	ns
$t_{HD;DAT}$	hold time of data ^[4]		0	300	-	ns
$t_{SU;DAT}$	set-up time of data in ^[5]		250	-	-	ns
$t_{SU;STA}$	set-up time of repeat START condition ^[6]	90 % to 90 %	250	-	-	ns
$t_{SU;STO}$	set-up time of STOP condition ^[7]	90 % of SCLK to 90 % of SDATA	250	-	-	ns
t_r	rise time	SCLK and SDATA	-	-	1	μs
t_f	fall time	SCLK and SDATA	-	-	300	ns
t_{of}	output fall time	$C_L = 400\text{ pF}$; $I_O = 3\text{ mA}$	-	-	250	ns
$t_{to(SMBus)}$	SMBus time-out time ^[8]		25	-	35	ms

[1] The switching characteristics of the SA56004X fully meet or exceed all parameters specified in *SMBus version 2.0*. The following parameters specify the timing between the SCLK and SDATA signals in the SA56004X. They adhere to, but are not necessarily specified as the SMBus specifications.

[2] Delay from SDATA STOP to SDATA START.

[3] Delay from SDATA START to first SCLK HIGH-to-LOW transition.

[4] Delay from SCLK HIGH-to-LOW transition to SDATA edges.

[5] Delay from SDATA edges to SCLK LOW-to-HIGH transition.

[6] Delay from SCLK LOW-to-HIGH transition to restart SDATA.

[7] Delay from SCLK HIGH-to-LOW transition to SDATA STOP condition.

[8] LOW period for reset of SMBus.

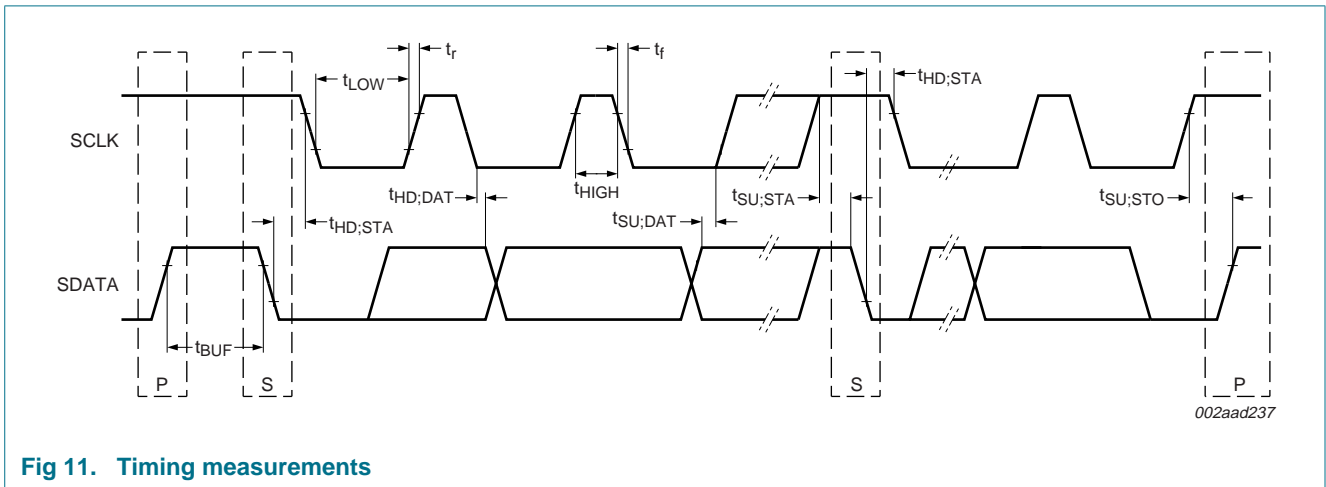


Fig 11. Timing measurements

11. Performance curves

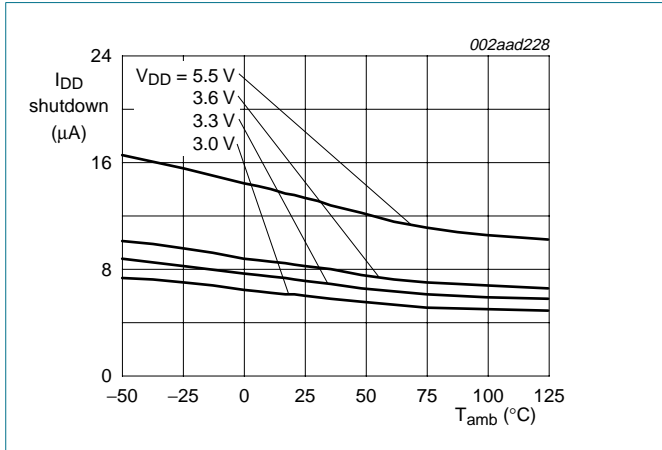


Fig 12. Typical I_{DD} shutdown versus temperature and V_{DD}

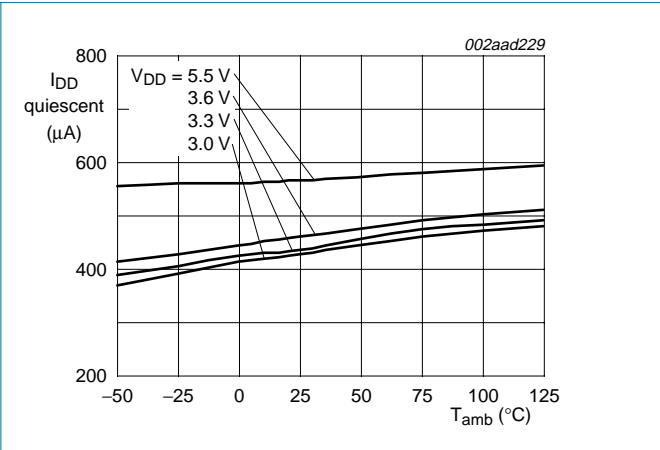


Fig 13. Typical I_{DD} quiescent current versus temperature and V_{DD} (conversion rate = 16 Hz)

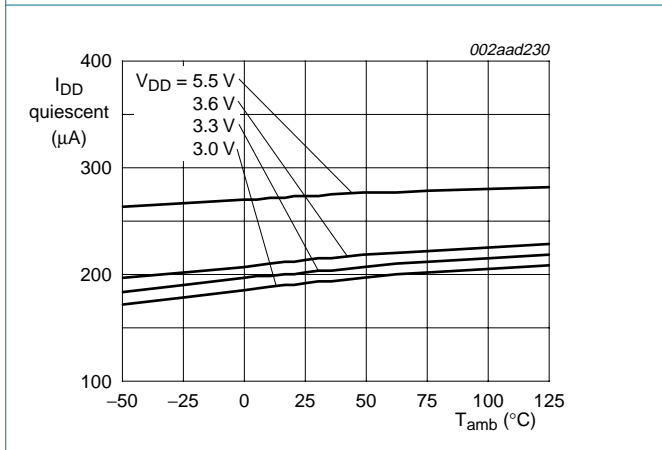
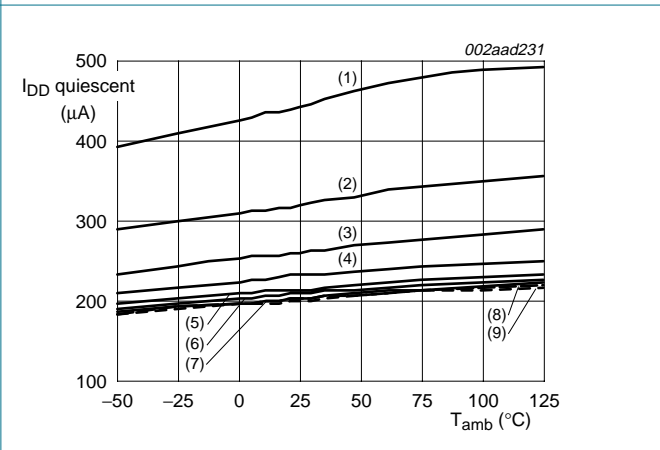


Fig 14. Typical I_{DD} quiescent current versus temperature and V_{DD} (conversion rate = 0.06 Hz)



Conversion rate:

- (1) 16 Hz
- (2) 8.0 Hz
- (3) 4.0 Hz
- (4) 2.0 Hz
- (5) 1.0 Hz
- (6) 0.5 Hz
- (7) 0.25 Hz
- (8) 0.12 Hz
- (9) 0.06 Hz

Fig 15. Typical I_{DD} quiescent current versus temperature and conversion rate ($V_{DD} = 3.3$ V)

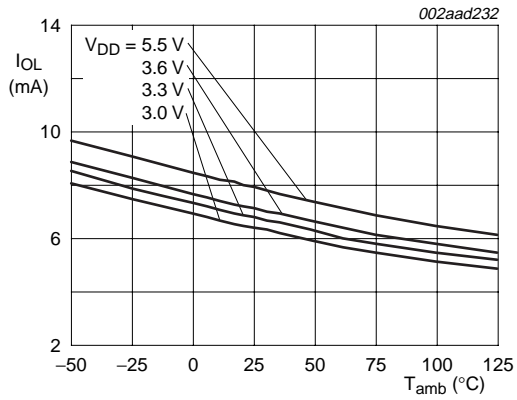


Fig 16. Typical T_CRIT I_{OL} versus temperature and V_{DD} ($V_{OL} = 0.4$ V)

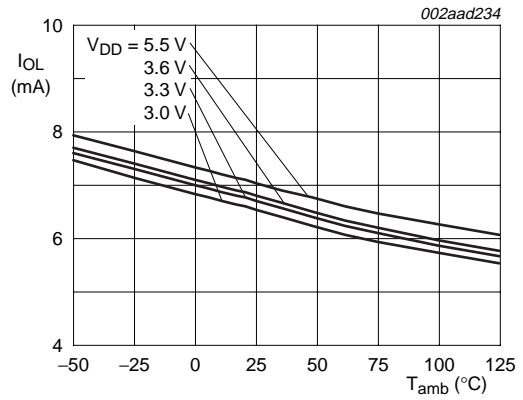


Fig 17. Typical \overline{ALERT} I_{OL} versus temperature and V_{DD} ($V_{OL} = 0.4$ V)

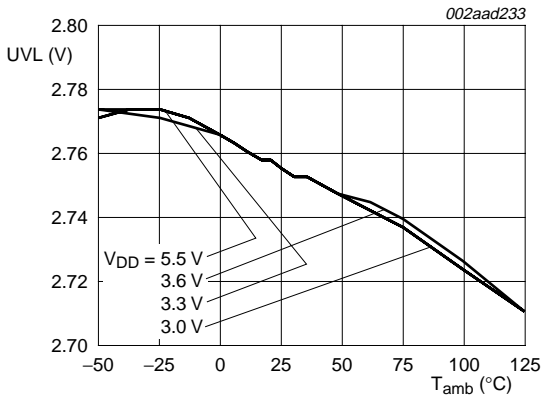


Fig 18. Typical UVL versus temperature and V_{DD}

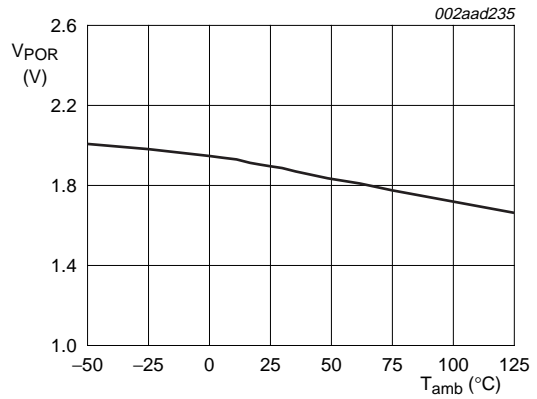


Fig 19. Typical V_{POR} versus temperature

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

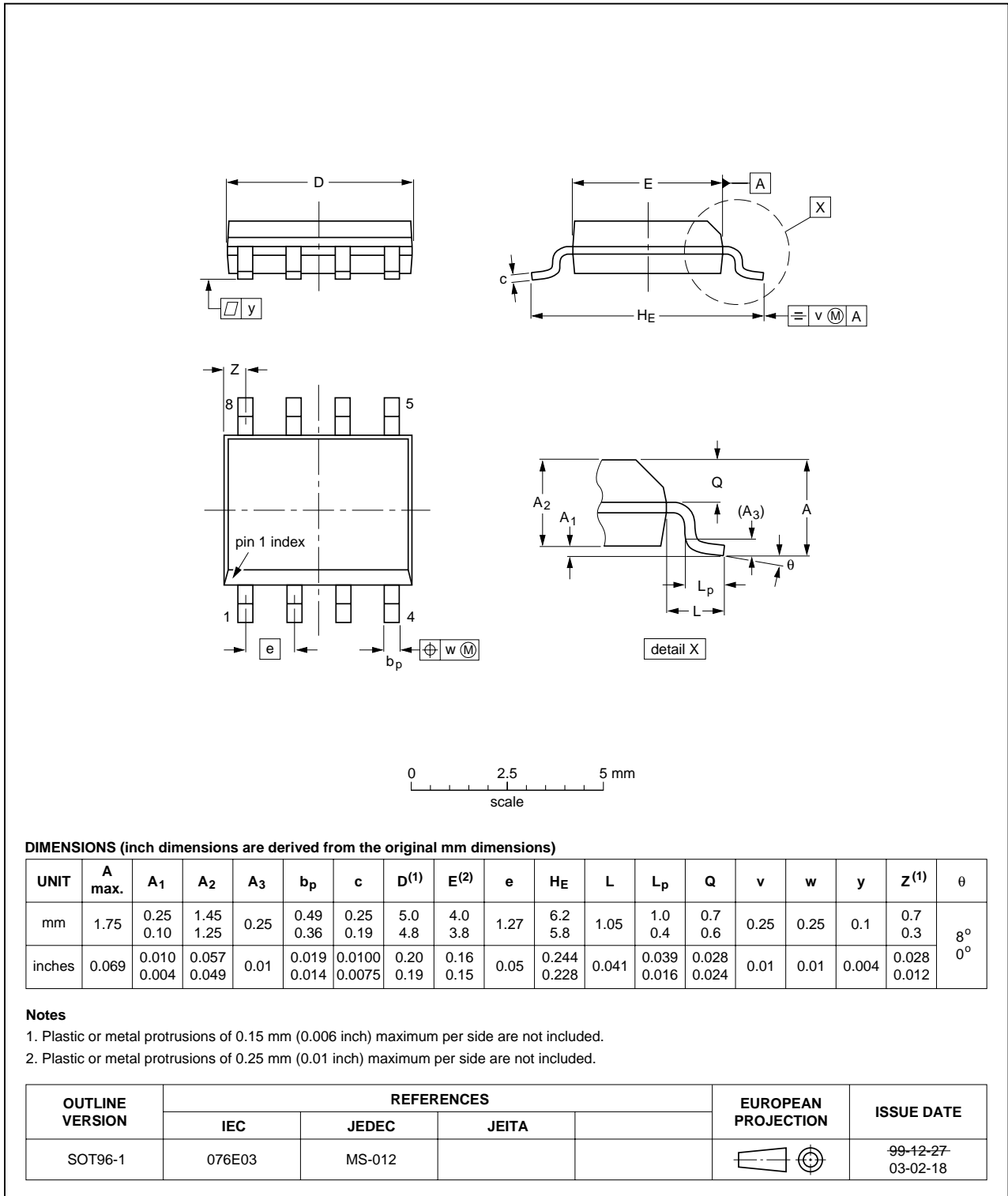


Fig 20. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1

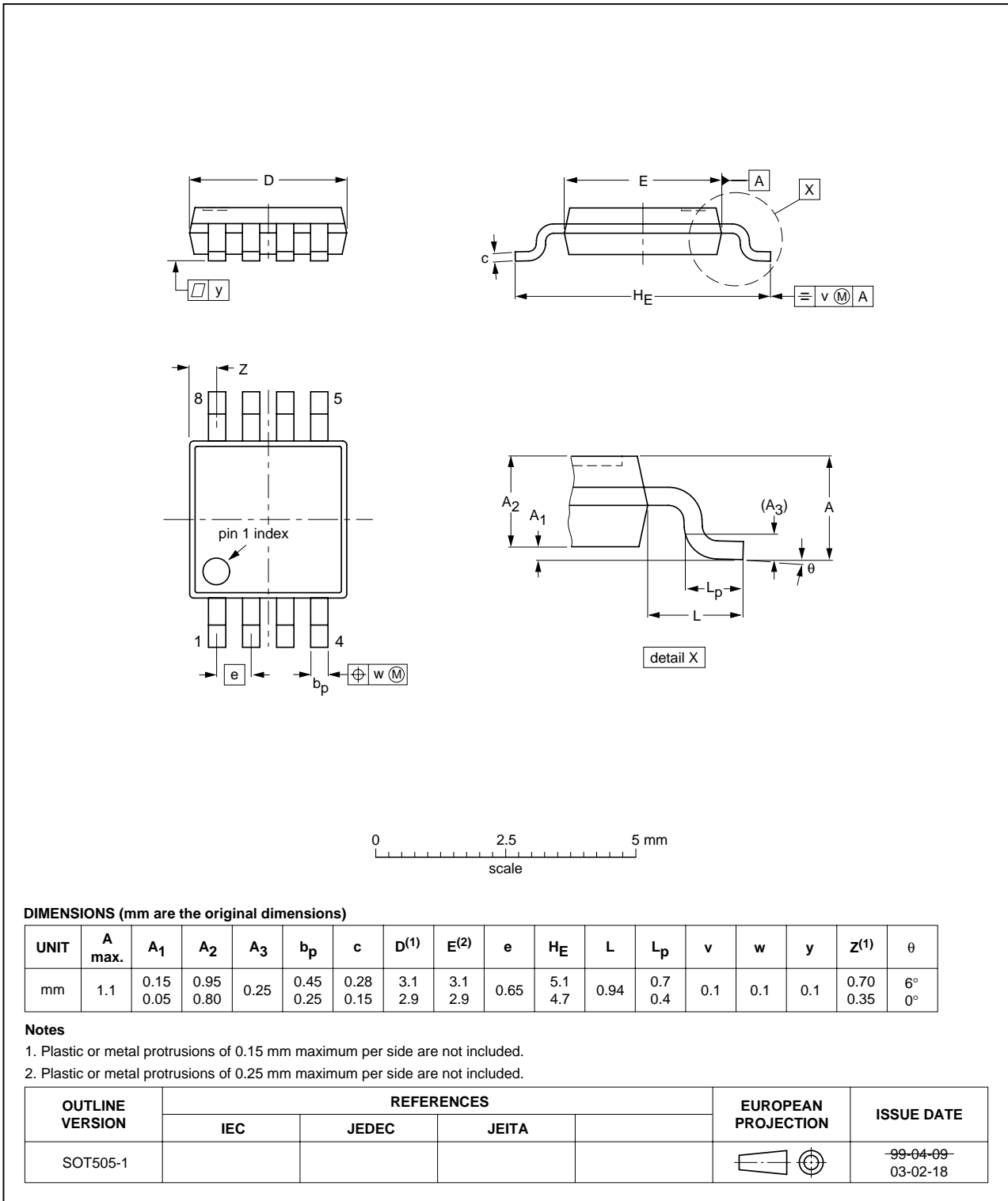
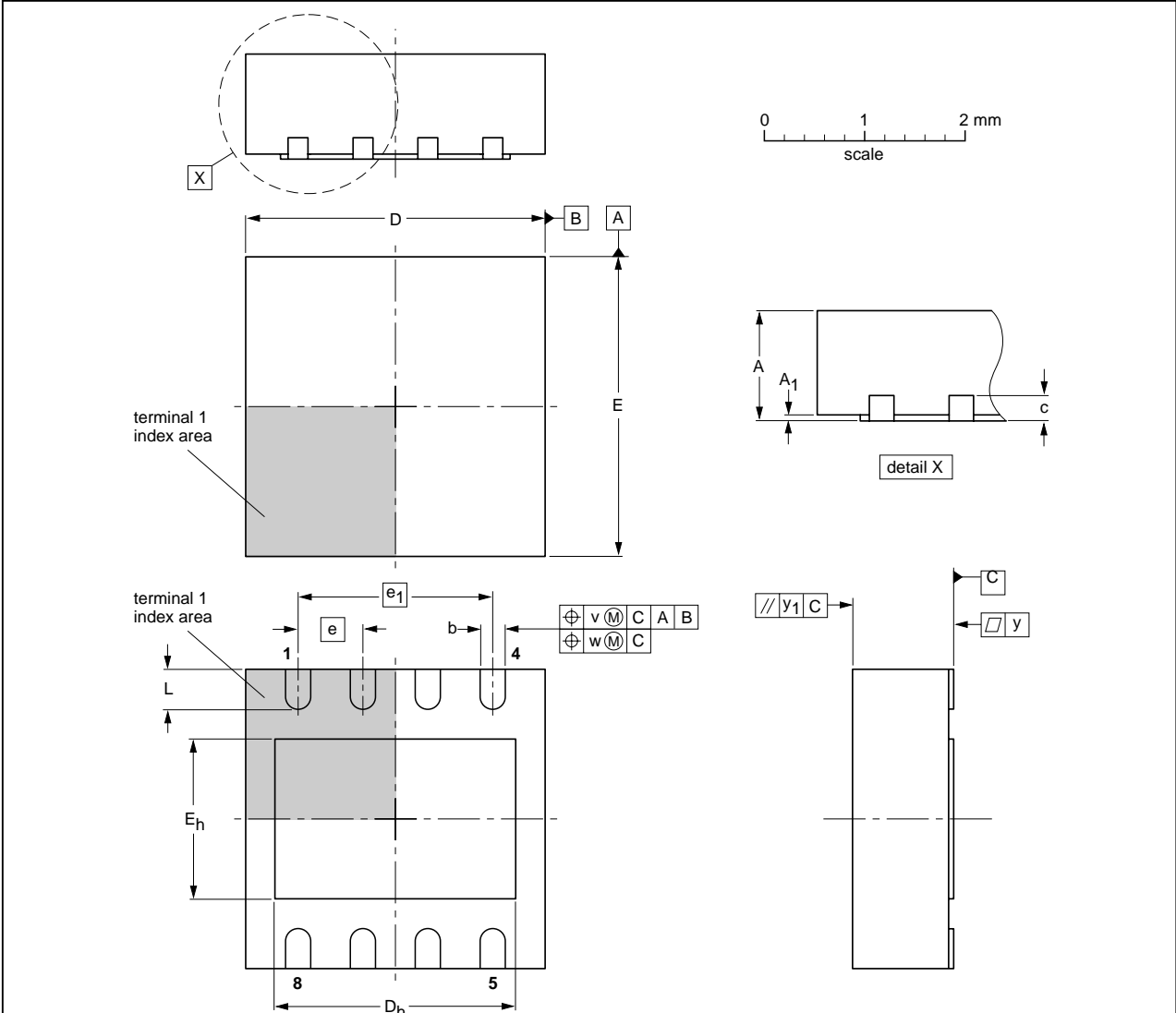


Fig 21. Package outline SOT505-1 (TSSOP8)

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm

SOT782-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max.	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	L	v	w	y	y ₁
mm	1	0.05 0.00	0.35 0.25	0.2	3.1 2.9	2.55 2.25	3.1 2.9	1.75 1.45	0.65	1.95	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT782-1	---	MO-229	---		03-01-29

Fig 22. Package outline SOT782-1 (HVSON8)

13. Packing information

The SA56004X is packed in reels, as shown in [Figure 23](#).

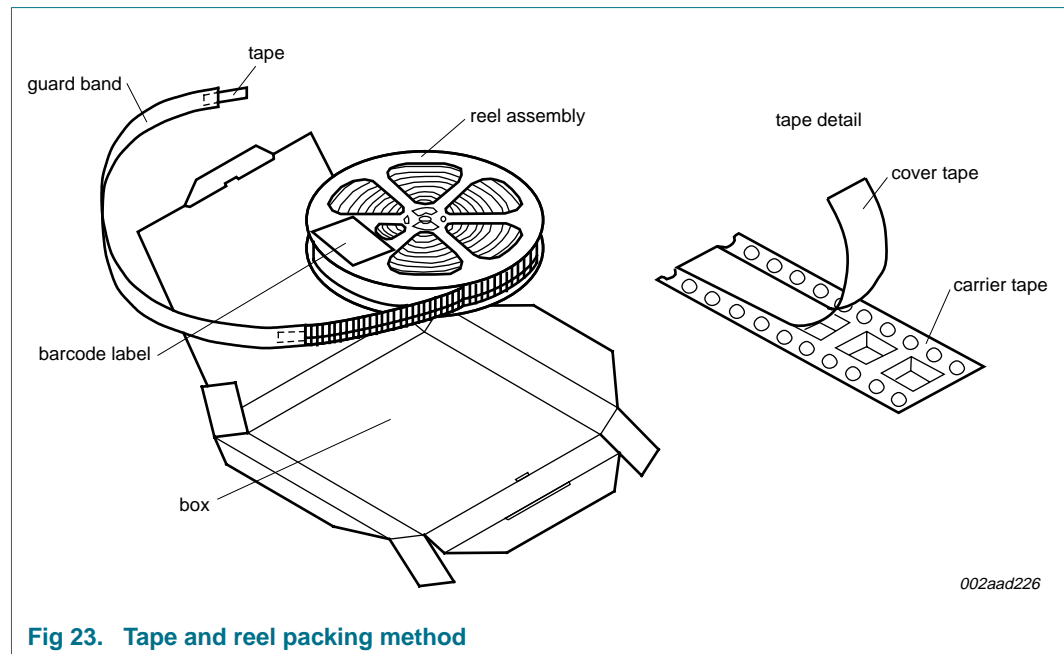


Fig 23. Tape and reel packing method

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 24](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 20](#) and [21](#)

Table 20. SnPb eutectic process (from J-STD-020C)

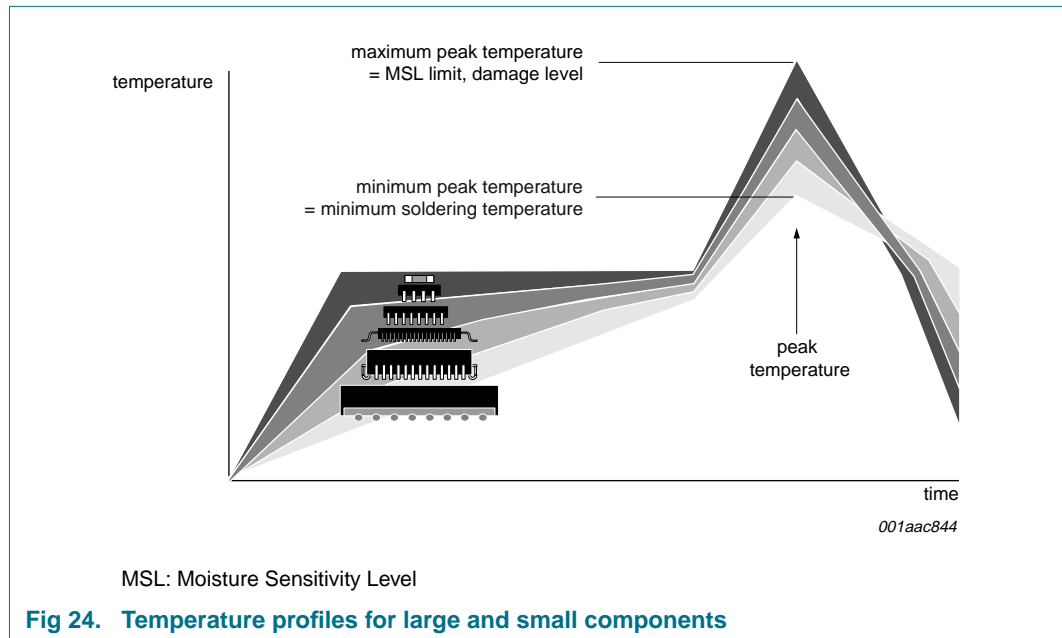
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 21. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 24](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

15. Mounting

15.1 Printed-circuit board layout considerations

Care must be taken in Printed-Circuit Board (PCB) layout to minimize noise induced at the remote temperature sensor inputs, especially in extremely noisy environments, such as a computer motherboard. Noise induced in the traces running between the device sensor inputs and the remote diode can cause temperature conversion errors. Typical sensor signal levels to the SA56004X is a few microvolts. The following guidelines are recommended:

1. Place the SA56004X as close as possible to the remote sensor. It can be from 4 inches to 8 inches, as long as the worst noise sources such as clock generator, data and address buses, CRTs are avoided.

2. Route the D+ and D– lines parallel and close together with ground guards enclosing them (see [Figure 25](#)).
3. Leakage currents due to printed-circuit board contamination must be considered. Error can be introduced by these leakage currents.
4. Use wide traces to reduce inductance and noise pick-up. Narrow traces more readily pick up noise. The minimum width of 10 mil and space of 10 mil are recommended.
5. Place a bypass capacitor of 10 nF close to the V_{DD} pin and an input filter capacitor of 2200 pF close to the D+ and D– pins.
6. A shielded twisted pair is recommended if remote sensor is located several feet away from the temperature sensor. Under this circumstance, connect the shield of the cable at the device side to the SA56004X GND pin and leave the shield at the remote end unconnected to avoid ground loop currents. Also notice that the series resistance of the cable may introduce measurement error; 1 Ω can introduce about 0.5 °C.



Fig 25. D+ and D– trace layout

16. Abbreviations

Table 22. Abbreviations

Acronym	Description
A/D	Analog-to-Digital
ARA	Alert Response Address
ASIC	Application Specific Integrated Circuit
CRT	Cathode Ray Tube
ESD	ElectroStatic Discharge
HBM	Human Body Model
HVAC	Heating, Ventilating and Air Conditioning
I ² C-bus	Inter-Integrated Circuit bus
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
OTP	One-Time Programmable
POR	Power-On Reset
PTAT	Proportional To Absolute Temperature
SMBus	System Management Bus
UVL	Under Voltage Lockout

17. Revision history

Table 23. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SA56004X_5	20080522	Product data sheet	-	SA56004X_4
Modifications:		<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added HVSON8 package option • Table 17 "Limiting values": removed "P, power dissipation" specification from this table • Table 19 "SMBus interface characteristics": <ul style="list-style-type: none"> – descriptions of parameters moved to table notes – t_{LOW}: Min changed from "4.7 μs" to "600 ns"; Typ changed from "5.0 μs" to "5000 ns" – t_{HIGH}: Min changed from "4.0 μs" to "600 ns"; Typ changed from "5.0 μs" to "5000 ns" – t_{BUF}: Min changed from "4.7 μs" to "600 ns" – $t_{HD;STA}$: Min changed from "4.0 μs" to "600 ns" – $t_{HD;DAT}$: Min changed from "-" to "0 ns" – $t_{SU;STO}$: Min changed from "4.0 μs" to "250 ns" – symbol "$t_{TIMEOUT}$, SMBus TIMEOUT" changed to "$t_{to(SMBus)}$, SMBus time-out time" 		
SA56004X_4	20060808	Product data sheet	-	SA56004X_3
SA56004X_3 (9397 750 13841)	20041006	Product data sheet	-	SA56004X_2
SA56004X_2 (9397 750 12015)	20030903	Objective data	-	SA56004-X_1
SA56004-X_1 (9397 750 10993)	20030819	Objective data	-	-

18. Legal information

18.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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