ES_LPC1112

Errata sheet LPC1112

Rev. 2 — 15 November 2010 **Errata sheet**

Document information

Info	Content
Keywords	LPC1112 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table at the end of the document.

Revision history

Rev	Date	Description
2	20101115	• Added ADC.1. • Added Rev. ‘B’.
1	20100510	• Initial version

Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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1. Product identification

The LPC1112 devices typically have the following top-side marking:

LPC1112x

/xxx

xxxxxxx

xxYYWWxR[x]

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC1112:

Table 1. Device revision table

Revision identifier (R)	Revision description
'B'	Second device revision
'A'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
ADC.1	External sync inputs not operational	'A', 'B'	Section 3.1 on page 4

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes

Note	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

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3. Functional problems detail

3.1 ADC.1: External sync inputs not operational

Introduction:

In software-controlled mode (BURST bit is 0), the 10-bit ADC can start conversion by using the following options in the A/D Control Register:

26:24	START		When the BURST bit is 0, these bits control whether and when an A/D conversion is started:	0
		0x0	No start (this value should be used when clearing PDN to 0).	
		0x1	Start conversion now.	
		0x2	Start conversion when the edge selected by bit 27 occurs on PIO0_2/SSEL/CT16B0_CAP0.	
		0x3	Start conversion when the edge selected by bit 27 occurs on PIO1_5/DIR/CT32B0_CAP0.	
		0x4	Start conversion when the edge selected by bit 27 occurs on CT32B0_MAT0.	
		0x5	Start conversion when the edge selected by bit 27 occurs on CT32B0_MAT1.	
		0x6	Start conversion when the edge selected by bit 27 occurs on CT16B0_MAT0.	
		0x7	Start conversion when the edge selected by bit 27 occurs on CT16B0_MAT1.	

Problem:

The external start conversion feature, AD0CR:START = 0x2 or 0x3, may not work reliably and ADC external trigger edges on PIO0_2 or PIO1_5 may be missed. The occurrence of this problem is peripheral clock (pclk) dependent. The probability of error (missing a ADC trigger from GPIO) is estimated as follows:

- For PCLK_ADC = 100 MHz, probability error = 12 %
- For PCLK_ADC = 50 MHz, probability error = 6 %
- For PCLK_ADC = 12 MHz, probability error = 1.5 %

The probability of error is not affected by the frequency of ADC start conversion edges.

Work-around:

In software-controlled mode (BURST bit is 0), the START conversion options (bits 26:24 set to 0x1 or 0x4 or 0x5 or 0x6 or 0x7) can be used. The user can also start a conversion by connecting an external trigger signal to a capture input pin (CAPx) from a Timer peripheral to generate an interrupt. The timer interrupt routine can then start the ADC conversion by setting the START bits (26:24) to 0x1. The trigger can also be generated from a timer match register.

4. AC/DC deviations detail

No known errata.

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5. Errata notes

No known errata.

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