# ES_LPC11Cxx

## Errata sheet LPC11C12/14/22/24

**Rev. 4.1 — 23 February 2016** **Errata sheet**

### Document information

| Info | Content |
|---|---|
| **Keywords** | LPC11C12FBD48; LPC11C14FBD48; LPC11C22FBD48; LPC11C24FBD48 errata |
| **Abstract** | This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.<br>Each deviation is assigned a number and its history is tracked in a table. |

### Revision history

| Rev | Date | Description |
|---|---|---|
| 4.1 | 20160223 | • Added VDD.2. |
| 4 | 20130117 | • Added I2C.1. |
| 3.2 | 20120118 | • Added ADC.2. |
| 3.1 | 20110901 | • Added Note.1. |
| 3 | 20110301 | • Combined errata for LPC11C12, LPC11C14, LPC11C22, and LPC11C24 into one document.<br>• Added VDD.1.<br>• Section 3.1: Removed text “For PCLK_ADC = 100 MHz....” |
| 2 | 20101115 | • Added ADC.1. |
| 1 | 20100510 | • Initial version |

## Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

# 1. Product identification

The LPC11Cxx devices typically have the following top-side marking:

LPC11Cxxx

/xxx

xxxxxxx

xxYYWWxR[x]

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC11Cxx:

**Table 1. Device revision table**

| Revision identifier (R) | Revision description |
|---|---|
| 'A' | Initial device revision |

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

# 2. Errata overview

**Table 2. Functional problems table**

| Functional problems | Short description | Revision identifier | Detailed description |
|---|---|---|---|
| ADC.1 | External sync inputs not operational | 'A' | Section 3.1 |
| ADC.2 | A/D Global Data register should not be used with burst mode or hardware triggering. | 'A' | Section 3.2 |
| I2C.1 | In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. | 'A' | Section 3.3 |
| VDD.1 | The minimum voltage of the power supply ramp must be 200 mV or below | 'A' | Section 3.4 |
| VDD.2 | External $\overline{\text{RESET}}$ pin must be held LOW until the power supply on the VDD pin reaches minimum operating voltage of 1.8 V. | 'A' | Section 3.5 |

**Table 3. AC/DC deviations table**

| AC/DC deviations | Short description | Revision identifier | Detailed description |
|---|---|---|---|
| n/a | n/a | n/a | n/a |

**Table 4. Errata notes**

| Note | Short description | Revision identifier | Detailed description |
|---|---|---|---|
| Note.1 | During power-up, an unexpected glitch (low pulse) could occur on the port pins as the $V_{DD}$ supply ramps up. | 'A' | Section 5.1 |

# 3. Functional problems detail

## 3.1 ADC.1: External sync inputs not operational

### Introduction:

In software-controlled mode (BURST bit is 0), the 10-bit ADC can start conversion by using the following options in the A/D Control Register:

| | | | | |
|---|---|---|---|---|
| 26:24 | START | | When the BURST bit is 0, these bits control whether and when an A/D conversion is started: | 0 |
| | | 0x0 | No start (this value should be used when clearing PDN to 0). | |
| | | 0x1 | Start conversion now. | |
| | | 0x2 | Start conversion when the edge selected by bit 27 occurs on PIO0_2/SSEL/CT16B0_CAP0. | |
| | | 0x3 | Start conversion when the edge selected by bit 27 occurs on PIO1_5/DIR/CT32B0_CAP0. | |
| | | 0x4 | Start conversion when the edge selected by bit 27 occurs on CT32B0_MAT0. | |
| | | 0x5 | Start conversion when the edge selected by bit 27 occurs on CT32B0_MAT1. | |
| | | 0x6 | Start conversion when the edge selected by bit 27 occurs on CT16B0_MAT0. | |
| | | 0x7 | Start conversion when the edge selected by bit 27 occurs on CT16B0_MAT1. | |

### Problem:

The external start conversion feature, AD0CR:START = 0x2 or 0x3, may not work reliably and ADC external trigger edges on PIO0_2 or PIO1_5 may be missed. The occurrence of this problem is peripheral clock (pclk) dependent. The probability of error (missing an ADC trigger from GPIO) is estimated as follows:

- For PCLK_ADC = 50 MHz, probability error = 6 %
- For PCLK_ADC = 12 MHz, probability error = 1.5 %

The probability of error is not affected by the frequency of ADC start conversion edges.

### Work-around:

In software-controlled mode (BURST bit is 0), the START conversion options (bits 26:24 set to 0x1 or 0x4 or 0x5 or 0x6 or 0x7) can be used. The user can also start a conversion by connecting an external trigger signal to a capture input pin (CAPx) from a Timer peripheral to generate an interrupt. The timer interrupt routine can then start the ADC conversion by setting the START bits (26:24) to 0x1. The trigger can also be generated from a timer match register.

## 3.2 ADC.2: A/D Global Data register should not be used with burst mode or hardware triggering

### Introduction:

On the LPC11Cxx, the START field and the BURST bit in the A/D control register specify whether A/D conversions are initiated via software command, in response to some hardware trigger, or continuously in burst ("hardware-scan") mode. Results of the ADC conversions can be read in one of two ways. One is to use the A/D Global Data Register to read all data from the ADC. Another is to use the individual A/D Channel Data Registers.

### Problem:

If the burst mode is enabled (BURST bit set to ‘1’) or if hardware triggering is specified, the A/D conversion results read from the A/D Global Data register could be incorrect. If conversions are only launched directly by software command (BURST bit = '0' and START = ‘001’), the results read from the A/D Global Data register will be correct provided the previous result is read prior to launching a new conversion.

### Work-around:

When using either burst mode or hardware triggering, the individual A/D Channel Data registers should be used instead of the A/D Global Data register to read the A/D conversion results.

## 3.3 I2C.1: In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register

### Introduction:

The I2C monitor allows the device to monitor the I2C traffic on the I2C bus in a non-intrusive way.

### Problem:

In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. If this is not done, the received data from the slave device will be corrupted. To allow the monitor mode to have sufficient time to process the data on the I2C bus, the device may need to have the ability to stretch the I2C clock. Under this condition, the I2C monitor mode is not 100% non-intrusive.

### Work-around:

When setting the device in monitor mode, enable the ENA_SCL bit in the MMCTRL register to allow clock stretching.

Software code example to enable the ENA_SCL bit:

```
LPC_I2C_MMCTRL |= (1<<1); //Enable ENA_SCL bit
```

In the I2C ISR routine, for the status code related to the slave-transmitter mode, write the value of 0xFF into the DAT register to prevent data corruption. In order to avoid stretching the SCL clock, the data byte can be saved in a buffer and processed in the Main loop. This ensures the SI flag is cleared as fast as possible.

Software code example for the slave-transmitter mode:

```
case 0xA8:     // Own SLA + R has been received, ACK returned
case 0xB0:
case 0xB8:     // data byte in DAT transmitted, ACK received
case 0xC0:     // (last) data byte transmitted, NACK received
case 0xC8:     // last data byte in DAT transmitted, ACK received
    DataByte = LPC_I2C->DATA_BUFFER;//Save data. Data can be process in Main loop
    LPC_I2C->DAT = 0xFF;            // Pretend to shift out 0xFF
    LPC_I2C->CONCLR = 0x08;         // clear flag SI
break;
```

## 3.4 VDD.1: The minimum voltage of the power supply ramp must be 200 mV or below

### Introduction:

The datasheet specifies that the power supply (on the VDD pin) must ramp-up from a minimum voltage of 400 mV or below with a ramp-up time of 500 ms or faster. Also, the minimum time the power supply (on the VDD pin) needs to be below 400 mV or below before ramping up is 12 μs.

### Problem:

The device might not always start-up if the power supply (on the VDD pin) does not reach 200 mV. The minimum voltage of the power supply ramp (on the VDD pin) must be 200 mV or below with ramp-up time of 500 ms or faster.

### Work-around:

None.

## 3.5 VDD.2: The external $\overline{\text{RESET}}$ pin must be held LOW until the power supply on the VDD pin reaches minimum operating voltage of 1.8 V.

### Introduction:

Based on the data sheet (power-up ramp conditions specification) and errata sheet (Section 3.4 “VDD.1: The minimum voltage of the power supply ramp must be 200 mV or below”), the power supply (on the VDD pin) must ramp-up from a minimum voltage of 200 mV or below with a ramp-up time of 500 ms or faster. Also, the minimum time the power supply (on the VDD pin) needs to be below 200 mV or below before ramping up is 12 μs.

### Problem:

For linear power-supply ramp-up rates of 5.5 V/mS or less, the device might not always start-up.

### Work-around:

For linear power-supply ramp-up rates of 5.5 V/mS or less, the external $\overline{\text{RESET}}$ pin must be held LOW until the power supply on the VDD pin reaches minimum operating voltage of 1.8 V. The minimum time the external $\overline{\text{RESET}}$ pin must be held LOW can be calculated using the following equation:

$$\text{time} = \frac{1.8\ \text{V}}{\text{ramp rate}\left(\frac{\text{V}}{\text{mS}}\right)}$$

**Fig 1. Minimum time**

For linear power-supply ramp-up rates more than 5.5 V/mS, the external $\overline{\text{RESET}}$ pin does not need to be held LOW.

# 4. AC/DC deviations detail

No known errata.

# 5. Errata notes

## 5.1 Note.1

The General Purpose I/O (GPIO) pins have configurable pull-up/pull-down resistors where the pins are pulled up to the $V_{DD}$ level by default. During power-up, an unexpected glitch (low pulse) could occur on the port pins as the $V_{DD}$ supply ramps up.

# 6. Legal information

## 6.1 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

## 6.2 Disclaimers

**Limited warranty and liability —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

## 6.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 7. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 23 February 2016**
**Document identifier: ES_LPC11CXX**