## Document information

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<th>Info</th>
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<tr>
<td>Keywords</td>
<td>LPC1549JBD100; LPC1549JBD64; LPC1549JBD48; LPC1548JBD100; LPC1548JBD64; LPC1548JBD48; LPC1547JBD64; LPC1547JBD48; LPC1519JBD100; LPC1519JBD64; LPC1518JBD100; LPC1518JBD64; LPC1517JBD64; LPC1517JBD48</td>
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<td>Abstract</td>
<td>LPC15xx errata</td>
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## Revision history

<table>
<thead>
<tr>
<th>Rev</th>
<th>Date</th>
<th>Description</th>
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<tbody>
<tr>
<td>2.1</td>
<td>20151120</td>
<td>• Added DPD.1</td>
</tr>
<tr>
<td>2</td>
<td>20150417</td>
<td>• Added UART.1</td>
</tr>
<tr>
<td>1</td>
<td>20140224</td>
<td>• Initial version</td>
</tr>
</tbody>
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## Contact information

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For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)
1. Product identification

The LPC15xx devices typically have the following top-side marking:

LPC15xxxxxxx
xxxxxxx
xxYWWxR

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC15xx:

Table 1. Device revision table

<table>
<thead>
<tr>
<th>Revision identifier (R)</th>
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</tr>
</thead>
<tbody>
<tr>
<td>‘A’</td>
<td>Initial device revision</td>
</tr>
</tbody>
</table>

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

<table>
<thead>
<tr>
<th>Functional problems</th>
<th>Short description</th>
<th>Revision identifier</th>
<th>Detailed description</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB.1</td>
<td>USB controller is unable to generate STALL on EP0_OUT.</td>
<td>‘A’</td>
<td>Section 3.1</td>
</tr>
<tr>
<td>I2C_ROM.1</td>
<td>Slave transmit ROM API functions not working.</td>
<td>‘A’</td>
<td>Section 3.2</td>
</tr>
<tr>
<td>UART.1</td>
<td>The UART controller sets the Idle status bits for receive and transmit before the transmission of the stop bit is complete.</td>
<td>‘A’</td>
<td>Section 3.3</td>
</tr>
<tr>
<td>DPD.1</td>
<td>Deep power-down mode is not functional outside certain voltage and temperature ranges.</td>
<td>‘A’</td>
<td>Section 3.4</td>
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</table>

Table 3. AC/DC deviations table

<table>
<thead>
<tr>
<th>AC/DC deviations</th>
<th>Short description</th>
<th>Revision identifier</th>
<th>Detailed description</th>
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<td>n/a</td>
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Table 4. Errata notes

<table>
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<th>Note</th>
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<th>Detailed description</th>
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<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
</tr>
</tbody>
</table>
3. Functional problems detail

3.1 USB.1: USB controller is unable to generate STALL on EP0_OUT

Introduction:
The LPC15xx have a full-speed USB device controller with support for 10 physical endpoints.

Problem:
The USB device controller is unable to return a STALL handshake on an OUT data packet to endpoint zero. An NAK handshake is returned instead.

Work-around:
Endpoint zero is the control endpoint. All requests sent to the control endpoint consist of three stages (SETUP / DATA / STATUS). When an unsupported ControlWrite request (with data phase) is sent by the host to the device, the device is unable to STALL the data phase of this request.

To solve this problem, the device firmware must accept the data transmitted during the data phase of this ControlWrite request and return a STALL handshake when the IN token for the STATUS stage is received.
3.2 I2C_ROM.1: Slave transmit ROM API functions not working

Introduction:
The LPC15XX provide a ROM API for transmitting data via the i²C-bus interface in slave mode using the interrupt or polling method.

Problem:
The following I2C ROM API functions transmit 0xFF instead of the provided data:

- ErrorCode_t i2c_slave_transmit_intr( I2C_HANDLE_T* h_i2c, I2C_PARAM* ptp, I2C_RESULT* ptr)
- ErrorCode_t i2c_slave_transmit_poll( I2C_HANDLE_T* h_i2c, I2C_PARAM* ptp, I2C_RESULT* ptr)

Work-around:
Do not use the I2C slave transmit ROM API functions. The I2C register interface allows direct programming of the data transmit operation in slave mode.
3.3 UART.1

Introduction:

In receive mode, the UART controller provides a status bit (the RXIDLE bit in the UART STAT register) to check whether the receiver is currently receiving data. If RXIDLE is set, the receiver indicates it is idle and does not receive data.

In transmit mode, the UART controller provides two status bits (TXIDLE and TXDISSTAT bits in the UART STAT register) to indicate whether the transmitter is currently transmitting data. The TXIDLE bit is set by the controller after the last stop bit has been transmitted. The TXDISSTAT bit is set by the controller after the transmitter has sent the last stop bit and has become fully idle following a transmit disable executed by setting the TXDIS bit in the UART CTRL register.

The status bits can be used to implement software flow control, but their setting does not affect normal UART operation.
Problem:
The RXIDLE bit is incorrectly set for a fraction of the clock cycle between the reception of the last data bit and the reception of the start bit of the next word, that is while the stop bit is received. RXIDLE is cleared at the beginning of the start bit.

Both, TXIDLE and TXDISSTAT are set incorrectly between the last data bit and the stop bit while the transfer is still ongoing.

Work-around:
When writing code that checks for the setting of any of the status bits RXIDLE, TXIDLE, TXDISSTAT, check the value of the status bit in the STAT register:

- If status bit = 1, add a delay of one UART bit time (if STOPLEN = 0, one stop bit) or two bit times (if STOPLEN = 1, two stop bits) and check the value of the status bit again:
  - If status bit = 1, the receiver is idle.
  - If status bit = 0, the receiver is receiving data.
  - If the status bit = 0, the receiver is receiving data.
3.4 DPD.1

Introduction:
The LPC15xx has a supply voltage ($V_{DD}$) from 2.4 V to 3.6 V and can operate from -40 °C to 105 °C. The LPC15xx supports four reduced power modes (sleep, deep-sleep, power-down, and deep power-down mode). Deep power-down mode allows for maximal power savings where the entire system is shut down except for the general purpose registers in the PMU and the self wake-up timer. Only the general purpose registers in the PMU maintain their internal states in deep power-down mode.

Problem:
At temperatures $\leq 25$ °C, the deep power-down mode is not functional if the $V_{DD}$ supply voltage is $> 3.4$ V. At temperatures $> 25$ °C, the deep power-down mode is not functional if the $V_{DD}$ supply voltage is $> 3.35$ V.

Work-around:
Deep power-down mode operates correctly for the entire temperature range (-40 °C to 105 °C) if the $V_{DD}$ supply is between 2.4 V and 3.35 V. For temperatures $\leq 25$ °C, ensure that the supply voltage is not $> 3.4$ V ($V_{DD} = 2.4$ V to 3.4 V) when using deep power-down mode. For temperatures $> 25$ °C, ensure that the supply voltage is not $> 3.35$ V ($V_{DD} = 2.4$ V to 3.35 V) when using deep power-down mode.
4. **AC/DC deviations detail**

   No known errata.

5. **Errata notes**

   No known errata.
6. Legal information

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