ES_LPC2361

Errata sheet LPC2361

Rev. 8 — 1 June 2011 Errata sheet

Document information

Info	Content
Keywords	LPC2361 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
8	20110601	• Added USB.1.
7	20110420	• Added Note.2.
6	20110301	• Added ADC.1.
5	20100607	• Removed Ethernet.1; device does not have Ethernet feature.
4	20100401	• The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Added Ethernet.1
3	20100122	• Added VBAT.2
2	20090511	• Added Rev D
1	20080904	• First version

Contact information

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1. Product identification

The LPC2361 devices typically have the following top-side marking:

LPC2361xxx

xxxxxxx

xxYYWWR[x]

The last/second to last letter in the third line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the LPC2361:

Table 1. Device revision table

Revision identifier (R)	Revision description
‘B’	First device revision
‘D’	Second device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
Core.1	Incorrect update of the Abort Link register in Thumb state	‘B’, ‘D’	Section 3.1 on page 5
CAN.1	Data overrun condition can lock the CAN controller	‘B’	Section 3.2 on page 6
Deep power-down.1	Deep power-down mode is not functional	‘B’	Section 3.3 on page 6
VBAT.1	Increased power consumption on VBAT when VBAT is powered before the 3.3 V supply used by rest of device	‘B’	Section 3.4 on page 7
VBAT.2	The VBAT pin cannot be left floating	‘B’	Section 3.5 on page 7
ADC.1	External sync inputs not operational	‘B’, ‘D’	Section 3.6 on page 8
USB.1	USB host controller hangs on a dribble bit	‘B’, ‘D’	Section 3.7 on page 9

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Product version(s)	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
Note.1	When the input voltage is Vi ≥ V_{DD} I/O + 0.5 V on each of the following port pins P0.23, P0.24. P0.25, P0.26, P1.30, and P1.31 (configured as general purpose input pin (s)), current must be limited to less than 4 mA by using a series limiting resistor.	'B', 'D'	Section 5.1 on page 10
Note.2	On the LPC2361 Rev D, design changes to the Memory Accelerator Module were made to enhance timing and general performance.	'D'	Section 5.2 on page 10

3. Functional problems detail

3.1 Core.1: Incorrect update of the Abort Link register in Thumb state

Introduction:

If the processor is in Thumb state and executing the code sequence STR, STMIA or PUSH followed by a PC relative load, and the STR, STMIA or PUSH is aborted, the PC is saved to the abort link register.

Problem:

In this situation the PC is saved to the abort link register in word resolution, instead of half-word resolution.

Conditions:

The processor must be in Thumb state, and the following sequence must occur:

<any instruction>

<STR, STMIA, PUSH> <---- data abort on this instruction

LDR rn, [pc,#offset]

In this case the PC is saved to the link register R14_abt in only word resolution, not half-word resolution. The effect is that the link register holds an address that could be #2 less than it should be, so any abort handler could return to one instruction earlier than intended.

Work-around:

In a system that does not use Thumb state, there will be no problem.

In a system that uses Thumb state but does not use data aborts, or does not try to use data aborts in a recoverable manner, there will be no problem.

Otherwise the workaround is to ensure that a STR, STMIA or PUSH cannot precede a PC-relative load. One method for this is to add a NOP before any PC-relative load instruction. However this is would have to be done manually.

3.2 CAN.1: Data Overrun condition can lock the CAN controller

Introduction:

Each CAN controller provides a double Receive Buffer (RBX) per CAN channel to store incoming messages until they are processed by the CPU. Software task should read and save received data as soon as a message reception is signaled.

In cases where both receive buffers are filled and the contents are not read before the third message comes in, a CAN Data Overrun situation is signaled. This condition is signaled via the Status register and the Data Overrun Interrupt (if enabled).

Problem:

In a Data Overrun condition, the CAN controller is locked from further message reception.

Work-around:

1. Recovering from this situation is only possible with a soft reset to the CAN controller.
2. If software cannot read all messages in time before a third message comes in, it is recommend to change the acceptance filtering by adding further acceptance filter group(s) for messages, which are normally rejected. With this approach, the third incoming message is accepted and the Data Overrun condition is avoided. These additional messages are received with the corresponding group index number can be easily identified and rejected by software.

3.3 Deep power-down.1: Deep power-down mode is not functional

Introduction:

Deep power-down mode is like Power-down mode, but the on-chip regulator that supplies power to internal logic is also shut off. This produces the lowest possible power consumption without actually removing power from the entire chip.

Problem:

The power consumption in Deep power-down mode does not meet the specifications.

Work-around:

None.

3.4 VBAT.1: Increased power consumption on VBAT when VBAT is powered before the 3.3 V supply used by rest of the device

Introduction:

The device has a VBAT pin which provides power only to the RTC and Battery RAM. VBAT can be connected to a battery or the same 3.3 V supply used by rest of the device ($V_{DD(3V3)}$ pin, $V_{DD(DCDC)(3V3)}$ pin).

Problem:

If VBAT is powered before the 3.3 V supply, VBAT is unable to source the start-up current required for the Battery RAM. Therefore, power consumption on the VBAT pin will be high and will remain high until 3.3 V supply is powered up. Once 3.3 V supply is powered up, power consumption on the VBAT pin will reduce to normal and subsequent power cycle on the 3.3 V supply will not cause an increased power consumption on the VBAT pin.

Work-around:

Provide 3.3 V supply used by rest of the device first and then provide VBAT voltage.

3.5 VBAT.2: The VBAT pin cannot be left floating

Introduction:

The device has a VBAT pin which provides power only to the Real Time Clock (RTC) and Battery RAM. VBAT can be connected to a battery or the same supply used by rest of the device ($V_{DD(3V3)}$ pin, $V_{DD(DCDC)(3V3)}$ pin). The input voltage range on the VBAT pin is 2.0 V minimum to 3.6 V maximum for temperature –40 °C to +85 °C. Normally, if the RTC and the Battery RAM are not used, the VBAT pin can be left floating.

Problem:

If the VBAT pin is left floating, the internal reset signal within the RTC domain may get corrupted and as a result, prevents the device from starting-up.

Work-around:

The VBAT should be connected to a battery or the same supply used by rest of the device ($V_{DD(3V3)}$ pin, $V_{DD(DCDC)(3V3)}$ pin).

3.6 ADC.1: External sync inputs not operational

Introduction:

In software-controlled mode (BURST bit is 0), the 10-bit ADC can start conversion by using the following options in the A/D Control Register:

26:24	START		When the BURST bit is 0, these bits control whether and when an A/D conversion is started:	0
		000	No start (this value should be used when clearing PDN to 0).	
		001	Start conversion now.	
		010	Start conversion when the edge selected by bit 27 occurs on P2.10/EINT0.	
		011	Start conversion when the edge selected by bit 27 occurs on P1.27/CAP0.1.	
		100	Start conversion when the edge selected by bit 27 occurs on MAT0.1.	
		101	Start conversion when the edge selected by bit 27 occurs on MAT0.3.	
		110	Start conversion when the edge selected by bit 27 occurs on MAT1.0.	
		111	Start conversion when the edge selected by bit 27 occurs on MAT1.1.	

Fig 1. A/D control register options

Problem:

The external start conversion feature, AD0CR:START = 0x2 or 0x3, may not work reliably and ADC external trigger edges on P2.10 or P1.27 may be missed. The occurrence of this problem is peripheral clock (pclk) dependent. The probability of error (missing a ADC trigger from GPIO) is estimated as follows:

- For PCLK_ADC = 72 MHz, probability error = 12 %
- For PCLK_ADC = 50 MHz, probability error = 6 %
- For PCLK_ADC = 12 MHz, probability error = 1.5 %

The probability of error is not affected by the frequency of ADC start conversion edges.

Work-around:

In software-controlled mode (BURST bit is 0), the START conversion options (bits 26:24 set to 0x1 or 0x4 or 0x5 or 0x6 or 0x7) can be used. The user can also start a conversion by connecting an external trigger signal to a capture input pin (CAPx) from a Timer peripheral to generate an interrupt. The timer interrupt routine can then start the ADC conversion by setting the START bits (26:24) to 0x1. The trigger can also be generated from a timer match register.

3.7 USB.1: USB host controller hangs on a dribble bit

Introduction:

Full-/low-speed signaling uses bit stuffing throughout the packet without exception. If the receiver sees seven consecutive ones anywhere in the packet, then a bit stuffing error has occurred and the packet should be ignored.

The time interval just before an EOP is a special case. The last data bit before the EOP can become stretched by hub switching skews. This is known as dribble and can lead to a situation where dribble introduces a sixth bit that does not require a bit stuff. Therefore, the receiver must accept a packet for which there are up to six full bit times at the port with no transitions prior to the EOP.

Problem:

The USB host controller will hang indefinitely if it sees a dribble bit on the USB bus. It will hang the first time a dribble bit is seen. Once it is in this state there is no recovery other than a hard chip reset. This problem has no effect on the USB device controller.

Work-around:

None.

4. AC/DC deviations detail

4.1 n/a

5. Errata notes detail

5.1 Note.1

On each of the following port pins P0.23, P0.24, P0.25, P0.26, P1.30, and P1.31 (when configured as general purpose input pin (s)), leakage current increases when the input voltage is $V_i \geq V_{DD}$ I/O + 0.5 V. Care must be taken to limit the current to less than 4 mA by using a series limiting resistor.

5.2 Note.2

On the LPC2361 Rev D, design changes to the Memory Accelerator Module were made to enhance timing and general performance. Design changes are intended to enhance performance in general and will result in minor differences in the code execution timing between the previous device revisions and rev D. Actual performance impact is code dependent, some code sequences may speed up while other code sequences may slow down between the previous device revisions and rev D. This might be observed when using software delays and in such cases, a hardware timer should be used to generate a delay instead of a software delay.

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7. Contents

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