

# ES\_LPC2470

Errata sheet LPC2470

Rev. 8 — 1 June 2011

Errata sheet

## Document information

Info	Content
<b>Keywords</b>	LPC2470 errata
<b>Abstract</b>	<p>This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.</p> <p>Each deviation is assigned a number and its history is tracked in a table.</p>



**Revision history**

Rev	Date	Description
8	20110601	<ul style="list-style-type: none"><li>Added USB.1.</li></ul>
7	20110420	<ul style="list-style-type: none"><li>Added Note.2.</li></ul>
6	20110301	<ul style="list-style-type: none"><li>Added ADC.1.</li></ul>
5	20100401	<ul style="list-style-type: none"><li>The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Added Ethernet.1</li></ul>
4	20100209	<ul style="list-style-type: none"><li>Added date code info for IRC.2</li></ul>
3	20090814	<ul style="list-style-type: none"><li>Added IRC.2</li></ul>
2	20090511	<ul style="list-style-type: none"><li>Added Rev D</li></ul>
1	20081126	<ul style="list-style-type: none"><li>First version.</li></ul>

**Contact information**

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 1. Product identification

The LPC2470 devices typically have the following top-side marking:

```
LPC2470xxx
xxxxxxx
xxYYWWR[x]
```

The last/second to last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC2470:

**Table 1. Device revision table**

Revision identifier (R)	Revision description
'C'	Initial device revision
'D'	Second device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

## 2. Errata overview

**Table 2. Functional problems table**

Functional problems	Short description	Revision identifier	Detailed description
Ethernet.1	Ethernet TxConsumeIndex register does not update correctly after the first frame is sent	'C', 'D'	<a href="#">Section 3.1 on page 5</a>
Core.1	Incorrect update of the Abort Link register in Thumb state	'C', 'D'	<a href="#">Section 3.2 on page 6</a>
ADC.1	External sync inputs not operational	'C', 'D'	<a href="#">Section 3.3 on page 6</a>
USB.1	USB host controller hangs on a dribble bit	'C', 'D'	<a href="#">Section 3.4 on page 8</a>

**Table 3. AC/DC deviations table**

AC/DC deviations	Short description	Revision identifier	Detailed description
IRC.1	Accuracy of the Internal RC oscillator (IRC) frequency may be outside of the 4 MHz +/- 1 % specification only at extreme temperatures.	'C'	<a href="#">Section 4.1 on page 9</a>
IRC.2	Accuracy of the internal RC oscillator (IRC) frequency for devices only with date codes 0949 and before are outside of spec between -20 °C and -40 °C	'D'	<a href="#">Section 4.2 on page 10</a>

Table 4. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
Note.1	When the input voltage is $V_i \geq V_{DD} I/O + 0.5$ V on each of the following port pins P0.23, P0.24, P0.25, P0.26, P1.30, P1.31, P0.12, and P0.13 (configured as general purpose input pin (s)), current must be limited to less than 4 mA by using a series limiting resistor.	'C', 'D'	<a href="#">Section 5.1 on page 10</a>
Note.2	On the LPC2470 Rev D, design changes to the Memory Accelerator Module were made to enhance timing and general performance.	'D'	<a href="#">Section 5.2 on page 10</a>

### 3. Functional problems detail

---

#### 3.1 Ethernet.1: Ethernet TxConsumeIndex register does not update correctly after the first frame is sent

**Introduction:**

The transmit consume index register defines the descriptor that is going to be transmitted next by the hardware transmit process. After a frame has been transmitted hardware increments the index, wrapping the value to 0 once the value of TxDescriptorNumber has been reached. If the TxConsumeIndex equals TxProduceIndex the descriptor array is empty and the transmit channel will stop transmitting until software produces new descriptors.

**Problem:**

The TxConsumeIndex register is not updated correctly (from 0 to 1) after the first frame is sent. After the next frame sent, the TxConsumeIndex register is updated by two (from 0 to 2). This only happens the very first time, so subsequent updates are correct (even those from 0 to 1, after wrapping the value to 0 once the value of TxDescriptorNumber has been reached)

**Work-around:**

Software can correct this situation in many ways; for example, sending a dummy frame after initialization.

### 3.2 Core.1: Incorrect update of the Abort Link register in Thumb state

**Introduction:**

If the processor is in Thumb state and executing the code sequence STR, STMIA or PUSH followed by a PC relative load, and the STR, STMIA or PUSH is aborted, the PC is saved to the abort link register.

**Problem:**

In this situation the PC is saved to the abort link register in word resolution, instead of half-word resolution.

**Conditions:**

The processor must be in Thumb state, and the following sequence must occur:

```
<any instruction>
<STR, STMIA, PUSH> <---- data abort on this instruction
LDR rn, [pc,#offset]
```

In this case the PC is saved to the link register R14\_abt in only word resolution, not half-word resolution. The effect is that the link register holds an address that could be #2 less than it should be, so any abort handler could return to one instruction earlier than intended.

**Work-around:**

In a system that does not use Thumb state, there will be no problem.

In a system that uses Thumb state but does not use data aborts, or does not try to use data aborts in a recoverable manner, there will be no problem.

Otherwise the workaround is to ensure that a STR, STMIA or PUSH cannot precede a PC-relative load. One method for this is to add a NOP before any PC-relative load instruction. However this would have to be done manually.

### 3.3 ADC.1: External sync inputs not operational

**Introduction:**

In software-controlled mode (BURST bit is 0), the 10-bit ADC can start conversion by using the following options in the A/D Control Register:

26:24	START	When the BURST bit is 0, these bits control whether and when an A/D conversion is started:	0
	000	No start (this value should be used when clearing PDN to 0).	
	001	Start conversion now.	
	010	Start conversion when the edge selected by bit 27 occurs on P2.10/EINT0.	
	011	Start conversion when the edge selected by bit 27 occurs on P1.27/CAP0.1.	
	100	Start conversion when the edge selected by bit 27 occurs on MAT0.1.	
	101	Start conversion when the edge selected by bit 27 occurs on MAT0.3.	
	110	Start conversion when the edge selected by bit 27 occurs on MAT1.0.	
	111	Start conversion when the edge selected by bit 27 occurs on MAT1.1.	

Fig 1. A/D control register options

**Problem:**

The external start conversion feature, AD0CR:START = 0x2 or 0x3, may not work reliably and ADC external trigger edges on P2.10 or P1.27 may be missed. The occurrence of this problem is peripheral clock (pclk) dependent. The probability of error (missing a ADC trigger from GPIO) is estimated as follows:

- For PCLK\_ADC = 72 MHz, probability error = 12 %
- For PCLK\_ADC = 50 MHz, probability error = 6 %
- For PCLK\_ADC = 12 MHz, probability error = 1.5 %

The probability of error is not affected by the frequency of ADC start conversion edges.

**Work-around:**

In software-controlled mode (BURST bit is 0), the START conversion options (bits 26:24 set to 0x1 or 0x4 or 0x5 or 0x6 or 0x7) can be used. The user can also start a conversion by connecting an external trigger signal to a capture input pin (CAPx) from a Timer peripheral to generate an interrupt. The timer interrupt routine can then start the ADC conversion by setting the START bits (26:24) to 0x1. The trigger can also be generated from a timer match register.

### 3.4 USB.1: USB host controller hangs on a dribble bit

**Introduction:**

Full-/low-speed signaling uses bit stuffing throughout the packet without exception. If the receiver sees seven consecutive ones anywhere in the packet, then a bit stuffing error has occurred and the packet should be ignored.

The time interval just before an EOP is a special case. The last data bit before the EOP can become stretched by hub switching skews. This is known as dribble and can lead to a situation where dribble introduces a sixth bit that does not require a bit stuff. Therefore, the receiver must accept a packet for which there are up to six full bit times at the port with no transitions prior to the EOP.

**Problem:**

The USB host controller will hang indefinitely if it sees a dribble bit on the USB bus. It will hang the first time a dribble bit is seen. Once it is in this state there is no recovery other than a hard chip reset. This problem has no effect on the USB device controller.

**Work-around:**

None.

## 4. AC/DC deviations detail

---

### 4.1 IRC.1: Accuracy of the Internal RC oscillator (IRC) frequency may be outside of the 4 MHz +/- 1 % specification only at extreme temperatures

#### Introduction:

The device has a 4 MHz internal RC oscillator (IRC) which can be optionally used as the clock source for the Watch Dog Timer (WDT), and/or as the clock that drives the PLL and subsequently the CPU. The IRC frequency spec is 4 MHz +/- 1 % accuracy over the entire voltage and temperature range. During In-System Programming (ISP), the auto-baud routine is expecting the IRC frequency to be 4 MHz +/- 1 % and is used to synchronize with the host via serial port 0.

#### Problem:

On the LPC2470 Rev C device only, the accuracy of internal RC oscillator (IRC) frequency meets 4 MHz +/- 1 % specification only at room temperature however, at extreme temperatures, the accuracy of internal RC oscillator (IRC) frequency may be 4 MHz +/- 10 %. As a result, at extreme temperatures, this may affect the auto-baud routine's ability to synchronize with the host via serial port 0 during In-System Programming (ISP) at higher baud rates.

#### Work-around:

None

## 4.2 IRC.2: Accuracy of the Internal RC Oscillator (IRC) frequency for devices only with date codes 0949 and before are outside of the 4 MHz +/- 1 % specification only at temperatures between -20 °C and -40 °C

### Introduction:

The device has a 4 MHz internal RC oscillator (IRC) which can be optionally used as the clock source for the Watch Dog Timer (WDT), and/or as the clock that drives the PLL and subsequently the CPU. The IRC frequency spec is 4 MHz +/- 1 % accuracy over the entire voltage and temperature range. During In-System Programming (ISP), the auto-baud routine is expecting the IRC frequency to be 4 MHz +/- 1 % and is used to synchronize with the host via serial port 0.

### Problem:

On the LPC2470 Rev D device (only with date codes 0949 and before), the accuracy of internal RC oscillator (IRC) frequency does not meet the 4 MHz +/- 1 % specification for temperatures between -20 °C and -40 °C and the accuracy of internal RC oscillator (IRC) frequency is 4 MHz +/- 5 % instead. As a result, only at these temperatures, this may affect the auto-baud routine's ability to synchronize with the host via serial port 0 during In-System Programming (ISP) at higher baud rates. For temperatures above -20 °C, the accuracy of internal RC oscillator (IRC) frequency meets the 4 MHz +/- 1 % specification.

### Work-around:

None

## 5. Errata notes detail

### 5.1 Note.1

On each of the following port pins P0.23, P0.24, P0.25, P0.26, P1.30, P1.31, P0.12, and P0.13 (when configured as general purpose input pin (s)), leakage current increases when the input voltage is  $V_i \geq V_{DD} I/O + 0.5$  V. Care must be taken to limit the current to less than 4 mA by using a series limiting resistor.

### 5.2 Note.2

On the LPC2470 Rev D, design changes to the Memory Accelerator Module were made to enhance timing and general performance. Design changes are intended to enhance performance in general and will result in minor differences in the code execution timing between the previous device revisions and rev D. Actual performance impact is code dependent, some code sequences may speed up while other code sequences may slow down between the previous device revisions and rev D. This might be observed when using software delays and in such cases, a hardware timer should be used to generate a delay instead of a software delay.

## 6. Legal information

### 6.1 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

### 6.2 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on a weakness or default in the customer application/use or the application/use of customer's third party customer(s) (hereinafter both referred to as "Application"). It is customer's sole responsibility to check whether the NXP Semiconductors product is suitable and fit for the Application planned. Customer has to do all necessary testing for the Application in order to avoid a default of the Application and the product. NXP Semiconductors does not accept any liability in this respect.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

### 6.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 7. Contents

---

<b>1</b>	<b>Product identification</b>	<b>3</b>
<b>2</b>	<b>Errata overview</b>	<b>3</b>
<b>3</b>	<b>Functional problems detail</b>	<b>5</b>
3.1	Ethernet.1: Ethernet TxConsumeIndex register does not update correctly after the first frame is sent	5
	Introduction:	5
	Problem:	5
	Work-around:	5
3.2	Core.1: Incorrect update of the Abort Link register in Thumb state	6
	Introduction:	6
	Problem:	6
	Conditions:	6
	Work-around:	6
3.3	ADC.1: External sync inputs not operational	6
	Introduction:	6
	Problem:	7
	Work-around:	7
3.4	USB.1: USB host controller hangs on a dribble bit	8
	Introduction:	8
	Problem:	8
	Work-around:	8
<b>4</b>	<b>AC/DC deviations detail</b>	<b>9</b>
4.1	IRC.1: Accuracy of the Internal RC oscillator (IRC) frequency may be outside of the 4 MHz +/- 1 % specification only at extreme temperatures	9
	Introduction:	9
	Problem:	9
	Work-around:	9
4.2	IRC.2: Accuracy of the Internal RC Oscillator (IRC) frequency for devices only with date codes 0949 and before are outside of the 4 MHz +/- 1 % specification only at temperatures between -20 °C and -40 °C	10
	Introduction:	10
	Problem:	10
	Work-around:	10
<b>5</b>	<b>Errata notes detail</b>	<b>10</b>
5.1	Note.1	10
5.2	Note.2	10
<b>6</b>	<b>Legal information</b>	<b>11</b>
6.1	Definitions	11
6.2	Disclaimers	11
6.3	Trademarks	11
<b>7</b>	<b>Contents</b>	<b>12</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 1 June 2011

Document identifier: ES\_LPC2470