ERRATA SHEET

Date: **2009 August 11**
Document Release: **Version 1.2**
Device Affected: **LPC2880**

This errata sheet describes both the functional problems and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

2009 August 11

NXP
Semiconductors

founded by Philips

Document revision history

Rev	Date	Description
1.2	August 11, 2009	Added ESD.1
1.1	May 23 2008	Added USB.1
1.0	May 23, 2007	First version

Identification

The typical LPC2880 devices have the following top-side marking:

LPC2880xxx

xxxxxxx

xxYYWW R

The last letter in the third line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the LPC2880:

Revision Identifier (R)	Comment
‘-’	Initial device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	Device Revision the problem occurs in
MCI.1	Rx FIFO is not functional	-
USB.1	Initial SYNC pattern too short in full-speed mode	-

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	Device Revision the deviation occurs in
ESD.1	ESD weakness on the $V_{DD(DADC1V8)}$, DCDC_$V_{DDO(1V8)}$, $V_{DD1(FLASH1V8)}$, VDD2$_{(USB1V8)}$, SCL, D0/P[0], DP and LD1/ P4[5] pins.	-

Errata Notes

Note	Short Description
NA	NA

Functional Problems of LPC2880

MCI.1: Rx FIFO is not functional

Introduction: The MCI block has a 16 word deep, 32 bits wide FIFO for incoming data. A total of 64 bytes can be buffered before they must be read by the CPU or the DMA controller. The FIFO is always in the data path, and cannot be disabled.

Problem: A read access to the MCI FIFO correctly returns the top word from the FIFO. However, every read access (either by CPU or by the DMA controller) also takes a second word from FIFO, and this word is lost. Hence, DMA cannot be used with the MCI RX FIFO, because DMA transfers are only requested once the MCI FIFO is half full.

Workaround: Every incoming word should be read from the MCI FIFO, before a second word arrives. A read access to the MCI FIFO will then return that particular word. The undesired second read access will be a dummy read on an empty FIFO, and no data is lost. This can be achieved by using the 'RxDataAvlbl' condition which causes an interrupt as soon as new word is present in the FIFO. Once the interrupt fires, software should immediately read the FIFO before the next word arrives.

USB.1: Initial SYNC pattern too short in full-speed mode

Introduction: When the device is forced to run at full-speed (by connecting the device under a “full-speed only” host/hub), the data rate in full-speed transmission should be 12 Mbps +/- 0.25 % (USB Spec 7.1.11).

Problem: The device generates an imperfect SYNC pattern when running at full-speed. When the device starts transmitting, the first SYNC bit is too short and out of the specification. This occurs only in full-speed.

Workaround: None.

AC/DC Deviations of the LPC2880

ESD.1: **ESD weakness on the $V_{DD(DADC1V8)}$, DCDC_$V_{DDO(1V8)}$, $V_{DD1(FLASH1V8)}$, $VDD2_{(USB1V8)}$, SCL, D0/P[0], DP and LD1/P4[5] pins.**

Introduction: The LPC2880 is rated for 2kV ESD HBM specification.

Problem: The LPC2880 does not meet the 2kV ESD HBM requirements on the $V_{DD(DADC1V8)}$, DCDC_$V_{DDO(1V8)}$, $V_{DD1(FLASH1V8)}$, $VDD2_{(USB1V8)}$, SCL, D0/P[0], DP and LD1/P4[5] pins.

Workarounds: Observe proper ESD handling precautions on these pins.