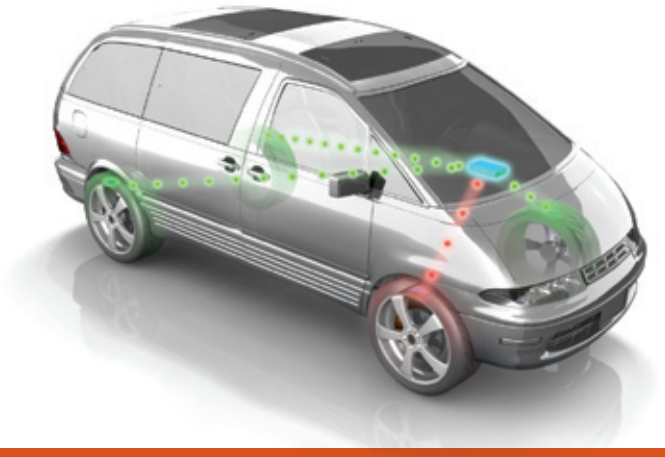

P2SC Signal Conditioning Chip family

Designed for tire pressure monitoring

A true world leader in RF identification technologies, NXP is spearheading the innovative use of this technology in Tire Pressure Monitoring Systems (TPMS). Designed for all remote sensing and signal conditioning applications, the P2SC family provides an extremely robust and accurate solution, which is also highly convenient, flexible and cost-effective.

Features

- Highly integrated single-chip solution
- Fully programmable, low-power RISC signal conditioning IC
- Two multiplexed, high-precision sensor inputs with programmable gain
- Smart power management with wake-up on demand from power down by port or 3D-LF interface
- 32-bit unique ID
- Digital Sensor Signal Processing
- 12-bit ADC
- On-chip temperature sensor and shutdown
- Wide operating temperature range -40 to +125 °C

Benefits

- Greater flexibility in system development
- Reduced time-to-market, bill of materials and development costs
- Easy, software upgrade of system
- One receiver for Remote Keyless Entry and Tire Pressure Monitoring
- Auto-localization of wheels after car maintenance
- Long product / battery life (10 years or more)
- Sensor module identification

The first member of the P2SC family is the PCH7970, a high performance device for signal conditioning and data framing in applications such as TPMS. This provides increased passenger and driver safety by constantly monitoring individual tire pressures directly, in line with recent legislation.

Based on a low power, 8-bit micro RISC kernel (MRKII), the PCH7970 features a number of general purpose I/Os to control external circuitry and a high precision 12-bit (11-bit and sign) ADC to read the output voltage of a piezo-resistive bridge sensor. Two multiplexed sensors may be connected to the device with both the sensor and ADC operating ratiometrically.

128 bytes of on-chip EEPROM stores

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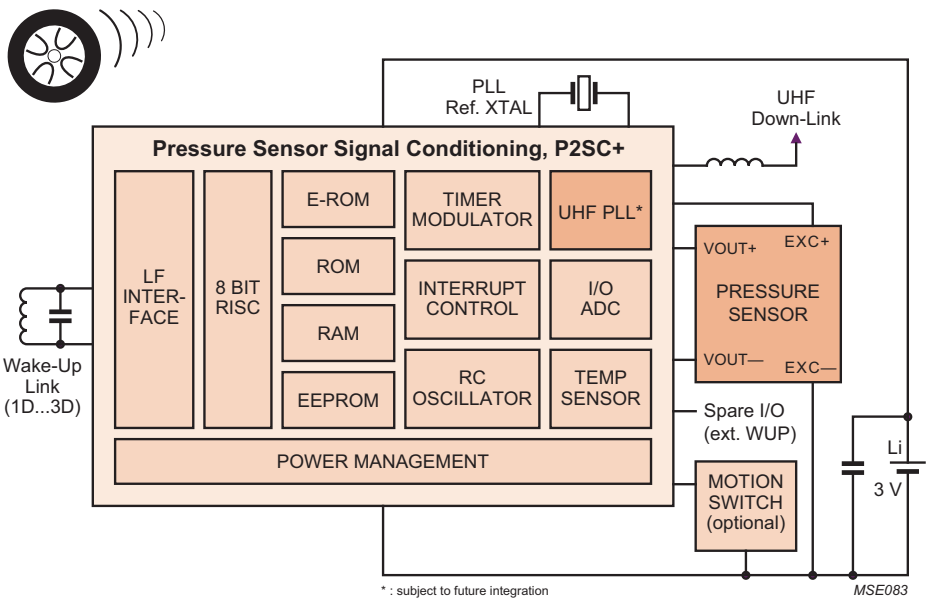
the calibration data for the Digital Sensor Signal Processing (DSSP) and correction characteristics are determined by the RISC controller and user's program. The device also incorporates 128 bytes RAM and 4 Kbyte E-ROM, enabling Flash-like programming of application code for development and low volume applications. Furthermore the device features 4 kbyte ROM for device firmware and DSSP algorithm. A dedicated ROM version for high volume applications is available.

The device is powered by an external, single-cell battery and offers programmable low battery detection. The lifetime of the battery can be extended by use of the power down mode, which minimizes the quiescent current, and a 3D-LF interface, which enables on demand wake-up. An independent interval timer provides a programmable, periodic wake-up from power down mode.

P2SC: PCH7970 (737x, ROM)



RISC controller

The 8-bit RISC (MRKII) controller at the heart of the PCH7970 features a single level interrupt architecture and low power consumption, operating at 400 µA and drawing currents of 30 µA and 200 nA in idle and power down modes. The controller is optimized for serial data processing, with instruction execution times as fast as 0.5 µs. Timing is governed by an on-chip, low tolerance RC oscillator with a programmable system clock capable of speeds up to 2 MHz.

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