The LPC800 series offers a range of low-power, space efficient, low-pin-count options for a variety of applications including: sensor gateways, IoT end nodes, human machine interface (HMI) and communications interface for wireless protocols. Unique to the LPC800 series is a switch matrix and patent-pending SCTimer/PWM, giving embedded developers unprecedented design flexibility.

KEY FEATURES

- ARM® Cortex-M0+™ processor
  - Up to 30 MHz
  - Backward compatibility to the Cortex-M0™
  - Upwards compatibility with Cortex-M3™ and Cortex-M4™
  - Nested Vectored Interrupt Controller (NVIC)
  - Serial Wire Debug (SWD) and JTAG boundary scan modes
  - Micro Trace Buffer (MTB)
  - Single Cycle Access to all port pins

- Memories:
  - Up to 32 kB Flash (with 64 Byte page size)
  - Up to 8 kB SRAM

- 4 Serial Peripherals
  - Three USART interfaces
  - Two SPI controllers
  - Up to 4 I2C

- Timers
  - Multiple-channel multi-rate timer (MRT)
  - State Configurable Timer (SCT)
  - Self Wake-up Timer (WKT) clocked from either the IRC or a low-power clock source
  - Windowed Watchdog timer (WWDT)
  - System tick timer

- Analog peripherals
  - 12-bit, 12 channel ADC with sample rates of up to 1.2 Msps (LPC82x only)
  - Comparator with external voltage reference

- Digital Peripherals
  - Switch matrix for flexible configuration of each I/O pin function
  - Up to 29 General-Purpose I/O (GPIO) pins
  - GPIO interrupt generation capability with boolean pattern-matching capability
  - DMA with 18 channels and 9 trigger points
  - Digital glitch filter with programmable time constant
  - CRC engine

- Clock Generation Unit
  - 12 MHz internal RC oscillator trimmed to 1% accuracy
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz
  - Programmable watchdog oscillator
  - 10 kHz low-power oscillator for the WKT.
  - PLL allows max CPU rate without a high-frequency crystal.

- ROM API Support
  - Boot loader
  - On chip ROM APIs for ADC, SPI, I2C, USART, power configuration (power profiles) and integer divide
  - Flash In-Application Programming (IAP) and In-System Programing (ISP)
The LPC800 series is extremely power-efficient and straightforward to use. Based on an ultra-low-power 30-MHz ARM® Cortex-M0+ processor, the LPC800 is fully compatible with the Cortex-M architecture and instruction set. The Cortex-M0+ handles 32-bit data more efficiently than an 8-bit processor by requiring less code, memory and 30% less dynamic power from the Cortex-M0+ processor. At the same time, it easily outperforms 8-bit and 16-bit MCUs. The LPC800 includes two innovative features controlled via GUI-based configuration tools. A new flexible switch matrix enables designers to assign on-chip peripherals to any pin, giving the LPC800 enormous flexibility without adding complexity. The State Configurable Timer (SCT) combines a powerful 32-bit timer — or two 16-bit timers — with a configurable state machine. In the LPC800, the SCT implements virtually any timing or PWM function found on popular 8-bit MCUs. The LPC800 is available in a range of low-pin-count packages, including SO20, TSSOP20, TSSOP16, XSON16, and HVQFN.

DEVELOPMENT TOOLS
LPCXpresso, the full-featured, easy-to-use Eclipse-based software development tool, supports the complete product design cycle for the LPC800. The LPC800 is also fully supported by the Keil-MDK by ARM, the Embedded Workbench from IAR Systems, as well as other third party development tools. Additional support, free tools, and sample code are available on the web at www.lpcware.com. For further information on LPCXpresso, visit www.nxp.com/lpcxpresso. The order code for this development board is OM13071 and is available from authorized distributors.

ORDERING INFORMATION

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