PN533

Near Field Communication (NFC) controller

Rev. 3.2 — 2 February 2012
158232

Product short data sheet
PUBLIC

1. General description

The PN533 is a highly integrated transceiver module for contactless communication at 13.56 MHz based on the 80C51 microcontroller core. A dedicated ROM code is implemented to handle different RF protocols.

1.1 RF protocols

The PN533 supports four main operating modes:

- ISO/IEC 14443A Reader/Writer (including MIFARE product family)
- ISO/IEC 14443B Reader/Writer
- FeliCa Reader/Writer
- ISO/IEC 18092, ECMA 340 Peer-to-Peer

The PN533 hardware implements a demodulator and decoder for signals from ISO/IEC 14443A compatible cards and transponders. The PN533 hardware handles the complete ISO/IEC 14443A framing and error detection and upper layers of this protocol (i.e. ISO/IEC 14443-4) are implemented in firmware.

The PN533 supports all MIFARE products (e.g. MIFARE crypto method). It supports contactless communication using higher transfer speeds up to 848 kbit/s in both directions.

The PN533 hardware supports layers 2 and 3 of the ISO/IEC 14443B Reader/Writer communication scheme, except anticollision. Anticollision is implemented in firmware as well as upper layers (i.e. ISO/IEC 14443-4).

The PN533 can demodulate and decode FeliCa coded signals. The PN533 handles the FeliCa framing and error detection. It supports contactless communication using FeliCa Higher transfer speeds up to 424 kbit/s in both directions.

Compliant to ECMA 340 and ISO/IEC 18092 NFCIP-1 Passive and Active communication modes, the PN5331B3HN/C270 offers the possibility to communicate to another NFCIP-1 compliant device, at transfer speeds up to 424 kbit/s. The PN533 handles the complete NFCIP-1 framing and error detection.

1.2 Interfaces

The PN533 supports USB 2.0 full speed interface (bus powered or host powered mode). PN533 also has a master I^2C interface enabling the drive of following peripherals:

- An external EEPROM
- A TDA8029 smart card reader

1.3 Standards compliancy

PN533 offers commands in order for applications to be compliant in reader mode with “Paypass-ISO/IEC 14443 Implementation v1.1”.

PN533 supports RF protocols ISO/IEC 14443A and B such as compliancy with Smart eID standard can be achieved at application level.

A dedicated command is implemented in PN533 firmware to support NFC secure applications in accordance with “NFC sec Security layer for NFC” specification in order to enable USB wireless or BT enabler applications in a host baseband.

2. Features and benefits

- 80C51 microcontroller core with 45056 bytes ROM and 1224 bytes RAM
- Highly integrated demodulator and decoder
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF level detector
- Integrated data mode detector
- Supports ISO/IEC 14443A Reader/Writer mode up to 848 kbit/s
- Supports ISO/IEC 14443B Reader/Writer mode up to 848 kbit/s
- Supports MIFARE encryption in Reader/Writer mode and higher transfer speed communication at 212 kbit/s, 424 kbit/s and 848kbit/s
- Supports contactless communication according to the FeliCa protocol at 212 kbit/s and 424 kbit/s
- Typical operating distance in Reader/Writer mode for communication to ISO/IEC 14443A/MIFARE, ISO/IEC 14443B or FeliCa cards up to 50 mm depending on antenna size and tuning
- Support NFCIP-1 mode up to 424 kbit/s
- Typical operating distance in NFCIP-1 mode up to 50 mm depending on antenna size, tuning and power supply
- Supported USB 2.0 full speed interface
- Restricted I^2C master interface to control an external I^2C EEPROM or TDA8029 smart card reader
- Low-power modes
  - Hard-Power-Down mode
  - Soft-Power-Down mode
- 27.12 MHz Crystal oscillator
- On-Chip PLL to generate internally 96 MHz for the USB interface
- Power modes
  - USB bus power mode
  - 2.5 V to 3.6 V power supply operating range in non-USB bus power mode
- Dedicated IO ports for external device control

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BUS}	bus supply voltage			4.02	5	5.25	V
		(non-USB mode); $V_{BUS} = V_{DDD}$; $V_{SSD} = 0$ V		2.5	3.3	3.6	V
V_{DDA}	analog supply voltage	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1]	2.5	3.3	3.6	V
V_{DDD}	digital supply voltage		[1]	2.5	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage		[1]	2.5	3.3	3.6	V
$V_{DD(PVDD)}$	PVDD supply voltage			1.6	-	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V; reserved for future use		V_{DDD} −0.1	-	V_{DDD}	V
I_{BUS}	bus supply current	maximum load current (USB mode); measured on V_{BUS}				150	mA
		maximum inrush current limitation; at power-up (curlimoff = 0)				100	mA
I_{pd}	power-down current	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)} = 3$ V; not powered from USB					
		hard power-down; RF level detector off				10	µA
		soft power-down; RF level detector on				30	µA
I_{CCSL}	suspended low-power device supply current	RF level detector on, (without resistor on DP/DM)	[1]	-	-	250	µA
I_{DDD}	digital supply current	RF level detector on, $V_{DD(SVDD)}$ switch off	[1]	-	15	-	mA
$I_{DD(SVDD)}$	SVDD supply current	$V_{DDS} = 3$ V		-	-	30	mA
I_{DDA}	analog supply current	RF level detector on		-	6	-	mA
$I_{DD(TVDD)}$	TVDD supply current	during RF transmission; $V_{DD(TVDD)} = 3$ V		-	60	100	mA
P_{tot}	total power dissipation	$T_{amb} = -30$ °C to +85 °C		-	-	0.55	W
T_{amb}	ambient temperature			−30	-	+85	°C

[1] V_{DDD}, V_{DDA} and $V_{DD(TVDD)}$ must always be at the same supply voltage.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN5331B3HN/C270[1][2]	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm	SOT618-1

[1] 70 refers to the ROM code version described in User Manual.

[2] Refer to Section 9.4 “Licenses”

5. Block diagram

The following block diagram describes hardware blocks controlled by PN533 firmware or which can be accessible for data transaction by a host baseband.

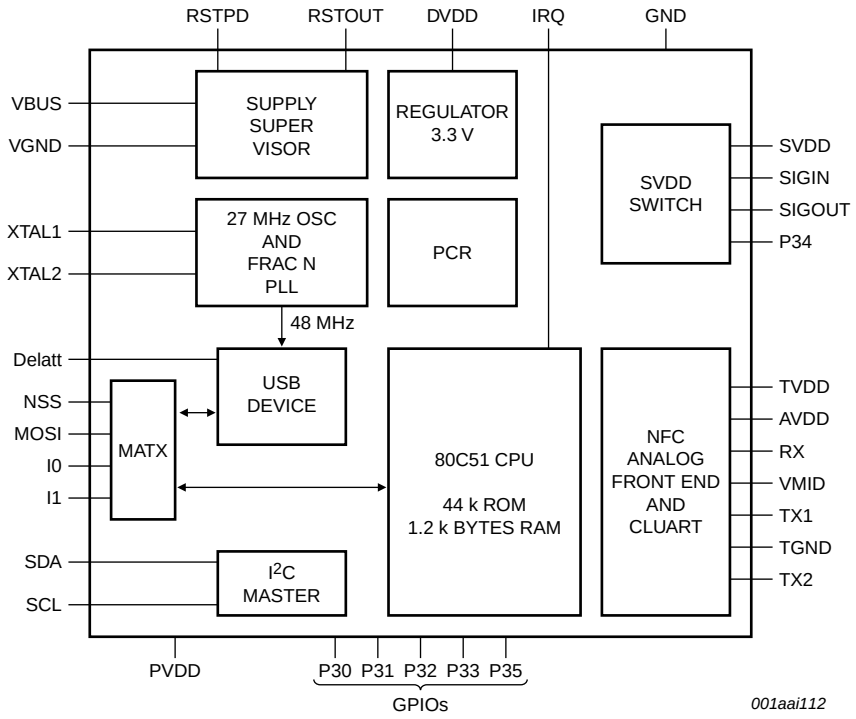

Fig 1. Block diagram

6. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDA}	analog supply voltage			–0.5	+4	V
V_{DDD}	digital supply voltage			–0.5	+4	V
$V_{DD(TVDD)}$	TVDD supply voltage			–0.5	+4	V
$V_{DD(PVDD)}$	PVDD supply voltage			–0.5	+4	V
$V_{DD(SVDD)}$	SVDD supply voltage			–0.5	+4	V
V_{BUS}	bus supply voltage			–0.5	+5.5	V
P_{tot}	total power dissipation			-	500	mW
$I_{DD(SVDD)}$	SVDD supply current	maximum current in V_{DDS} switch		-	30	mA
V_i	input voltage	TX1, TX2, RX pins		–0.5	+4	V
V_{ESD}	electrostatic discharge voltage	HBM	[1]		±2.0	kV
		MM	[2]	-	200	V
		CDM	[3]	-	±1	kV
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–40	+125	°C

[1] 1500 Ω, 100 pF; EIA/JESD22-A114-A

[2] 0.75 mH, 200 pF; EIA/JESD22-A115-A

[3] Field induced model; EIA/JESC22-C101-C

7. Abbreviations

Table 4. Abbreviations

Acronym	Description
CDM	Charge Device Model
CRC	Cyclic Redundancy Check
EEPROM	Electrically Erasable Programmable Read-Only Memory
HBM	Human Body Model
HPD	Hard Power Down
MM	Machine Model
NFC	Near Field Communication
SPD	Soft Power-Down Mode

8. Revision history

Table 5. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PN533_SDS v.3.2	20120202	Product short data sheet	-	PN5331B3HN_ SDS_N_1
Modifications:	• Section 1 “General description”: updated			
PN5331B3HN_SDS_N_1	20081231	Product short data sheet PUBLIC	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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RATP/Innovatron Technology

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