High PF, low output ripple, double stage led-driver SSL2109 design

Date: 10 June 2014

Status:

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<th>Design Idea</th>
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<th>Demo Board</th>
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See appendix for explanation

Keywords
Power Factor, THDi, ripple, Buck, LED, SSL2109, SSL5015, SSL5018

NXP device(s)
SSL2109AT

Description of Application
The application in this solution brief is an LED driver with double stage topology (one boost stage and one buck stage), while only one IC is used for the implementation. The application realizes high PF and low THDi, while low output current ripple can be realized.

Features and Specifications
- Typical operating (source) voltage: 230 V (AC)
- Typical LED current: 152 mA
- Excellent output current regulation
- Efficiency 84% - 87%
- Power Factor 0.95
- Output ripple 30% with 2.2 µF output capacitor
- Output ripple 5% with 47 µF output capacitor
- Input power 11.6 Watt, output power 10 Watt
- No mains dimming
- 34 external components
Component List

Table 1: component list

<table>
<thead>
<tr>
<th>Part ref.</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Package</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>C14</td>
<td>47 nF</td>
<td>Ycap 250 VAC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C15</td>
<td>10 nF</td>
<td>Ycap, 250 VAC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C16</td>
<td>33 nF</td>
<td></td>
<td>≥350 VDC</td>
<td></td>
</tr>
<tr>
<td>C17</td>
<td>100 pF</td>
<td>≥450 VDC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C21</td>
<td>2.2 µF or 47 µF</td>
<td></td>
<td>30% or 5% output current ripple</td>
<td></td>
</tr>
<tr>
<td>C22</td>
<td>4.4 µF</td>
<td>450 VDC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C18</td>
<td>100 nF</td>
<td>50 VDC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D11,D12,D13,D14,D19</td>
<td>1N4007</td>
<td>slow</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D15,D16,D17</td>
<td>GSD2004W-V</td>
<td>fast</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D18</td>
<td>6.2 V</td>
<td>¼ Watt</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L1</td>
<td>5.6 mH</td>
<td>Isat ≥ 0.2 A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L2</td>
<td>2.7 mH</td>
<td>Isat ≥ 0.4 A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L3</td>
<td>1.8 mH</td>
<td>Isat ≥ 0.4 A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q1</td>
<td>2N60</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q2A, Q3A</td>
<td>BC847B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R2</td>
<td>10 Ω</td>
<td>Fusible resistor</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R3, R4</td>
<td>10 kΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R5</td>
<td>100 Ω</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R6, R8</td>
<td>1.1 MΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R7</td>
<td>39 kΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R9</td>
<td>1 Ω</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R10</td>
<td>22 kΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R11</td>
<td>1.8 Ω</td>
<td>1% tolerance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R12</td>
<td>47 Ω</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>U3</td>
<td>SSL2109AT</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 2: Optional additional components (see figure 2)

<table>
<thead>
<tr>
<th>Part ref.</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Package</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>D21</td>
<td>75 V</td>
<td></td>
<td>¼ Watt</td>
<td></td>
</tr>
<tr>
<td>Q4</td>
<td>BT169D</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R13</td>
<td>10 kΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R14</td>
<td>33 Ω</td>
<td></td>
<td>1 Watt</td>
<td></td>
</tr>
</tbody>
</table>

Operation and Performance

In this application, the SSL2109AT is used in a double stage Boost - Buck topology instead of the designated Buck topology. There are two reasons why this is done:

- With a boost stage at the input side, the input capacitance of the system can keep at a minimum, allowing high power factor.
- With a buck stage at output side, the output ripple can be low due to the stable bus voltage supplied by the prior boost stage.

With this buck-boost application, only one switching FET is required to draw current through the Boost and through the Buck stage. The switching current of the boost stage, plus the switching current of the buck stage is flowing through the same switching FET. The IC senses the current through the sense resistor (R11) and switches off when the peak current is reached. The peak current through the sense resistor flows mainly through the output LEDs. The Boost current follows a different return path through R9 and only slightly effects the peak current through the sense resistor (R11), therefore the output current can be calculated similarly as an SSL2109AT Buck converter (formula 1; also see UM10482).
The input current waveform is shaped by the return current of the boost stage, therefore the power factor and THDi depend on the ratio between the Boost inductor (L2) and the Buck inductor (L3). Smaller ratio of Lboost/Lbuck will generally provide higher PF and lower THDi, but also higher bus voltage (i.e. the voltage on C22). In the realized application Lboost > Lbuck; otherwise the ripple voltage on the bus capacitor comes too close to its voltage rating of 450 V. Table 2 shows an example of these the Lboost/Lbuck dependencies.

### Table 2: Inductor ratio dependencies

<table>
<thead>
<tr>
<th>Lboost (mH)</th>
<th>Lbuck (mH)</th>
<th>PF</th>
<th>THDi (%)</th>
<th>Bus Voltage @ 230 VAC (VDC)</th>
<th>Class C compliant</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.7</td>
<td>1.8</td>
<td>0.95</td>
<td>32</td>
<td>400 typical</td>
<td>no</td>
</tr>
<tr>
<td>1.8</td>
<td>1.8</td>
<td>0.96</td>
<td>27</td>
<td>410 typical</td>
<td>yes</td>
</tr>
<tr>
<td>1.8</td>
<td>2.7</td>
<td>0.97</td>
<td>22</td>
<td>430 typical</td>
<td>yes</td>
</tr>
</tbody>
</table>

The output current ripple is mainly ripple at the switching frequency (~90 kHz). A small portion of the output ripple is low frequent ripple (2 * F_mains, i.e. 100 Hz). The magnitude of the output current ripple is mainly dependent on the output capacitance (C21) and the LED impedance. Ripple was measured at 30 % with an output capacitor of 2.2 μF. Lower output ripple, down to 5%, can be realized by implementing an output capacitor (C21) of ~47 μF; actual capacitor size depends on the LED impedance. The residual 5% current ripple is than mainly low frequent (100 Hz).

The voltage rating of the output capacitor can be limited to 100 V, but some extra components (figure 2; D21, Q4, R13, R14) are then recommended in order to protect the output capacitor for potential high voltages. The circuit provides low impedance in case the output voltage exceeds the zener voltage of D21. The IC is able to detect this as a short at the output, and will then go in output short protection (latched protection).

**Additional protections** are embedded for input over voltage protection (R8, R6, R7, R10, D18, Q2A) and over current protection for the Boost stage (R9, Q3A). The input over voltage protection turns off the IC when too high bus voltage is on C22. The input over voltage protection pulls the VCC voltage down in case the bus voltage exceeds a limit. The limit can be tuned with the ratio between R8, R6 and R7. It is essential that the limit is tuned below the maximum voltage rating of the bus capacitor (C22). The protection will restart automatically when the input voltage is reduced.

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**Formula 1**

\[
I_{\text{out}} = \frac{1}{2} I_{\text{peak}} \frac{t_{\text{ch}} + t_{\text{dch}}}{t_{\text{ch}} + t_{\text{dch}} + t_{\text{ring}}} \approx \frac{0.26}{R_{\text{sense}}}
\]

**Fig 2: Over voltage protection circuit diagram**
The over current protection for the Boost stage (R9, Q3A) pulls down the VCC voltage in case the Boost peak current exceeds $V_{th}/R9$, where $V_{th}$ is the threshold voltage of Q3A. This circuit is not active under typical conditions, but the circuit is recommended since the IC will not be able to detect too high peak currents of the Boost stage in this topology.

**Literature**
- SSL2109T / SSL2109AT; NXP datasheet
- AN10876; NXP Application Note
- AN11041; NXP Application Note
- AN11136; NXP Application Note
- UM10482; User Manual of a buck converter based on SSL21081
# Appendix

<table>
<thead>
<tr>
<th>Status</th>
<th>Description</th>
</tr>
</thead>
</table>
| Design Idea          | • Principle application design  
                       • Based upon native behavior of the constituting components and the elementary interactions  
                       • No or only coarse dimensioning of components  
                       • Not implemented and tested  |
| Design Concept       | • Principle application design  
                       • Based upon building blocks that are known to operate correctly and that are known to interact without conflicts  
                       • At least coarse dimensioning of components  
                       • All individual building blocks were individually implemented and tested but not in the presented configuration |
| Design Prototype     | • Full implementation of an application principle  
                       • Implemented on a breadboard or prototype PCB  
                       • (Basic) operation verified and evaluated  
                       • Proper dimensioning of components, but not optimized  
                       • (Limited) operational performance data available |
| Demo Board Design    | • Full implementation of an application  
                       • Implemented on a PCB  
                       • Operation and performance under typical conditions verified  
                       • Optimal component dimensioning for typical operation  
                       • The demo board is intended for evaluation and offers the possibility to experiment with various implementation options; the demo board can be a versatile starting point for developing an end-application  
                       • The design and the PCB are not meant as a blueprint for an end-application or mass production |
| Reference Design     | • Full implementation of an application  
                       • Implemented on a PCB that conforms to the requirements in the specific application segment (form factor, UL requirements, manufacturability, etc.)  
                       • Operation and performance under all required conditions verified  
                       • Optimal component dimensioning for operation under all required conditions  
                       • Full documentation (User Manual) available  
                       • The design and the PCB can be used as a blueprint for an end-application or mass production |
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