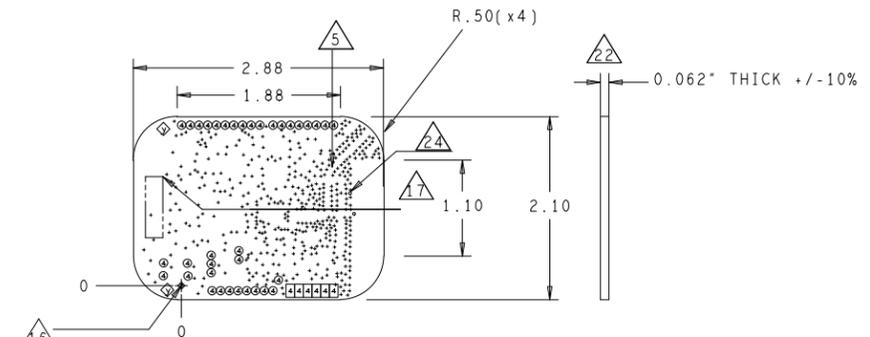


NOTES (UNLESS OTHERWISE SPECIFIED):

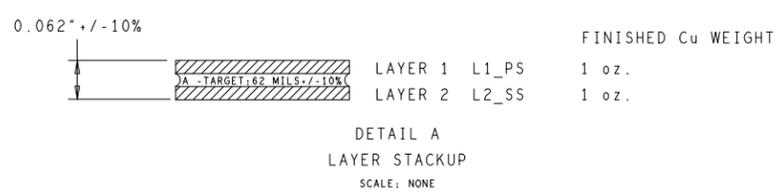
1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).
2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98 Dk MUST MEET THE FOLLOWING CRITERIA $4.0 < Dk < 4.5$
Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
5. CHARACTERISTIC IMPEDANCE - TRACES WITH 0.030" WIDTH SHALL BE 50 OHM SINGLE ENDED
5.a THE TRACES INDICATED IN DETAIL 'B' WITH AN ARROW ARE CRITICAL DIMENSIONS AND SHALL MEET 30 +/- 1% MILS WIDE, GAP SHALL MEET 5 +/- 1% MILS.
6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .008"/.005"
7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
.05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER
2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL.
8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.
9. SOLDERMASK - GREEN COLOR(TAIYO OR EQUIVALENT). BOTH SIDES.
MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM FREESCALE.
10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.
11. ELECTRICAL TEST - 100% IPCD356.
12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS.
UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.
14. TEARDROPS MAYBE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
15. 2 SOLDER SAMPLES TO BE PROVIDED.
16. BASIC GRID INCREMENT AT 1:1 IS .0001.
17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
- MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (P6)
19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)
20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP.
ALL HOLE LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM.
21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS.
THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER.PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.
22. OVERALL PCB DIELECTRIC THICKNESS ARE TARGETED (A) 62MILS +/- 10% AS SHOWN IN DETAIL 'A'
23. COMPONENTS C1 AND C4 SHARE PINS
24. THIS LINE ON TOP LAYER (X= 1943, Y = 1054) IS INTENDED TO BE CONNECTED TO RF_ANTENNA NET AND GND
25. INTENTIONAL SHORTS AT:
SH1 RTS & RTS_b_XCVR
SH2 IRO & IRO_B
SH3 SS & SPI:SS
SH4 MOSI & SPI:MOSI
SH5 MISO & SPI:MISO
SH6 CLK & SPI:CLK
SH7 Rx_SW & RX_SWITCH
J6 VCC_3V3 & P3V3_IC
SH8 A3 & RGB_BLUE
SH9 A4 & RGB_GREEN
SH10 A5 & RGB_RED

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	X1	ORIGINAL RELEASE	07-22-14	A.O
	X2	IC TRANSLATORS	07-28-14	A.O
	X3	BOM UPDATE, SHIELD UPDATE	08-01-14	A.O
	A	PRODUCTION RELEASE	09-01-14	A.O
	B	RGB DRIVEN BY EXTERNAL MCU	11-18-14	A.O

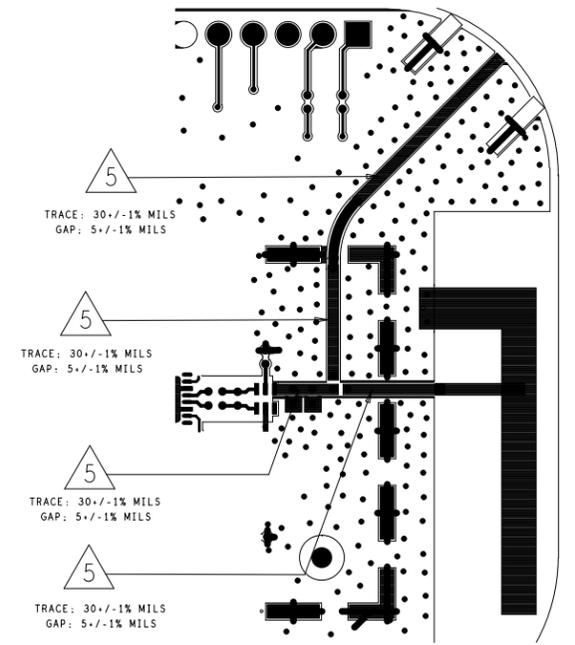
DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	8.0	+0.0/-8.0	PLATED	438
•	8.0	+2.0/-2.0	PLATED	20
•	12.0	+2.0/-2.0	PLATED	2
⊙	40.0	+3.0/-3.0	PLATED	36
⊠	41.0	+3.0/-3.0	PLATED	6
◆	25.0	+2.0/-2.0	NON-PLATED	1
◇	125.0	+2.0/-2.0	NON-PLATED	2



PRIMARY DATUM
GRID ORIGIN



DETAIL B
IMPEDANCE REQUIREMENTS
IMPEDANCE 50 OHMS



PART NO. 170-28535		FREESCALE SEMICONDUCTOR	
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO FREESCALE AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF FREESCALE.		6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA	
TOLERANCES ARE: DECIMALS .XX .01 ANGLES D-30° XXX .005 RMS ALL MACHINED SURFACES BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS. UNDERLINED DIM. NOT TO SCALE. THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.		TITLE: PRINTED WIRING BOARD X-FRDM-MCR20A	
APPROVALS DRAWN ANTONIO QUIROZ CHECKED ALFREDO ALVAREZ DESIGN ENGINEER ANTONIO QUIROZ	DATE 11-18-14 11-18-14 11-18-14	SIZE D	CAD FILE NAME LAY-28535
SCALE 1/1		DO NOT SCALE DRAWING	DWG. NO. FAB-28535
SHEET 1 OF 1		REV B	