NSB3640 Ver:70AX COVER SHEET

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Revisions

Rev	Description	Date	Approved
XA	**LS2085A-RDB (PROTOTYPE)**	2014/07/25	**Teck Chin,**
XB	**LS2085A-RDB**	2014/11/28	
XC	**LS2085A-RDB**	2014/12/26	
XD	**LS2085A-RDB**	2015/02/02	
XE	**LS2085A-RDB**	2015/03/24	
XF	**LS2085A-RDB**	2016/10/28	

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Title: **Cover Sheet**

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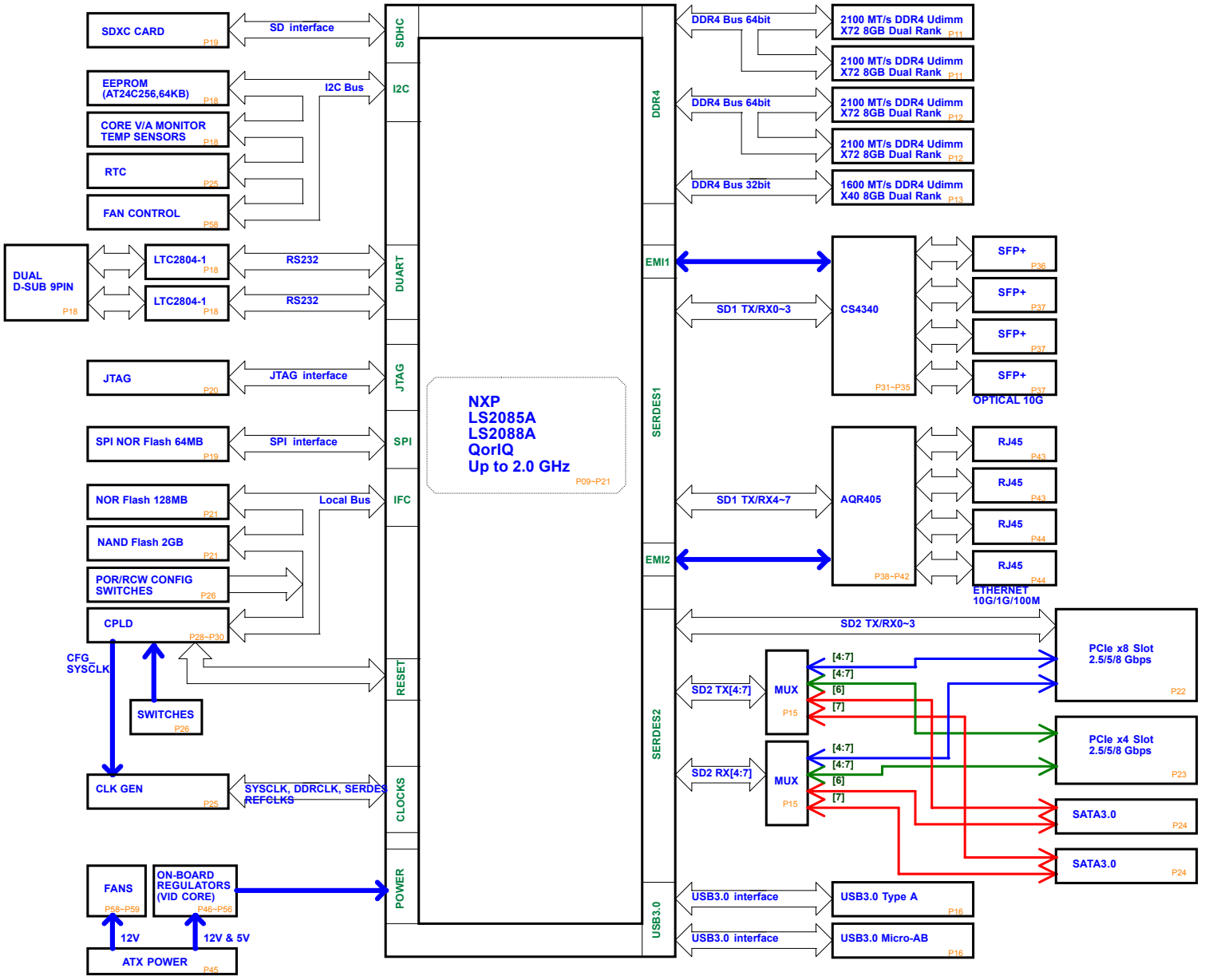
Block Diagram



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Block Diagram		
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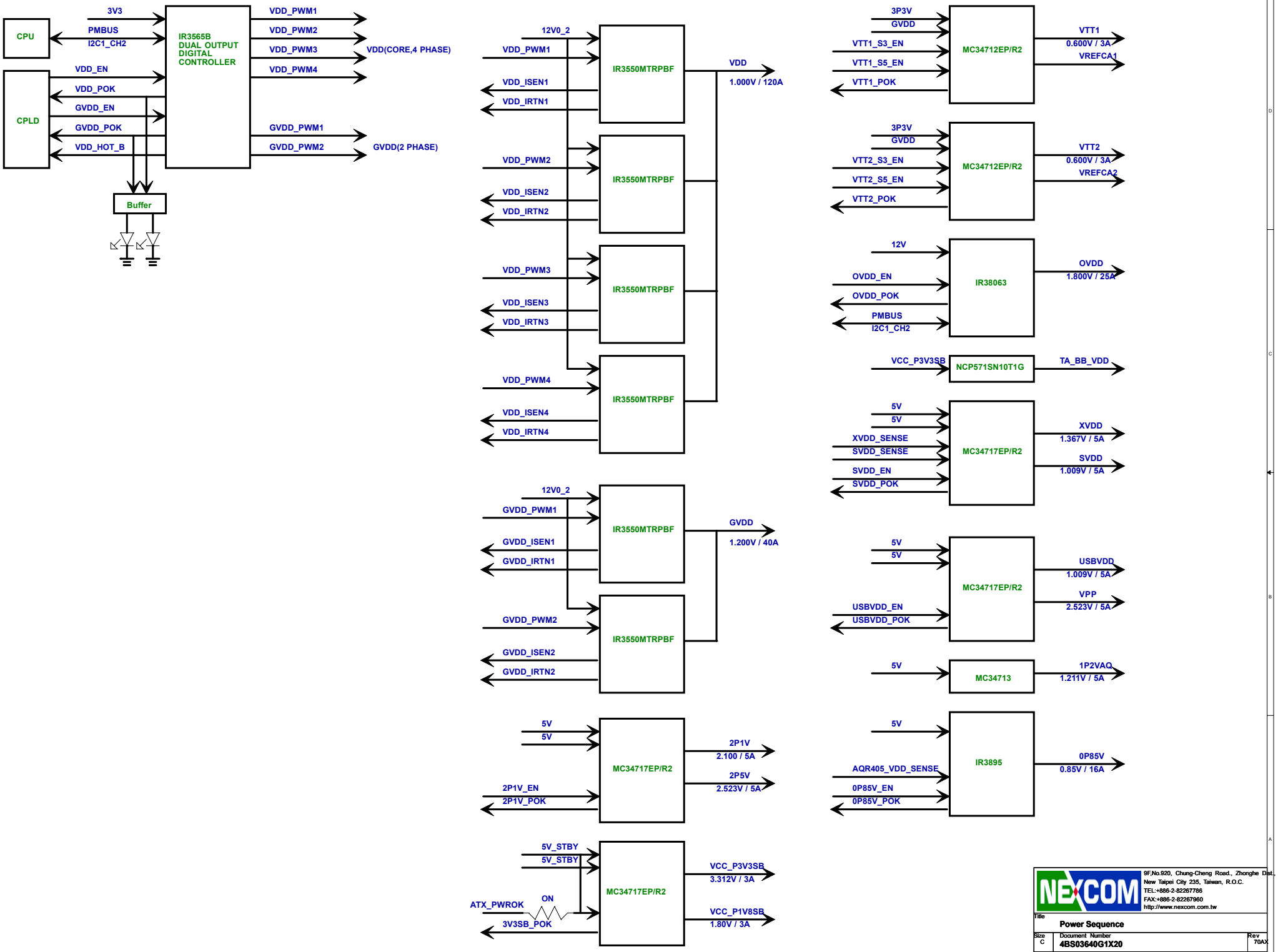

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Title: **Power Sequence**

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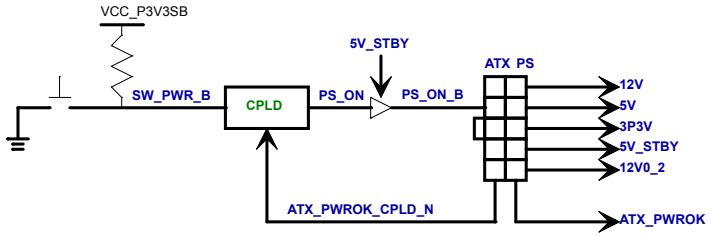
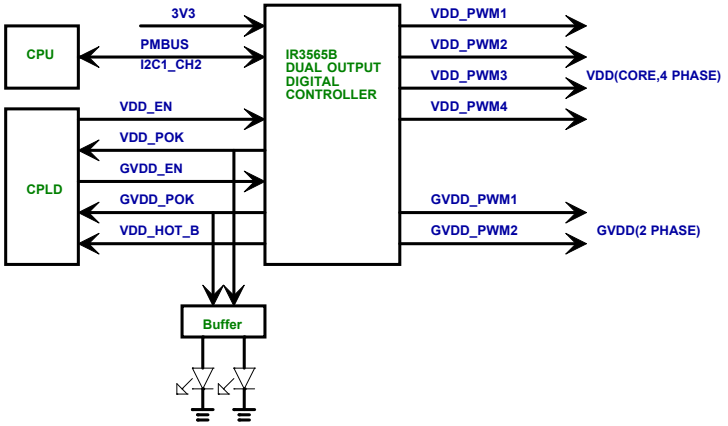
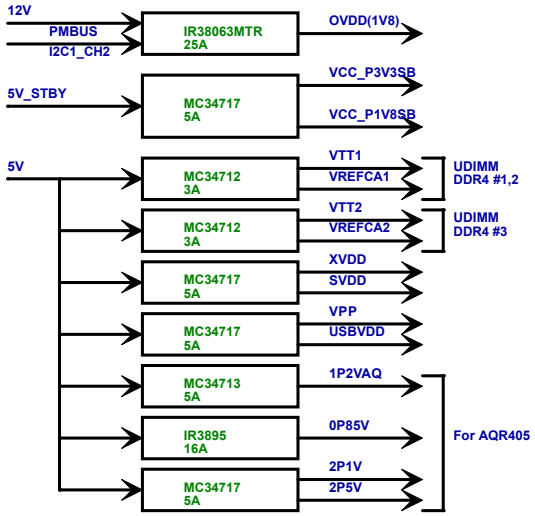
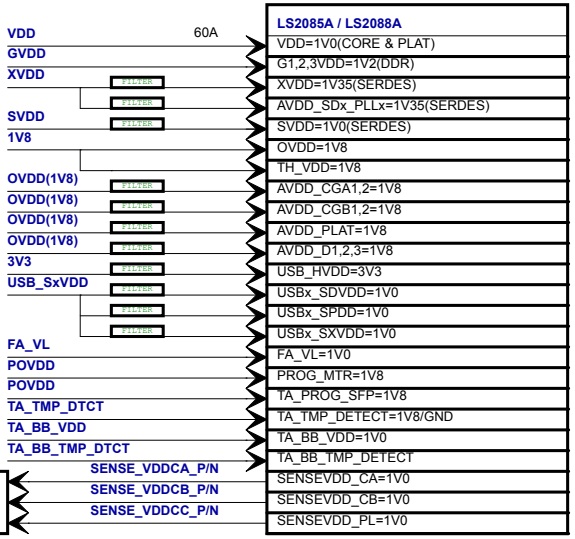
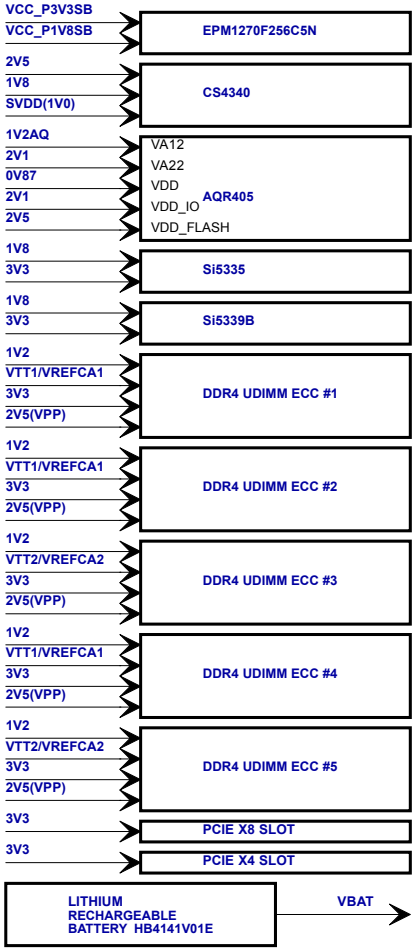
Power Delivery

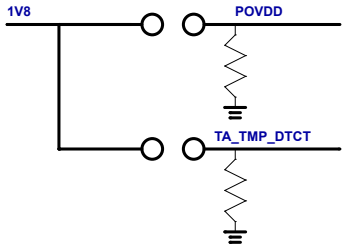


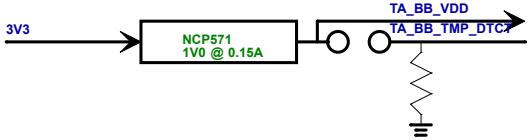


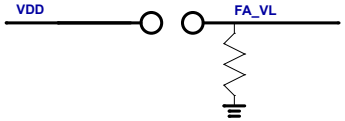












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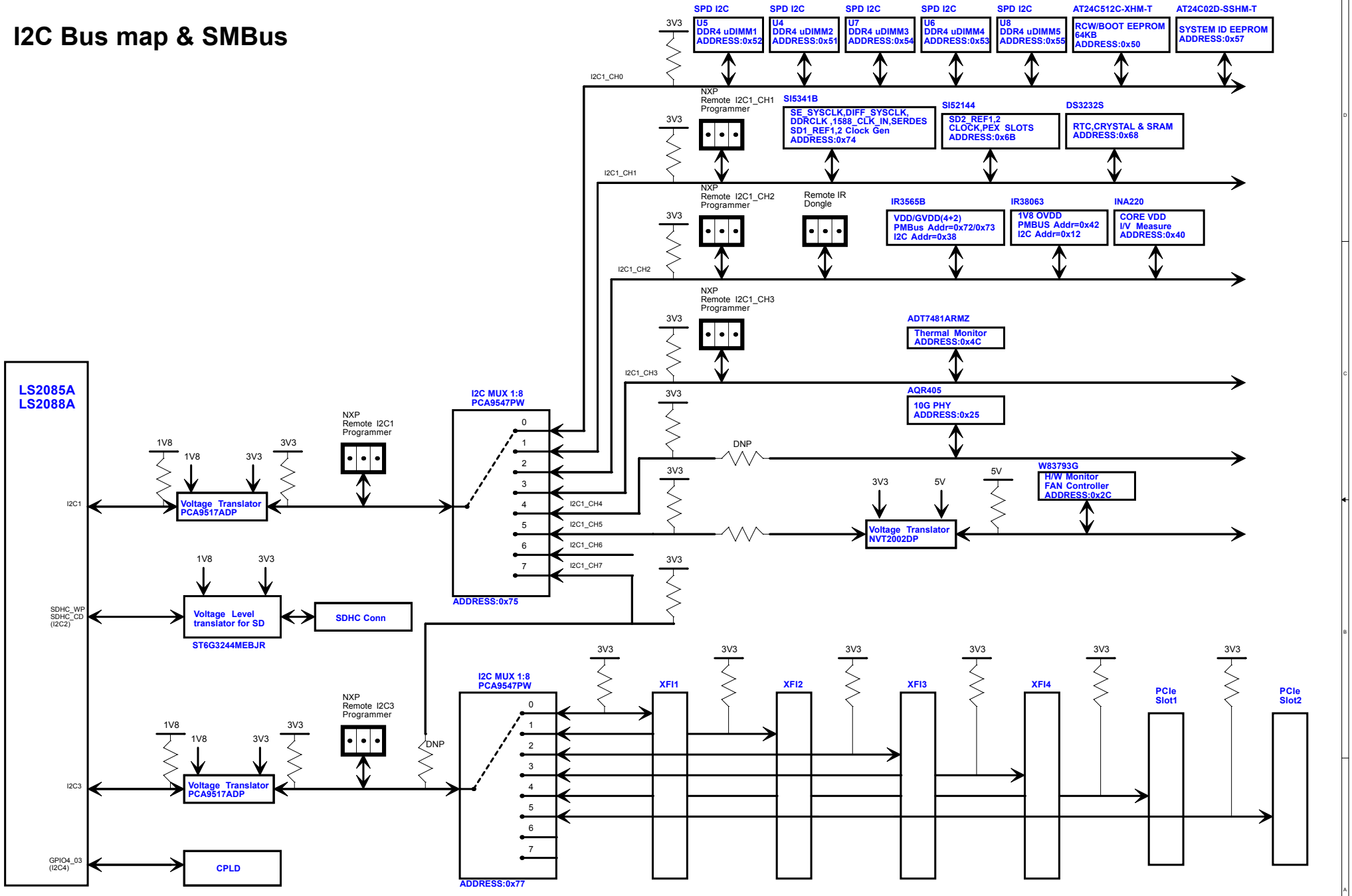
I2C Bus map & SMBus



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Title	I2C Bus map & SMBus	
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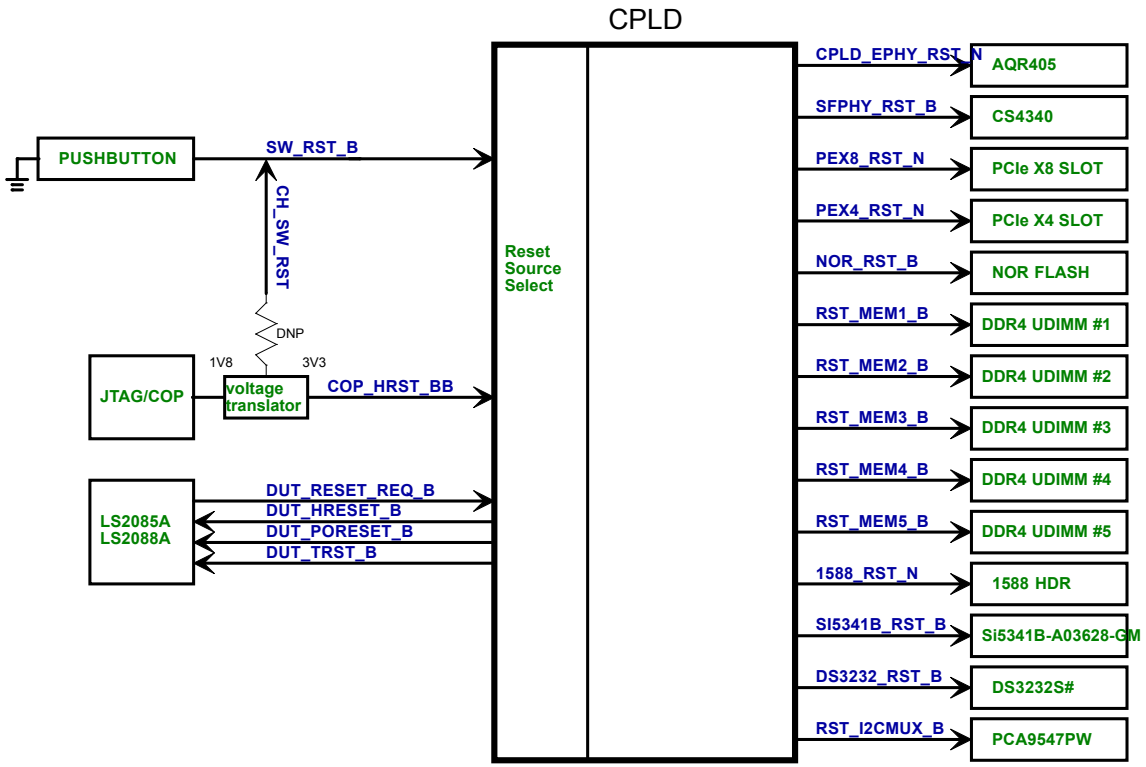
RESET Map



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RESET Map		
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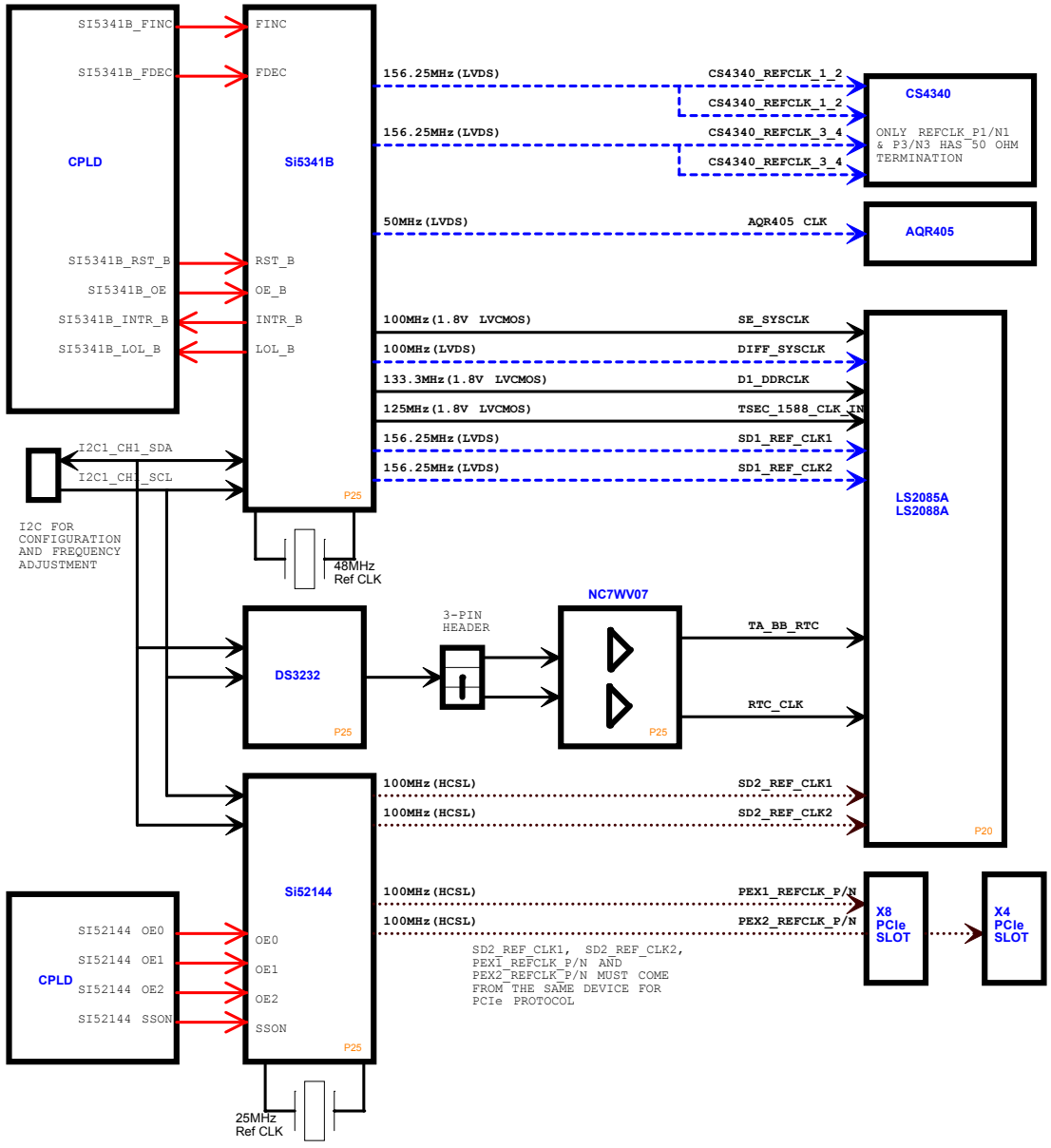
Clock map

SI5341B-A03628-GM OUTPUTS ARE:
CS4340 REFCLK 1/2 & 3/4 = 156.25 MHZ LVDS
SD1_REF_CLK1 = 156.25 MHZ LVDS
SD1_REF_CLK2 = 156.25 MHZ LVDS
TSEC_1588_CLK = 125 MHZ 1.8V LVCMOS
AQR405 CLK = 50 MHZ LVDS
DIFF_SYSCLK = 100 MHZ LVDS
SE_SYSCLK = 100 MHZ 1.8V LVCMOS
USBCLKIN = 24 MHZ 1.8V LVCMOS
DDRCLK = 133.3333 MHZ 1.8V LVCMOS



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Clock map			
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Memory sub system	
DDR5	DDR4 Slot X 5 UDIMM
NOR flash	128MB, 16-bit width
NAND flash	2GB, 8-bit width,Page size(2048 + 64 bytes)
SATA	SATA3.0 CONNECTOR X2
SD	SDXC Card socket X 1
Serial Proms	RCW/Boot EEPROM 64KB System ID EEPROM 256B
eMMC	NO

Networking sub system	
10G PHY	4 PORT SFP+
10G PHY	4 PORT RJ45

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Title: **Mem & Net sub system**

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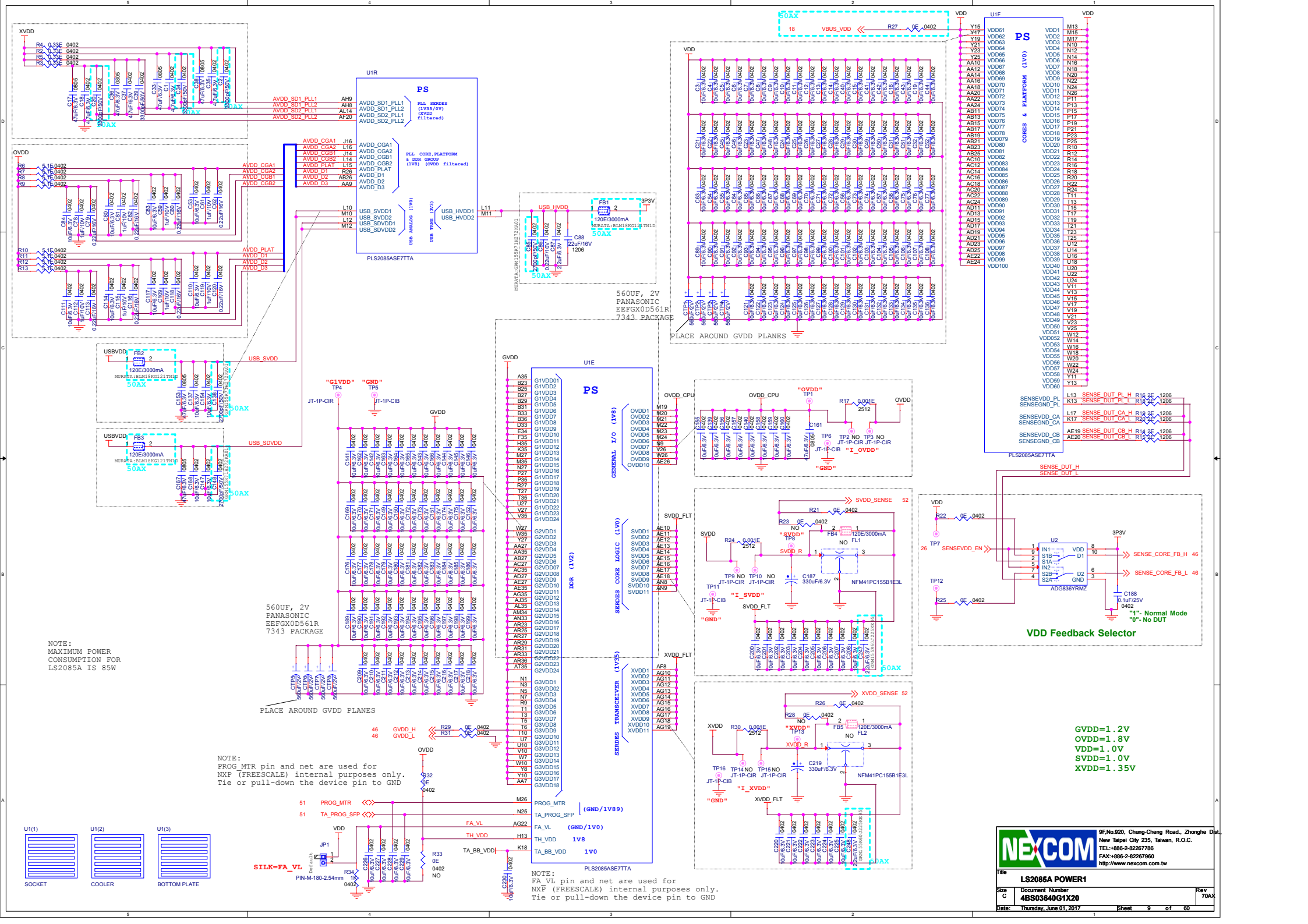

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Title	LS2085A POWER1		
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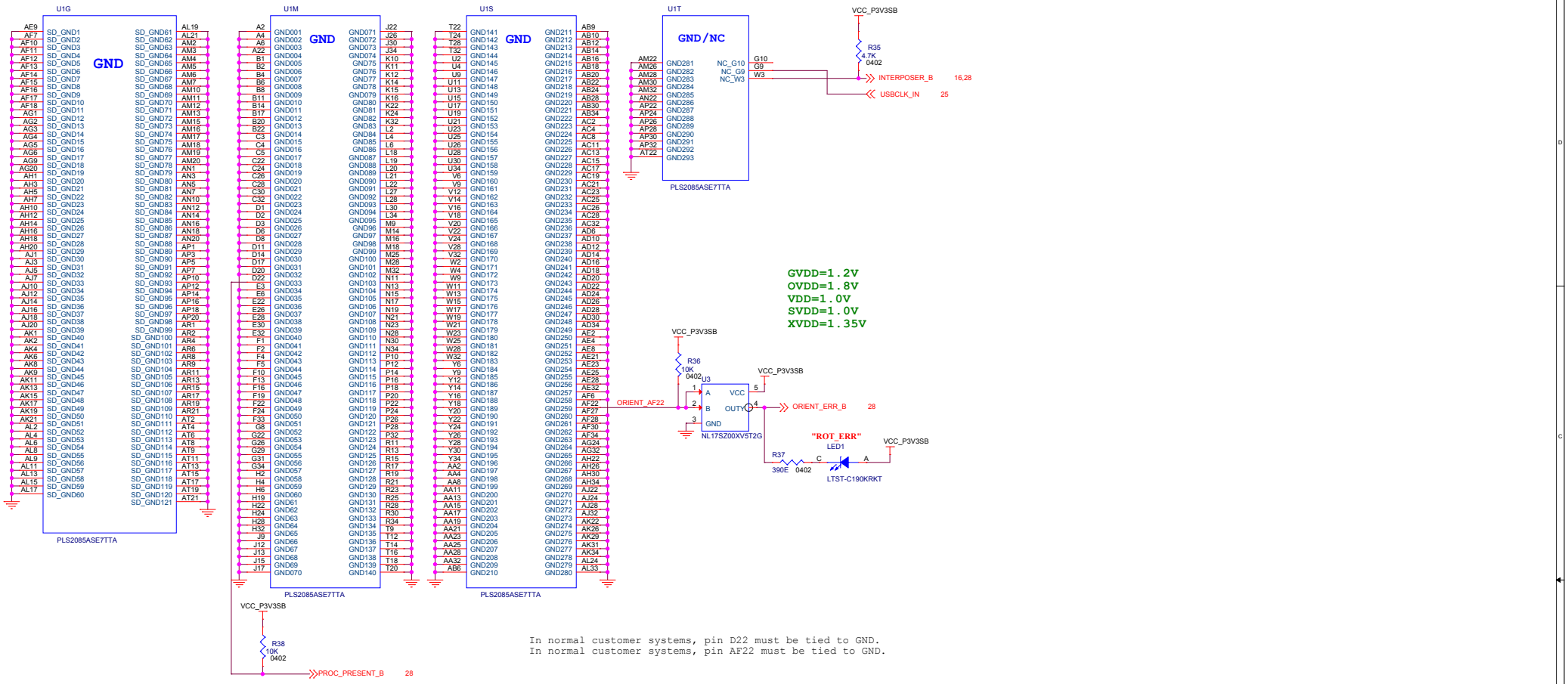

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Title	LS2085A POWER2	
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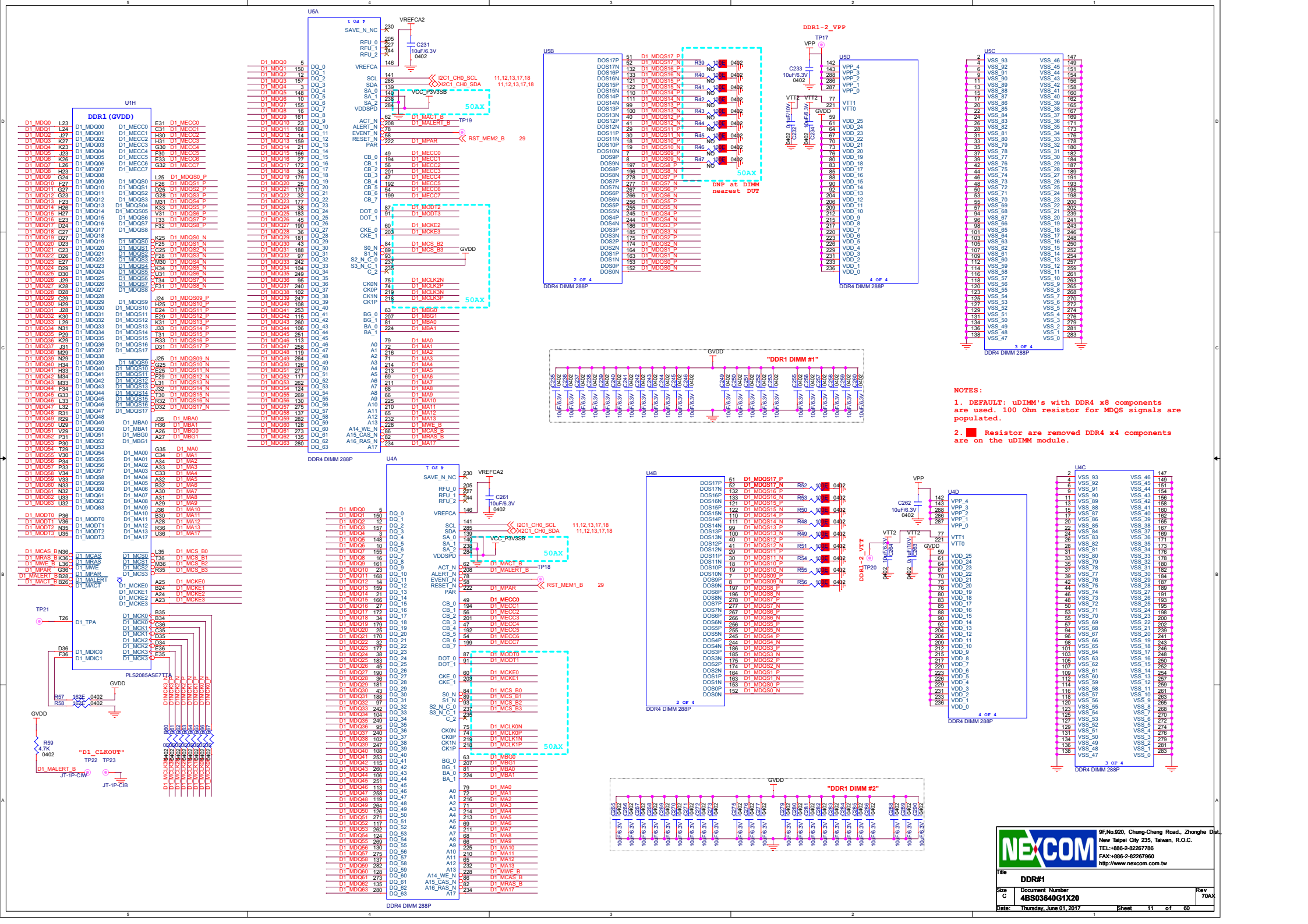
U1H
DDR1 (GVDD)
PLS2085ASE7T1A
U5A
U5B
U5C
U5D
U4A
U4B
U4C
U4D
DDR4 DIMM 288P
"DDR1 DIMM #1"
"DDR1 DIMM #2"
DDR1-2_VPP
DDR1-2_VTT
"D1_CLKOUT"
JT-1P-CIW
JT-1P-CIB
50AX
DNP at DIMM nearest DUT
NOTES:
1. DEFAULT: uDIMM's with DDR4 x8 components are used. 100 Ohm resistor for MDQS signals are populated.
2. Resistor are removed DDR4 x4 components are on the uDIMM module.
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DDR#1
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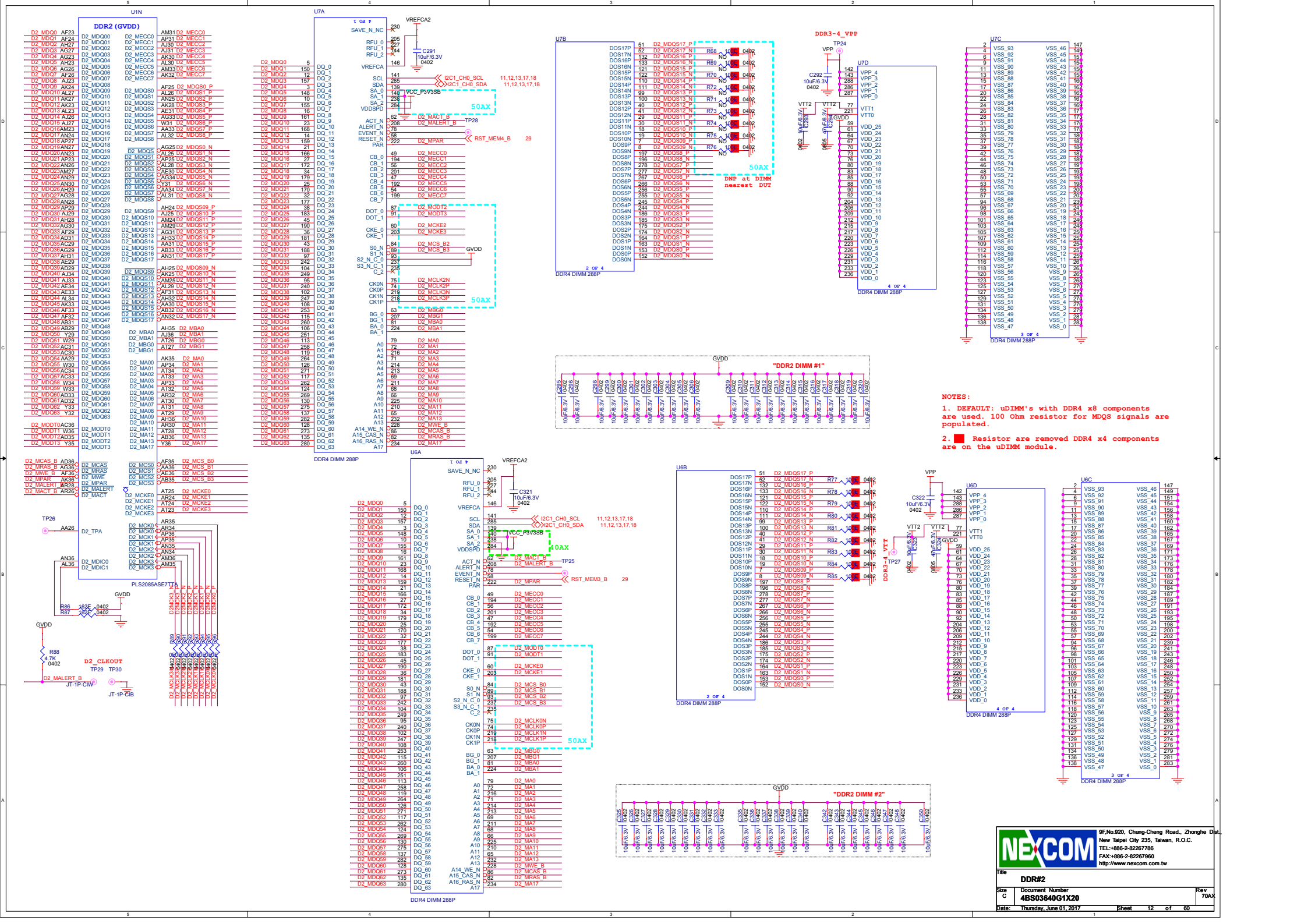

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Title	DDR#2		
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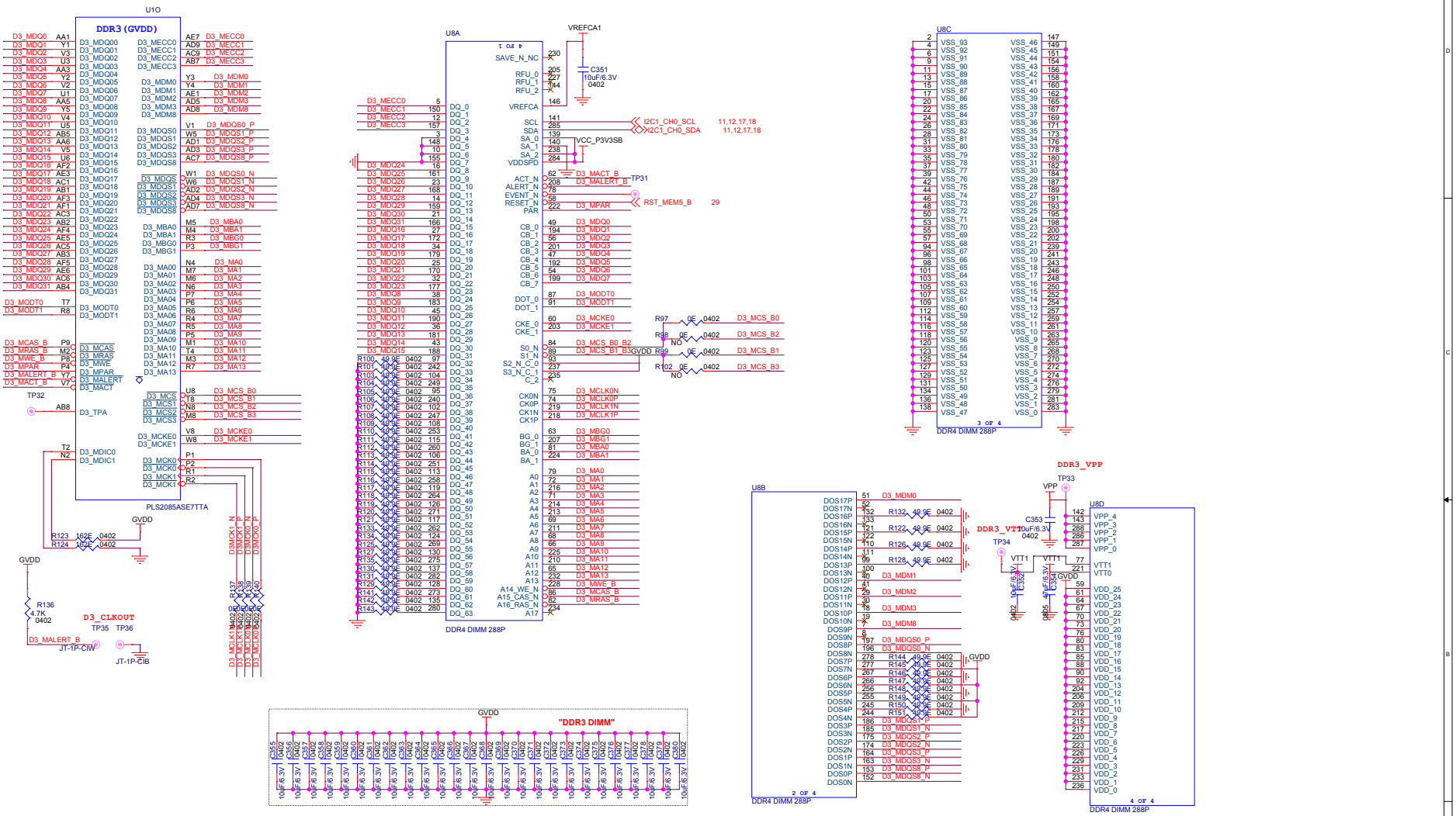
U1O
DDR3 (GVDD)
PLS2085ASE7TTA
U8A
DDR4 DIMM 288P
U8C
U8B
U8D
DDR3_VPP
DDR3_VTT
"DDR3 DIMM"
D3_CLKOUT
In order optimize layout following routing used:
- Byte ECC -> Byte0
- Byte3 -> Byte1
- Byte2 -> Byte2
- Byte1 -> Byte3
- Byte0 -> Byte ECC
GVDD=1.2V
OVDD=1.8V
VDD=1.0V
SVDD=1.0V
XVDD=1.35V
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Title
DDR#3
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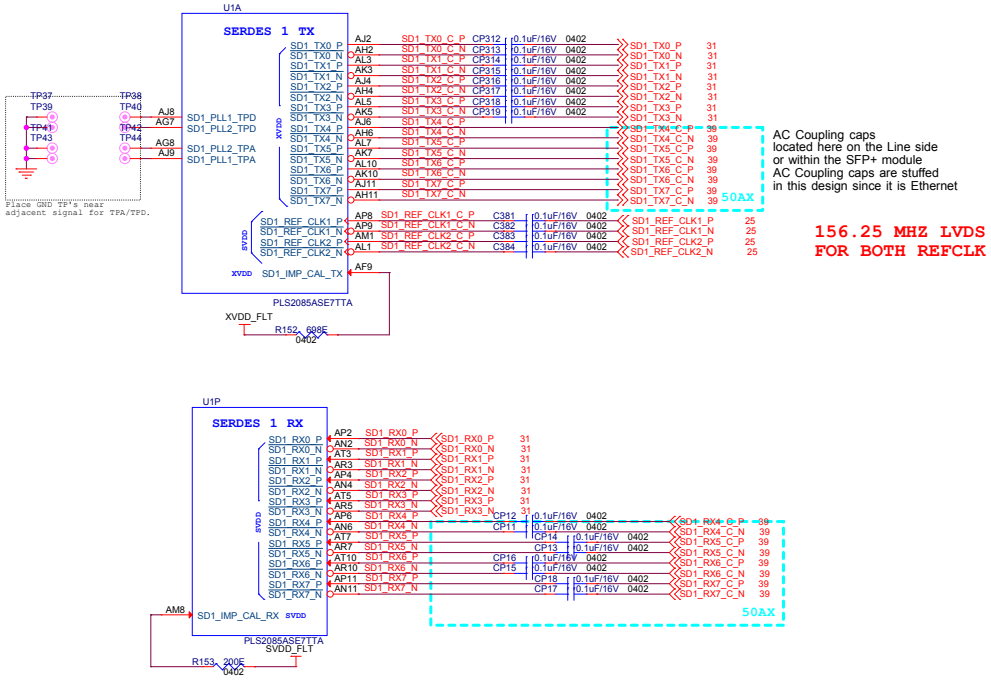

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Title	SERDES 1_RX_MUX	
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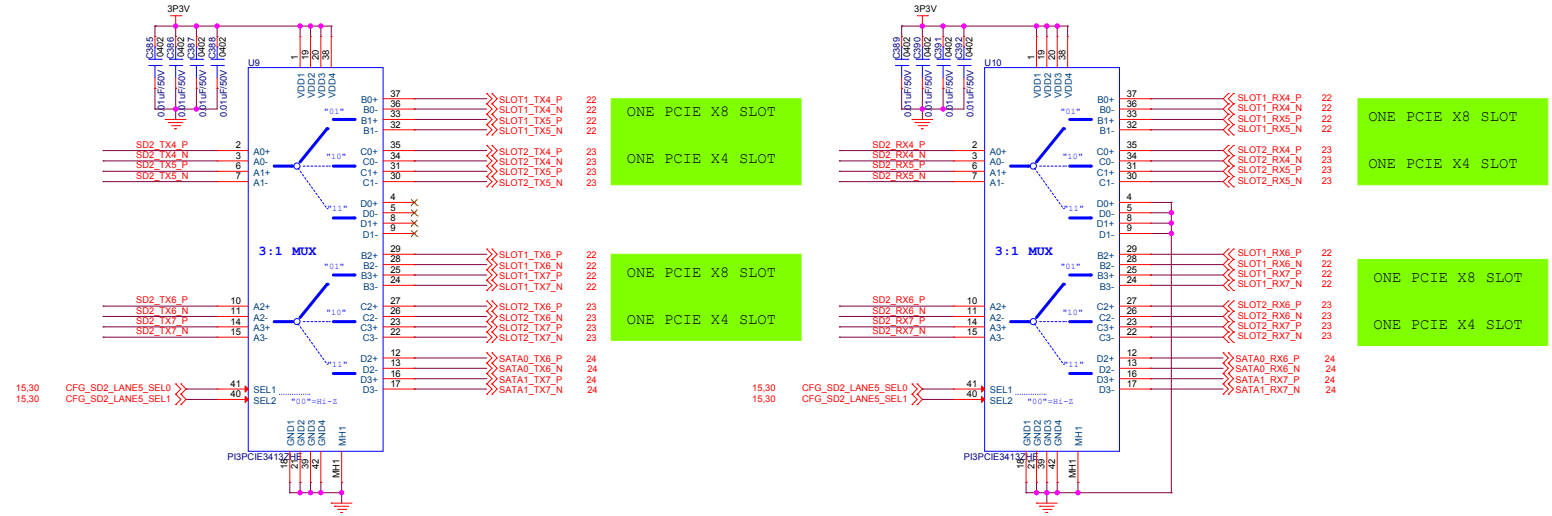

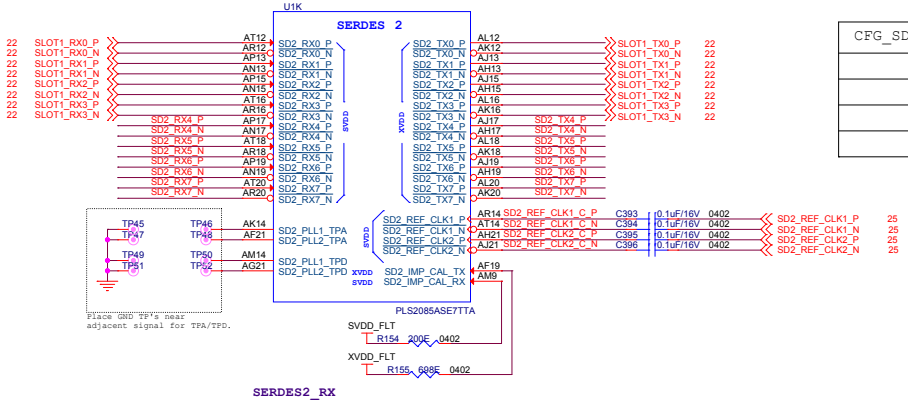

CFG_SD2_LANE5_SEL0	CFG_SD2_LANE5_SEL1	TARGET
0	0	HIGH-Z
0	1	ONE PCIE X8 SLOT
1	0	ONE PCIE X4 SLOT
1	1	2 SATA CONN

100 MHZ HCSL FOR BOTH REFCLK

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Title: SERDES 1_TX_MUX

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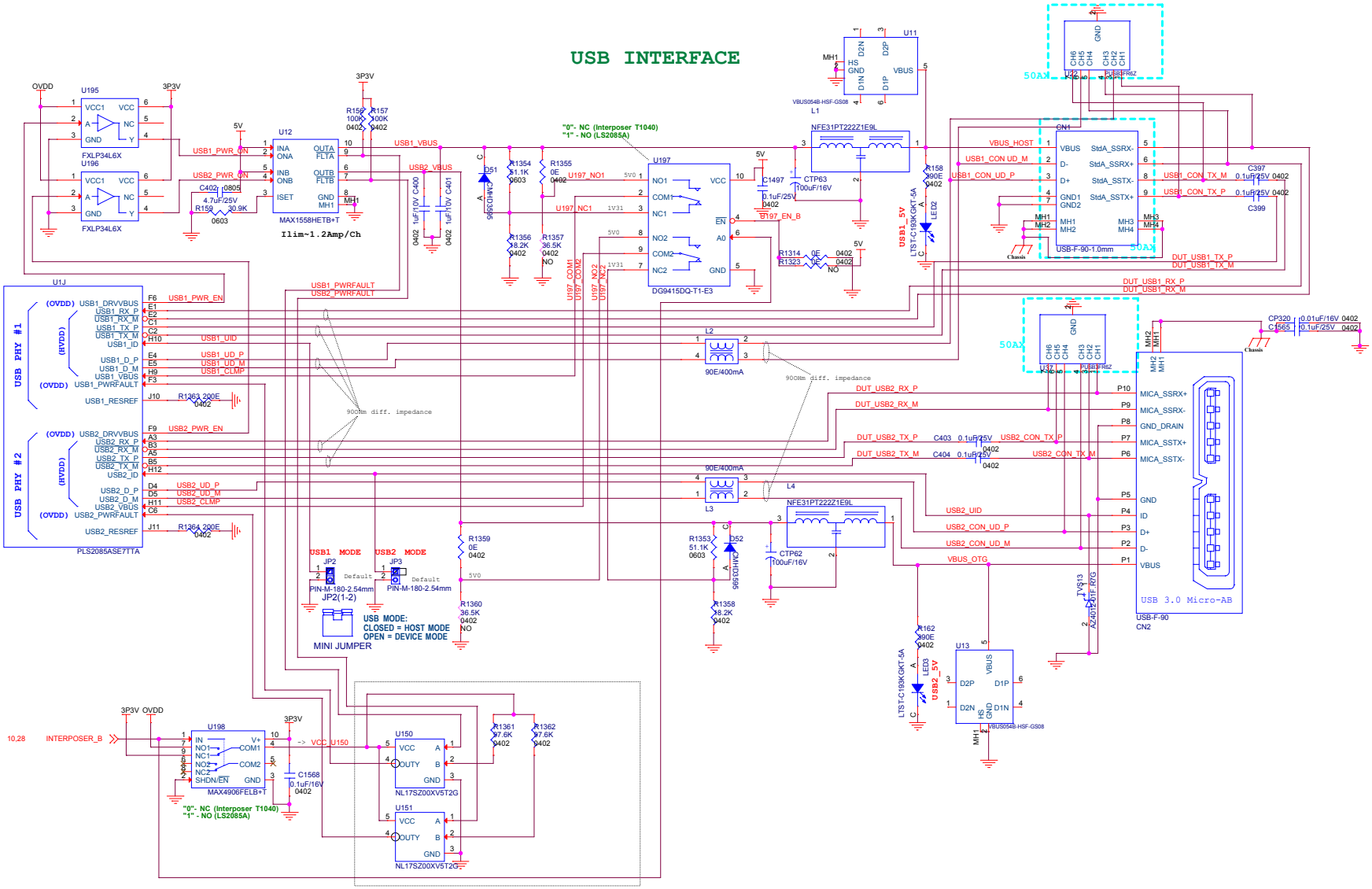
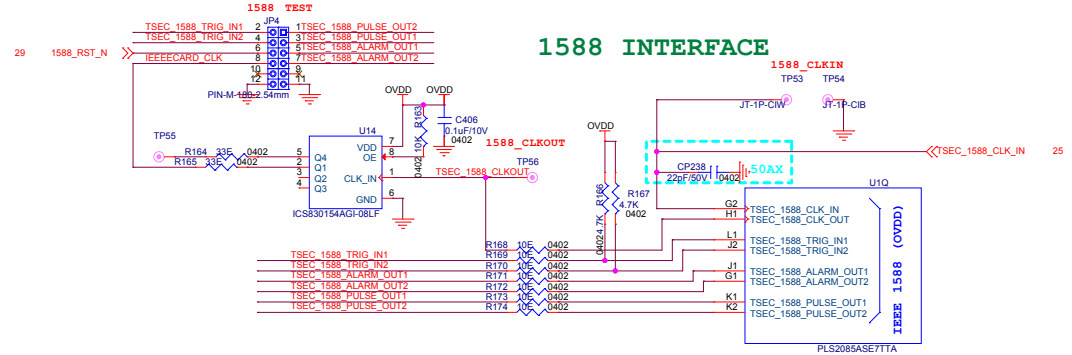
USB INTERFACE



1588 INTERFACE



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USB3.0			
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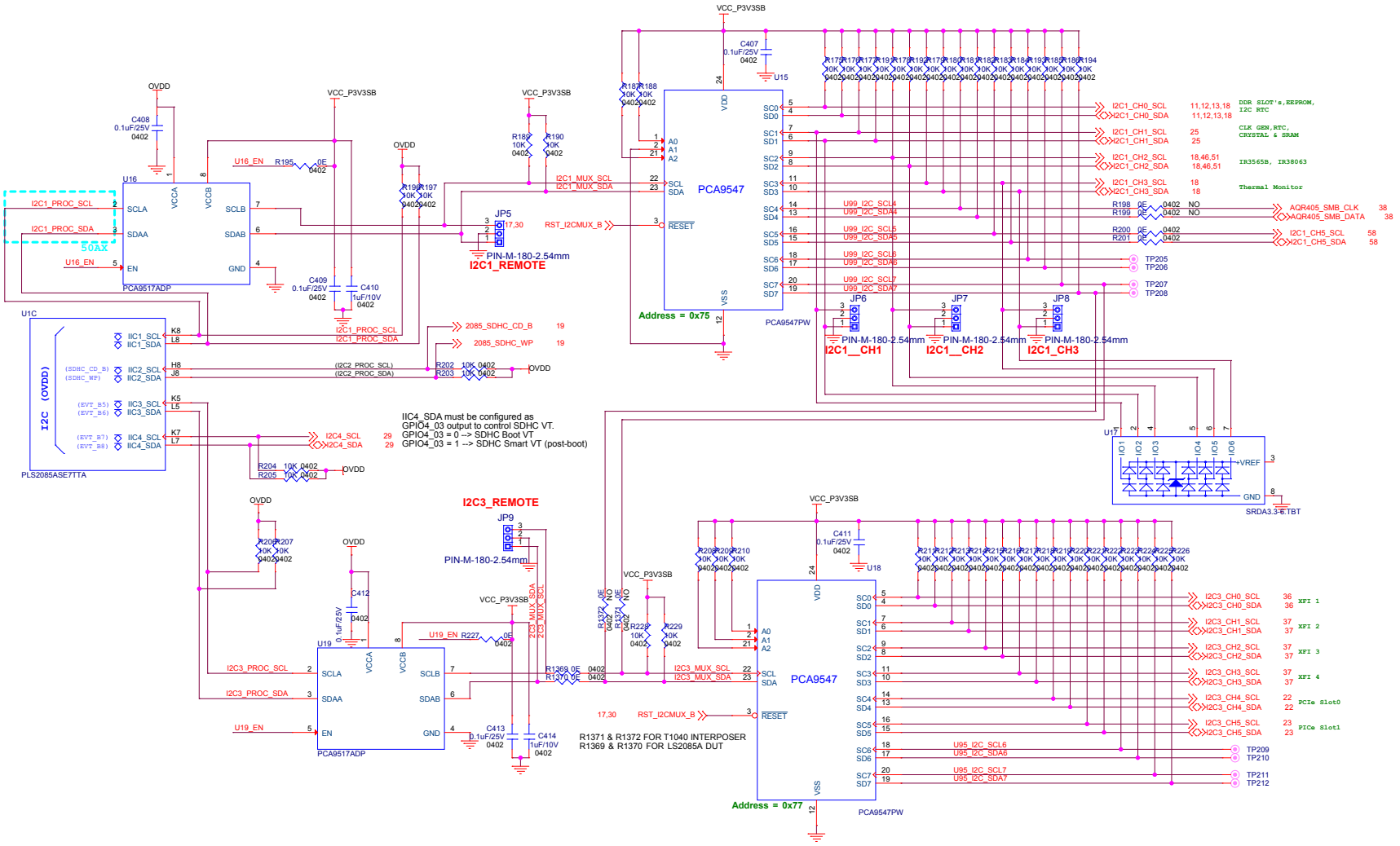

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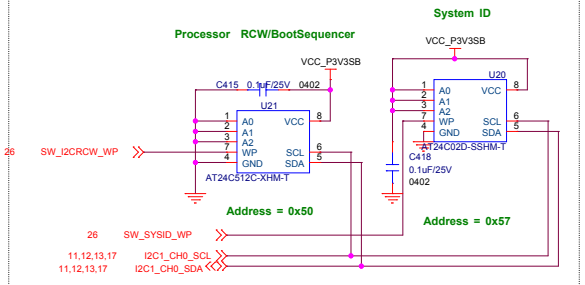
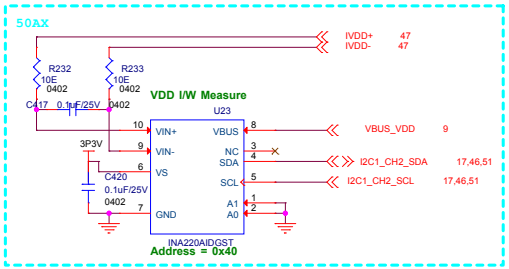
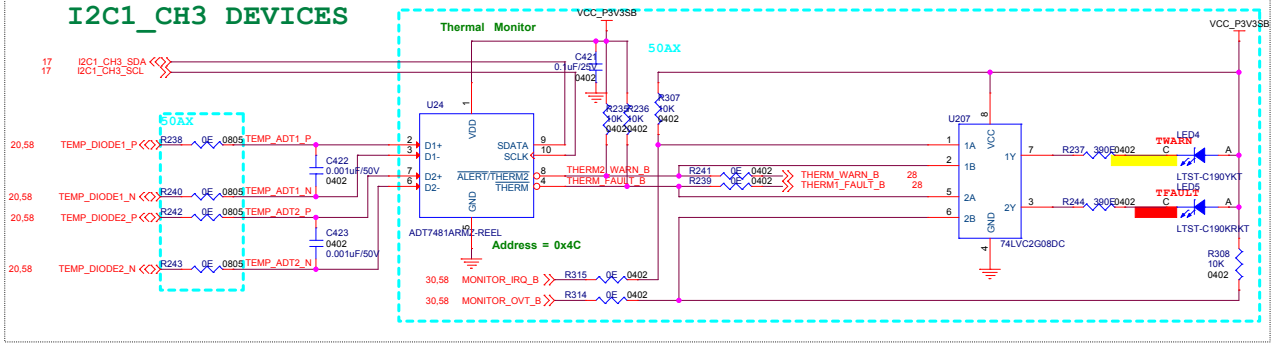
I2C1_CH0 DEVICES



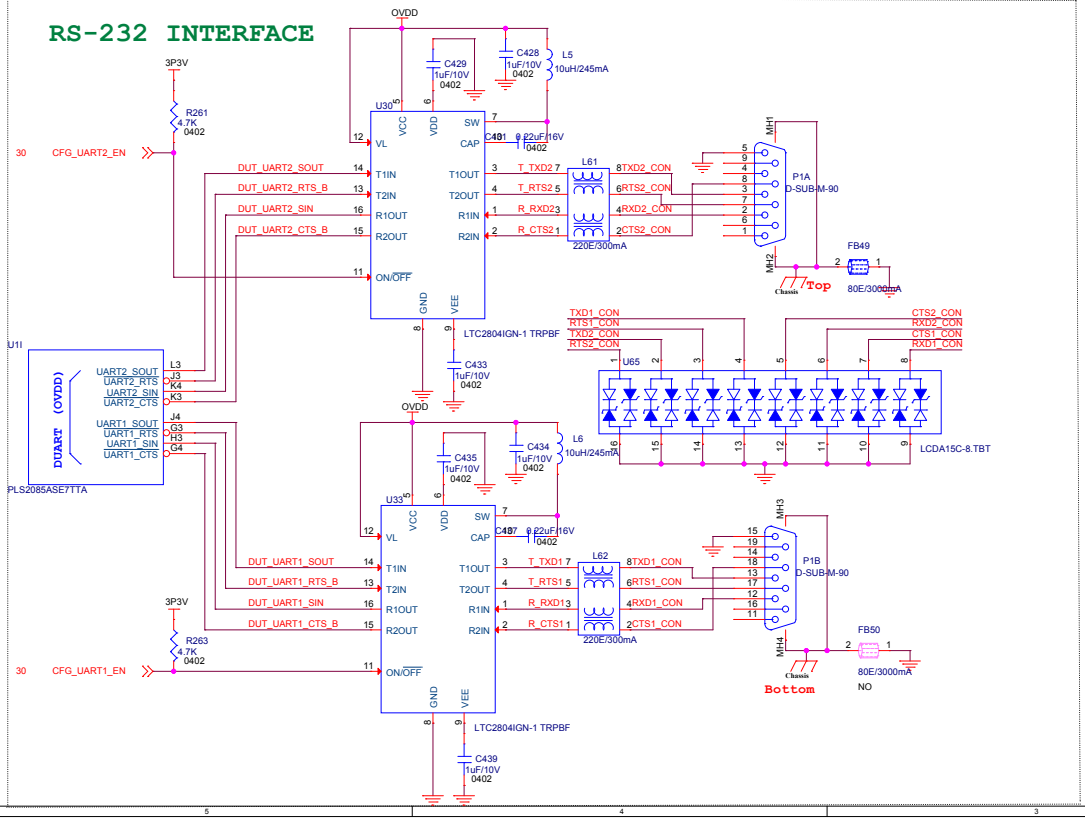
I2C1_CH2 DEVICES



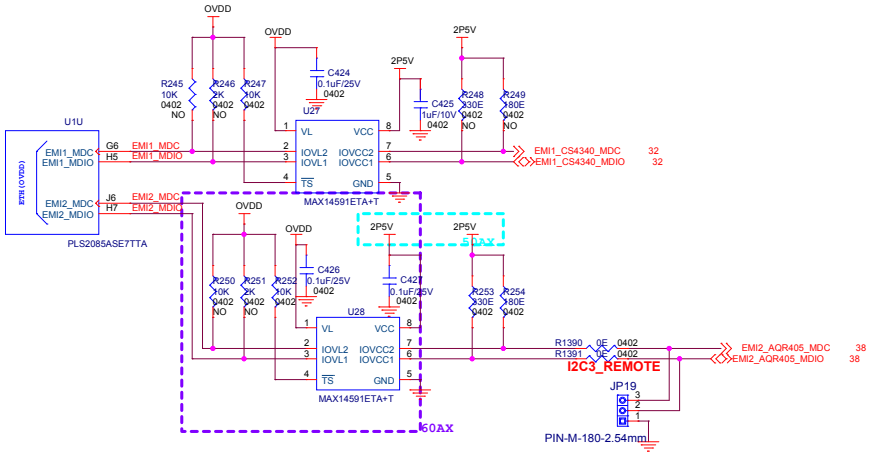
I2C1_CH3 DEVICES



RS-232 INTERFACE



MII1 MUXING & MII2



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Title		
I2C DEVICES & MII MUX's		
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SPI INTERFACE

S1	S0	SPI_SIN/SOUT/SCK connected to:
0	0	SDHC Sync loop
0	1	Reserved
1	**0**	**SPI Memory on-board (default)**
1	1	Reserved

S1	S0	SDHC/SPI_CS connected to:
0	0	SD Card Rev2.0/3.0
0	1	Reserved
1	**0**	**SPI Memory on-board (default)**
1	1	Reserved

SDHC INTERFACE

Boot VTs

SD CARD

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Title: **DUART, SPI & SDHC**

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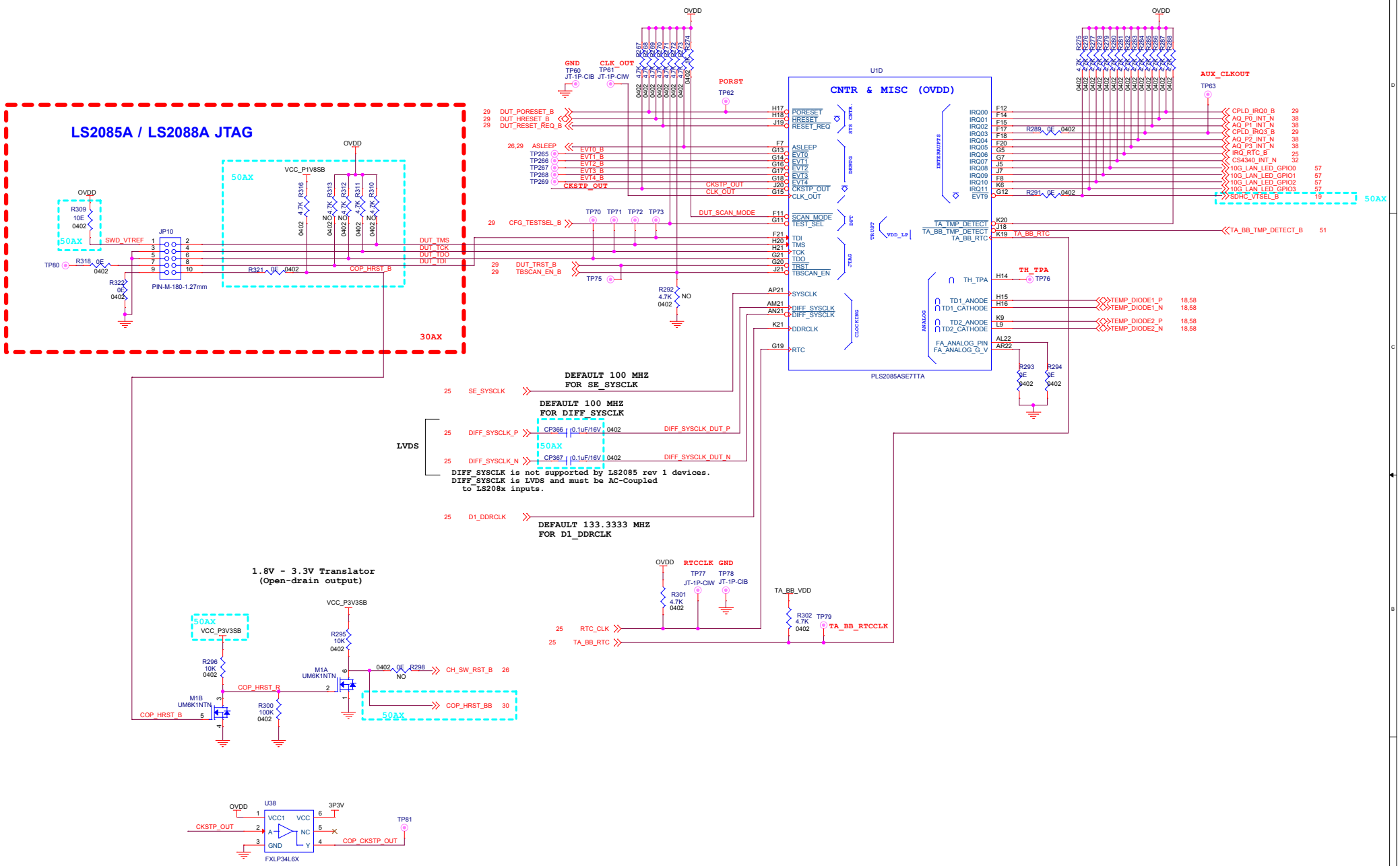

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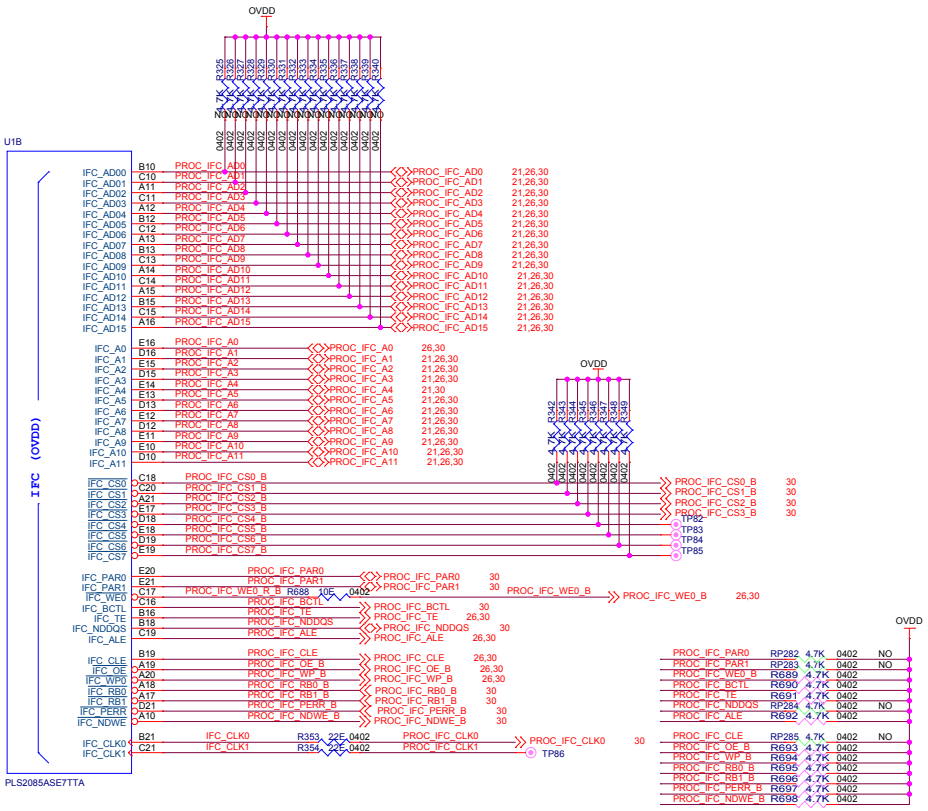

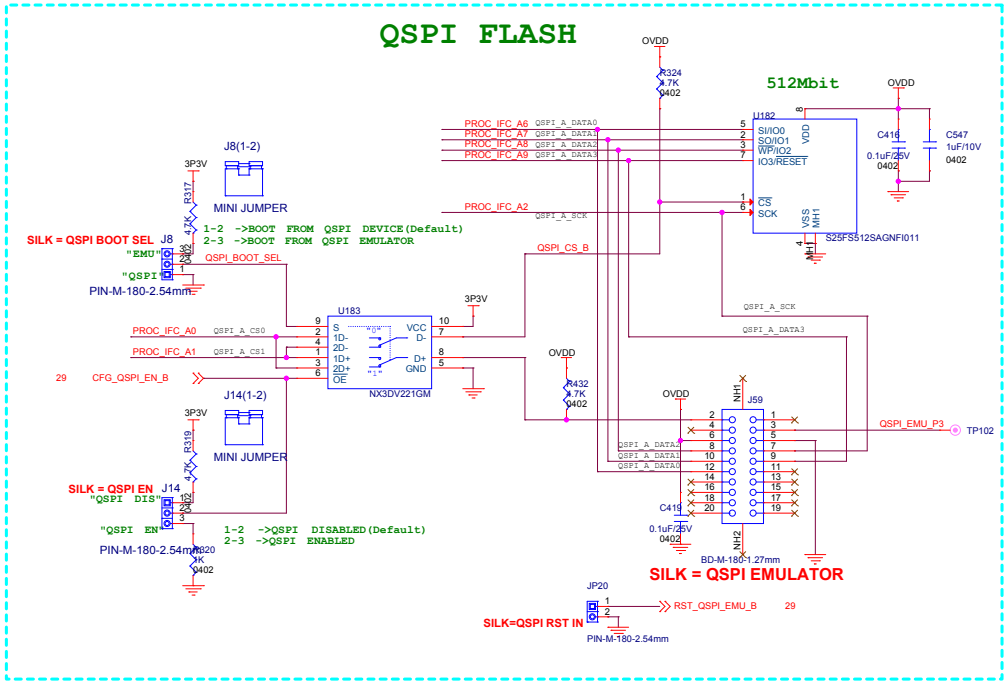

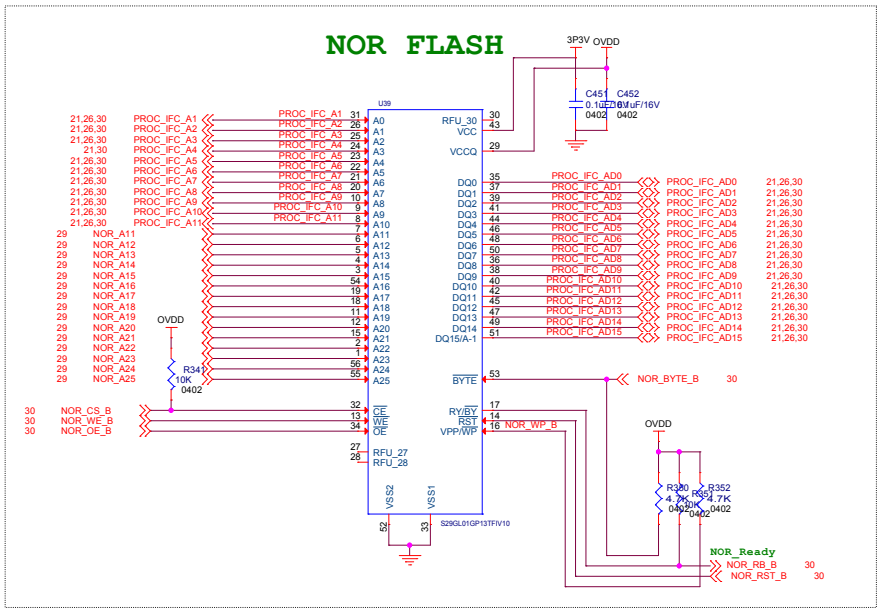

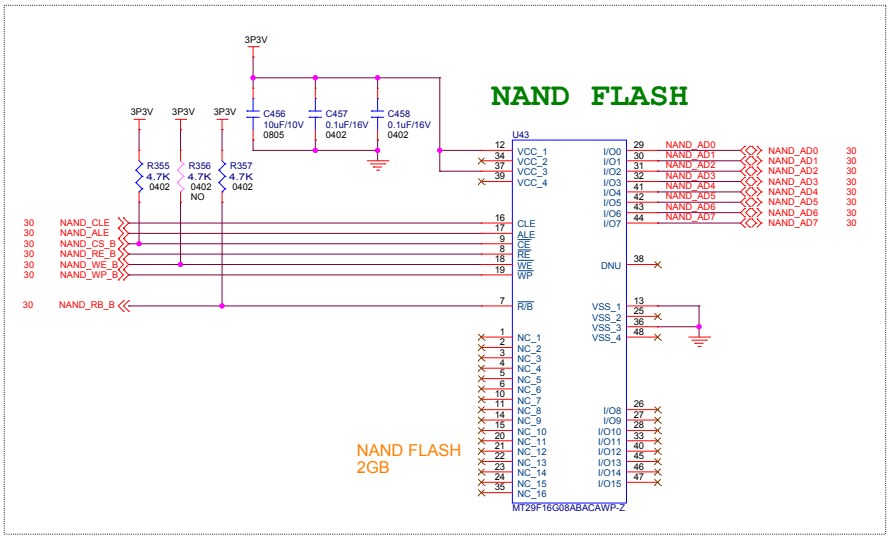

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Title		
IFC1		
Size: C	Document Number: 4BS03640G1X20	Rev: 70AX
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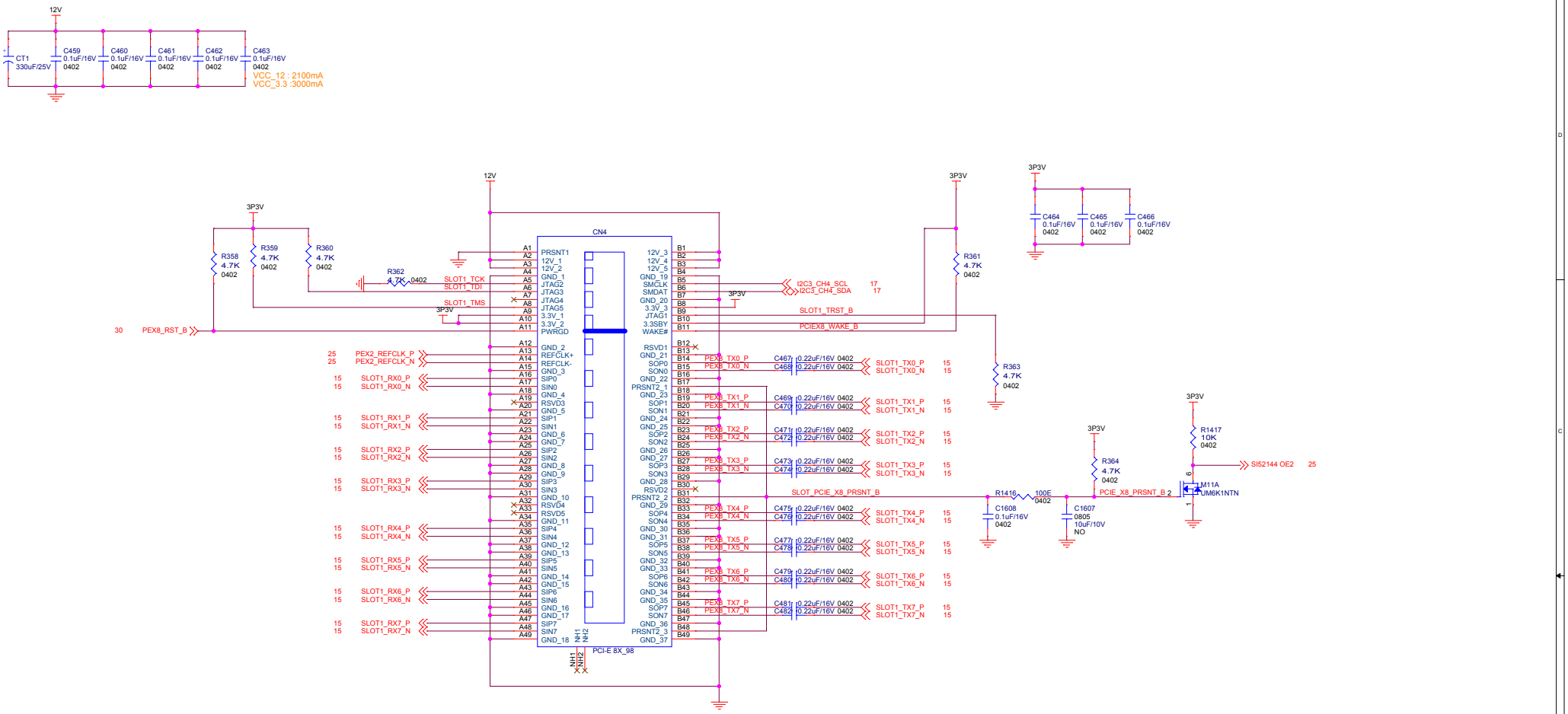

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Title	SERDES 2_MUX	
Size: C	Document Number: 4BS03640G1X20	Rev: 70AX
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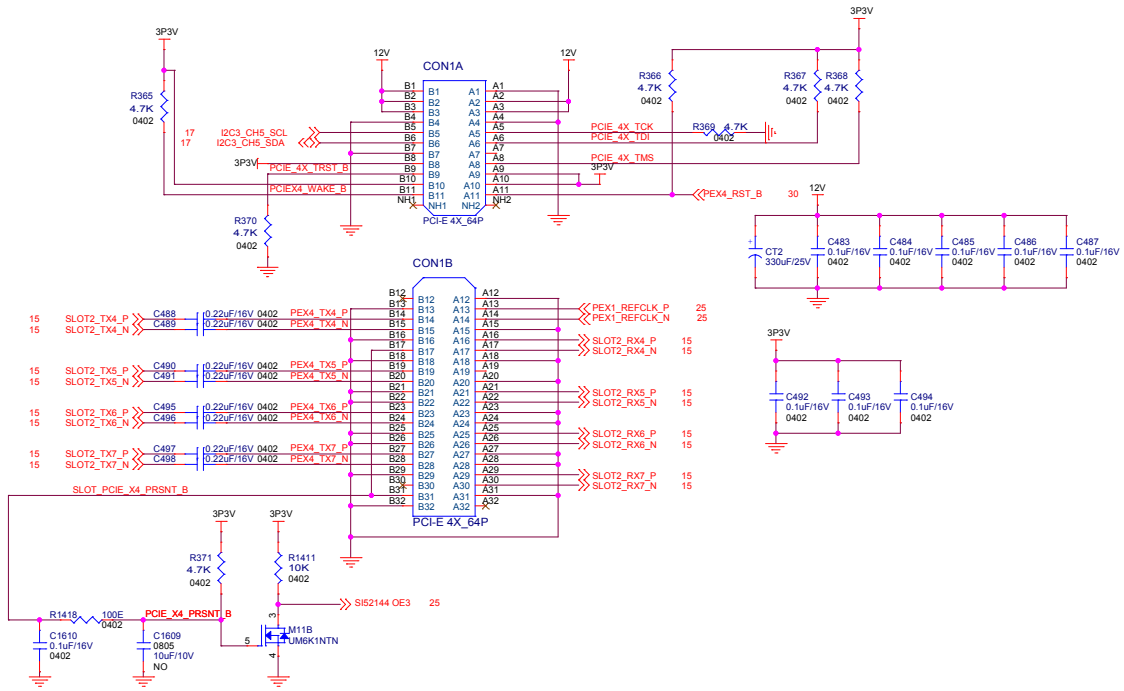

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Size C	Document Number 4BS03640G1X20	Rev 70AX
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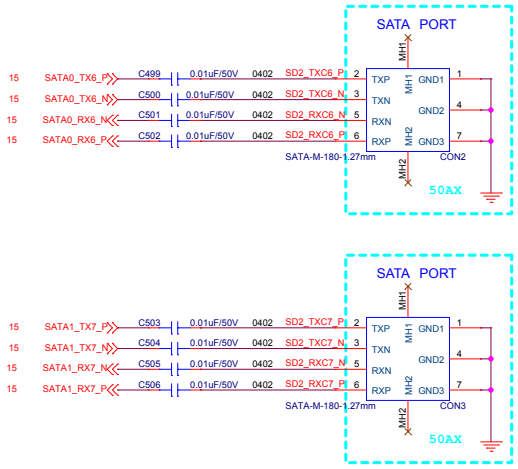

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Title	SATA 3.0	
Size C	Document Number 4BS03640G1X20	Rev 70AX
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SI5341B-A03628-GM OUTPUTS ARE:
CS4340 REFCLK 1/2 & 3/4 = 156.25 MHZ LVDS
SD1_REF_CLK1 = 156.25 MHZ LVDS
SD1_REF_CLK2 = 156.25 MHZ LVDS
TSEC_1588_CLK = 125 MHZ 1.8V LVCMOS
AQR405 CLK = 50 MHZ LVDS
DIFF_SYSCLK = 100 MHZ LVDS
SE_SYSCLK = 100 MHZ 1.8V LVCMOS
USBCLKIN = 24 MHZ 1.8V LVCMOS
DDRCLK = 133.3333 MHZ 1.8V LVCMOS

I2C_SEL PIN HAS INTERNALLY PULL-UP I2C MOD

I2C ADDRESS RANGE FOR SI5341B-A03628-GM IS 0X74 TO 0X77 (SELECTED VIA A1/A0 PINS)

DEFAULT I2C ADDRESS IS 0X74

DEFAULT I2C ADDRESS IS 0X6B

100 MHZ HCSL FOR ALL REFCLK OUTPUT FROM SI52144A

ADDRESS = 0X68

Spread Enable/ Disable

Mount	Spread
R393	Enable
R394	Disable

Output Control

Control	Control Output
OE0	DIFF0
OE1	DIFF1
OE2	DIFF2
OE3	DIFF3

ENABLE CLOCK OUTPUT, OE = 1
DISBLE CLOCK OUTPUT, OE = 0

Place 0.1uF to each power pin as close as possible

MINI JUMPER
2-3 ->RTC(Default)
1-2 ->TA_BB_RTC

SILK = RTC_CLK

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Title: CLK GEN
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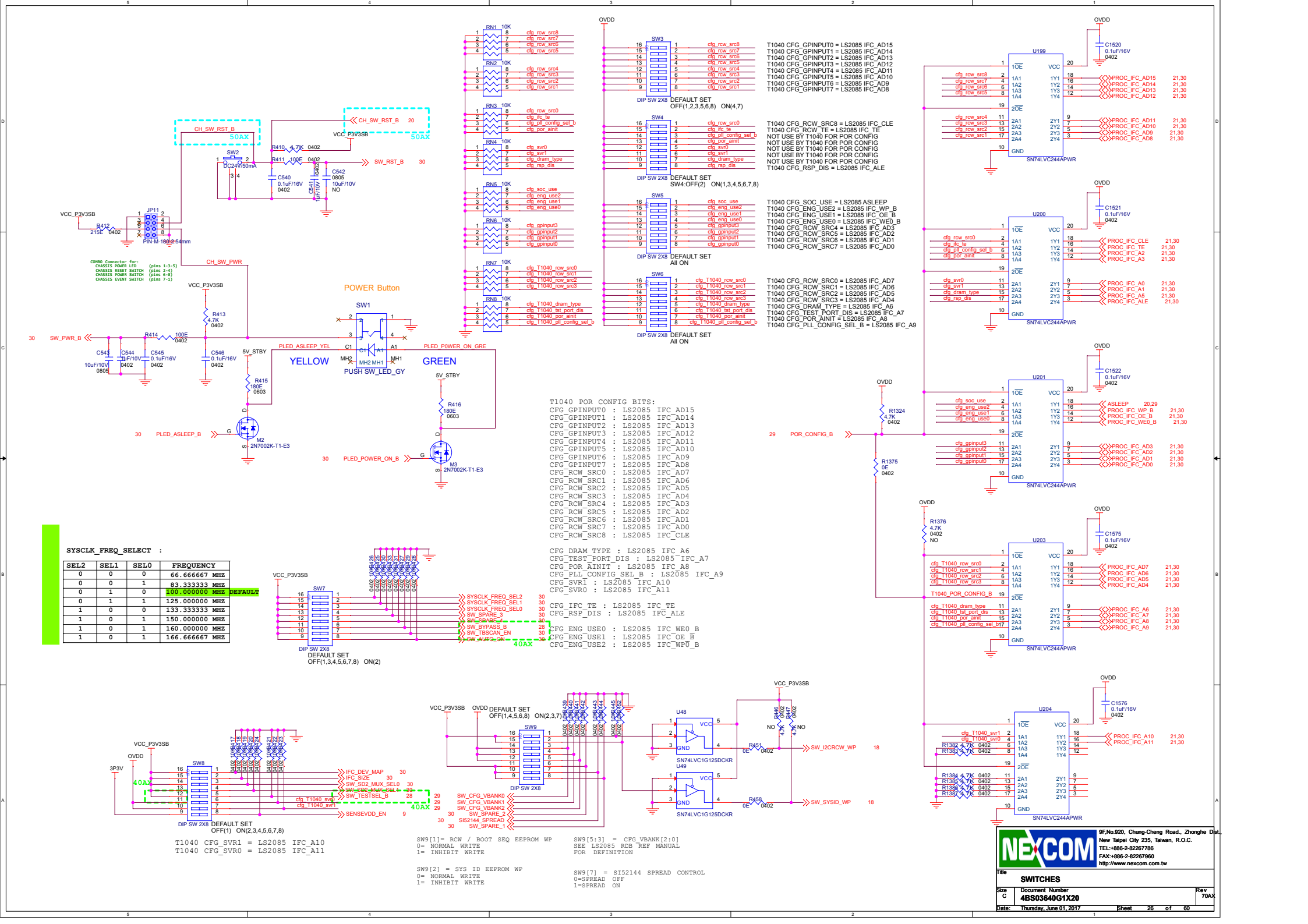
CH_SW_RST_B
50AX
SW2
DC24V/50mA
SW_RST_B
VCC_P3V3SB
JP11
PIN-M-180-2.54mm
COMBO Connector for:
CHASSIS POWER LED (pins 1-3-5)
CHASSIS RESET SWITCH (pins 2-4)
CHASSIS POWER SWITCH (pins 6-8)
CHASSIS EVENT SWITCH (pins 7-1)
CH_SW_PWR
POWER Button
SW1
SW_PWR_B
PLED_ASLEEP_YEL
YELLOW
PUSH SW_LED_GY
PLED_POWER_ON_GRE
GREEN
5V_STBY
PLED_ASLEEP_B
PLED_POWER_ON_B
M2
M3
2N7002K-T1-E3
RN1 10K
RN2 10K
RN3 10K
RN4 10K
RN5 10K
RN6 10K
RN7 10K
RN8 10K
cfg_rcw_src8
cfg_rcw_src7
cfg_rcw_src6
cfg_rcw_src5
cfg_rcw_src4
cfg_rcw_src3
cfg_rcw_src2
cfg_rcw_src1
cfg_rcw_src0
cfg_ifc_te
cfg_pll_config_sel_b
cfg_por_ainit
cfg_svr0
cfg_svr1
cfg_dram_type
cfg_rsp_dis
cfg_soc_use
cfg_eng_use2
cfg_eng_use1
cfg_eng_use0
cfg_gpinput3
cfg_gpinput2
cfg_gpinput1
cfg_gpinput0
cfg_T1040_rcw_src0
cfg_T1040_rcw_src1
cfg_T1040_rcw_src2
cfg_T1040_rcw_src3
cfg_T1040_dram_type
cfg_T1040_tst_port_dis
cfg_T1040_por_ainit
cfg_T1040_pll_config_sel_b
OVDD
SW3
SW4
SW5
SW6
DIP SW 2X8 DEFAULT SET
OFF(1,2,3,5,6,8) ON(4,7)
SW4:OFF(2) ON(1,3,4,5,6,7,8)
All ON
T1040 CFG_GPINPUT0 = LS2085 IFC_AD15
T1040 CFG_GPINPUT1 = LS2085 IFC_AD14
T1040 CFG_GPINPUT2 = LS2085 IFC_AD13
T1040 CFG_GPINPUT3 = LS2085 IFC_AD12
T1040 CFG_GPINPUT4 = LS2085 IFC_AD11
T1040 CFG_GPINPUT5 = LS2085 IFC_AD10
T1040 CFG_GPINPUT6 = LS2085 IFC_AD9
T1040 CFG_GPINPUT7 = LS2085 IFC_AD8
T1040 CFG_RCW_SRC8 = LS2085 IFC_CLE
T1040 CFG_RCW_TE = LS2085 IFC_TE
NOT USE BY T1040 FOR POR CONFIG
T1040 CFG_SOC_USE = LS2085 ASLEEP
T1040 CFG_ENG_USE2 = LS2085 IFC_WP_B
T1040 CFG_ENG_USE1 = LS2085 IFC_OE_B
T1040 CFG_ENG_USE0 = LS2085 IFC_WE0_B
T1040 CFG_RCW_SRC4 = LS2085 IFC_AD3
T1040 CFG_RCW_SRC5 = LS2085 IFC_AD2
T1040 CFG_RCW_SRC6 = LS2085 IFC_AD1
T1040 CFG_RCW_SRC7 = LS2085 IFC_AD0
T1040 CFG_RCW_SRC0 = LS2085 IFC_AD7
T1040 CFG_RCW_SRC1 = LS2085 IFC_AD6
T1040 CFG_RCW_SRC2 = LS2085 IFC_AD5
T1040 CFG_RCW_SRC3 = LS2085 IFC_AD4
T1040 CFG_DRAM_TYPE = LS2085 IFC_A6
T1040 CFG_TEST_PORT_DIS = LS2085 IFC_A7
T1040 CFG_POR_AINIT = LS2085 IFC_A8
T1040 CFG_PLL_CONFIG_SEL_B = LS2085 IFC_A9
U199
U200
U201
U203
U204
SN74LVC244APWR
PROC_IFC_AD15
PROC_IFC_AD14
PROC_IFC_AD13
PROC_IFC_AD12
PROC_IFC_AD11
PROC_IFC_AD10
PROC_IFC_AD9
PROC_IFC_AD8
PROC_IFC_CLE
PROC_IFC_TE
PROC_IFC_A2
PROC_IFC_A3
PROC_IFC_A0
PROC_IFC_A1
PROC_IFC_A5
PROC_IFC_ALE
ASLEEP
PROC_IFC_WP_B
PROC_IFC_OE_B
PROC_IFC_WE0_B
PROC_IFC_AD3
PROC_IFC_AD2
PROC_IFC_AD1
PROC_IFC_AD0
PROC_IFC_AD7
PROC_IFC_AD6
PROC_IFC_AD5
PROC_IFC_AD4
PROC_IFC_A6
PROC_IFC_A7
PROC_IFC_A8
PROC_IFC_A9
PROC_IFC_A10
PROC_IFC_A11
POR_CONFIG_B
T1040_POR_CONFIG_B
SYSCLK_FREQ_SELECT :
SEL2 SEL1 SEL0 FREQUENCY
0 0 0 66.666667 MHZ
0 0 1 83.333333 MHZ
0 1 0 100.000000 MHZ DEFAULT
0 1 1 125.000000 MHZ
1 0 0 133.333333 MHZ
1 0 1 150.000000 MHZ
1 0 1 160.000000 MHZ
1 0 1 166.666667 MHZ
SW7
SYSCLK_FREQ_SEL2
SYSCLK_FREQ_SEL1
SYSCLK_FREQ_SEL0
SW_SPARE_3
SW_SPARE_4
SW_BYPASS_B
SW_TBSCAN_EN
SW_AUTO_ON
40AX
DEFAULT SET
OFF(1,3,4,5,6,7,8) ON(2)
T1040 POR CONFIG BITS:
CFG_GPINPUT0 : LS2085 IFC_AD15
CFG_GPINPUT1 : LS2085 IFC_AD14
CFG_GPINPUT2 : LS2085 IFC_AD13
CFG_GPINPUT3 : LS2085 IFC_AD12
CFG_GPINPUT4 : LS2085 IFC_AD11
CFG_GPINPUT5 : LS2085 IFC_AD10
CFG_GPINPUT6 : LS2085 IFC_AD9
CFG_GPINPUT7 : LS2085 IFC_AD8
CFG_RCW_SRC0 : LS2085 IFC_AD7
CFG_RCW_SRC1 : LS2085 IFC_AD6
CFG_RCW_SRC2 : LS2085 IFC_AD5
CFG_RCW_SRC3 : LS2085 IFC_AD4
CFG_RCW_SRC4 : LS2085 IFC_AD3
CFG_RCW_SRC5 : LS2085 IFC_AD2
CFG_RCW_SRC6 : LS2085 IFC_AD1
CFG_RCW_SRC7 : LS2085 IFC_AD0
CFG_RCW_SRC8 : LS2085 IFC_CLE
CFG_DRAM_TYPE : LS2085 IFC_A6
CFG_TEST_PORT_DIS : LS2085 IFC_A7
CFG_POR_AINIT : LS2085 IFC_A8
CFG_PLL_CONFIG_SEL_B : LS2085 IFC_A9
CFG_SVR1 : LS2085 IFC_A10
CFG_SVR0 : LS2085 IFC_A11
CFG_IFC_TE : LS2085 IFC_TE
CFG_RSP_DIS : LS2085 IFC_ALE
CFG_ENG_USE0 : LS2085 IFC_WE0_B
CFG_ENG_USE1 : LS2085 IFC_OE_B
CFG_ENG_USE2 : LS2085 IFC_WP0_B
SW8
IFC_DEV_MAP
IFC_SIZE
SW_SD2_MUX_SEL0
SW_SD2_MUX_SEL1
SW_TESTSEL_B
SENSEVDD_EN
DEFAULT SET
OFF(1) ON(2,3,4,5,6,7,8)
T1040 CFG_SVR1 = LS2085 IFC_A10
T1040 CFG_SVR0 = LS2085 IFC_A11
SW9
SW_CFG_VBANK0
SW_CFG_VBANK1
SW_CFG_VBANK2
SW_SPARE_2
SI52144_SPREAD
SW_SPARE_1
DEFAULT SET
OFF(1,4,5,6,8) ON(2,3,7)
U48
U49
SN74LVC1G125DCKR
SW_I2CRCW_WP
SW_SYSID_WP
SW9[1]= RCW / BOOT SEQ EEPROM WP
0= NORMAL WRITE
1= INHIBIT WRITE
SW9[2] = SYS ID EEPROM WP
0= NORMAL WRITE
1= INHIBIT WRITE
SW9[5:3] = CFG_VBANK[2:0]
SEE LS2085 RDB REF MANUAL
FOR DEFINITION
SW9[7] = SI52144 SPREAD CONTROL
0=SPREAD OFF
1=SPREAD ON
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SWITCHES
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Document Number 4BS03640G1X20
Rev 70AX
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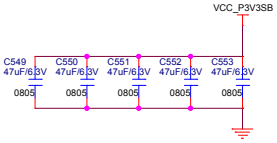
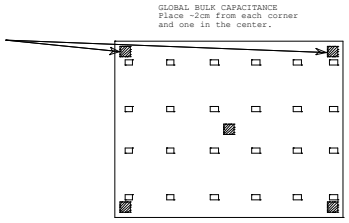
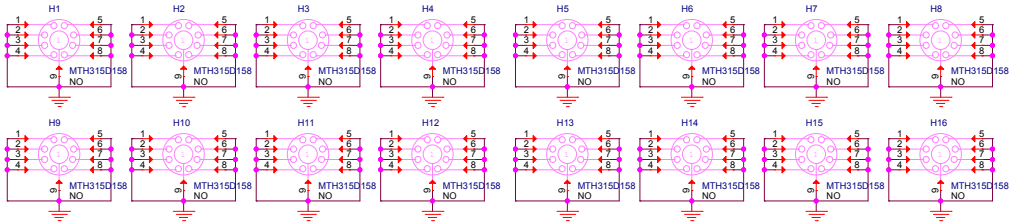
PCB1







SOCKET ASSEMBLY:
Mechanics, Heatsink, MPI, FR4 and FAN are included in SYSTEM BOM

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MISC		
Size: C	Document Number: 4BS03640G1X20	Rev: 70AX
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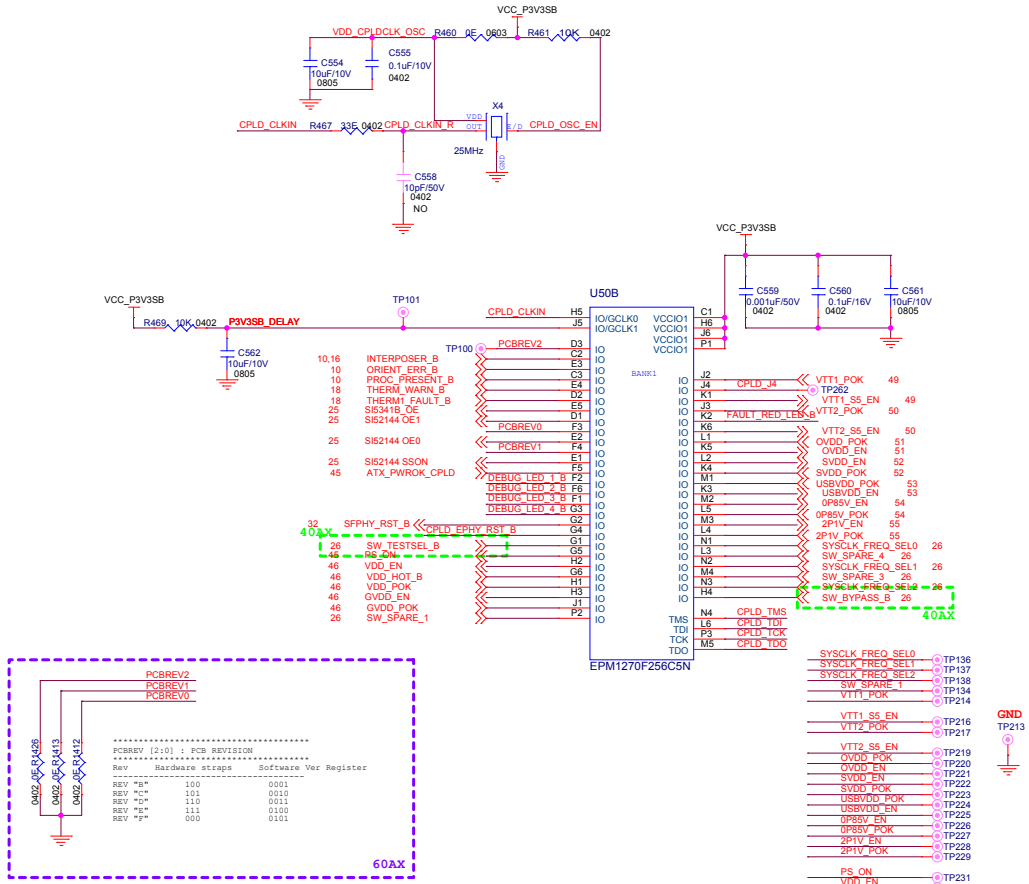
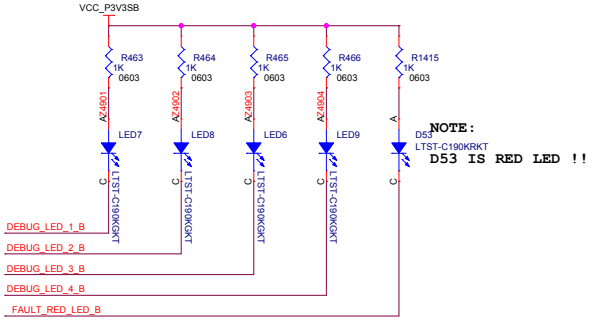
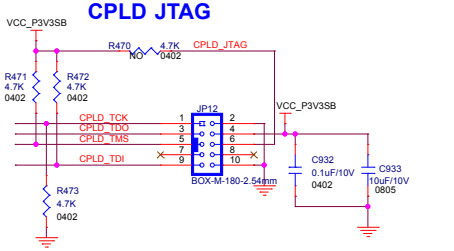


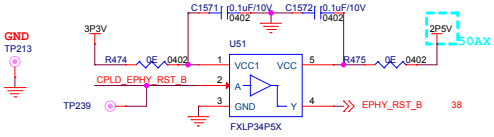
Table 2–7. MAX II MultiVolt I/O Support *(Note 1)*

	Input Signal					Output Signal				
VCCIO (V)	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	**5.0 V**	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	**5.0 V**
1.5	✓	✓	✓	✓	—	✓	—	—	—	—
1.8	✓	✓	✓	✓	—	✓ *(2)*	✓	—	—	—
2.5	—	—	✓	✓	—	✓ *(3)*	✓ *(3)*	✓	—	—
3.3	—	—	✓ *(4)*	✓	✓ *(5)*	✓ *(6)*	✓ *(6)*	✓ *(6)*	✓	✓ *(7)*



CPLD JTAG





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Title: **CPLD PART1**

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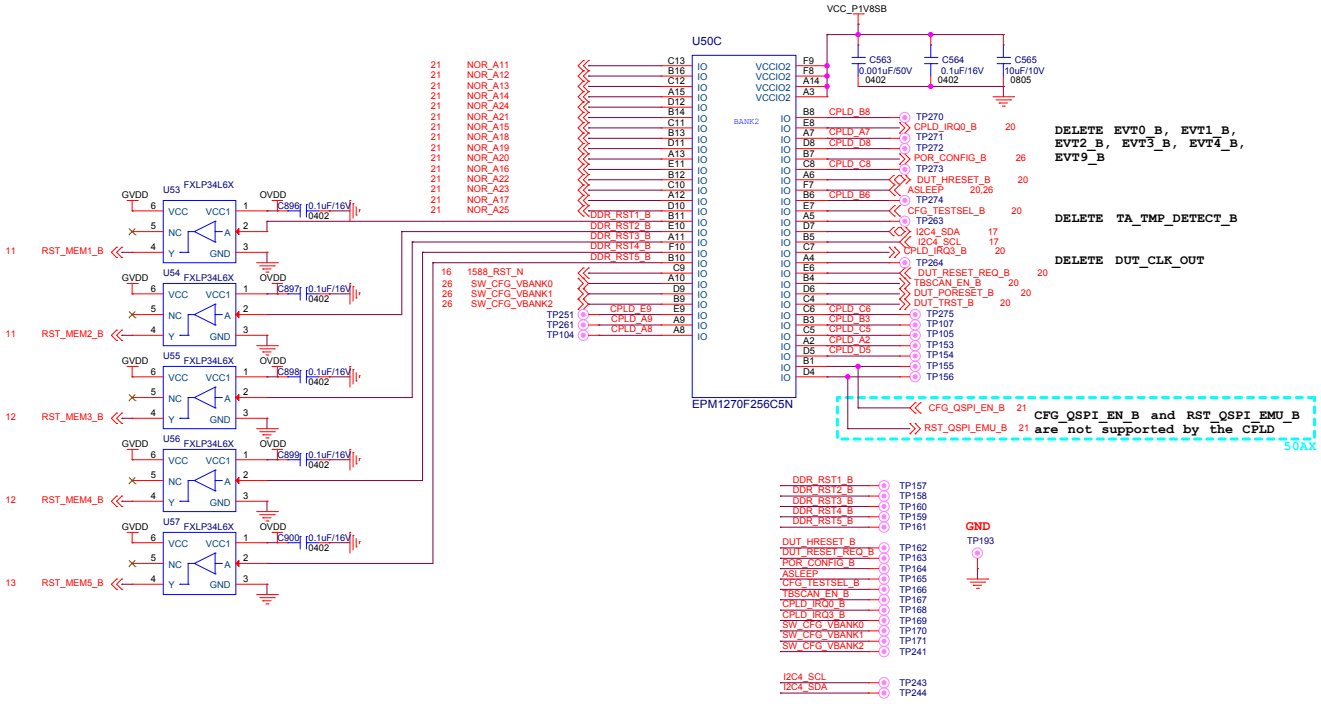

Table 2–7. MAX II MultiVolt I/O Support *(Note 1)*

	Input Signal					Output Signal				
VCCIO (V)	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	**5.0 V**	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	**5.0 V**
1.5	✓	✓	✓	✓	—	✓	—	—	—	—
1.8	✓	✓	✓	✓	—	✓ *(2)*	✓	—	—	—
2.5	—	—	✓	✓	—	✓ *(3)*	✓ *(3)*	✓	—	—
3.3	—	—	✓ *(4)*	✓	✓ *(5)*	✓ *(6)*	✓ *(6)*	✓ *(6)*	✓	✓ *(7)*

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Title: **CPLD PART2**

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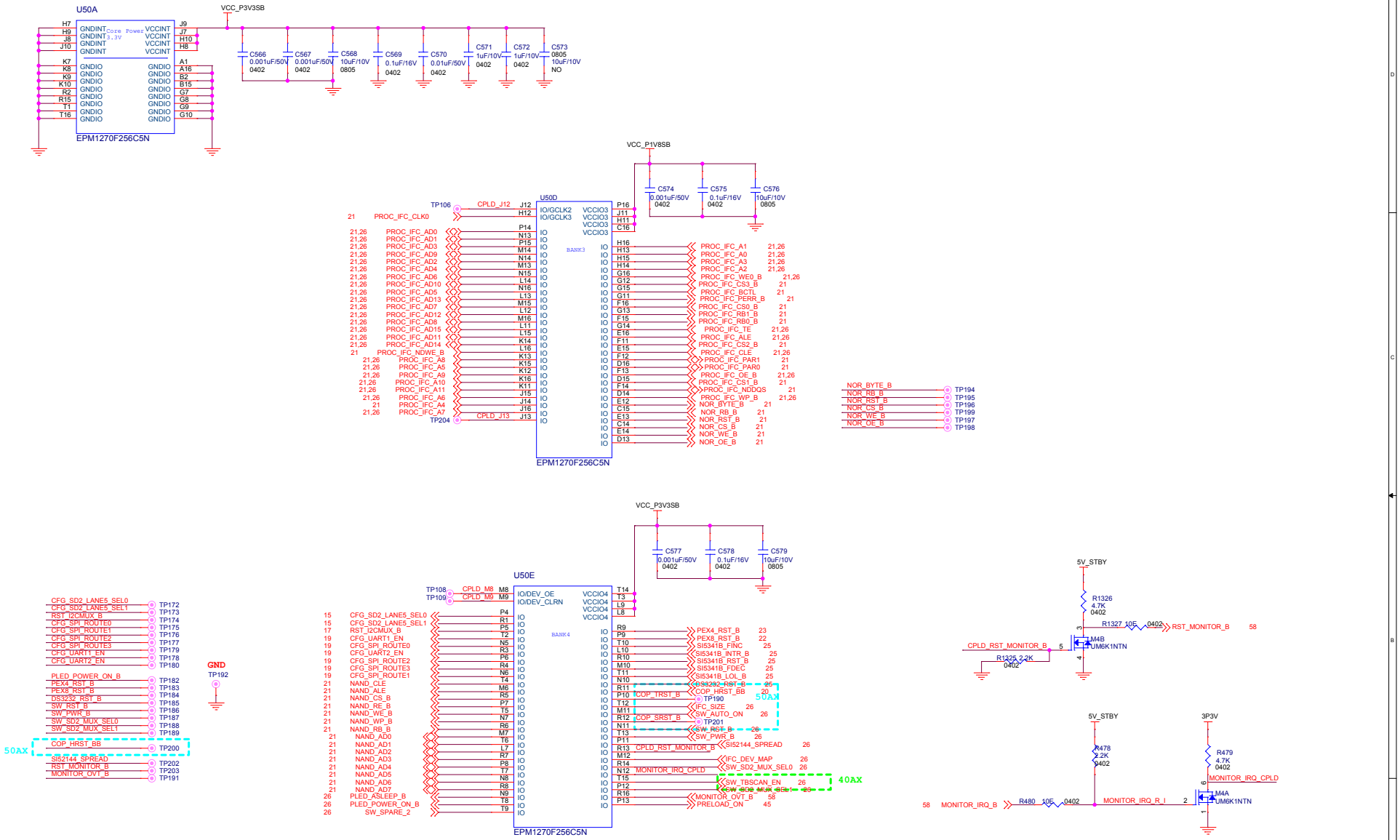

Table 2–7. MAX II Multi-Volt I/O Support *(Note 1)*

VCCIO (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓	✓	—	✓	—	—	—	—
1.8	✓	✓	✓	✓	—	✓ (2)	✓	—	—	—
2.5	—	—	✓	✓	—	✓ (3)	✓ (3)	✓	—	—
3.3	—	—	✓ (4)	✓	✓ (5)	✓ (6)	✓ (6)	✓ (6)	✓	✓ (7)

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Title: CPLD PART3

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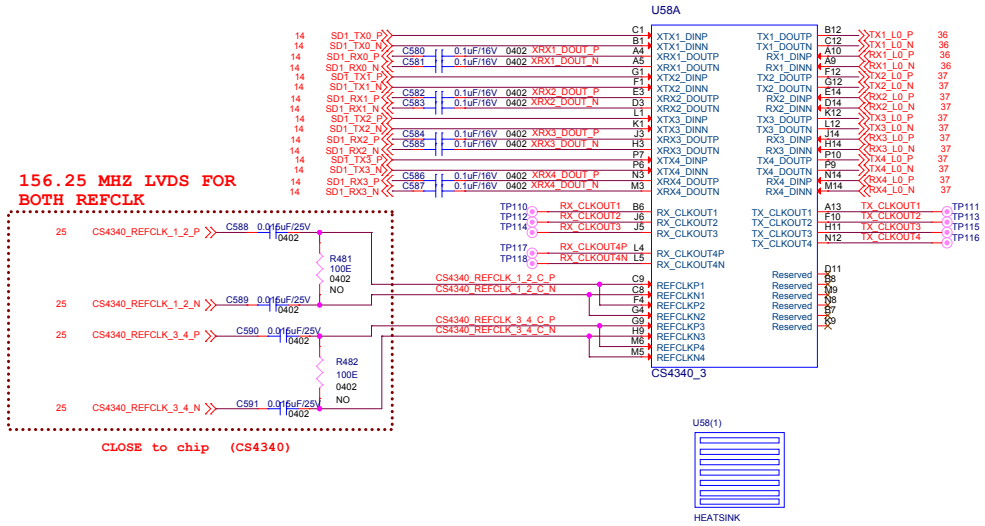

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Title	CS4340_XFI		
Size C	Document Number 4BS03640G1X20		Rev 70AX
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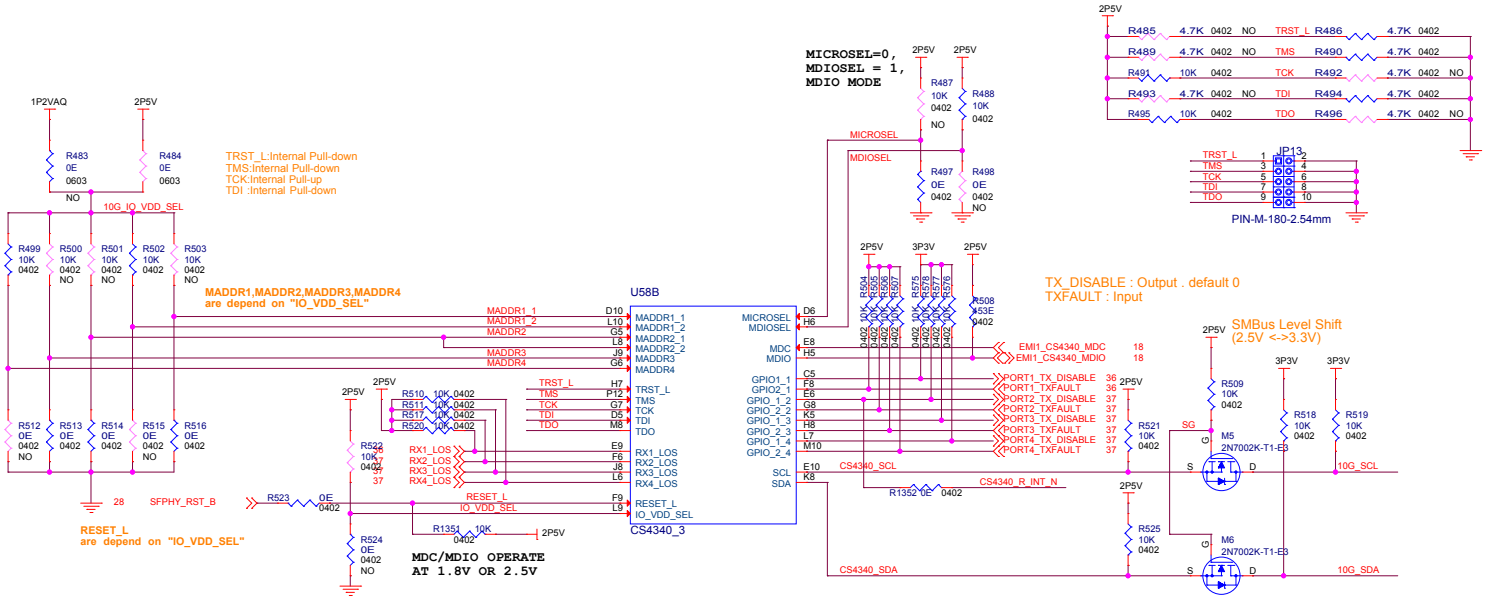

IO_VDD_SEL	L9	DC	LVCMOS Input Internal Pullup	Microprocessor interface voltage select. **Value** / **Meaning** 0 — MDC and MDIO operate at 1.0 V (IEEE 802.3a Clause 45 compliant) 1 — MDC and MDIO operate at 1.8/2.5 V. This is the default. **Note:** The I/O voltages of RESET_L, MADDR1, MADDR2, MADDR3 and MADDR4 are also controlled by IO_VDD_SEL.

Table 11 Microprocessor Interface Modes

	Mode	MICROSEL	MDIOSEL	MADDR Pin						
				MADDR0(1)	MADDR1_1 (2)	MADDR1_2	MADDR2_1 (3)	MADDR2_2	MADDR3	MADDR4
Default	MDIO(4)	0	1	PRTAD[0] hardwired inside the package	PRTAD[1] Tie to VSS	PRTAD[1] Tie to VDD	PRTAD[2] Tie together with MADDR2_2	PRTAD[2] Tie together with MADDR2_1	PRTAD[3]	PRTAD[4]
	I2C(5)	1	0	slave_addr[0] hardwired inside the package	slave_addr[1] Tie to VSS	slave_addr[1] Tie to VDD	slave_addr[2] Tie together with MADDR2_2	slave_addr[2] Tie together with MADDR2_1	slave_addr[3]	slave_addr[4]
	SPI	1	1	hardwired inside the package	chip select, device #1 (active low)	chip select, device #3 (active low)	chip select, device #2 (active low)	chip select, device #4 (active low)	MOSI	X

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Title: CS4340_STRAP PIN

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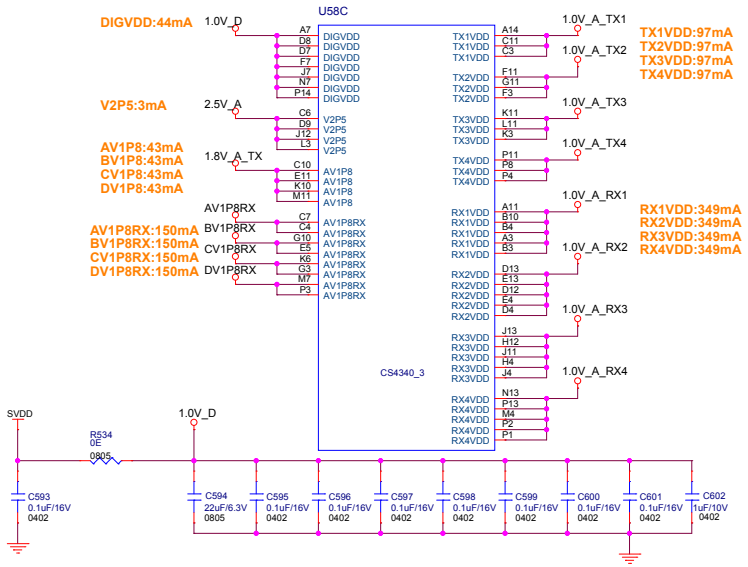

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Title: CS4340_PWR_P1V0

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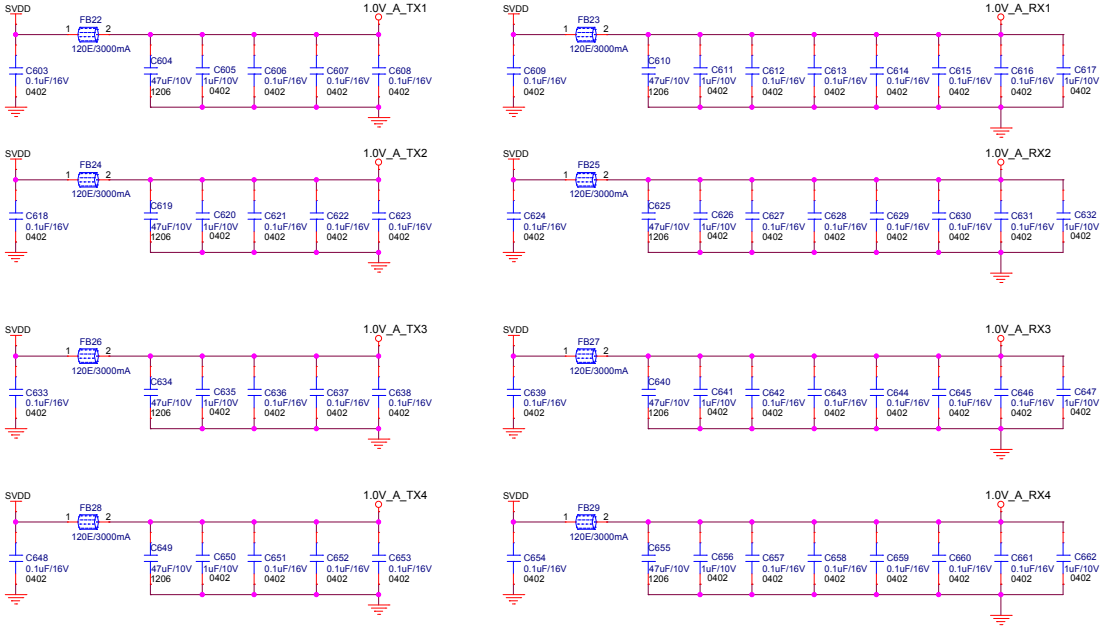

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Title: CS4340_PWR_P1V0_FILTER

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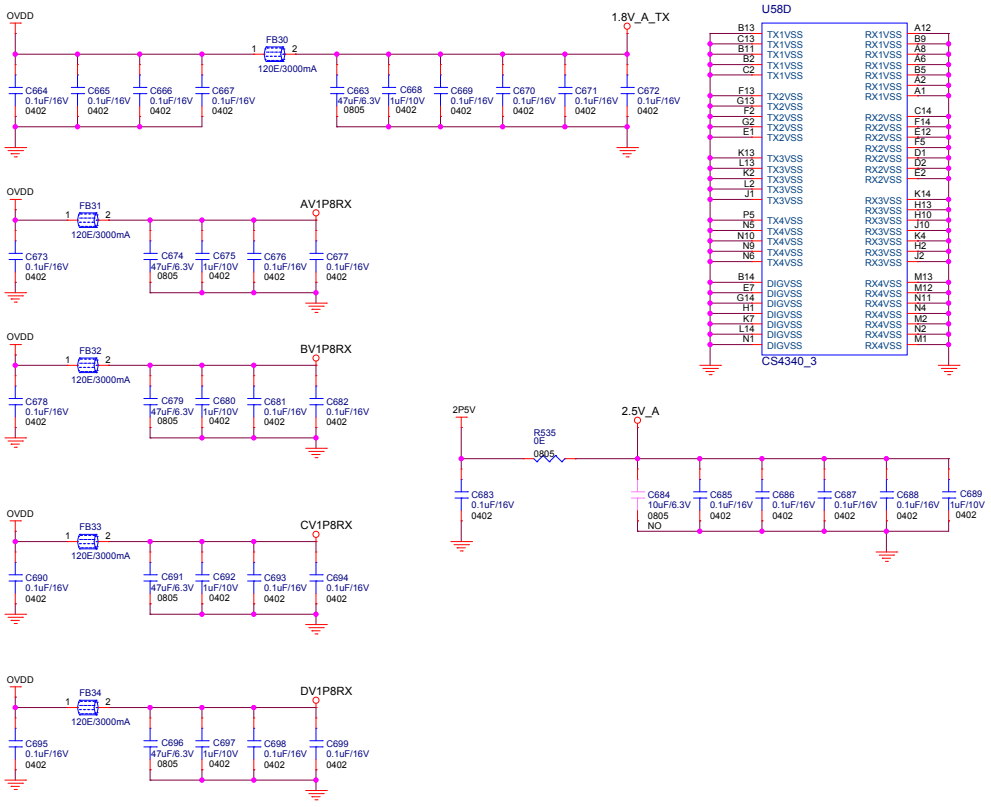

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Title	CS4340_PWR_P1V8_P2V5	
Size: C	Document Number: 4BS03640G1X20	Rev: 70AX
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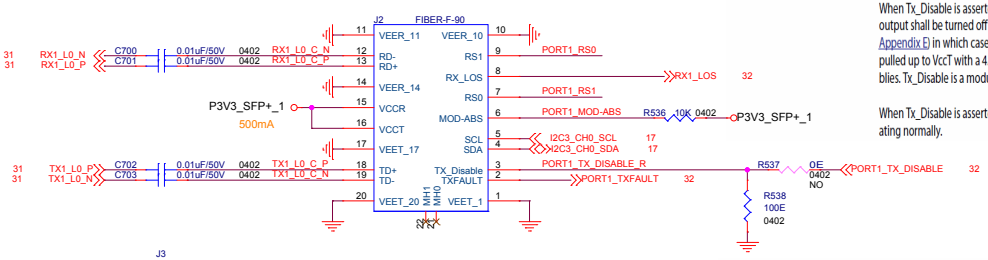
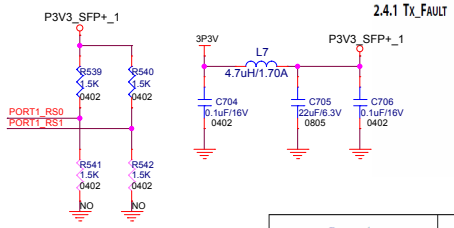
2.4.2 Tx_Disable



When Tx_Disable is asserted high or left open, the SFP+ module transmitter output shall be turned off unless the module is a passive cable assembly (see Appendix F) in which case this signal may be ignored. This contact shall be pulled up to VccT with a 4.7 kΩ to 10 kΩ resistor in modules and cable assemblies. Tx_Disable is a module input contact.

When Tx_Disable is asserted low or grounded the module transmitter is operating normally.

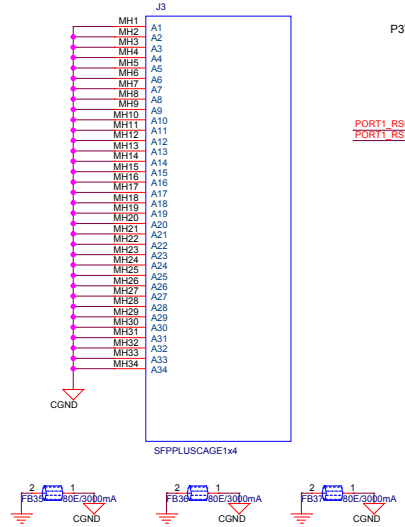
2.4.1 Tx_Fault



Tx_Fault is a module output that when high, indicates that the module transmitter has detected a fault condition related to laser operation or safety. If Tx_Fault is not implemented, the Tx_Fault contact signal shall be held low by the module and may be connected to Vee within the module.

The Tx_Fault output is an open drain/collector and shall be pulled up to the Vcc_Host in the host with a resistor in the range 4.7 kΩ to 10 kΩ, or with an active termination according to Table 6.

Parameter	*State*	*Conditions*
RS0	Low	RX signalling rate less than or equal to 4.25 GBd
	High	RX signalling rate greater than 4.25 GBd
RS1	Low	TX signalling rate less than or equal to 4.25 GBd
	High	TX signalling rate greater than 4.25 GBd



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Title: PORT0 SFP+

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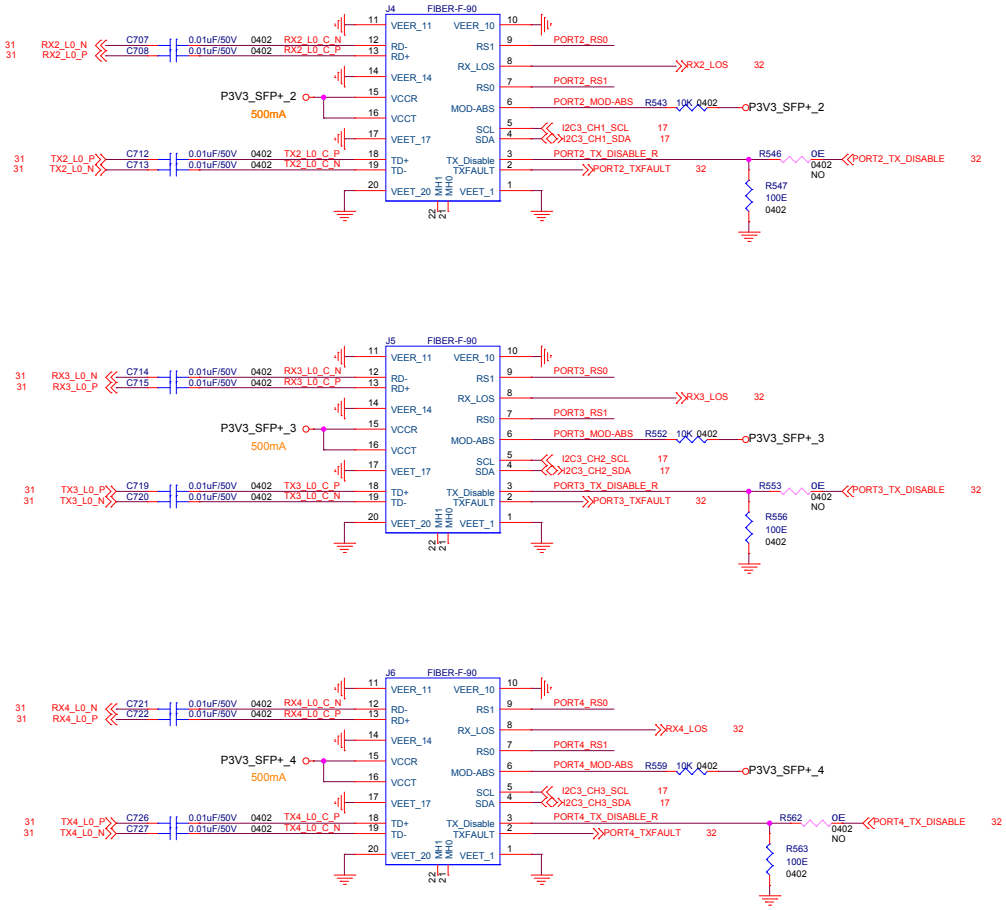

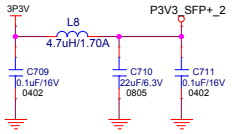

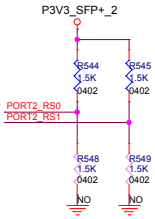

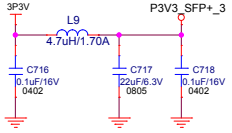

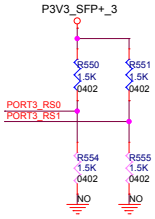

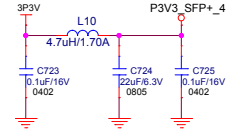

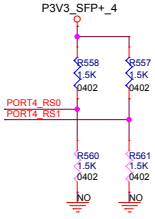

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PORT1 SFP+		
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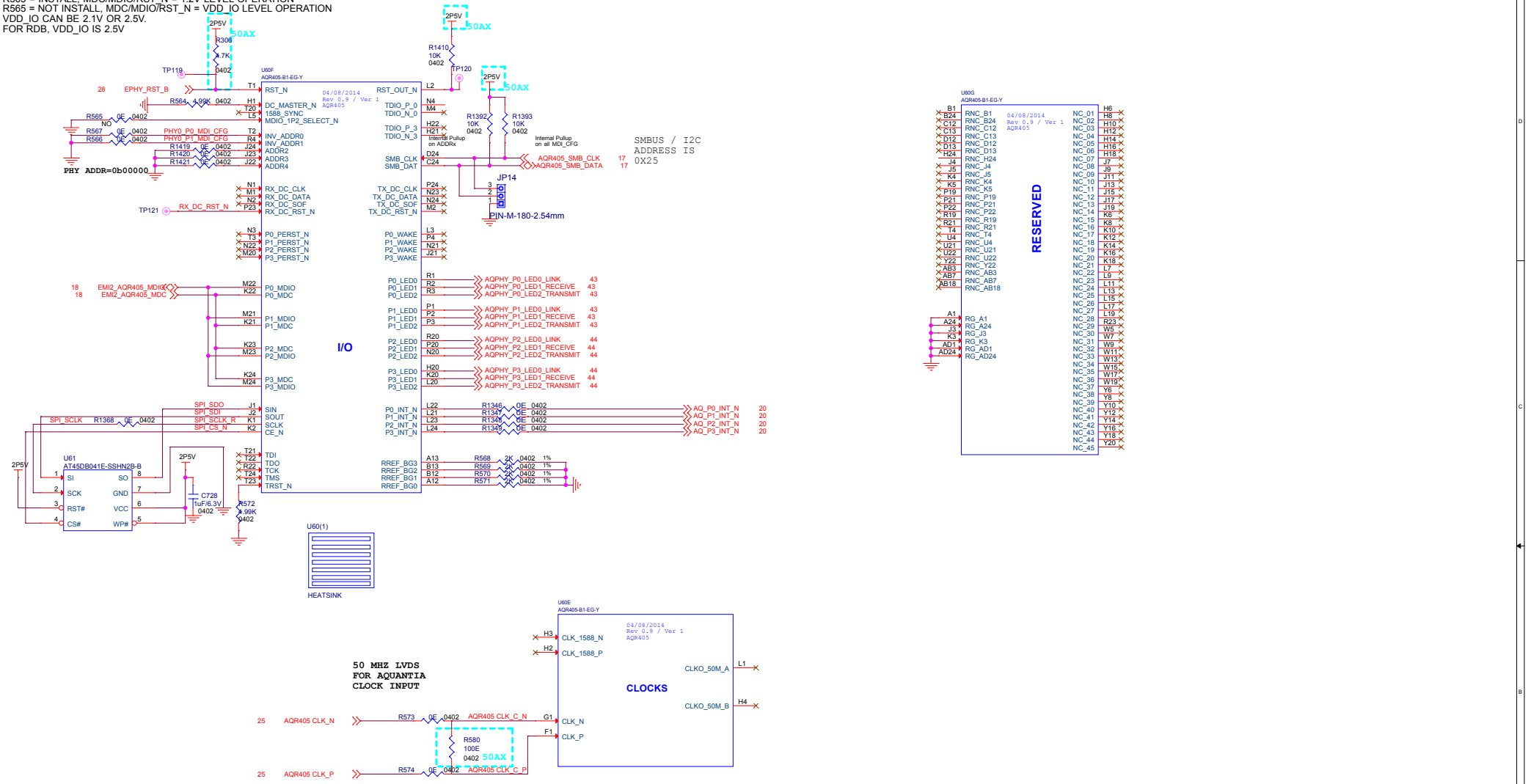
PIN L5 (MDIO_1P2_SELECT_N) :
R565 = INSTALL, MDC/MDIO/RST_N = 1.2V LEVEL OPERATION
R565 = NOT INSTALL, MDC/MDIO/RST_N = VDD_IO LEVEL OPERATION
VDD_IO CAN BE 2.1V OR 2.5V.
FOR RDB, VDD_IO IS 2.5V



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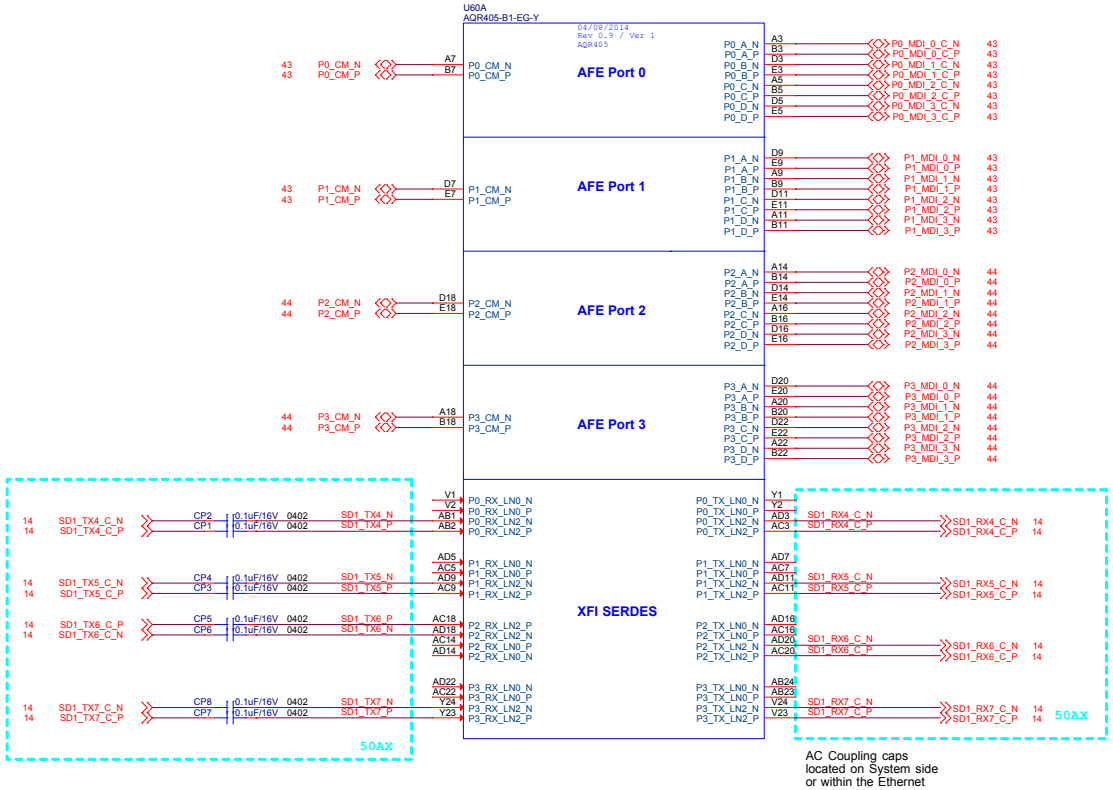

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Title: **AQR405 Datapath**

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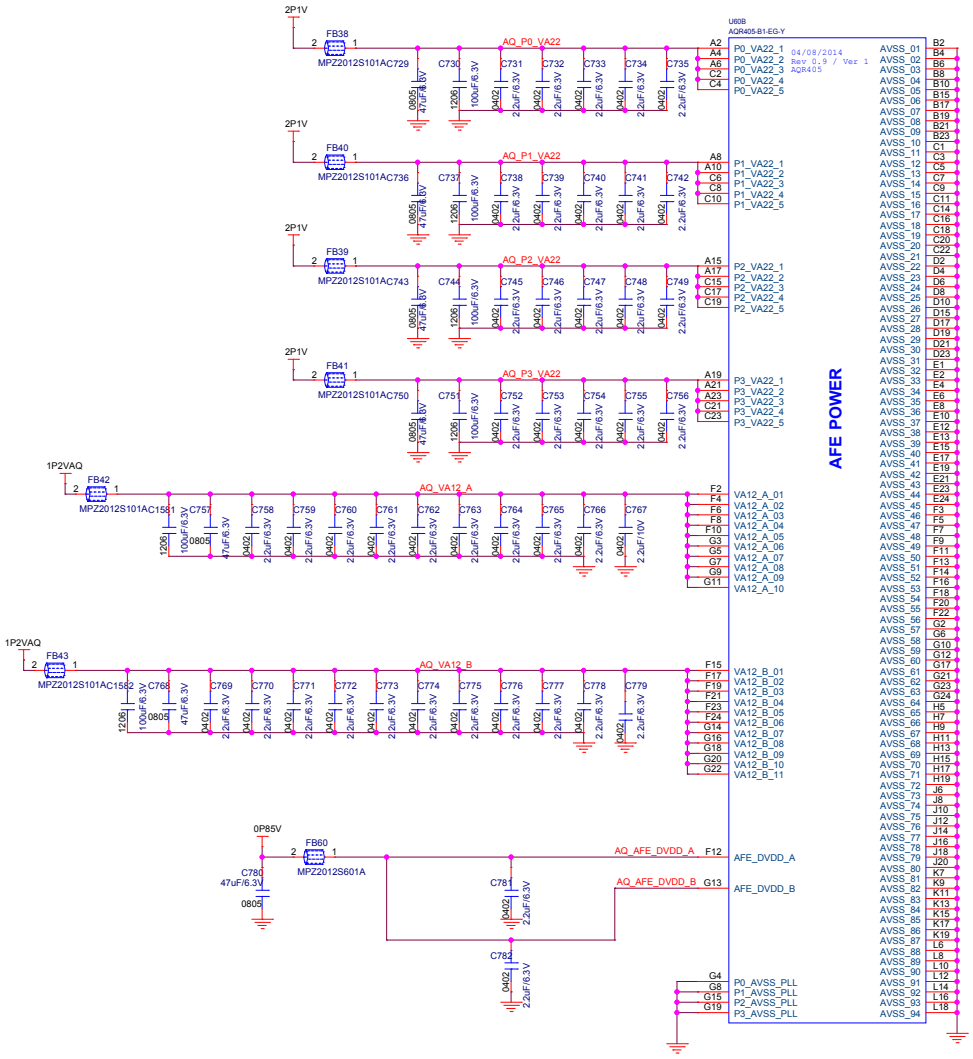

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Title: AQR405 1.2V/2.5V Power

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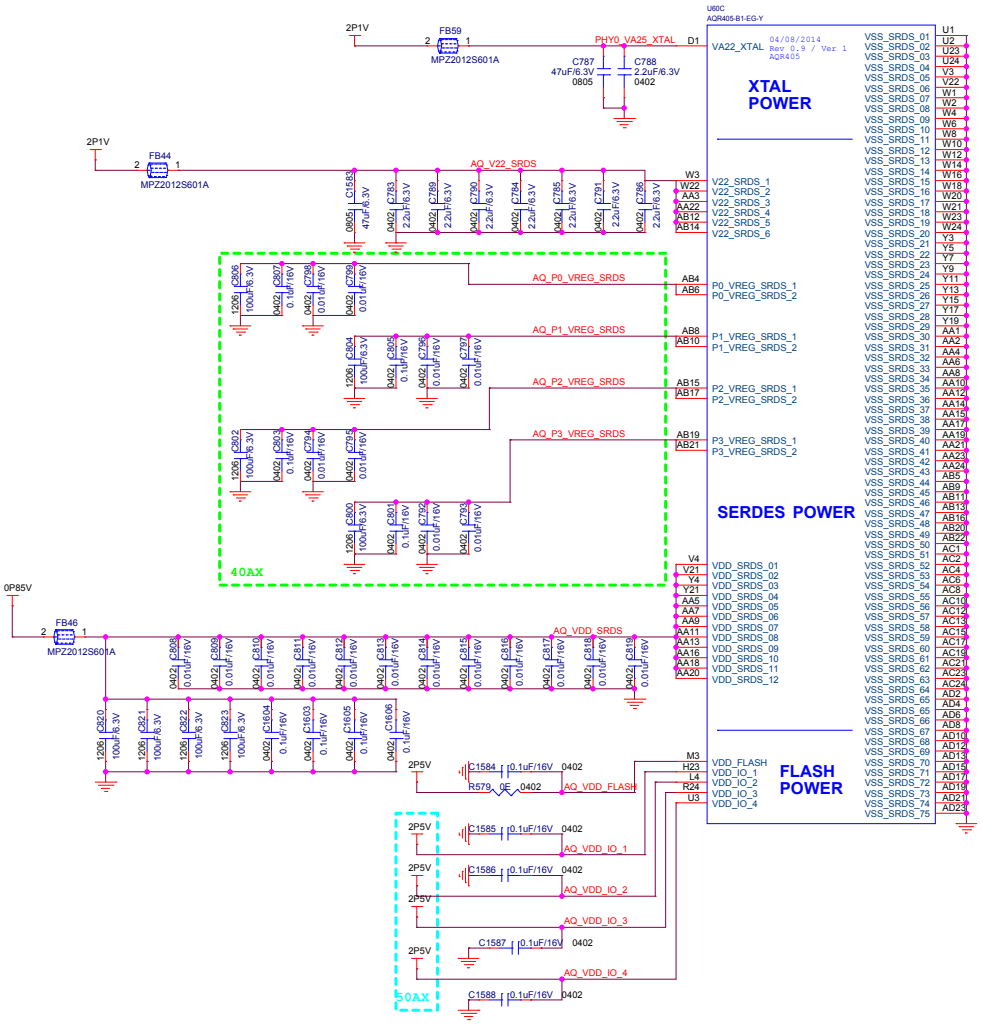

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Title: **AQR405 SERDES Power**

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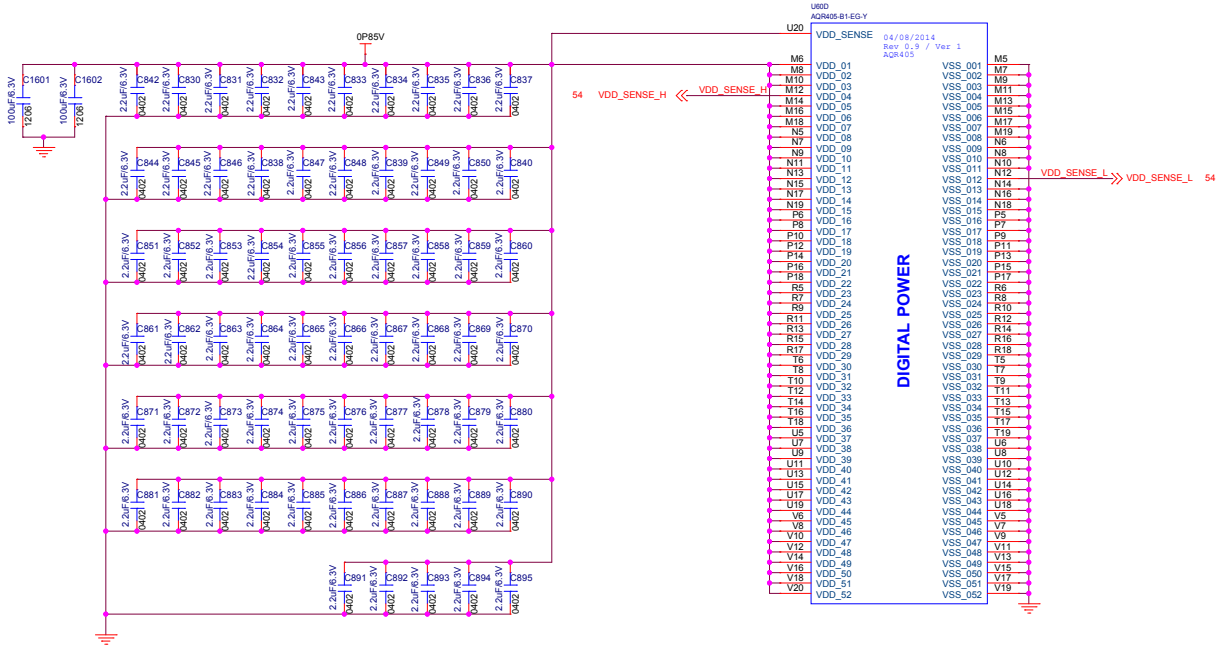

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Title: **AQR405 DIGITAL Power**

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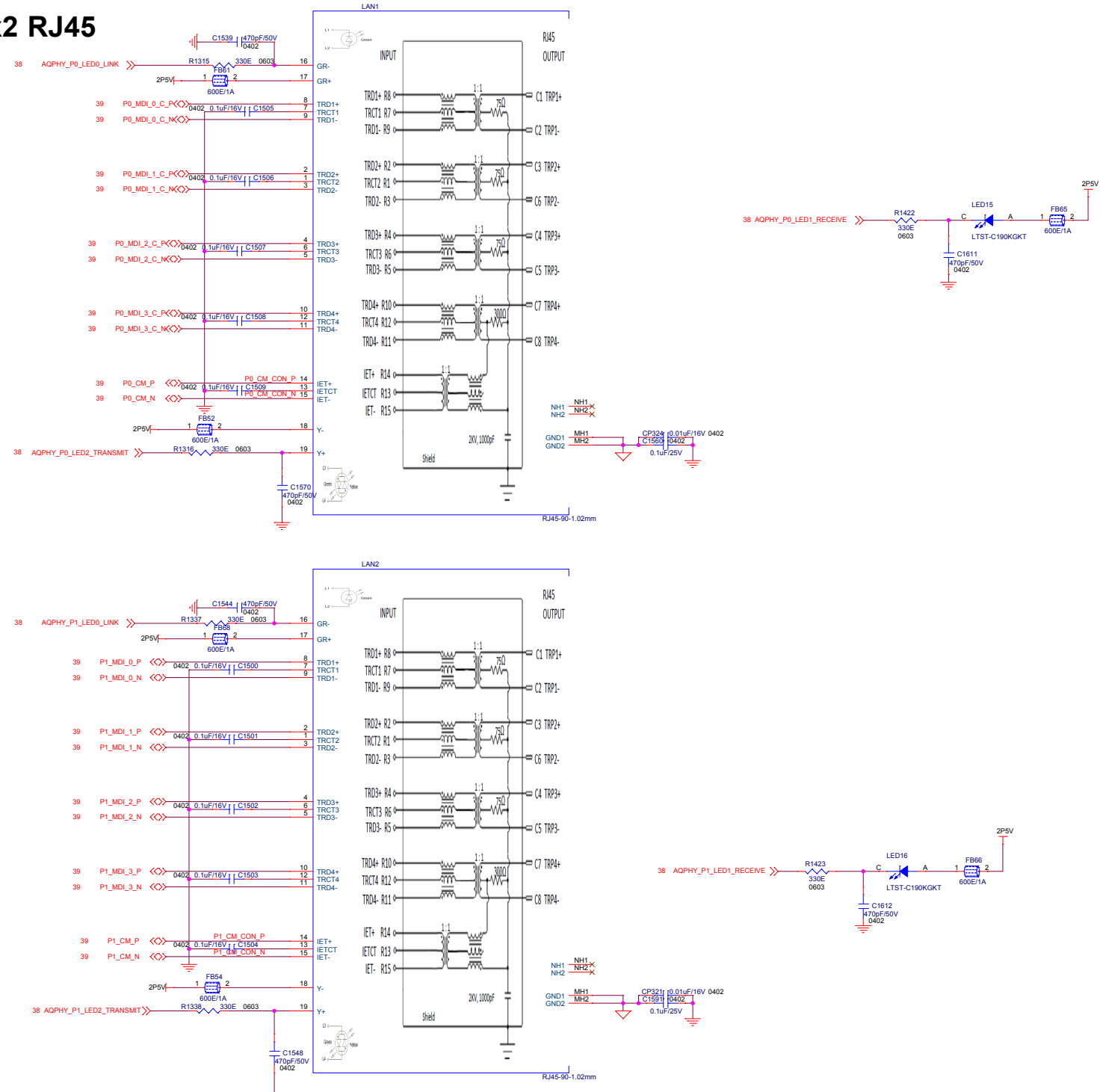
LAN 1x2 RJ45



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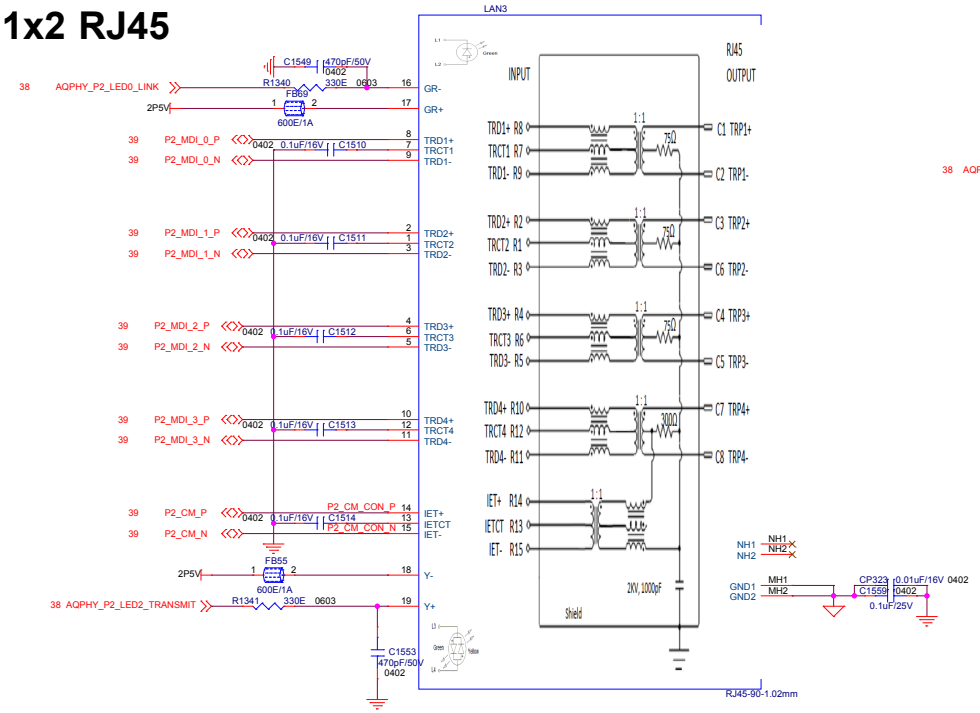
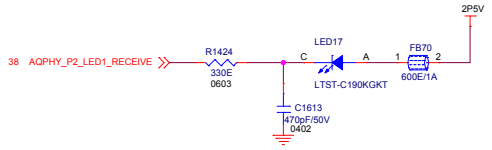
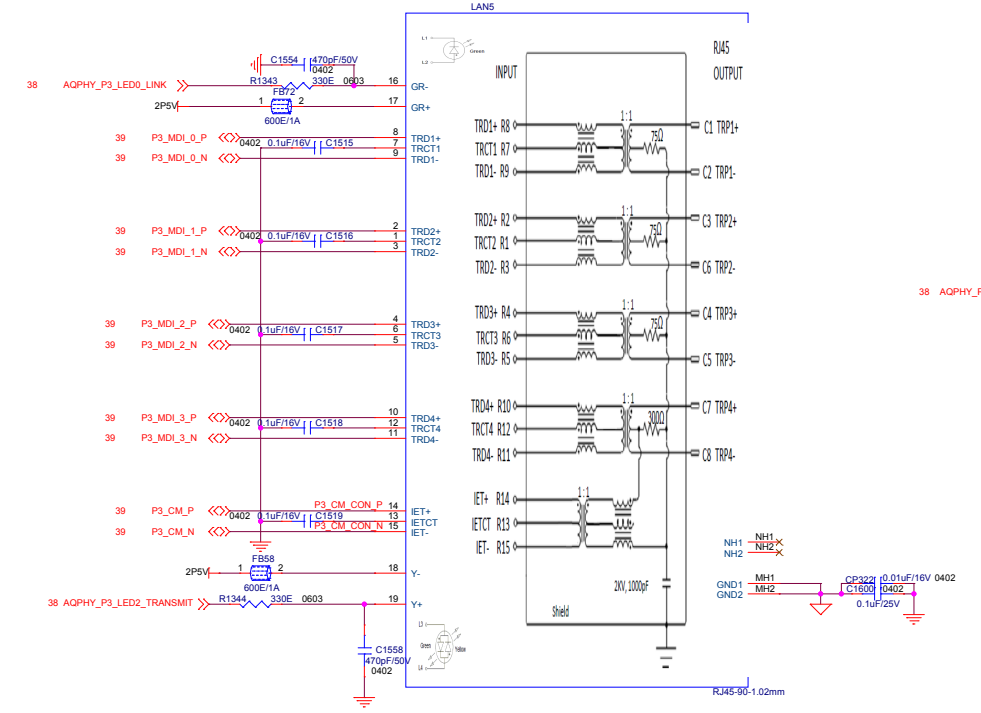
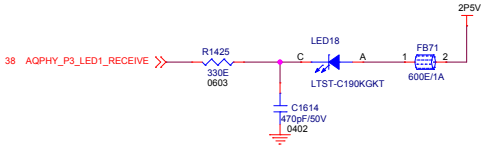
LAN 1x2 RJ45









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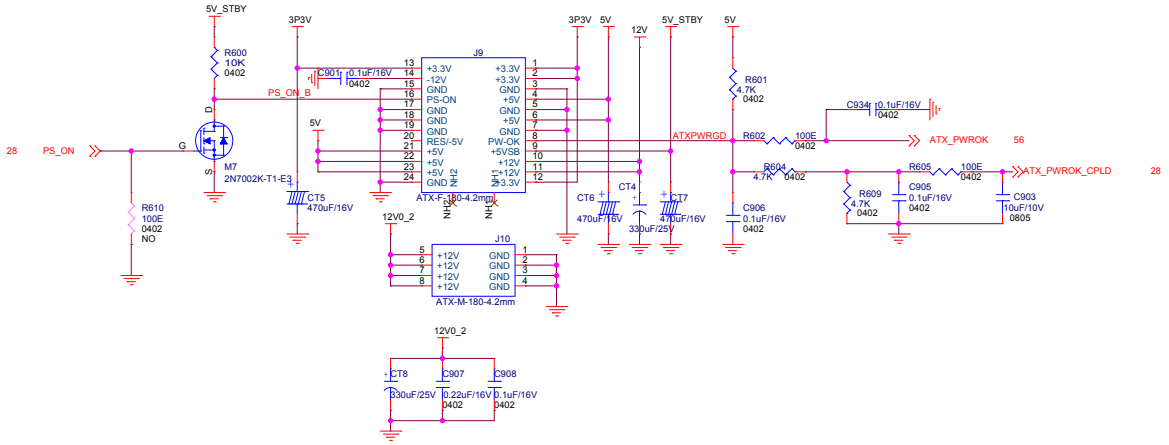
POWER ENTRY



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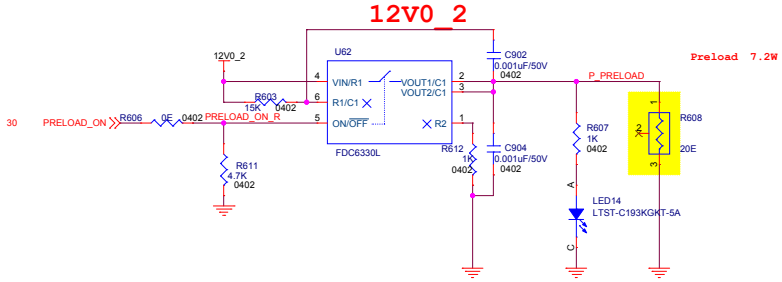

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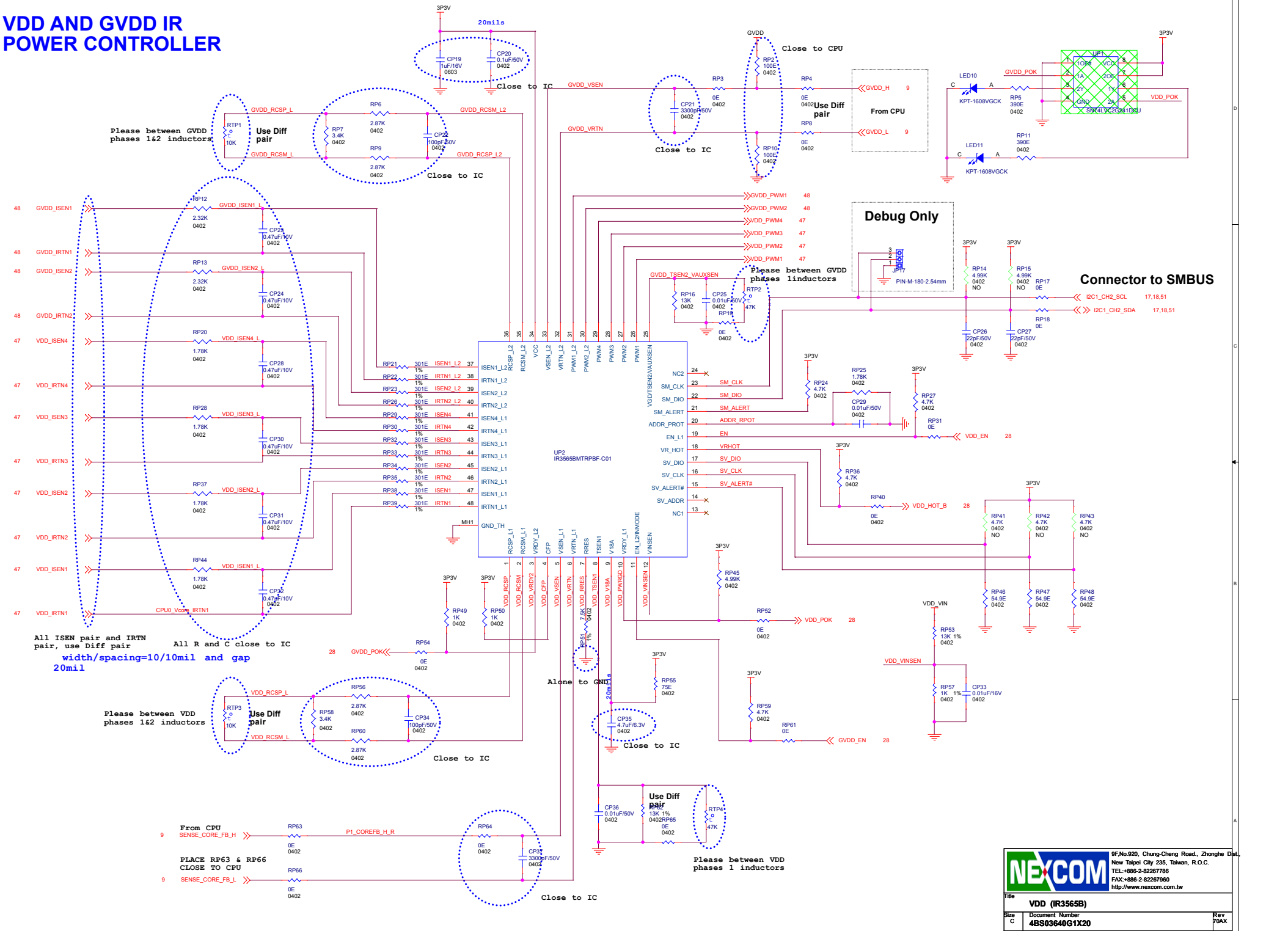
VDD AND GVDD IR POWER CONTROLLER



Title	VDD (IR3565B)
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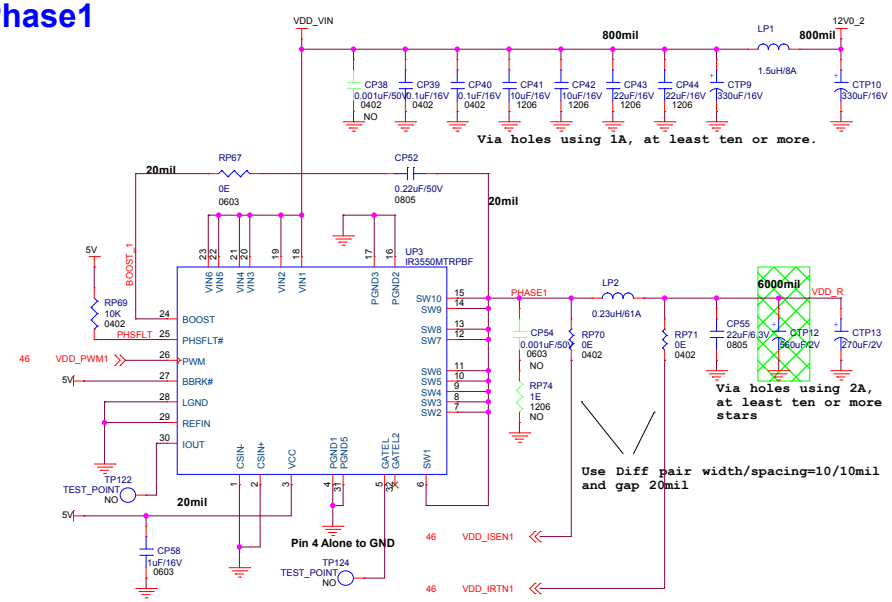
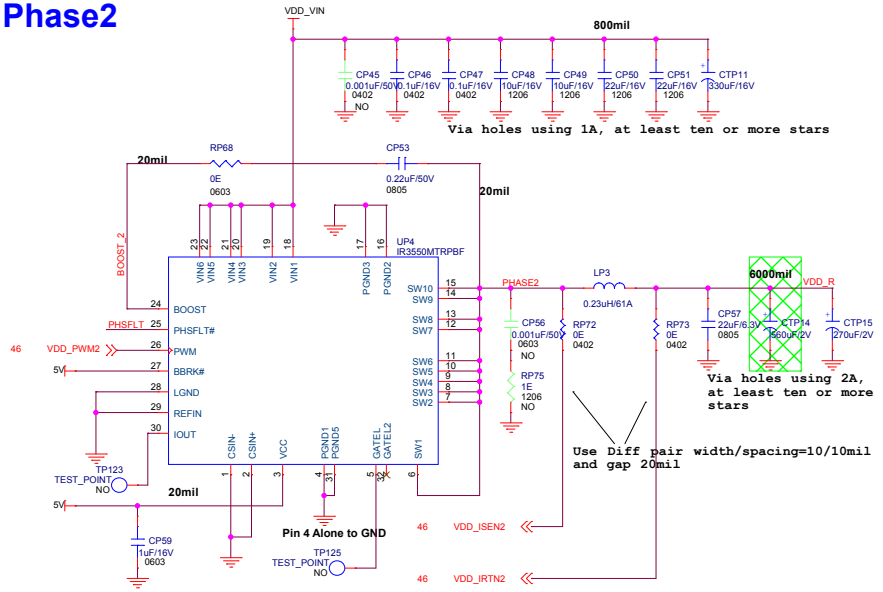
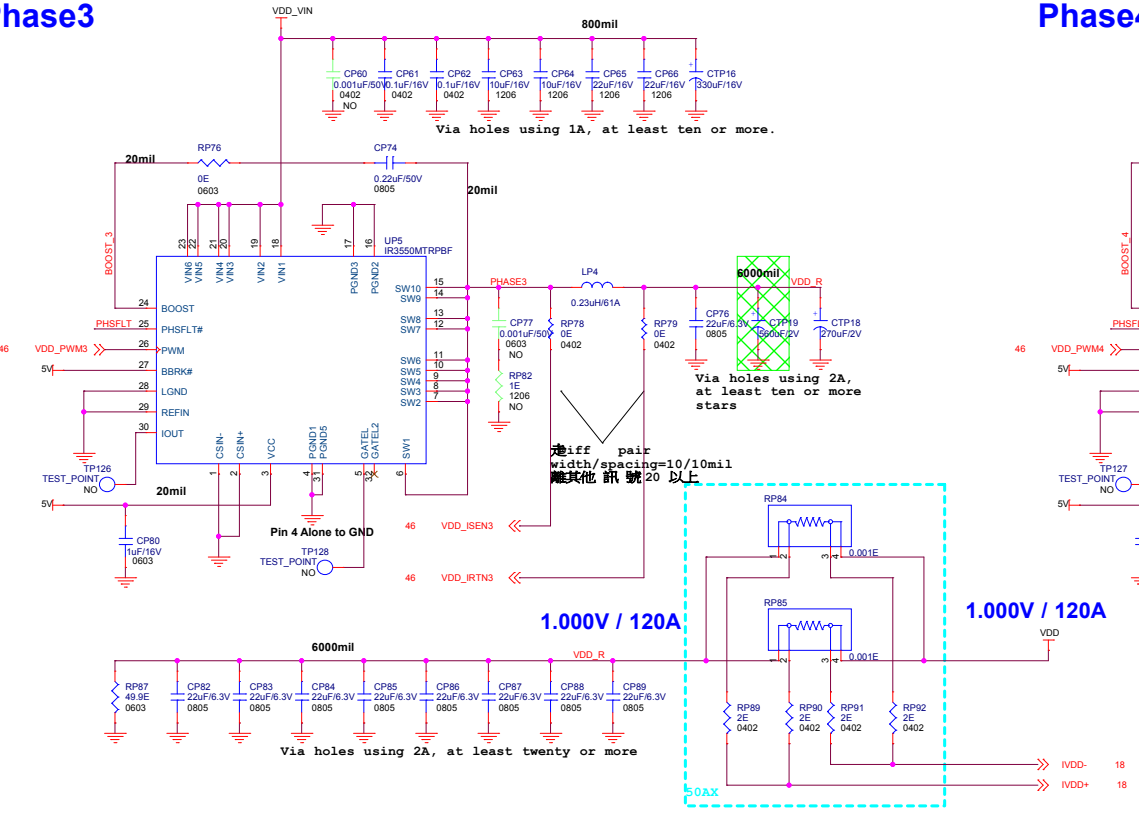
Phase1



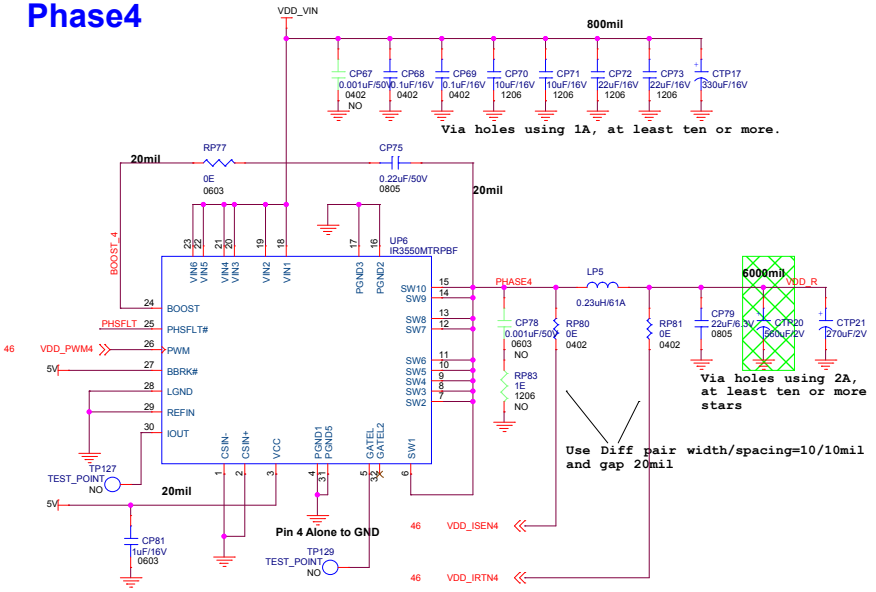
Phase2



Phase3



Phase4



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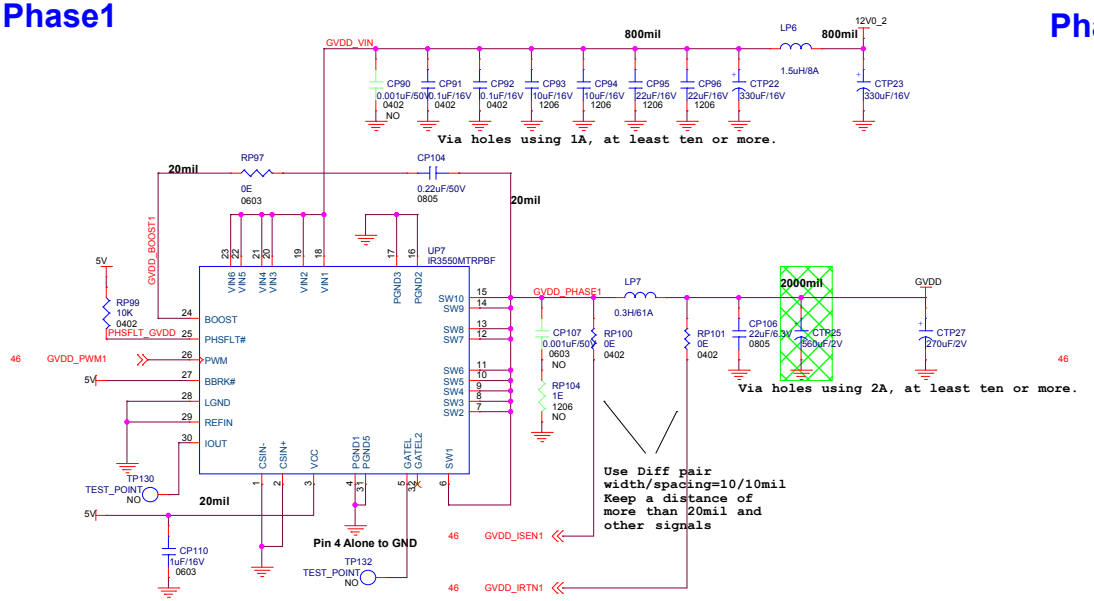
Phase1



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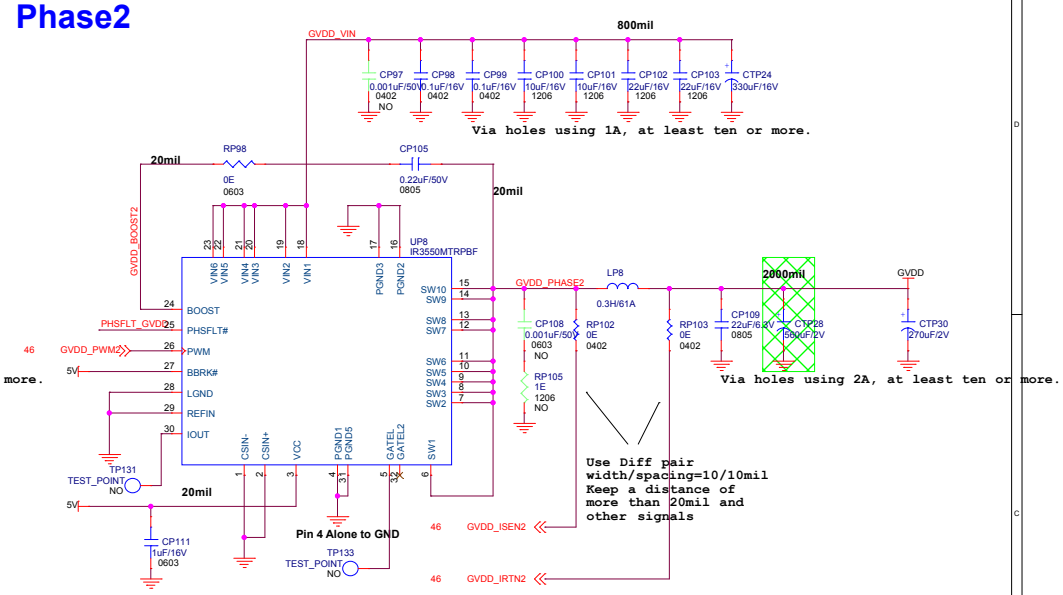
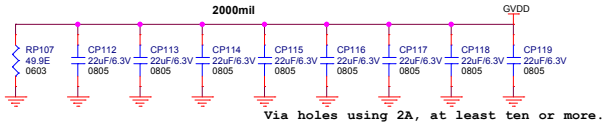


1.200V / 40A



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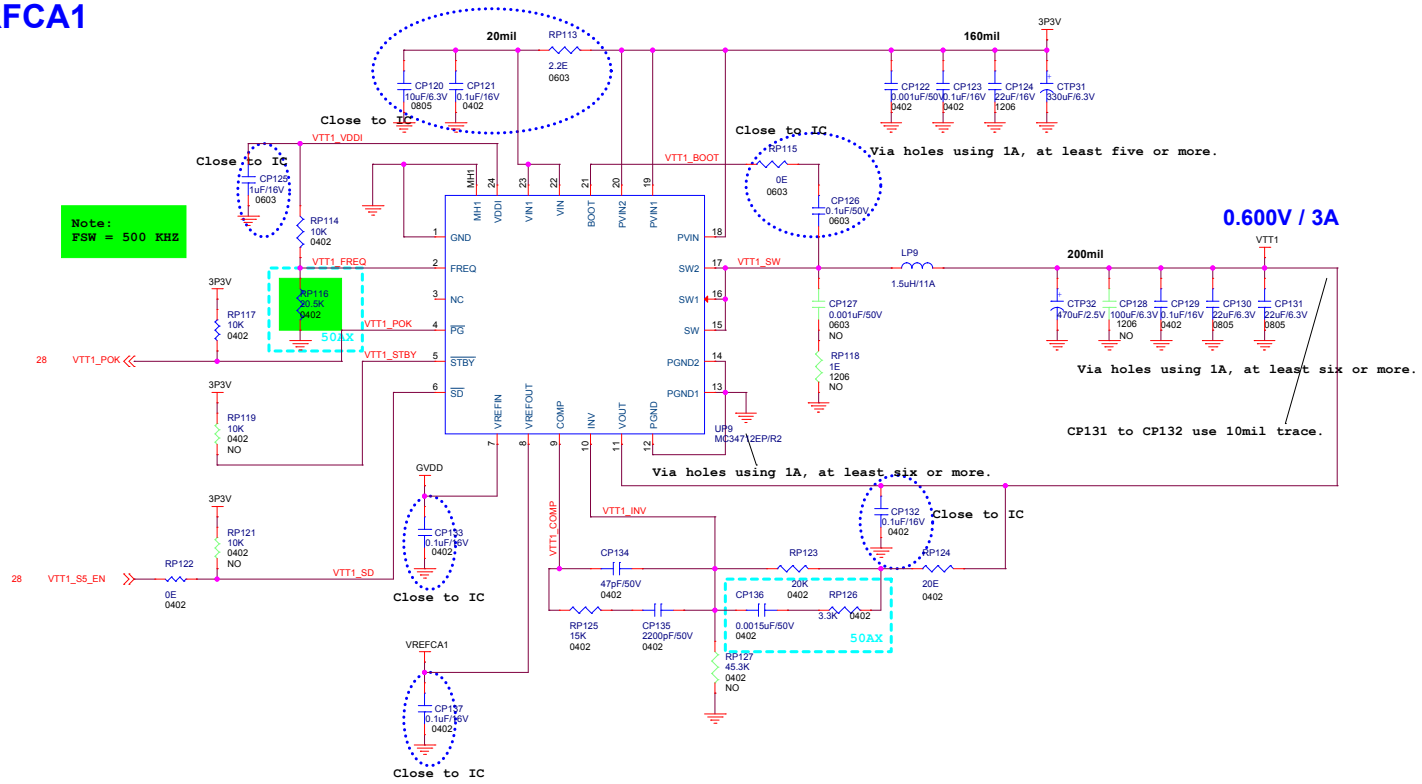
VTT1/VERFCA1



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VTT/VREF (MC34712EP)			
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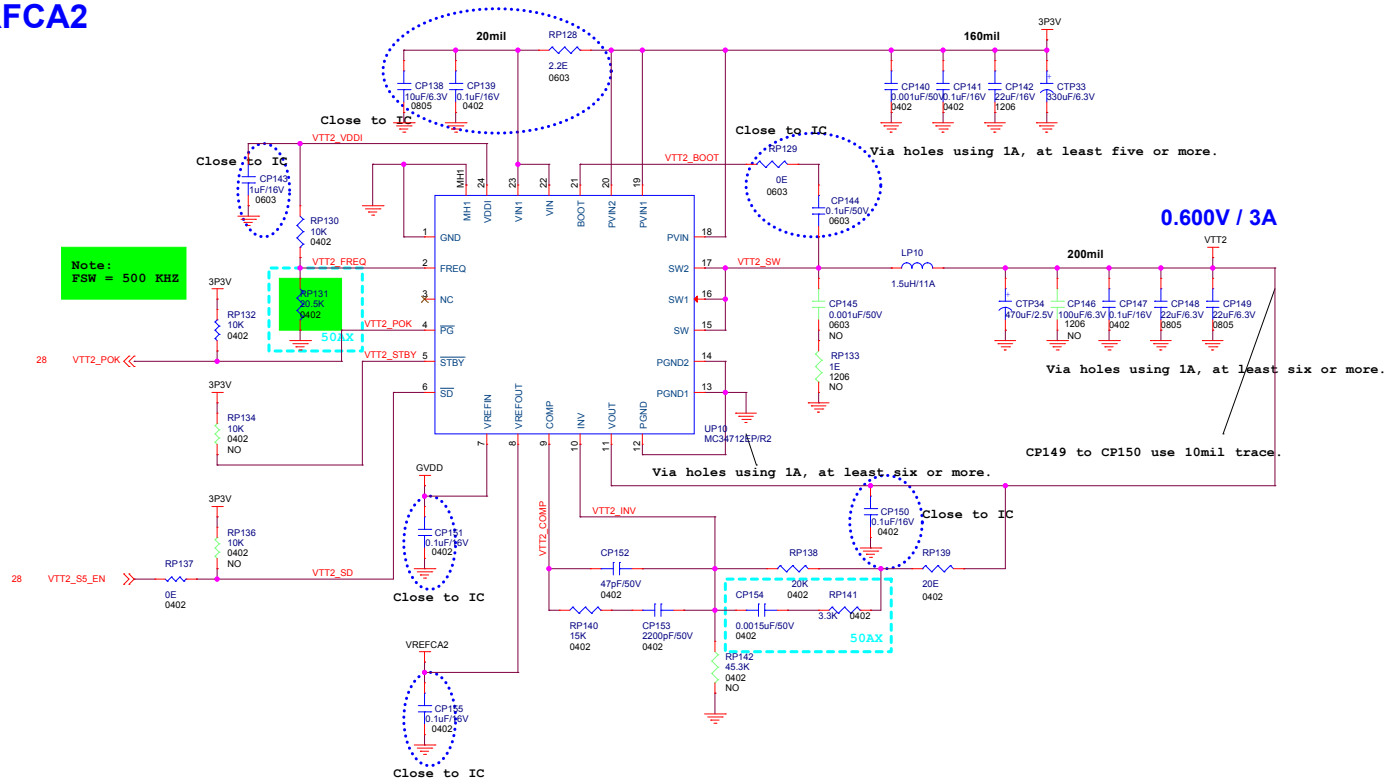
VTT2/VERFCA2



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Title	VTT2/VREF2 (MC34712EP)	
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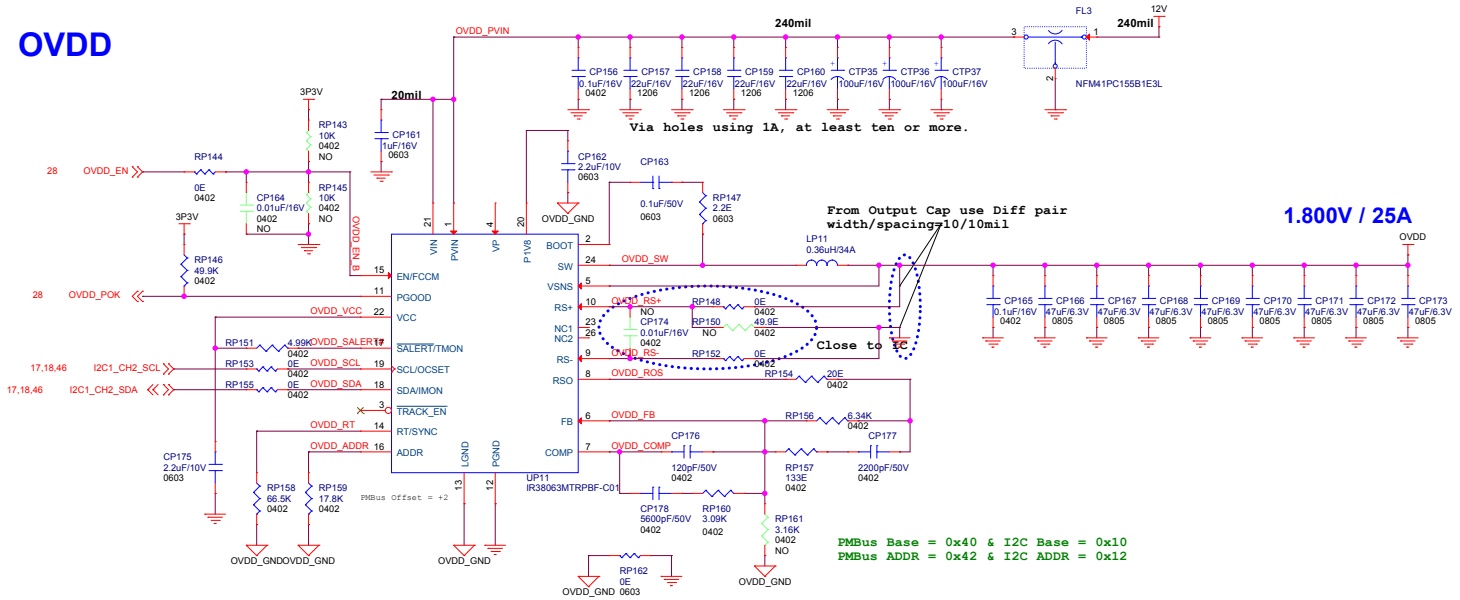
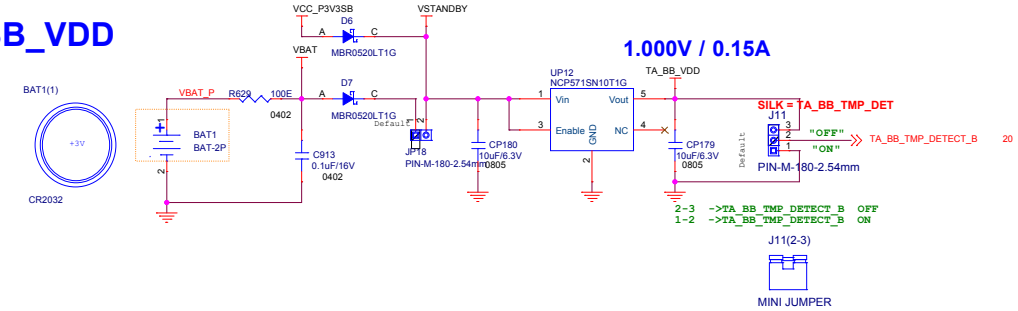
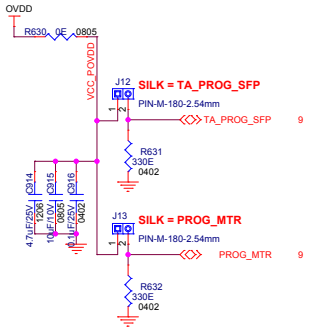
OVDD



TA_BB_VDD



POVDD POWER (1.8V)



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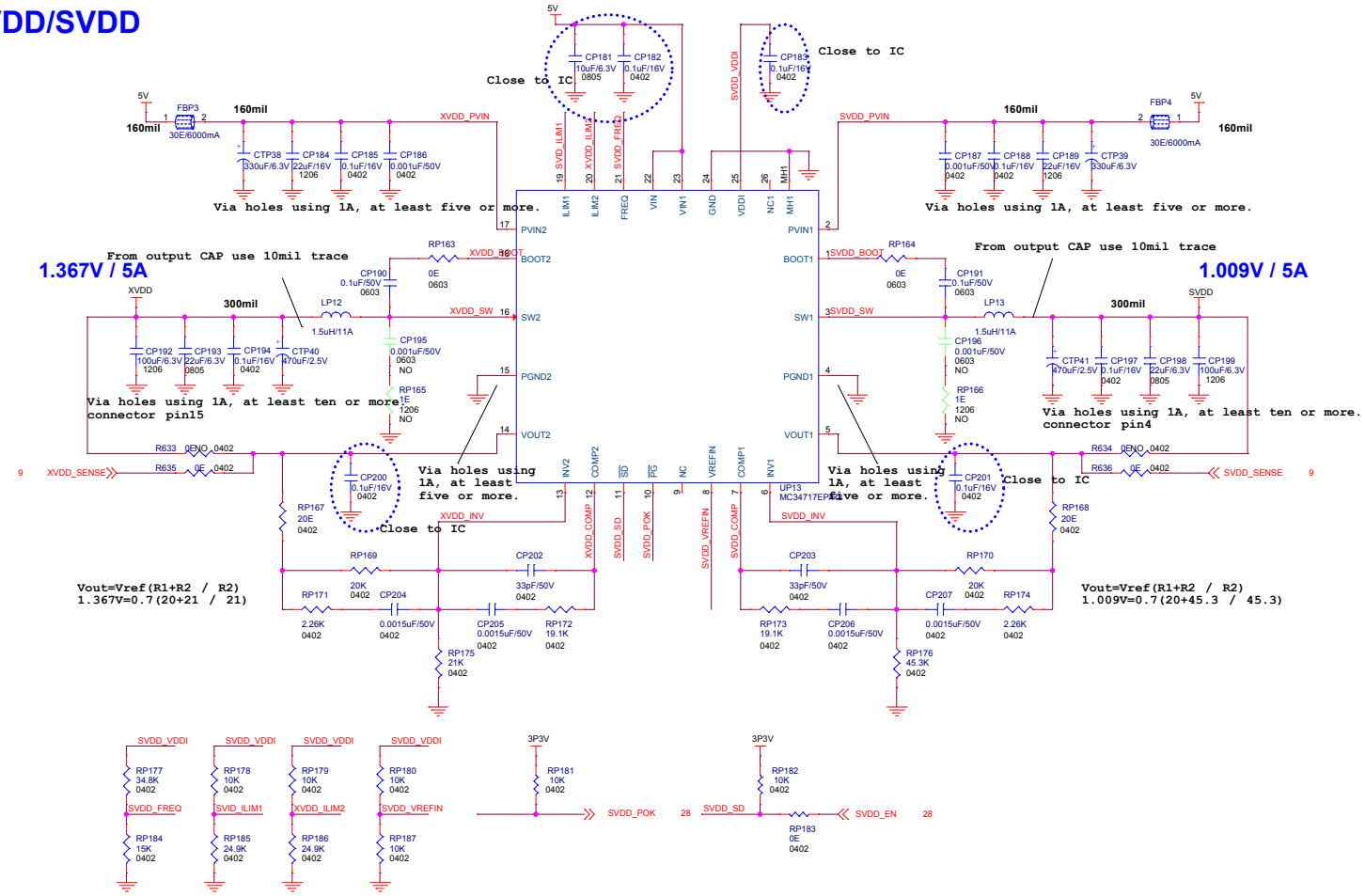
XVDD/SVDD



Title	XVDD/SVDD(MC34717EP)		
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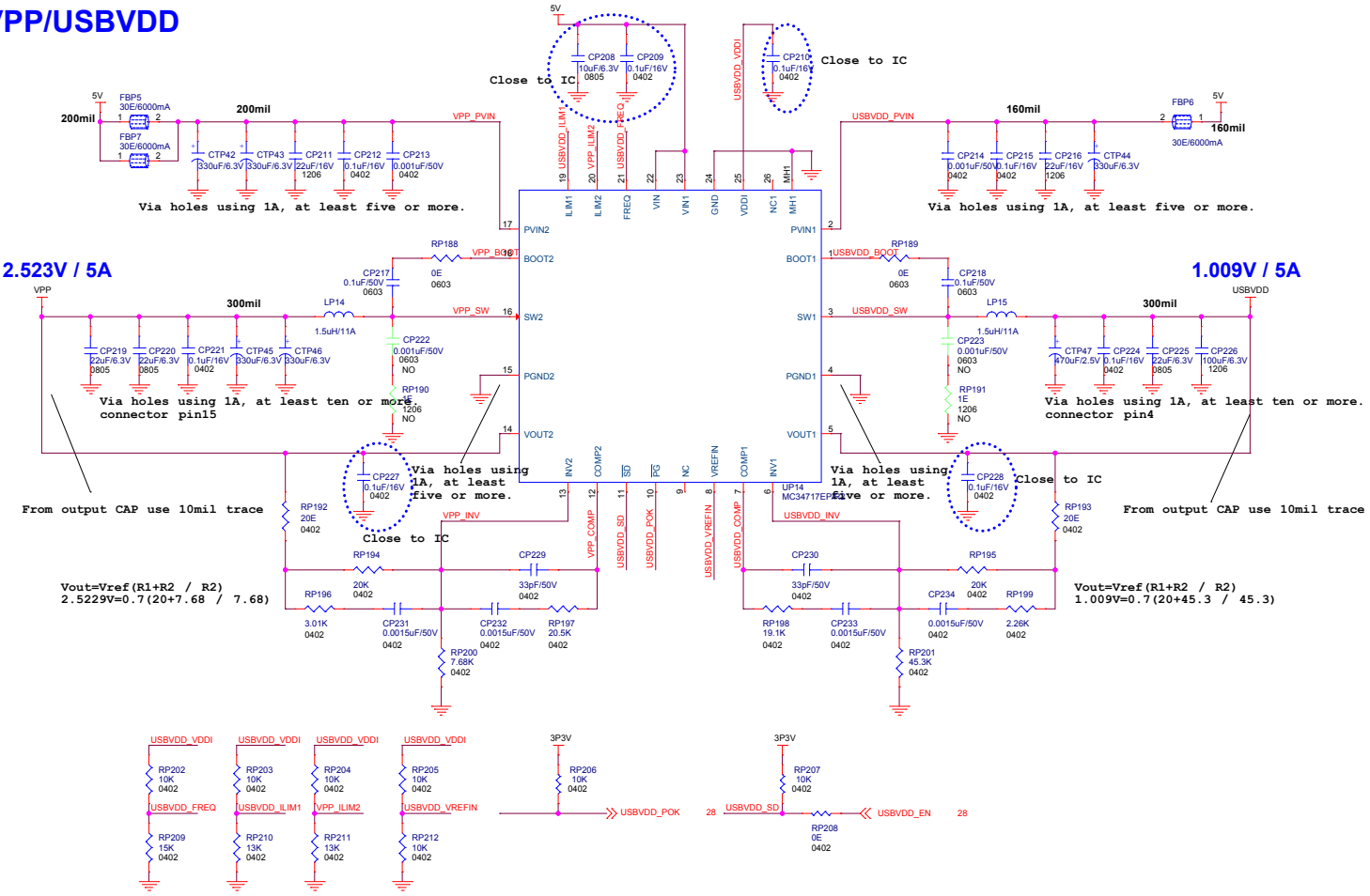
VPP/USBVDD



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Title	VPP/USBVDD(MC34717EP)	
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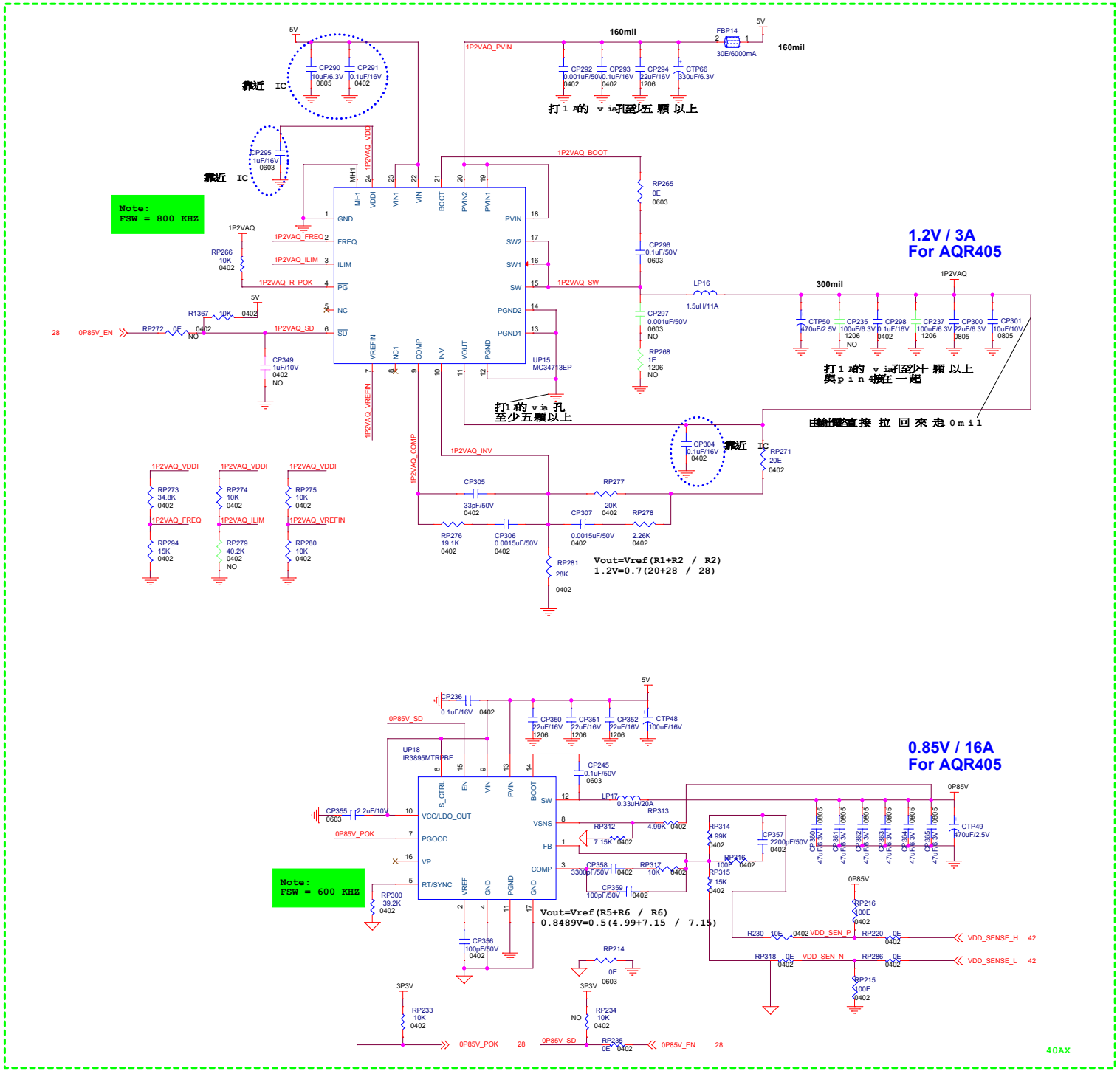
1P2VAQ/0P85V



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Title	1P2VAQ(MC34713)/0P85V(IR3895)	
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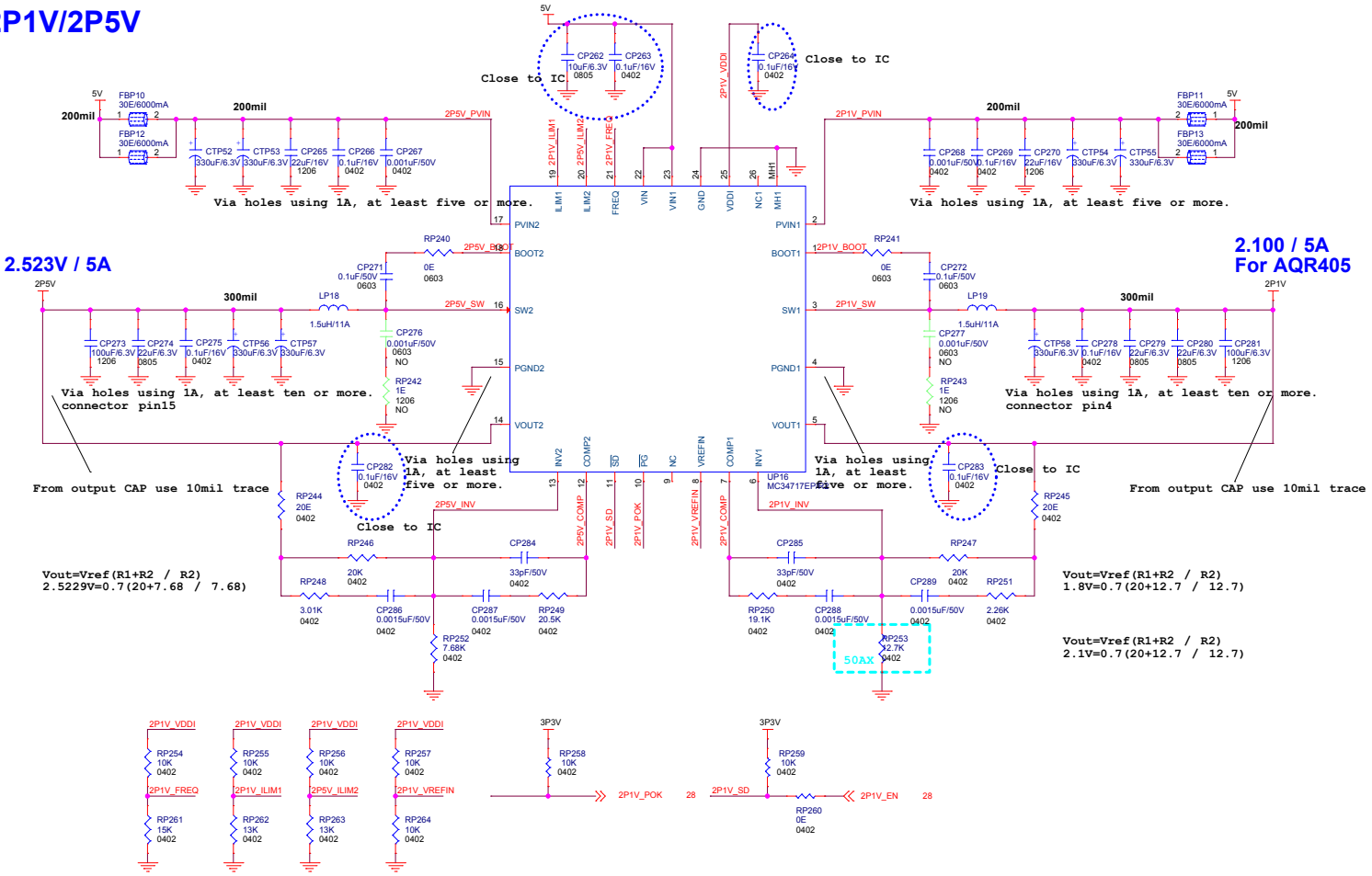
2P1V/2P5V



Title	2P1V/2P5V(MC34717EP)		
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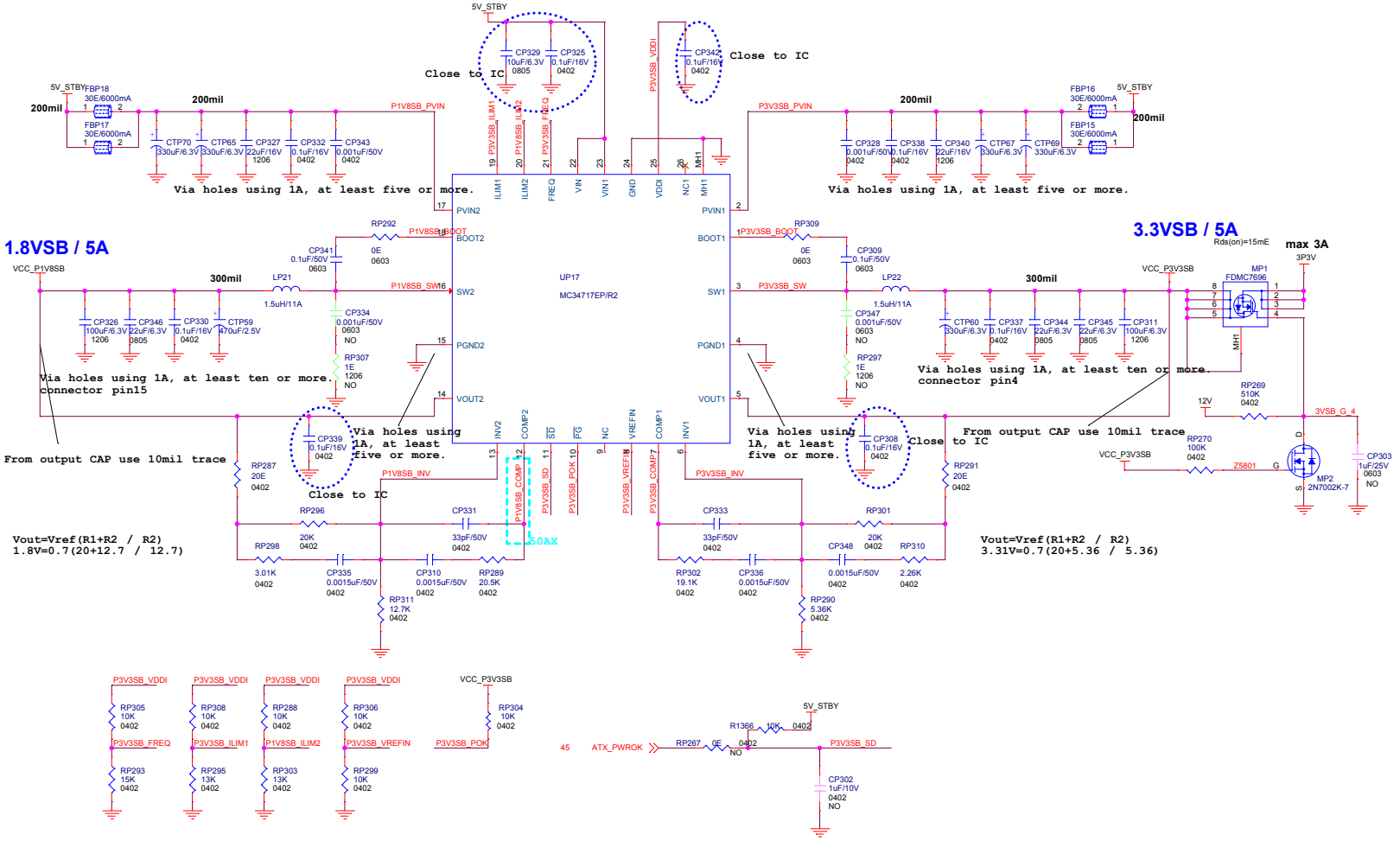
3.3VSB / 1.8VSB



Title	3.3VSB / 1.8VSB		
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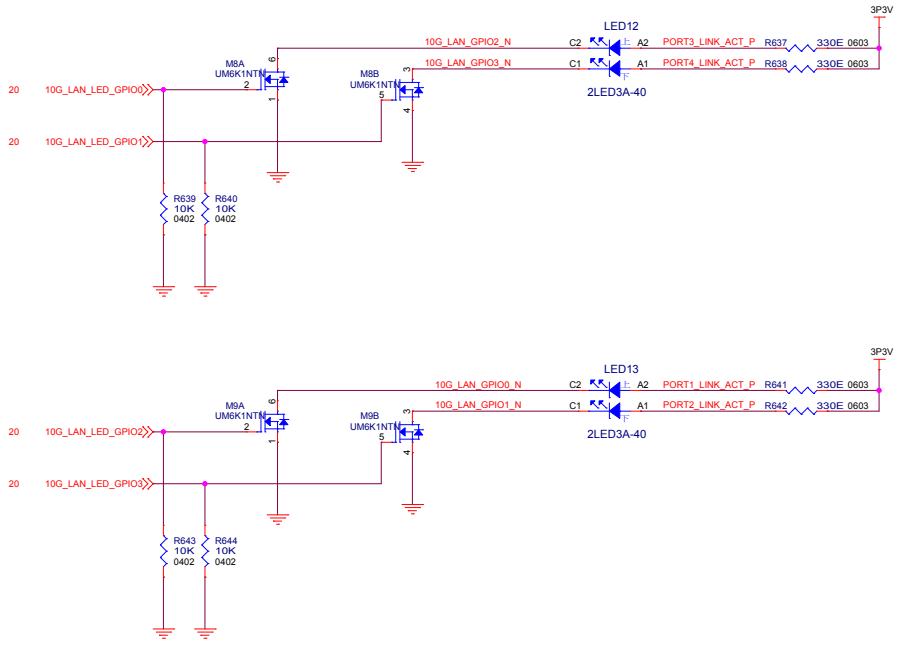

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Title	LED	
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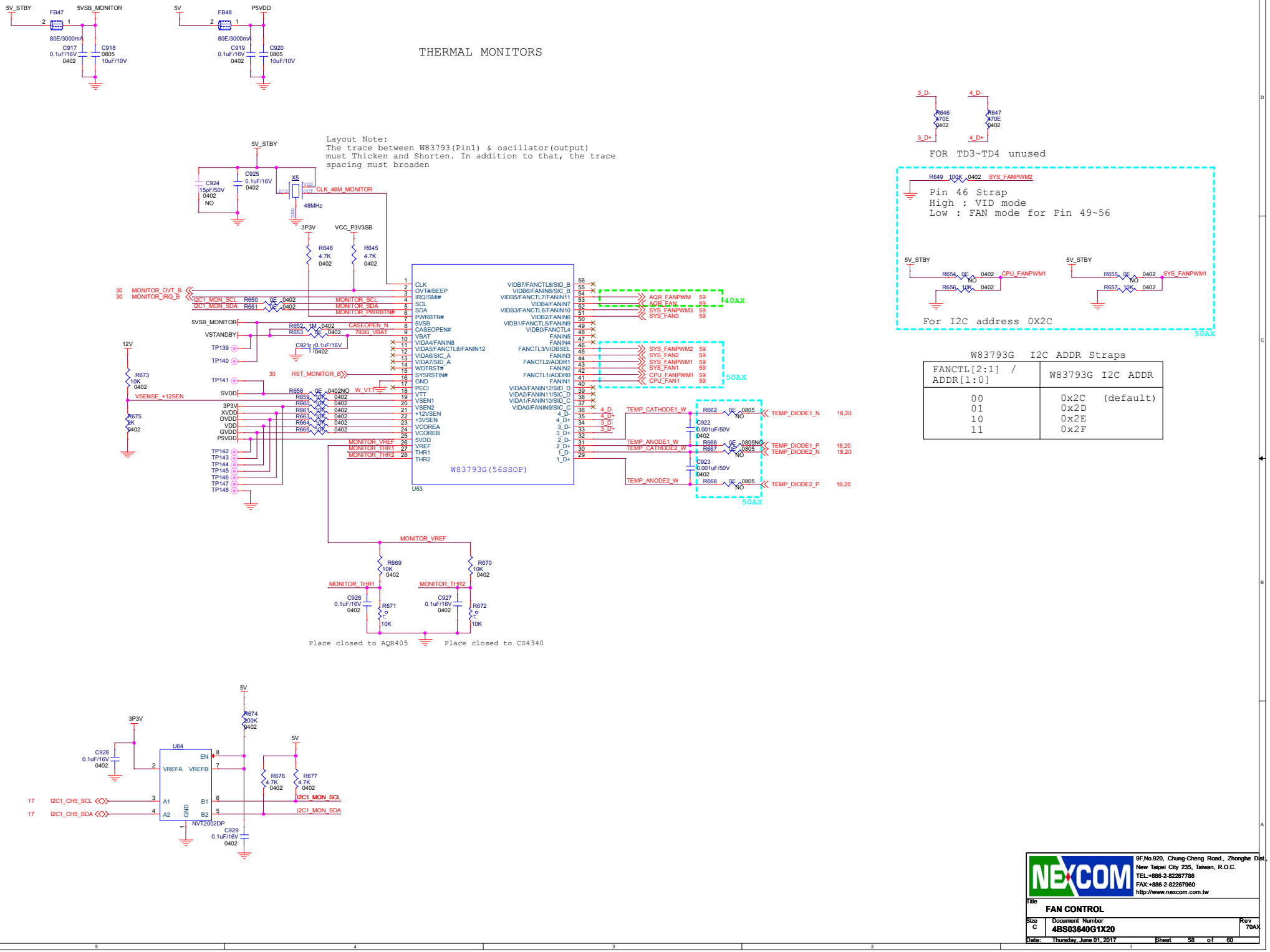
THERMAL MONITORS



W83793G I2C ADDR Straps

FANCTL[2:1] / ADDR[1:0]	W83793G I2C ADDR
00	0x2C (default)
01	0x2D
10	0x2E
11	0x2F

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Title: FAN CONTROL

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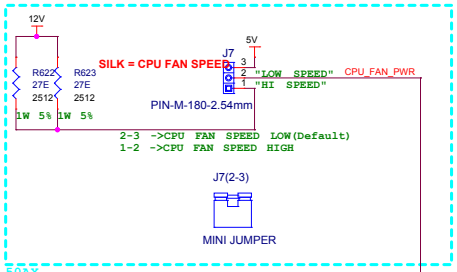
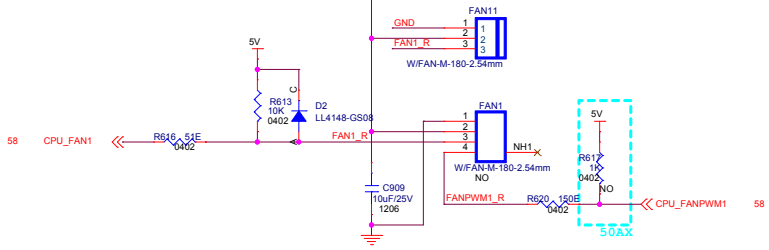
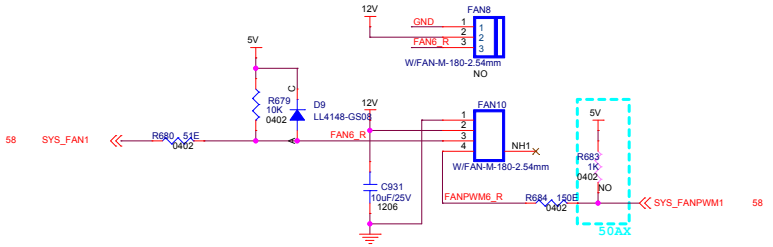
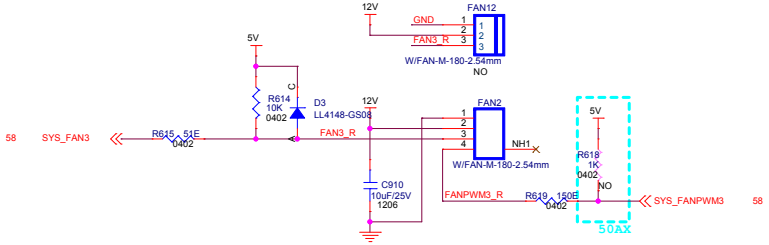




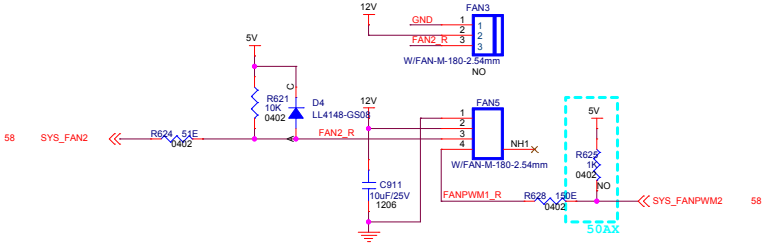
CPU FAN



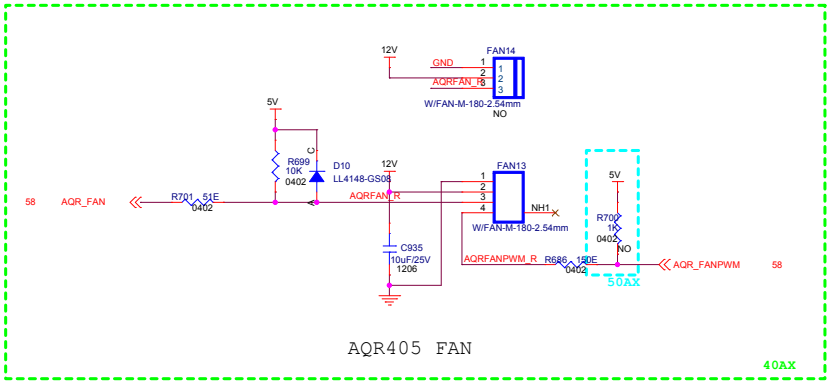
SYS FAN1



SYS FAN3



SYS FAN2



AQR405 FAN

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Title		
FAN CONTROLOR		
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DATE	Revision	Note
2014/07/25	10AX	First draft
2014/11/28	20AX	Page.12 1.U7.Pin 84 - should be connected to D2_MCS_B2 2.U7.Pin 89 - should be connected to D2_MCS_B3 3.U7.Pin 93 - should be connected to GVDD 4.U7.Pin 237 - should be connected to GVDD
2014/12/24	20BX	Page.9,51 1. Change FL1, FL2, FL3 form 4E0155B101X00 to 4E41PC1501X00 Page.26 1. Change U199 U200 U201 U203 U204 from 3ILVC24401X00 to 3I00024401X00 Page.28 ,29,30 1. Change U50 from 3G01270F01X00 to 3G01270F49X00 Page,28 1. Remove R470 Page.20 5. Remove U37, R304, R306, R307 ,R308 6. Mount R310, R311, R312, R313
2014/12/26	30AX	Page.20 1. Del U37, C448, C449, C450, R324 2. R309 connector to OVDD 3. Del COP_TDI, DUT_TDI connector to R314 Pin1 4. Del COP_TMS, DUT_TMS connector to R315 Pin1 5. Del COP_TCK, DUT_TCK connector to R316 Pin1 6. Del COP_TDO, DUT_TDO connector to R317 Pin1 Page.26 1. Change form 4WJ008D003X00 to 4WJ008S002X00 2. Change U199, U200, U201, U203, U204 from 3100024401X00 to 3ILVC24401X00 Page.56 1. Change UP17 from MC34713EP to MC34717EP/R2 2. Add VCC_P1V8SB for CPLD
2015/02/02	40AX	Page. 9 (Use LS2085A PCB footprint) 1. Change U1 form 4SCS129201X00 to 71F202G201X00 Page.12 (Fix U6 and U7 have same I2C address (0x54)) 1. U6 Pin139 connect to VCC_P3V3SB 2. U6 Pin140 connect to VCC_P3V3SB 3. U6 Pin238 connect to GND Page.12 (Fix U6 D2_MCLK1P and D2_MCLK1N signals are reversed) 1. U6 Pin219 connect to D2_MCLK1N 2. U6 Pin218 connect to D2_MCLK1P Page.25 (Fix Clocks are not generated properly to the PCIe slots) 1. NC the R394,R399 Page.26(Change to allow software TESTSEL control) 1. Delete R432 2. Change SW8 pin 12 from OVDD to VCC_P3V3SB. 3. Change net name to SW_TESTSEL_B. Page.28 (Update CPLD PCB REVISION) 1. NC the R1413 Page.41(cute Px VREG_SRDS) 1. Cut AQ_P0_VREG_SRDS->AQ_P3_VREG_SRDS Page.54(Change 1.2V & 0.85V power solution) 1. Del the MC34717 2. Add the MC34713 for 1.2V 3. Add the IR3895 for 0.85V Page.58 (Add AQR405 FAN signal to FAN CONTROL) 1. U63 pin53 connect AQR_FAN 2. U63 pin54 connect AQR_FANPWM Page.59 (Add AQR405 FAN connector) 1. Add FAN13
2014/04/11	40BX	Page.16 1. NC the TVS2,TVS3,TVS4,TVS5,TVS7,TVS8,TVS9,TVS10
2014/04/30	40CX	Page.9 1. Add the U1(1), U1(2), U1(3)
2015/05/22	40DX	Page.21 1. Change the U39 from 3MFS001G04X00 to 3MFS001G07X00
2015/06/30	40EX	Page.49 1. Change the RP116 from 3.3K to 20.5K 2. Change the CP136 from 0.001uF/50V to 1.5nF/50V 3. Change the RP126 from 300E to 3.3K Page.50 1. Change the RP131 from 3.3K to 20.5K 2. Change the CP154 from 0.001uF/50V to 1.5nF/50V 3. Change the RP141 from 300E to 3.3K Page.55 1. Change the RP253 from 10K to 12.7K Page.59 1. NC the FAN1
2015/09/02	40FX	Page.19 1. Change the U29 SPI FLASH from N25Q512A11GSF40F to MT25QU512ABB8ESF-0SIT (from 3MAS512M01X01 to 3MAS512M02X00) Page.21 1. Change the U39 NOR FLASH from S29GL01GP13TFIV10 to S29GL01GS11TFIV10 (from 3MFS001G08X01 to 3MFS001G10X01) Page.26,32,45 1. Change the M2 M3 M5 M6 M7 from 2N7002 to 2N7002K-T1-E3 (from 4H2N700204X00 to 4H2N700206X00)
2015/12/08	40GX	Page.17 1. Populate R189, R190, R228, R229 with 10K ohm resistors (fix the I2C issues)

DATE	Revision	Note
2015/05/04	50AX	Page.9 1. Add the R27 Page.18 1. Add the U23(VDD I/W Measure IC) Page.24 1. Change the SATA connectors CON2, CON3 from LE18077-Z54D-4H to 678005025. Page.47 1. Add the Kirchoff circuit. (RP84, RP85, RP89, RP90, RP91, RP92) Page.11 (DDR1 Slot swap) 1. U5 Change the reference name from U5 to U4 2. U4 Pin139 connect to VCC_P3V3SB 3. U4 Pin 140 connect to GND 4. U4 Pin 238 connect to GND 5. U4 Pin78 connect to TP18 6. U4 Pin58 connect to RST_MEM1_B 7. U4 Pin87 connect to D1_MODT0 8. U4 Pin91 connect to D1_MODT1 9. U4 Pin60 connect to D1_MCKE0 10. U4 Pin203 connect to D1_MCKE1 11. U4 Pin84 connect to D1_MCS_B0 12. U4 Pin89 connect to D1_MCS_B1 13. U4 Pin93 connect to D1_MCS_B2 14. U4 Pin237 connect to D1_MCS_B3 15. U4 Pin75 connect to D1_MCLK0N 16. U4 Pin74 connect to D1_MCLK0P 17. U4 Pin219 connect to D1_MCLK1N 18. U4 Pin218 connect to D1_MCLK1P 19. U4 Change the reference name from U4 to U5 20. U5.Pin139 connect to GND 21. U5.Pin140 connect to VCC_P3V3SB 22. U5.Pin238 connect to GND 23. U5.Pin78 connect to TP19 24. U5.Pin58 connect to RST_MEM2_B 25. U5 Pin87 connect to D1_MODT2 26. U5 Pin91 connect to D1_MODT3 27. U5 Pin60 connect to D1_MCKE2 28. U5 Pin203 connect to D1_MCKE3 29. U5 Pin84 connect to D1_MCS_B2 30. U5 Pin89 connect to D1_MCS_B3 31. U5 Pin93 connect to GVDD 32. U5 Pin237 connect to GVDD 33. U5 Pin75 connect to D1_MCLK2N 34. U5 Pin74 connect to D1_MCLK2P 35. U5 Pin219 connect to D1_MCLK3N 36. U5 Pin218 connect to D1_MCLK3P 37. DNP the R39, R40, R41, R42, R43, R44, R45, R46, R47 Page.12 (DDR2 Slot swap) 1. U7 Change the reference name from U7 to U6 2. U6 Pin139 connect to VCC_P3V3SB 3. U6 Pin 140 connect to VCC_P3V3SB 4. U6 Pin 238 connect to GND 5. U6 Pin78 connect to TP25 6. U6.Pin58 connect to RST_MEM3_B 7. U6 Pin87 connect to D2_MODT0 8. U6 Pin91 connect to D2_MODT1 9. U6 Pin60 connect to D2_MCKE0 10. U6 Pin203 connect to D2_MCKE1 11. U6 Pin84 connect to D2_MCS_B0 12. U6 Pin89 connect to D2_MCS_B1 13. U6 Pin93 connect to D2_MCS_B2 14. U6 Pin237 connect to D2_MCS_B3 15. U6 Pin75 connect to D2_MCLK0N 16. U6 Pin74 connect to D2_MCLK0P 17. U6 Pin219 connect to D2_MCLK1N 18. U6 Pin218 connect to D2_MCLK1P 19. U6 Change the reference name from U6 to U7 20. U7 Pin139 connect to GND 21. U7 Pin 140 connect to GND 22. U7 Pin 238 connect to VCC_P3V3SB 23. U7 Pin78 connect to TP28 24. U7 Pin58 connect to RST_MEM4_B 25. U7 Pin87 connect to D2_MODT2 26. U7 Pin91 connect to D2_MODT3 27. U7 Pin60 connect to D2_MCKE2 28. U7 Pin203 connect to D2_MCKE3 29. U7 Pin84 connect to D2_MCS_B2 30. U7 Pin89 connect to D2_MCS_B3 31. U7 Pin93 connect to GVDD 32. U7 Pin237 connect to GVDD 33. U7 Pin75 connect to D2_MCLK2N 34. U7 Pin74 connect to D2_MCLK2P 35. U7 Pin219 connect to D2_MCLK3N 36. U7 Pin218 connect to D2_MCLK3P 37. DNP the R68, R69, R70, R72, R71, R73, R74, R75, R76 Page. 16 (USB 3.0 ESD diode fix) 1. Remove the TVS1, TVS2, TVS3, TVS4, TVS5, TVS6, TVS7, TVS8, TVS9, TVS10, TVS11, TVS12 2. Add U22, U37 PUSB3FR6Z Page. 28 (change board revision from D to E) 1. NC the R1412. Page. 38 1. U60 PinL2 change pullup voltage from 2P1V to 2P5V 2. U60 PinN24 C24 change pullup voltage 2P1V to 2P5V 3. U60 PinL22 L21 L23 L24 change pullup voltage from 2P1V to 2P5V 4. NC the R565. Page.41 1. U60 PinH23 connect to 2P5V 2. U60 PinL4 connect to 2P5V 3. U60 PinR24 connect to 2P5V 4. U60 PinD3 connect to 2P5V 5. Remove R581, R583, R584, R586 Page. 45 1. Del SYS FAN4

DATE	Revision	Note
2015/05/04	50AX	Page. 16 1. Add CP238 (Optimize the quality of TSEC_1588_CLK_IN clock signals) Page. 38 1. Add R580 (Optimize the quality of AQR405 CLK_P / AQR405 CLK_N clock signals) Page. 59 1. Del SYS FAN5
2016/03/23	50AX	Page. 9 1. change the C20, C39, C34 and C2 from 4700pF to 3300pF. 2. Change the FB1, FB2, FB3 from GBD201209PGH121N(NEXCOM P/N:4IB1201D02X00) to BLM18KG121TN1(NEXCOM P/N: 4IB1201C04X00) 3. Add the C247, C248(GRM155R60J225KE95) 4. Change the C85, C138, C148 from 4700pF to 2700pF.(GRM155R71H272KA01) Page. 16 1. Change the CN1 from 4NBUF00903X00 to 4NBUF00913H00(Molex: 48404-0003) Page. 19 1. Add the R303, R304, R305, R290(Add 100K ohm pull-ups to OVDD on SDHC_DAT[0:3]) Page. 20 1. NC the R313, R312, R310. 2. Removed the net COP_TRST_B ,COP_SRST_B. 3. Removed the R303, R319, R320. 4. Removed the R304, R305, R306, R307, R308 (10K pullups to 3P3V). 5. Change the R309 from 10Ω ohm to 10 ohm. 6. Removed the R314, R315, R316, R317.
2016/05/05	50AX	Page. 18 1. U28 Pin1 change pullup voltage from 1P2VAQ to 2P5V. 2. R252, R253, R254 change pullup voltage from 1P2VAQ to 2P5V. Page. 28 1. U51 Pin5 change pullhi voltage from 1P2VAQ to 2P5V Page. 38 1. Remove pullups R1406, R1407, R1408, R1409. There are already pullups to OVDD on the four AQ_P[0:3]_INT_N signals on page 20.
2016/07/18	50AX	Changed "FREESCALE" to "NXP" throughout document Added LS2088A throughout document Page 1: Updated Table of Contents Page 2: Updated Block Diagram Page 4: Updated Block Diagram Page 5: Updated I2C addresses of several devices on Block Diagram Page 6: Updated Reset Block Diagram to match schematics Page 7: Updated Clock Block Diagram Page 8: Added Serial EEPROMs to Memory List Page 15: 1. Renamed nets "SLOT1xxx" to "SLOT2xxx". 2. Renamed nets "SLOT0xxx" to "SLOT1xxx". Page 17: 1. Corrected I2C address text on muxes 2. Add direct net connections for I2C1_PROC bus Page 18: 1. Change resistor body size of R238, R240, R242, R243 to 0805 and relocate on TOP side of PCB. 2. Replace U25 & U26 LED drivers with logical OR of Winbond thermal monitor signals. Added U207 74LVC2G08DC. Page 19: 1. Move RS-232 Circuit to page 18. Then add U205 and U208 SDHC VT buffers TXBN0304RSVR. 2. Add U209 inverter. Input from LS2 EVT9, output to SDHC VTSEL. 3. Add note that EVT9 must programmed as GPIO for SDHC VT select. Page 20: 1. Add R316 4.7K pullup to VCC_P1V8SB on COP_HRST_B. 2. Change pullup voltage at R296 from 3P3V to VCC_P3V3SB. 3. Populate R295 and R296. 4. Remove R323 pulldown resistor on DUT_TCK. 5. Add netname and footprint of MIA-pin6 called COP_HRST_BB. 6. Renamed CH_SW_RST to CH_SW_RST_B (active low). 7. Replaced R297 and R299 with 0.1uF caps (CP366 and CP367) to AC-couple LVDS DIFF SYSCLK to LS208x inputs. 8. Deleted TP74. Add net SDHC_VTSEL_B at R291 pin 2. Page 21: 1. Changed NAND FLASH (U43) part number from MT29F16G08ABABAWP:B to MT29F16G08ABACAWP-Z:C 2. Added QSPI (U182), QSPI Emulator (J59) and QSPI select logic (U183). Page 22: 1. Renamed nets "SLOT6xxx" to "SLOT1xxx". 2. Renamed nets "SLOT0xxx" to "SLOT1xxx". Page 23: Renamed nets "SLOT1xxx" to "SLOT2xxx". Page 25: Updated I2C Addr text for U45 to 0x6B Page 26: Renamed CH_SW_RST to CH_SW_RST_B (active low). Page 29: Added CFG_QSPI_EN_B and RST_QSPI_EMU_B signals to CPLD (U50C pins B1 and D4). Page 30: At CPLD (U50E) pin R11 and TP200, changed netname COP_HRST_B to COP_HRST_BB. Page 38: Change text to "VDDIO is 2.5V" Page 56: Change netname on UP17 pin 12 from 2P5V_COMP to P1V8SB_COMP (UP16 pin 12 had identical netname). Page 58: 1. Change netnames on three strap resistors. 2. Change resistor body size of R662, R666, R667, R668 to 0805. 3. Change R654 and R655 to NO (Do not populate). 4. Change R656 and R657 to 10K and populate them (change I2C address of Winbond to 0x2C). Page 59: 1. Depopulate R617, R618, R625, R683, R700. 2. Added DC Speed control jumper (J7) for CPU FAN.
2016/10/28	60AX	Page. 18 1. U28 Pin1 connect to OVDD, Pin2 connect to EMI2_MDC, Pin3 connect to EMI2_MDIO, Pin4 pullup to OVDD, Pin6 connect to R1391, Pin7 connect to R1390, Pin8 connect to 2P5V. Page. 25 1. Renamed connections on U44 pins 7 and 10 to common net called X1_GND. 2. Add R1427, R1428. 3. Change the C526, C528 dorm 33pF to 22pF. Page. 28 1. Added R1426 and PCBREV2 signal connection to U50 CPLD pin D3. Update Revision Table to provide PCB Rev F encoding.
2017/02/15	60AX	Page. 19 1. De-Populate U36. SDHC Smart Voltage Translation not supported.
2017/05/09	70AX	Page. 19 1. Add R1000 4.7K pullup to OVDD as shown below. 2. Depopulate R434 (=NO).

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Title: Revision change

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