8MNANOD3L-CPU

(i.MX8M Nano Reference Board)

Table of Content

Revision History

Rev. Code	Date	By	Description
A	2020-08-12	Vector	Initial version release
A1	2021-01-08	Vector	Remove CPU socket.
A2	2022-03-02	Vector	Remove WDOG note for ROHM PMIC.

1. Interrupted lines coded with the same letter or letter combinations are electrically connected.

2. Device type number is for reference only. The number varies with the manufacturer.

3. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Preliminary - Subject to Change without Notice!

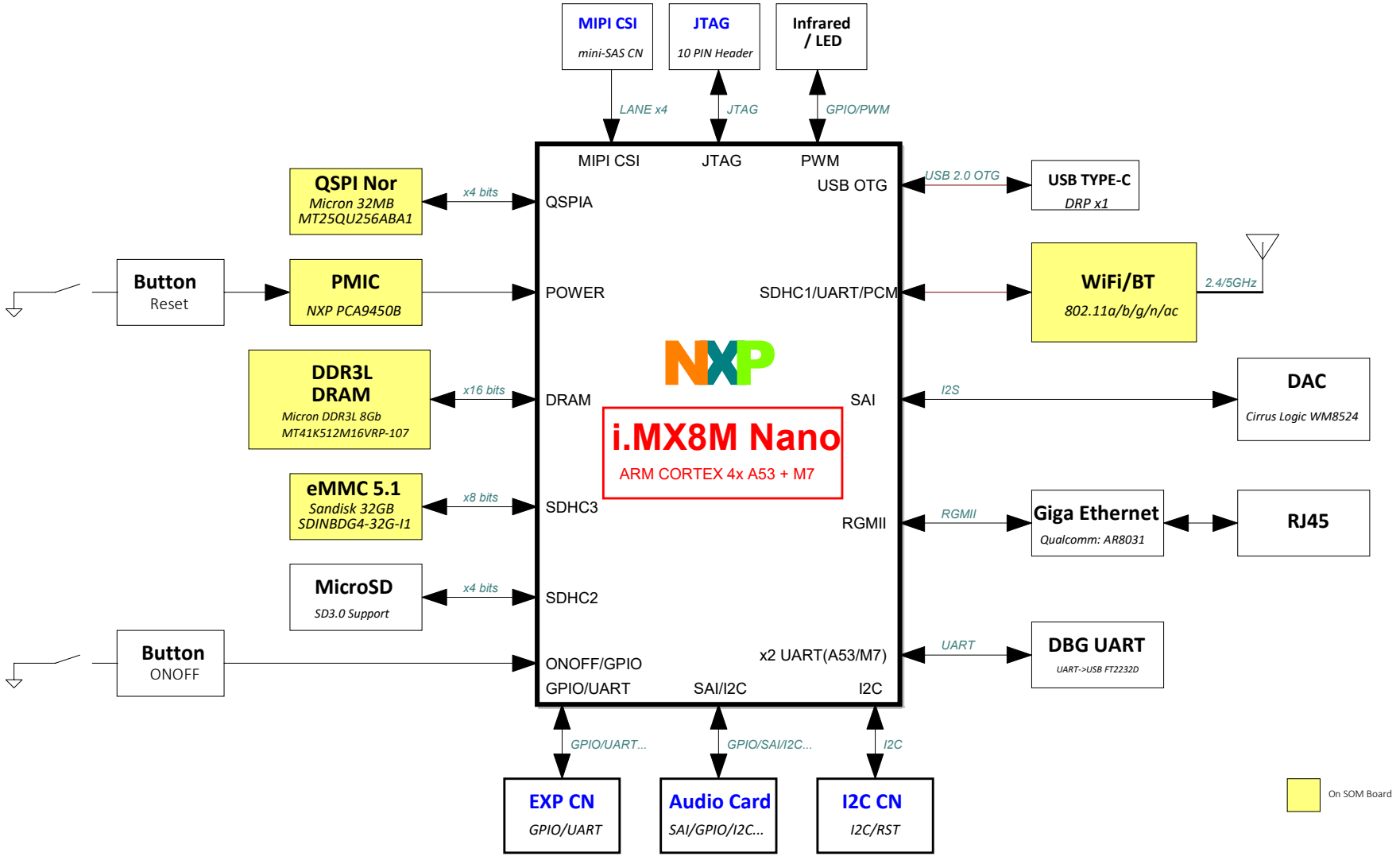
This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

Designer: Vector Cheng	Drawing Title: X-8MNANOD3L-CPU	
Drawn by: Vector Cheng	Page Title: Title and Rev History	
Approved: <Approver>	Size C / Document Number SCH-47569 PDF: SPF-47569	Rev A2
	Date: Friday, March 04, 2022	Sheet 1 of 13

8MNANOD3L-EVK Block Diagram



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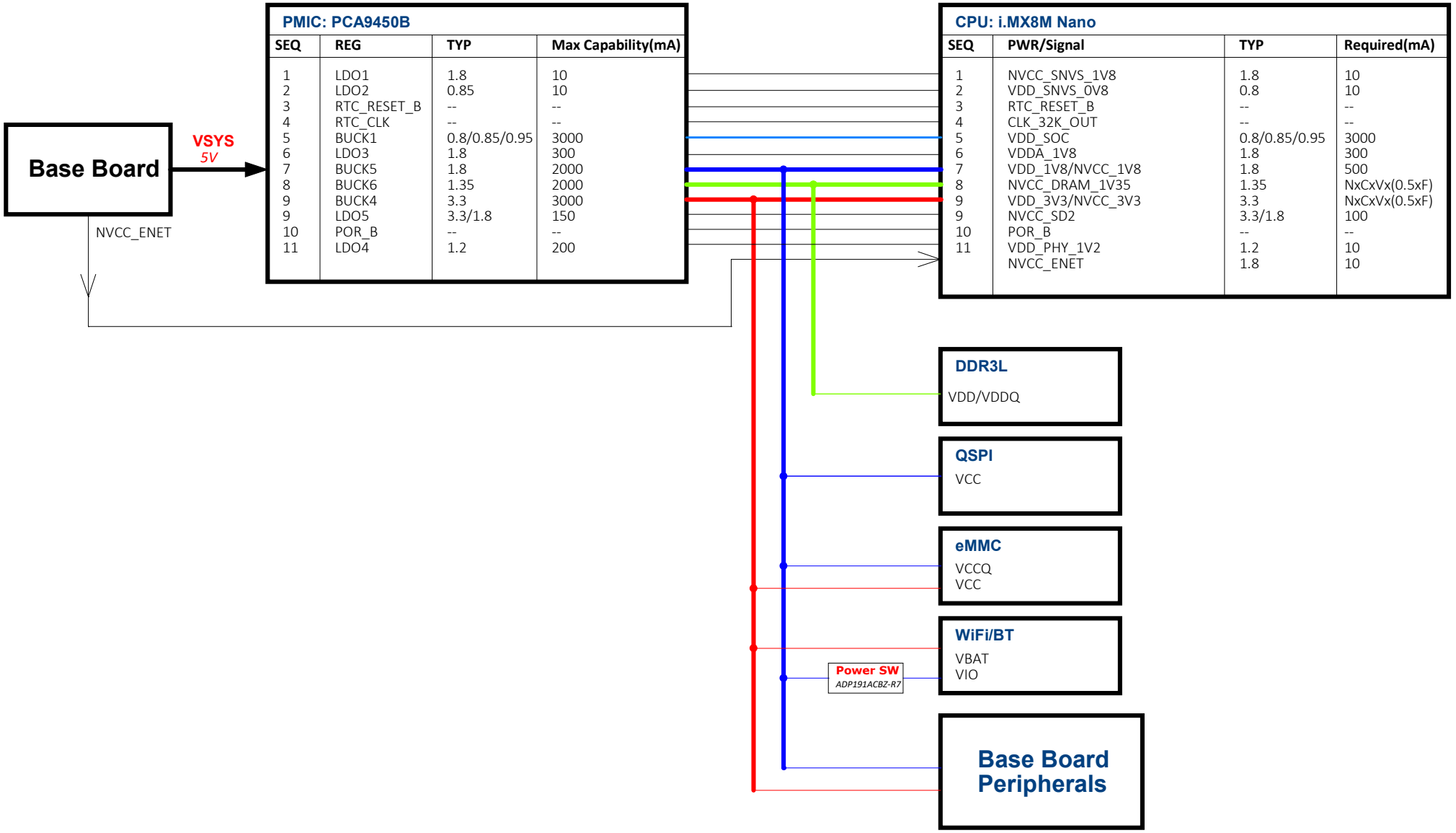
8MNANOD3L-EVK PWR TREE



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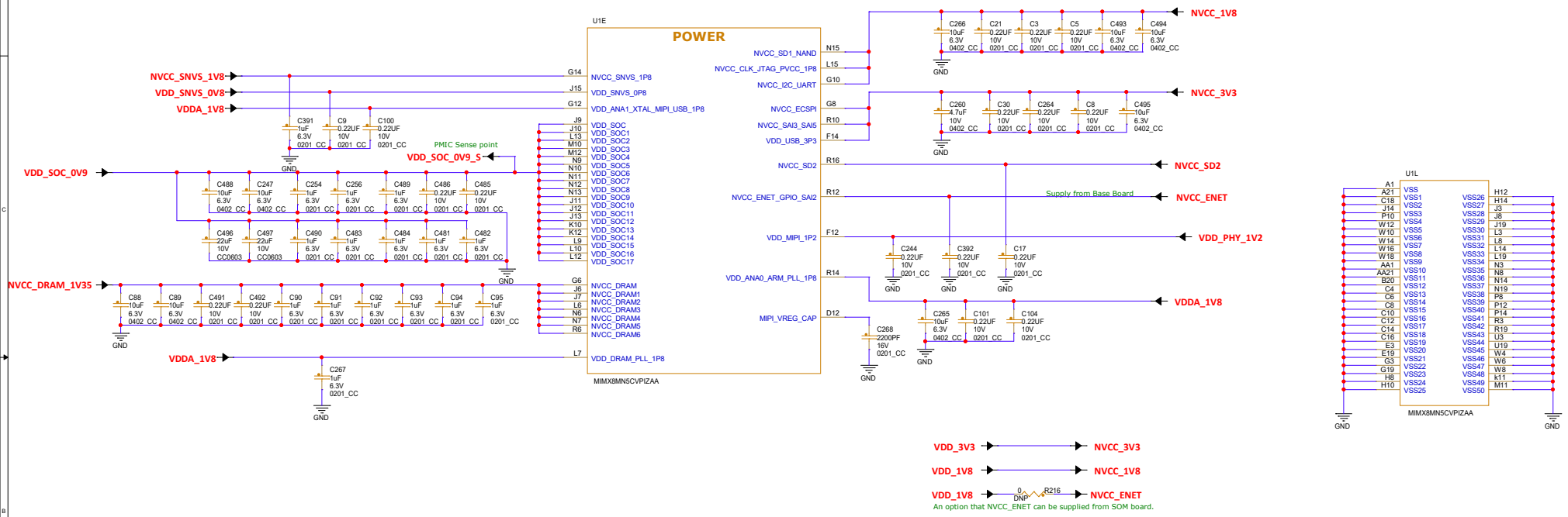
i.MX8M Nano PWR



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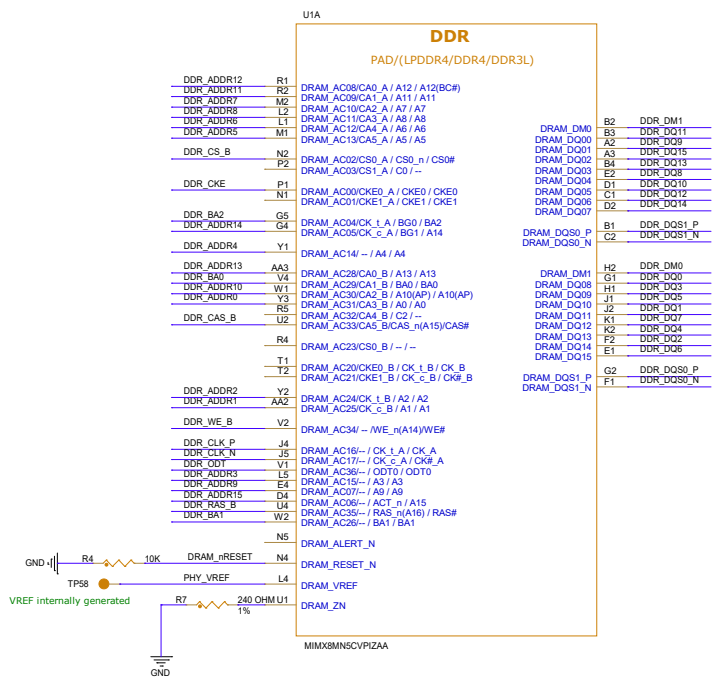
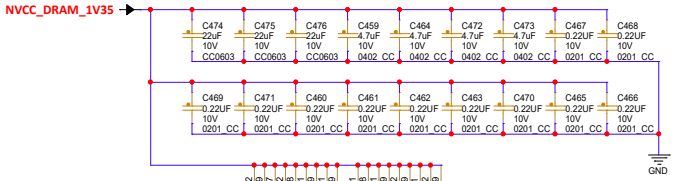
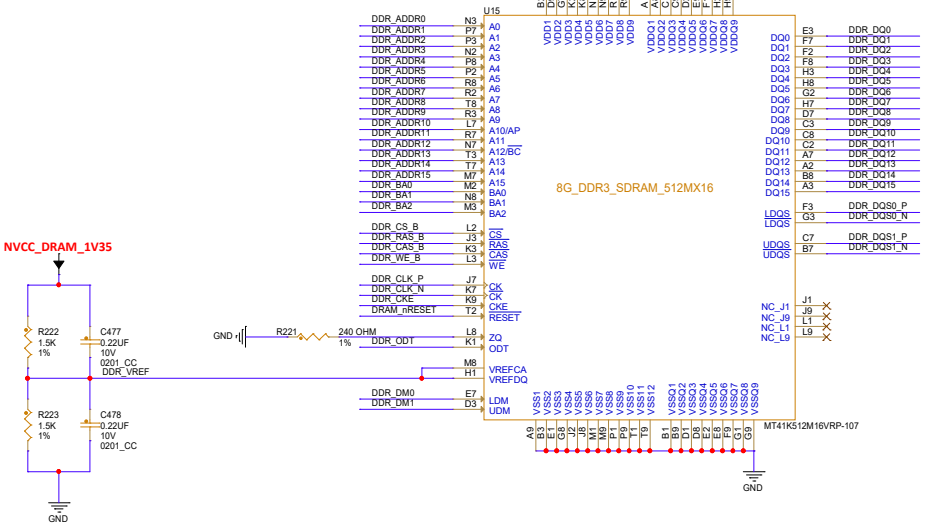
DDR3L 1GB







Command/Address

Ball name	Ball #	LPDDR4	DDR4	DDR3L
DRAM_AC00	P1	CKE0_A	CKE0	CKE0
DRAM_AC01	N1	CKE1_A	CKE1	CKE1
DRAM_AC02	N2	CS0_A	CS0_n	CS0#
DRAM_AC03	P2	CS1_A	C0	--
DRAM_AC04	G5	CK_t_A	BG0	BA2
DRAM_AC05	G4	CK_c_A	BG1	A14
DRAM_AC06	D4	-	ACT_n	A15
DRAM_AC07	E4	-	A9	A9
DRAM_AC08	R1	CA0_A	A12	A12/BC#
DRAM_AC09	R2	CA1_A	A11	A11
DRAM_AC10	M2	CA2_A	A7	A7
DRAM_AC11	L2	CA3_A	A8	A8
DRAM_AC12	L1	CA4_A	A6	A6
DRAM_AC13	M1	CA5_A	A5	A5
DRAM_AC14	Y1	-	A4	A4
DRAM_AC15	L5	-	A3	A3
DRAM_AC16	J4	-	CK_t_A	CK_A
DRAM_AC17	J5	-	CK_c_A	CK#_A
DRAM_AC20	T1	CKE0_B	CK_t_B	CK_B
DRAM_AC21	T2	CKE1_B	CK_c_B	CK#_B
DRAM_AC23	R4	CS0_B	-	-
DRAM_AC24	Y2	CK_t_B	A2	A2
DRAM_AC25	AA2	CK_c_B	A1	A1
DRAM_AC26	W2	-	BA1	BA1
DRAM_AC28	AA3	CA0_B	A13	A13
DRAM_AC29	V4	CA1_B	BA0	BA0
DRAM_AC30	W1	CA2_B	A10/AP	A10/AP
DRAM_AC31	Y3	CA3_B	A0	A0
DRAM_AC32	R5	CA4_B	C2	-
DRAM_AC33	U2	CA5_B	CAS_n/A15	CAS#
DRAM_AC34	V2	-	WE_n/A14	WE#
DRAM_AC35	V4	-	RAS_n/A16	RAS#
DRAM_AC36	V1	-	ODT0	ODT0

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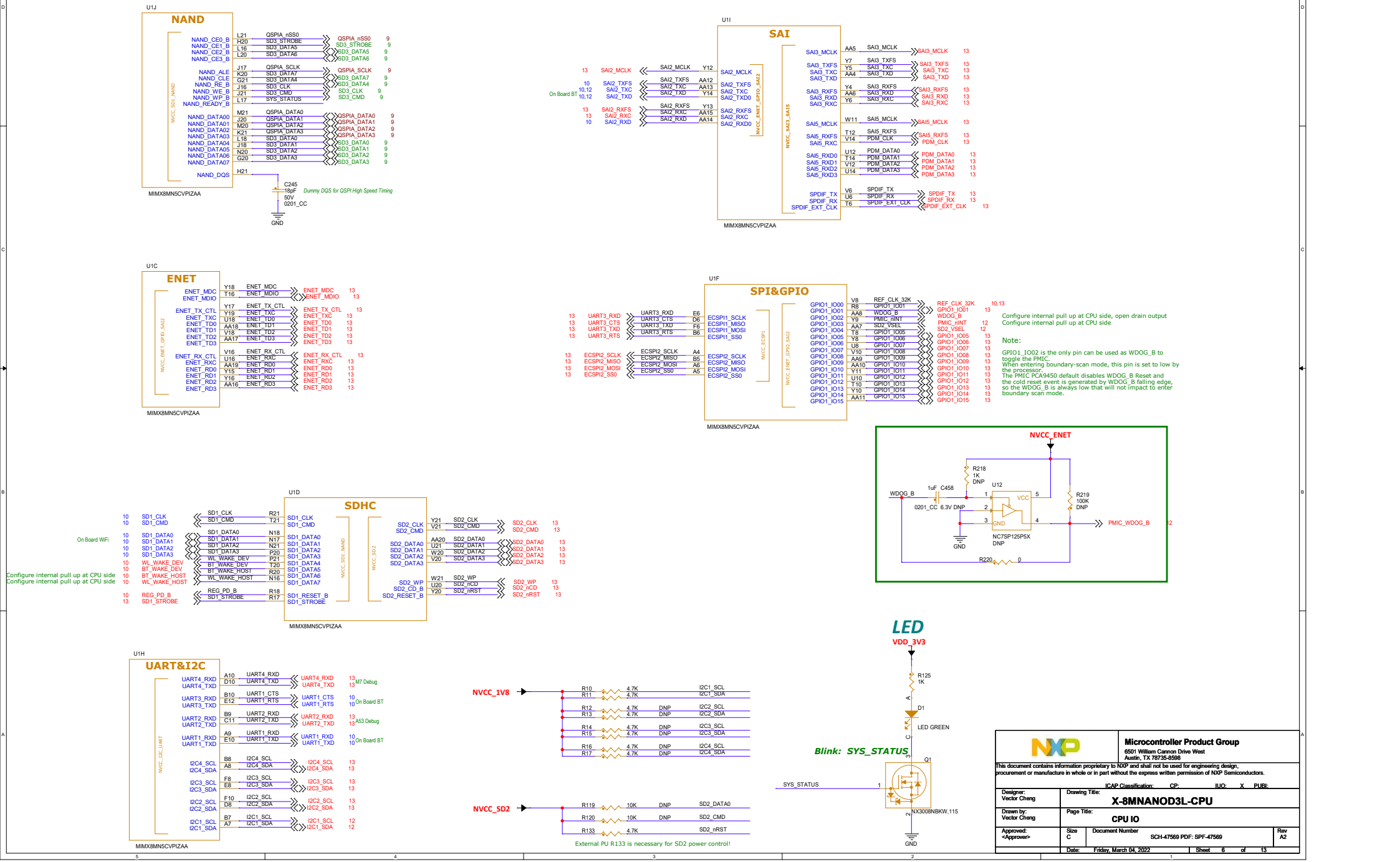
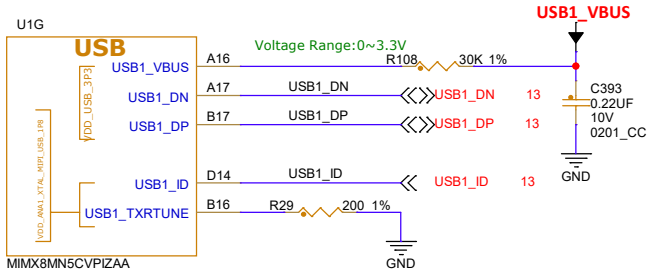
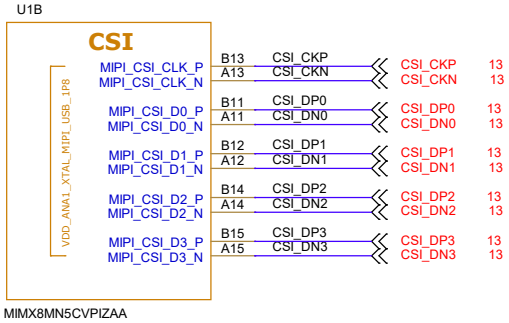
i.MX8M Nano IO Interface



i.MX8M Nano PHYs





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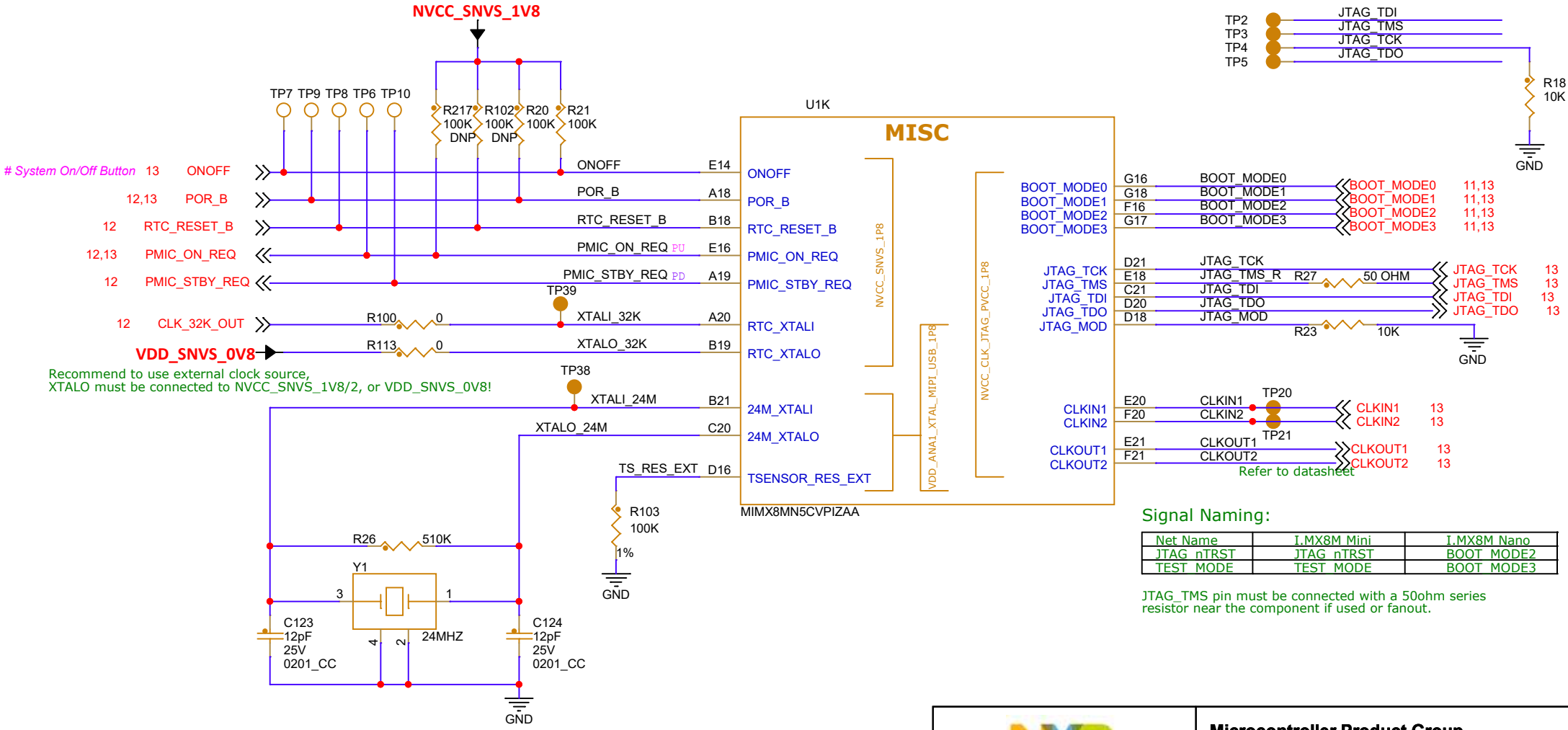
i.MX8M Nano MISC



JTAG Debug

Signal Naming:

Net Name	I.MX8M Mini	I.MX8M Nano
JTAG_nTRST	JTAG_nTRST	BOOT_MODE2
TEST_MODE	TEST_MODE	BOOT_MODE3

JTAG_TMS pin must be connected with a 50ohm series resistor near the component if used or fanout.

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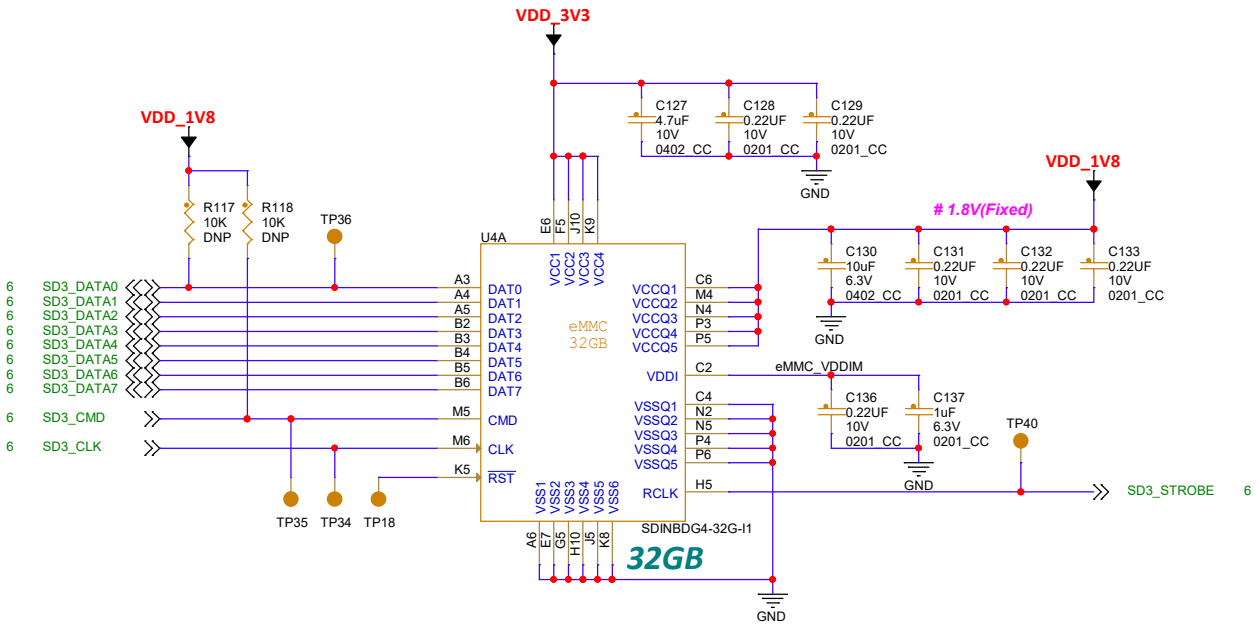
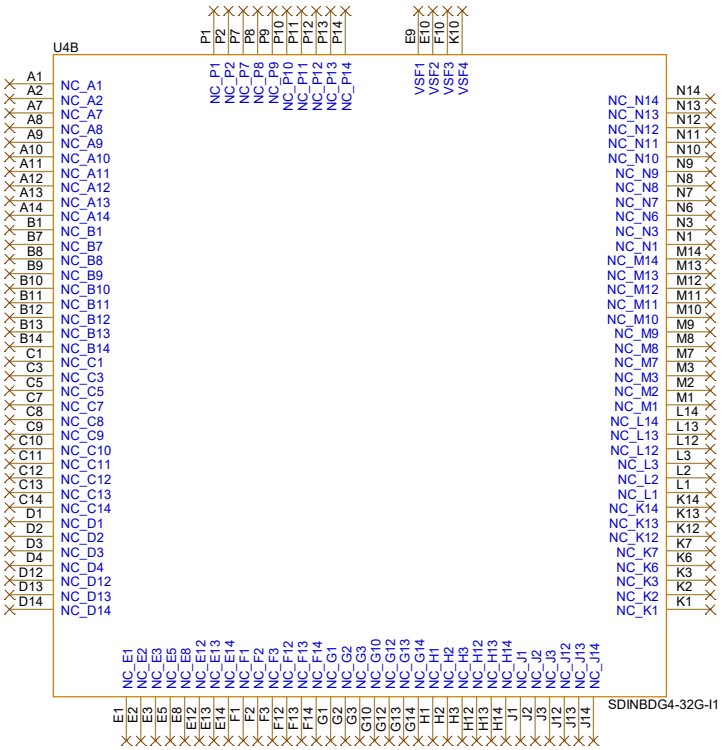
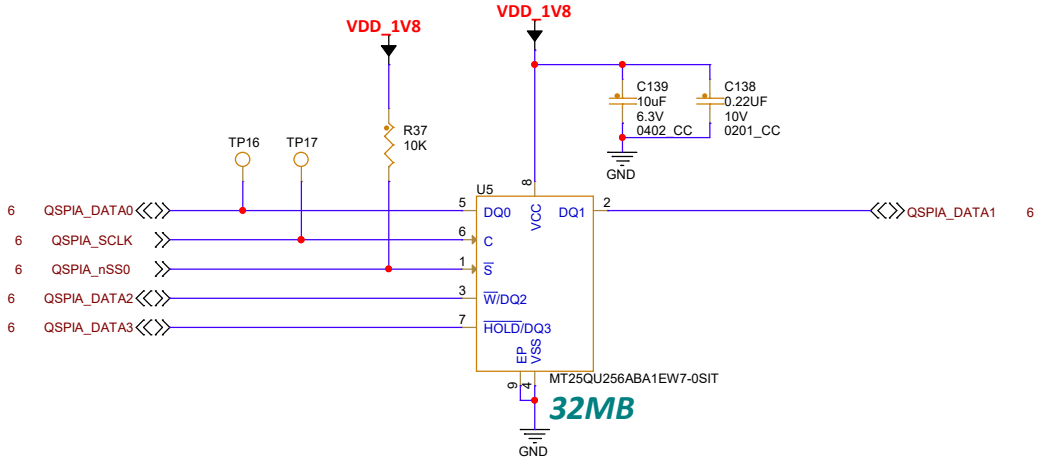
Storage

eMMC





QSPI Flash



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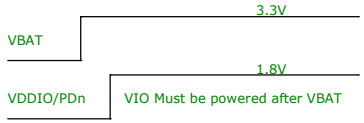
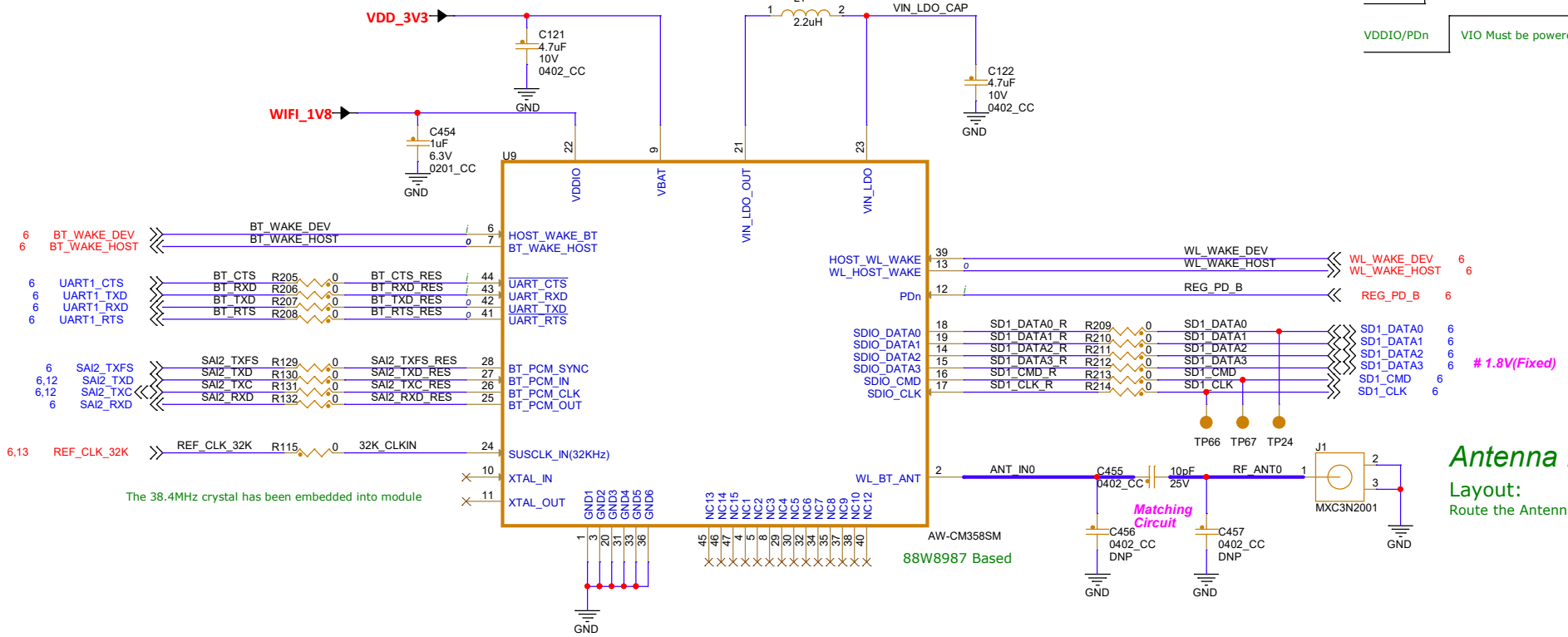
2.4G/5G WIFI/BT Module

Power Sequence

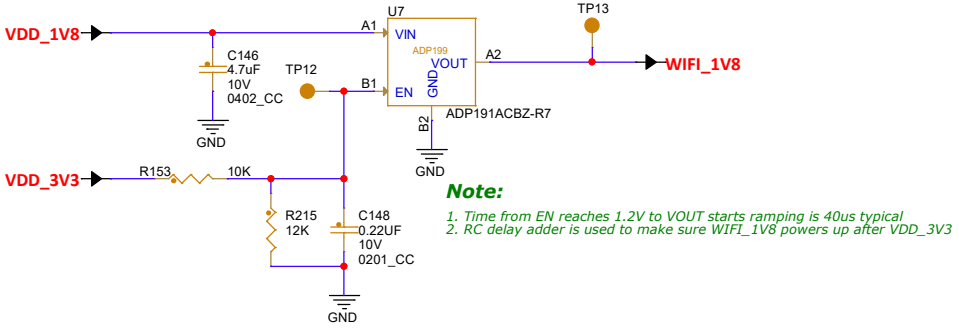




Antenna 2.4G/5G

Layout:

Route the Antenna trace as 50 ohm.



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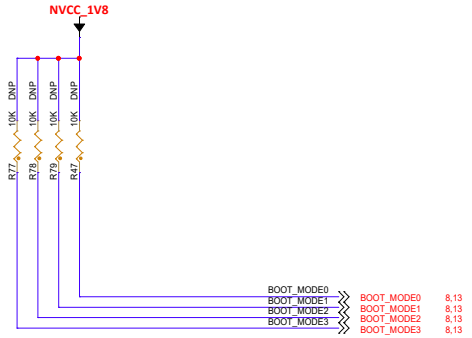
Boot Mode

i.MX8M Nano Boot Mode

BOOT_PIN[3]	BOOT_PIN[2]	BOOT_PIN[1]	BOOT_PIN[0]	Boot Modes
BOOT_MODE3 (TEST_MODE)	BOOT_MODE2 (JTAG_TRST_B)	BOOT_MODE1	BOOT_MODE0	Function
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	0	1	0	USDHC3 (eMMC boot only, SD3 8-bit)
0	0	1	1	USDHC2 (SD boot only, SD2)
0	1	0	0	NAND 8-bit single device 256 page
0	1	0	1	NAND 8-bit single device 512 page
0	1	1	0	QSPI 3B Read
0	1	1	1	QSPI Hyperflash 3.3V
1	0	0	0	ecSPI Boot
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved (Boot on I2C connected to BOOT PIN[3:2])
1	1	0	1	Reserved
1	1	1	0	Infinite Loop Mode
1	1	1	1	Test Mode



Note:

1. BOOT_MODE0-3 singals are used for boot selections

2. BOOT_MODE singals have internal PD before and after POR_B reset is deasserted!

3. When using Base Board for Multi boot selection, you must keep the resistors DNP on SOM board!

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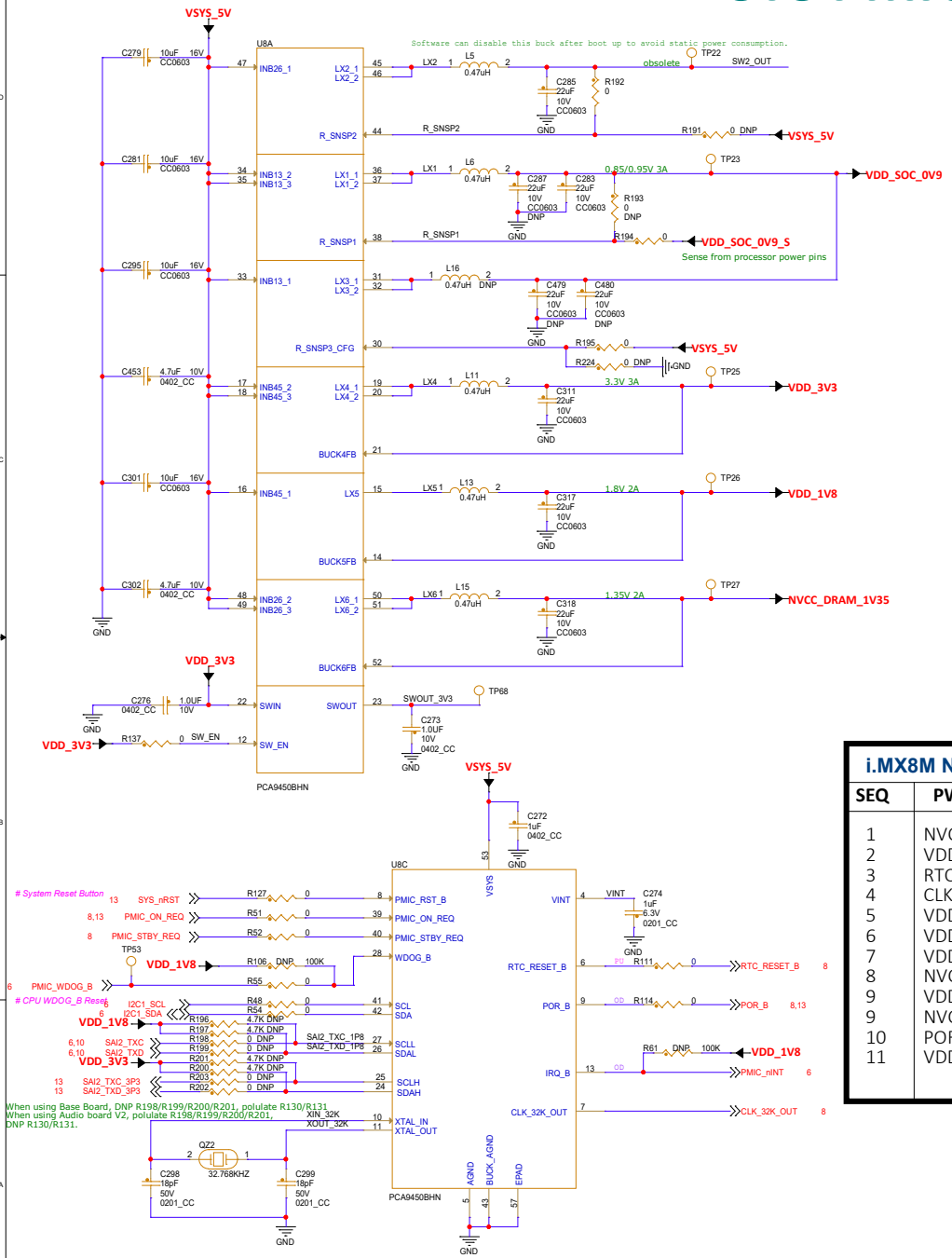
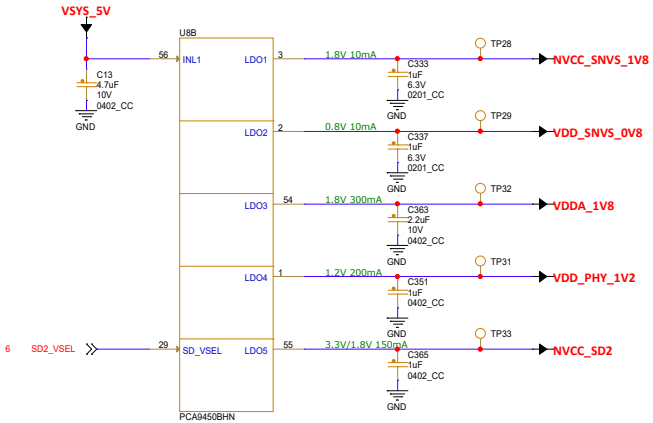
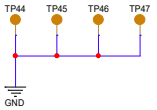
SYS PMIC

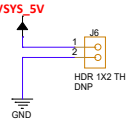




GND Testpoints



Backup PWR Supply



i.MX8M Nano DDR3L EVK Power Sequence

SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)
1	NVCC_SNVS_1V8	LDO1	1.62	1.8	1.98	10
2	VDD_SNVS_0V8	LDO2	0.76	0.8	0.9	10
3	RTC_RESET_B	RTC_RESET_B	--	--	--	--
4	CLK_32K_OUT	RTC_CLK	--	--	--	--
5	VDD_SOC_0V9	BUCK1	0.76/0.805/0.9	0.8/0.85/0.95	0.9/0.95/1.0	3000
6	VDDA_1V8	LDO3	1.71	1.8	1.89	300
7	VDD_1V8/NVCC_1V8	BUCK5	1.65	1.8	1.95	2000
8	NVCC_DRAM_1V35	BUCK6	1.283	1.35	1.417	2000
9	VDD_3V3/NVCC_3V3	BUCK4	3	3.3	3.6	3000
9	NVCC_SD2	LDO5	3.0/1.65	3.3/1.8	3.6/1.95	150
10	POR_B	POR_B	--	--	--	--
11	VDD_PHY_1V2	LDO4	1.14	1.2	1.26	200

Note:

1. WDOG_B is used as Cold Reset, external pull up is needed. On EVK, R106 is not necessary, since WDOG_B/GPIO1_IO02 of CPU has internal pull up.
2. PMIC_nINT is open drain output, external pull up is needed. On EVK, R61 is not necessary, since PMIC_nINT/GPIO1_IO03 of CPU has internal pull up.
3. AGND/BUCK_AGND should be connected to ground plane through Via. Do not short to EP directly on top layer

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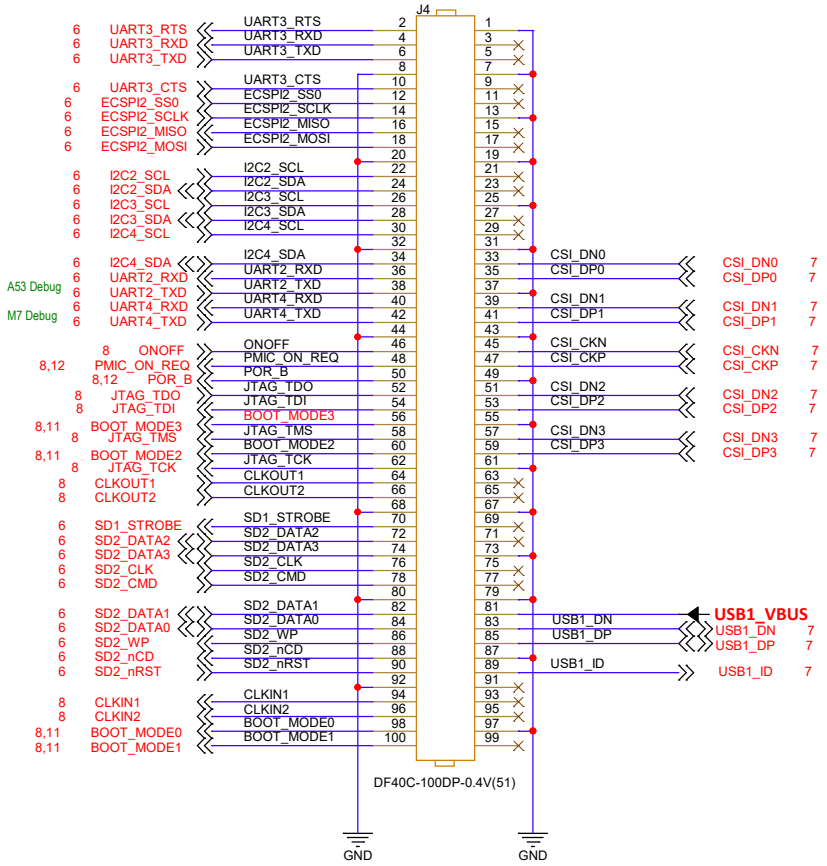
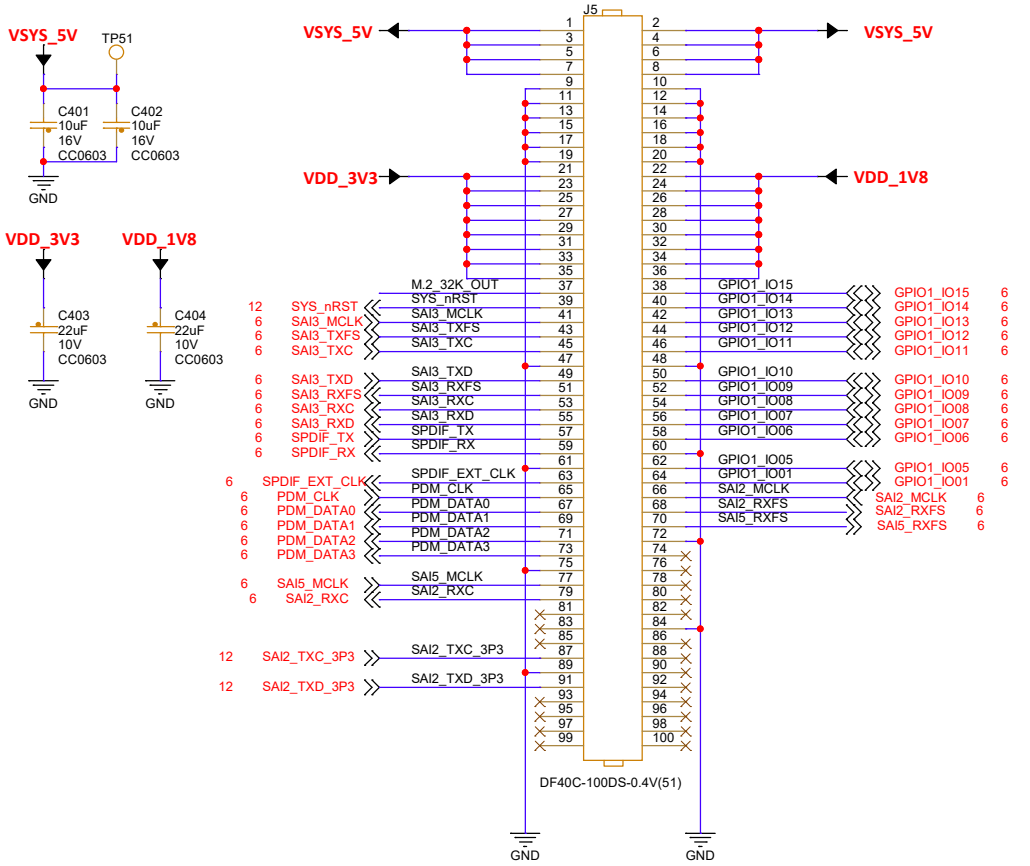
B2B Connector for CPU Board

Header



Receptacle



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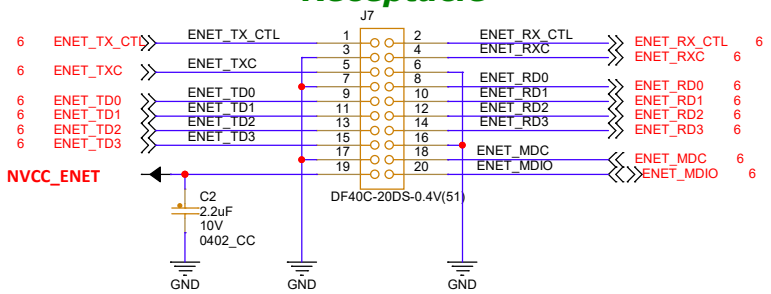

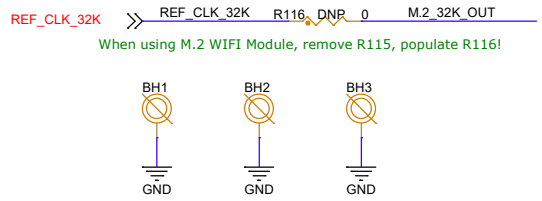

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