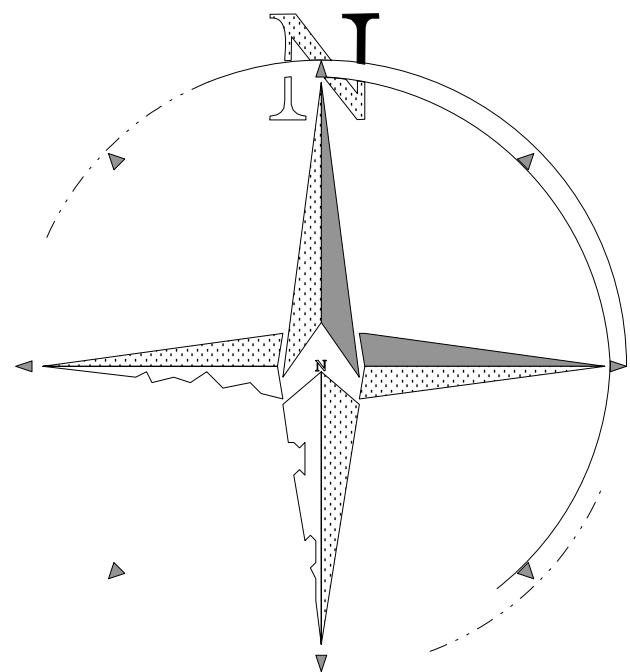


freescale™
semiconductor

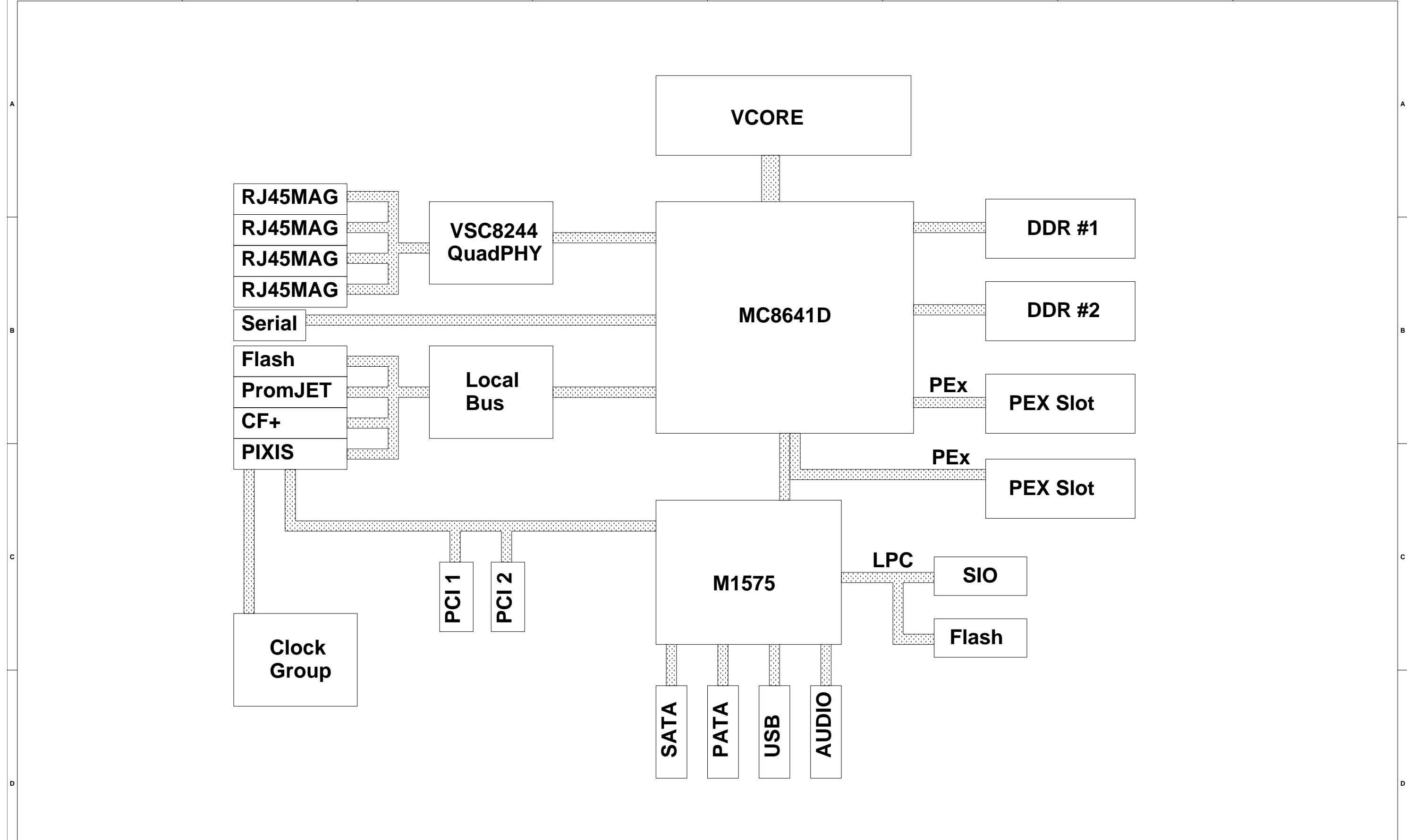


HPCN: High-Performance Computing platform for Networking

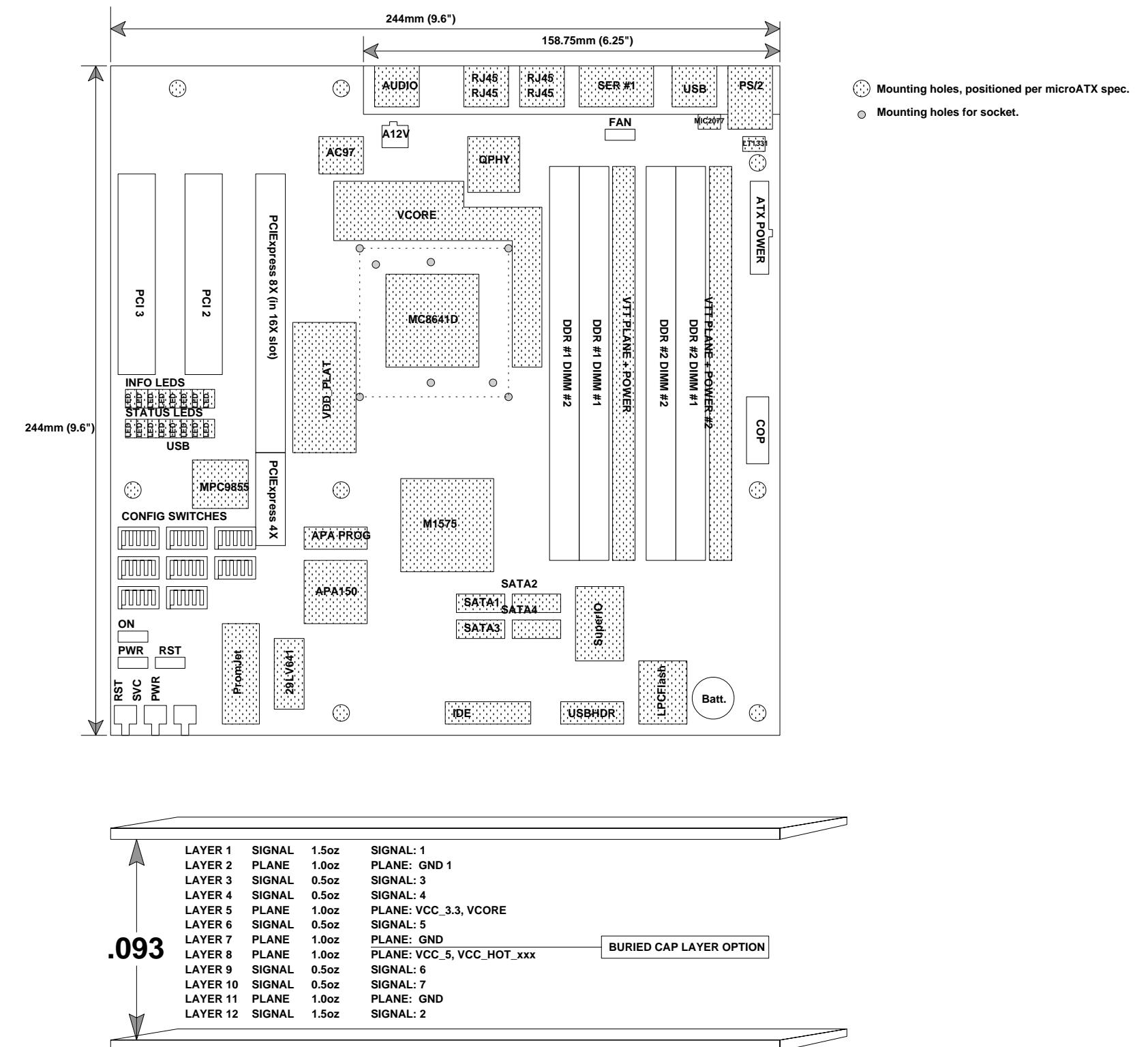
by

**Cass Arnett
Steve Foster
Gary Milliorn
Tiffany Tran-Chandler**

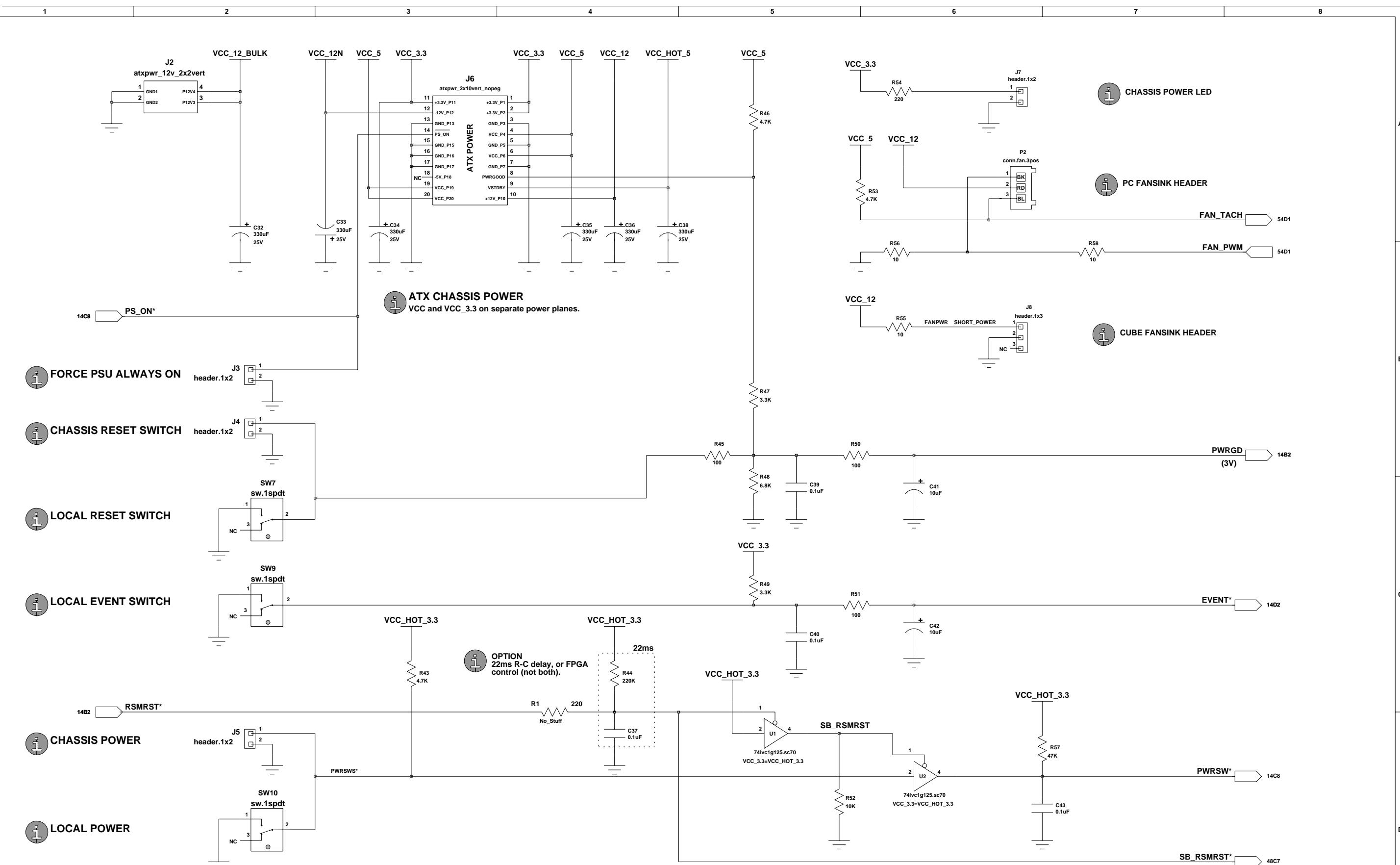
1	2	3	4	5	6	7	8
Schematic Notes							
A	1. Unless otherwise specified: All resistors are SMD0402, in ohms, 0.08W, +/-5%. All capacitors are SMD0402, in microfarads (uF), +/-20%. All inductances are in microhenries (uH). All ferrites are Z=50 ohms at 100 MHz. All fuses are self-resetting polyswitch (PTC) devices. Board impedance is 55 +/- 5 ohms.						
2.	Integrated circuits have default connections to power and ground unless explicitly shown otherwise. Global power connections are: VCC_3.3 VCC_2.5 GND VCC_5 VCC_1.2 VCORE						
3.	Part numbers used are for reference only; compatible parts may be used; refer to the bill of materials.						
4.	Freescale and the Freescale logo are registered trademarks of Freescale Semiconductor. PowerPC is a trademark of IBM. Other trademarks are the respective property of their respective copyright holders. Anyone perfect must be lying, anything easy has it's cost, anyone plain can be lovely, anyone loved can be lost. All rights reserved. No warranty is made, express or implied.						
5.	The sheet-to-sheet cross reference format is: Sheet VertZoneLetter HorizZoneNumber						
6.	Components with the label "No. Stuff" are not to be installed by default; they are for test or manufacturing purposes only. 						
B	7. All buses follow big-endian bit numbering order (bit 0 is the most-significant bit), except where industry standards apply (i.e. PCI). Little-endian numbering is noted at the source component.						
	This schematic is provided for reference purposes only. All information is subject to change without notice. No warranty, expressed or applied, is made as to the accuracy of the information contained herein. Contact Freescale Sale/FAEs to obtain the latest information on this product.						
D	REV	DATE	CHANGES				
V1.0	2005Aug03	Initial version					
V1.0a	2006Feb27	Initial production					
V1.02	2006Nov07	PCB Tweaks					
		Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Gary Milliorn	Date Changed: Thursday, February 1, 2007 Time Changed: 2:05:47 pm	Title: Information, please	Page: 02
1	2	3	4	5	6	7	8

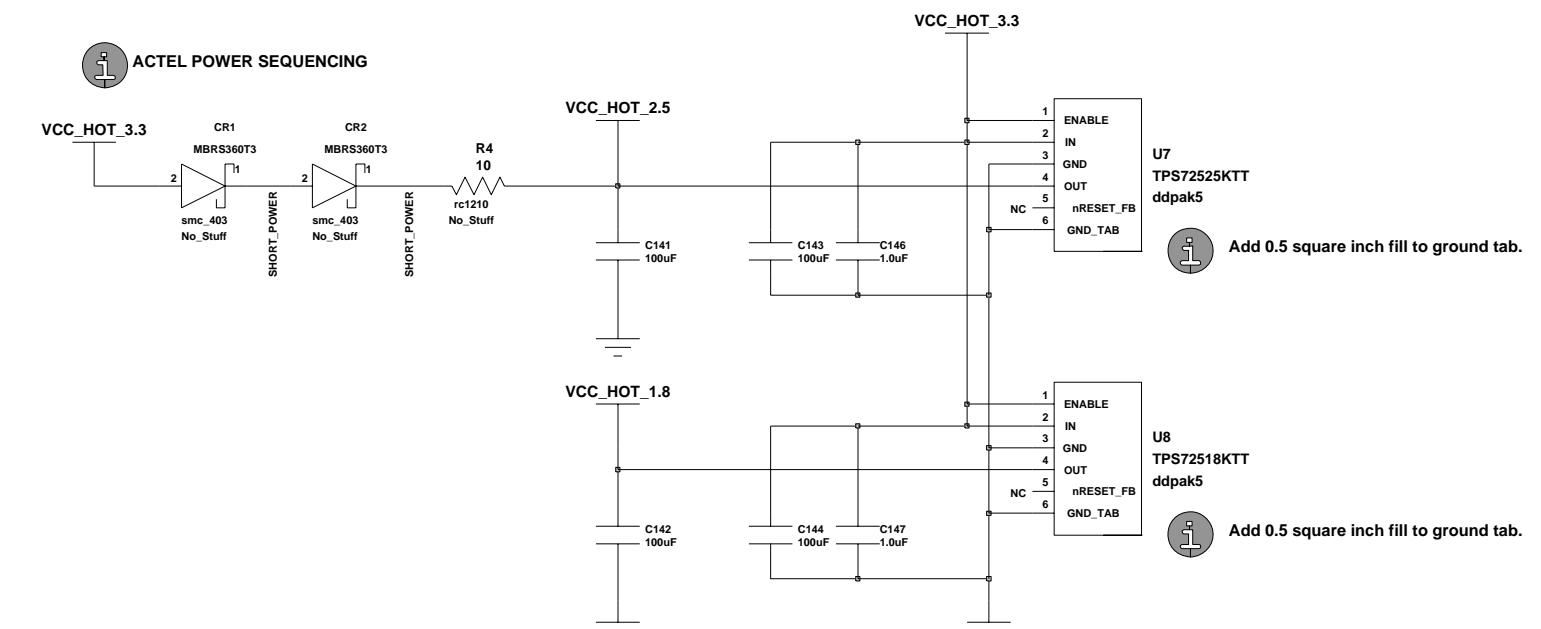
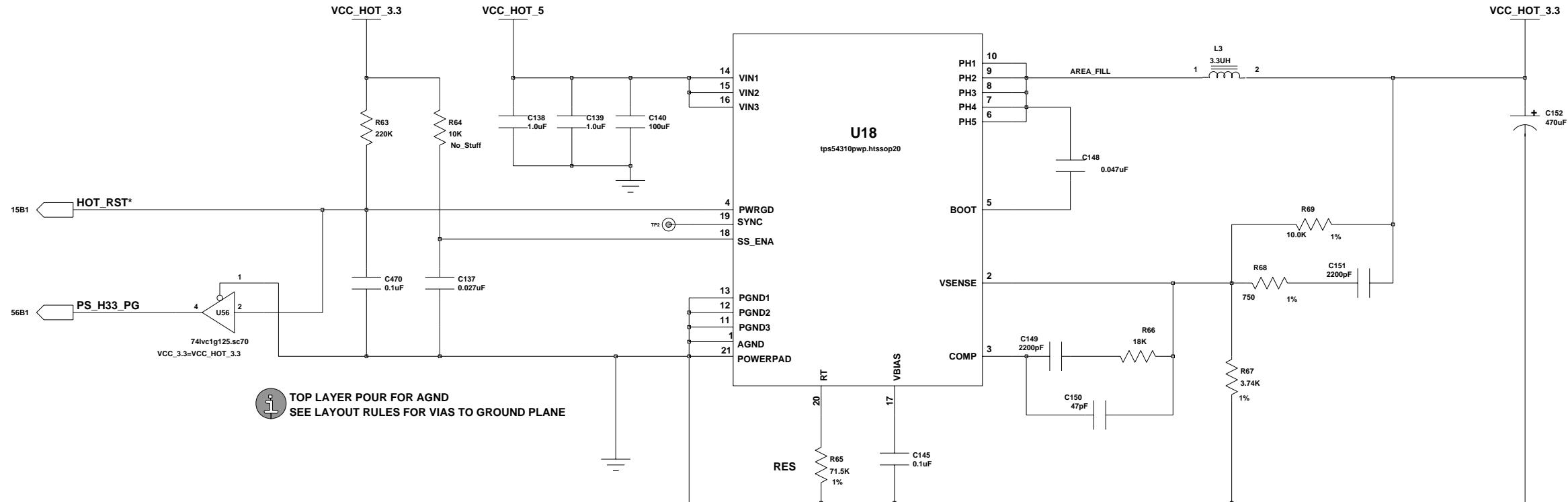


Note: Not Definitive -- see
Design Workbook.

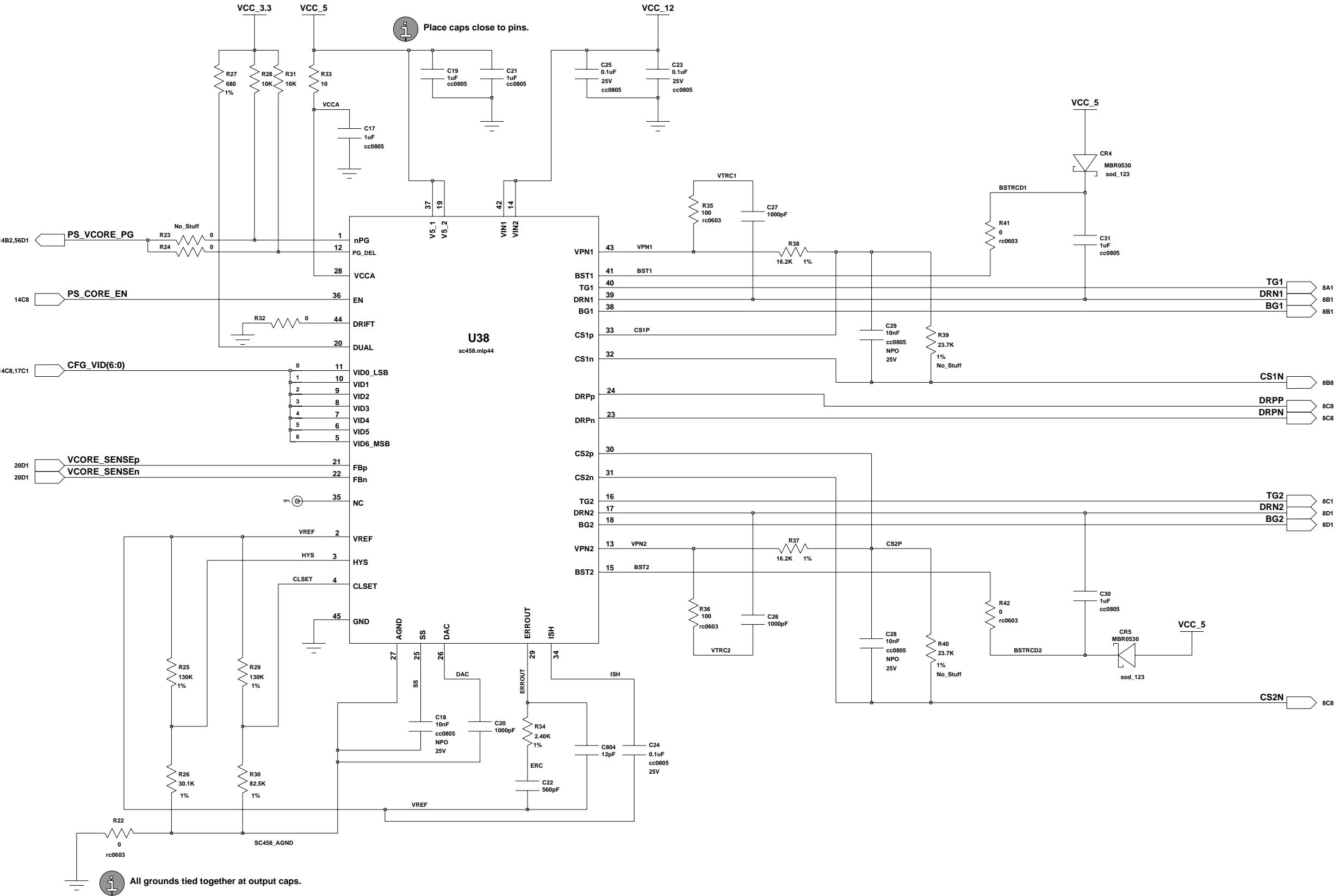


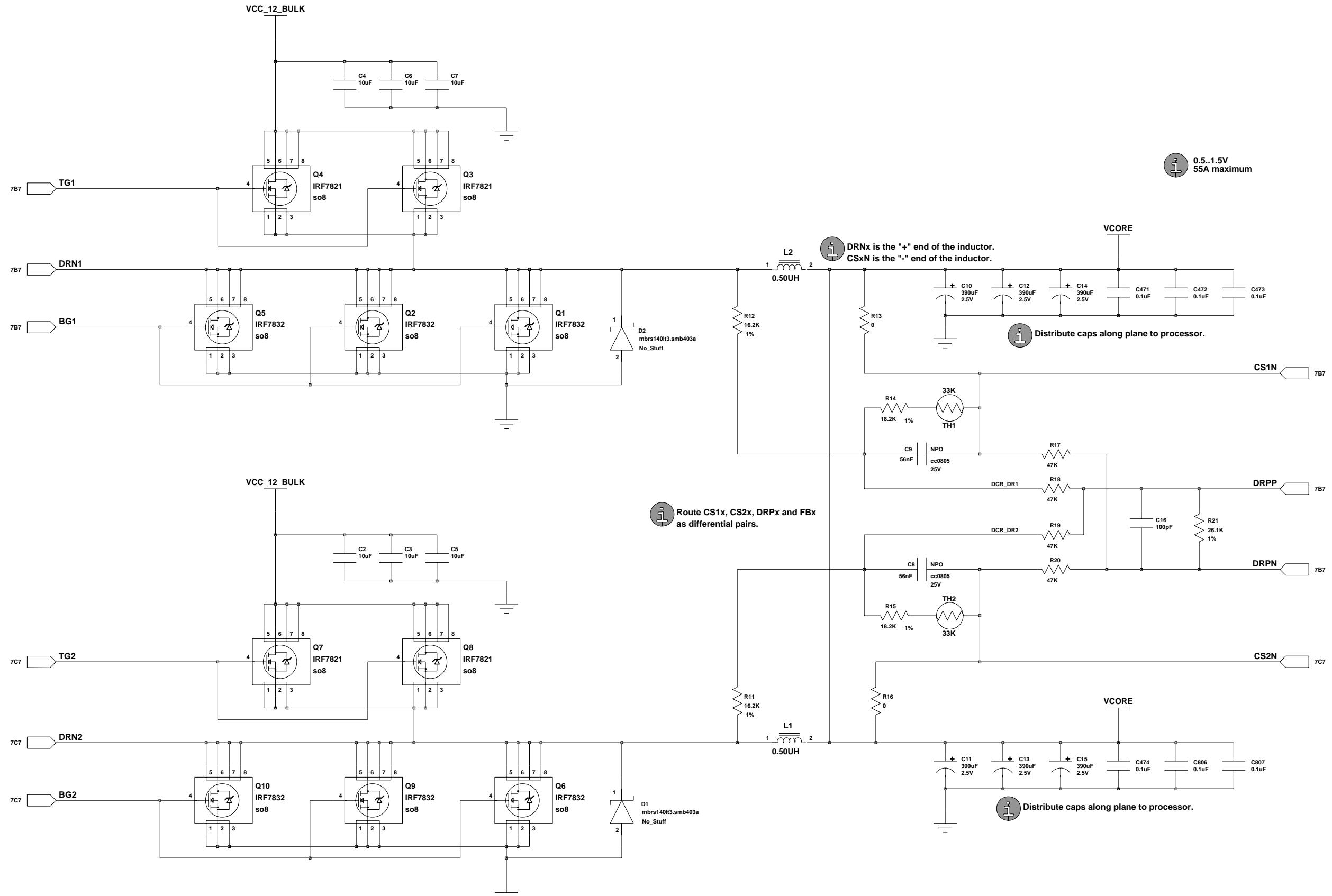
 freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Gary Milliorn	Date Changed: Thursday, February 1, 2007 Time Changed: 2:06:05 pm	Title: Placement Guide and PCB Stackup	Page: 04
1	2	3	4	5	6	7





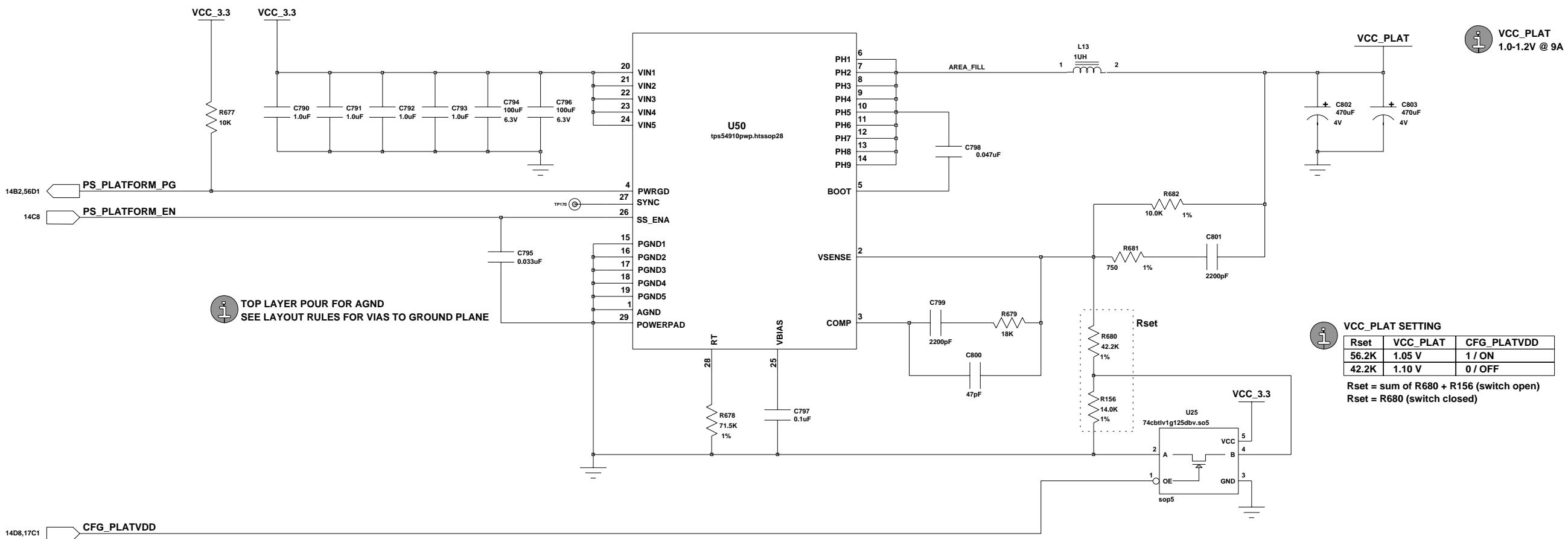
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1	2	3	4	5	6	7





freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Cass Arnett	Date Changed: Thursday, February 1, 2007 Time Changed: 2:07:45 pm	Title: Processor VDD (Vcore) Supply, Part 2	Page: 08
1	2	3	4	5	6	7

A



B

C

D

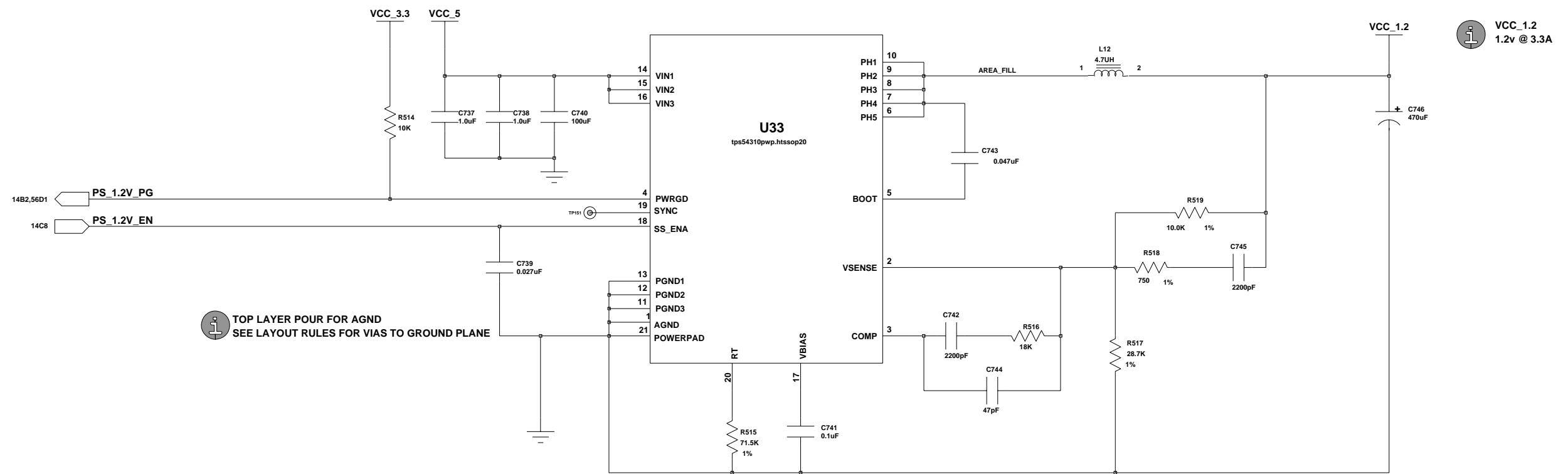
A

B

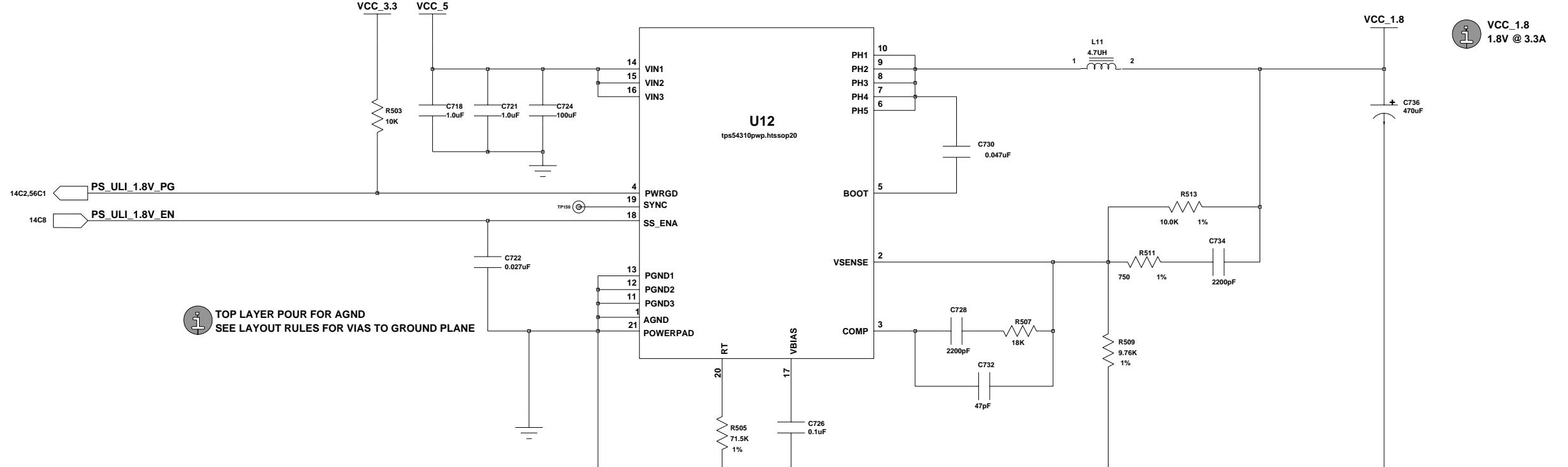
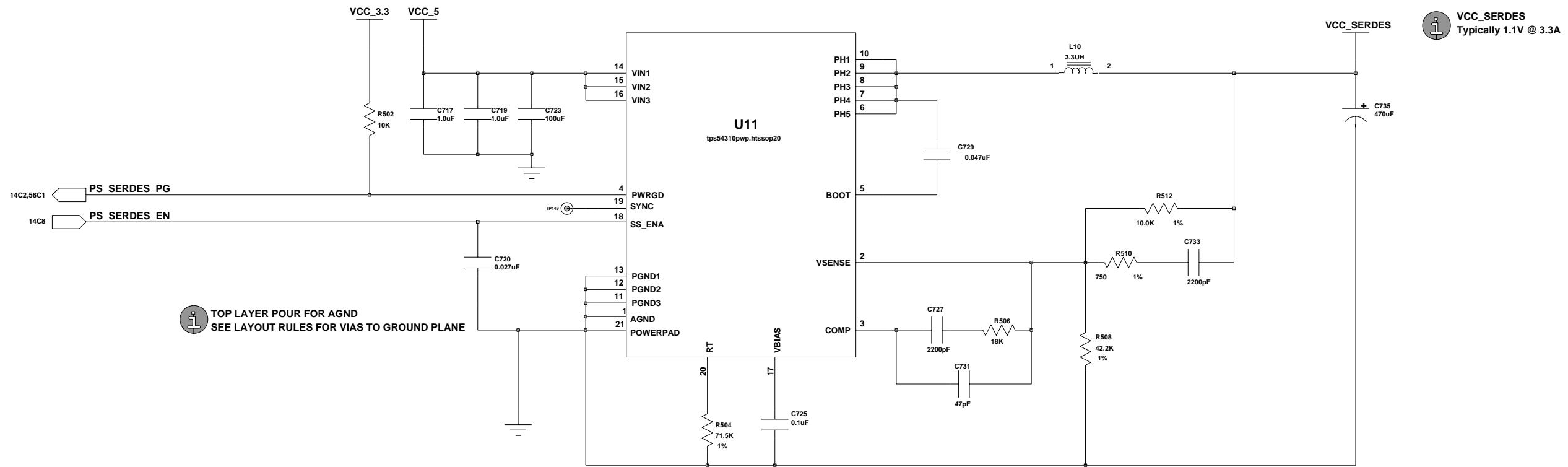
C

D

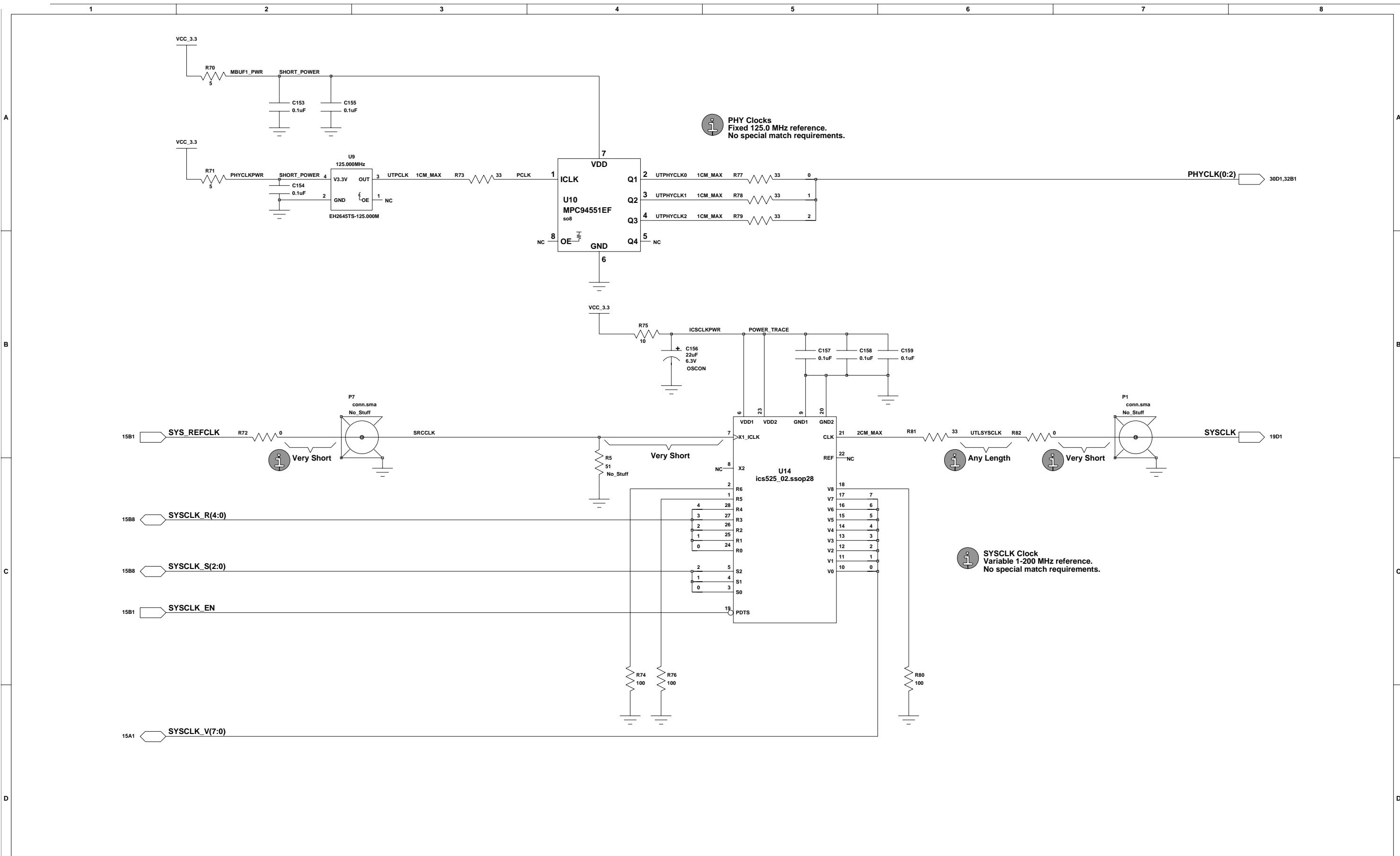
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1	2	3	4	5	6	7

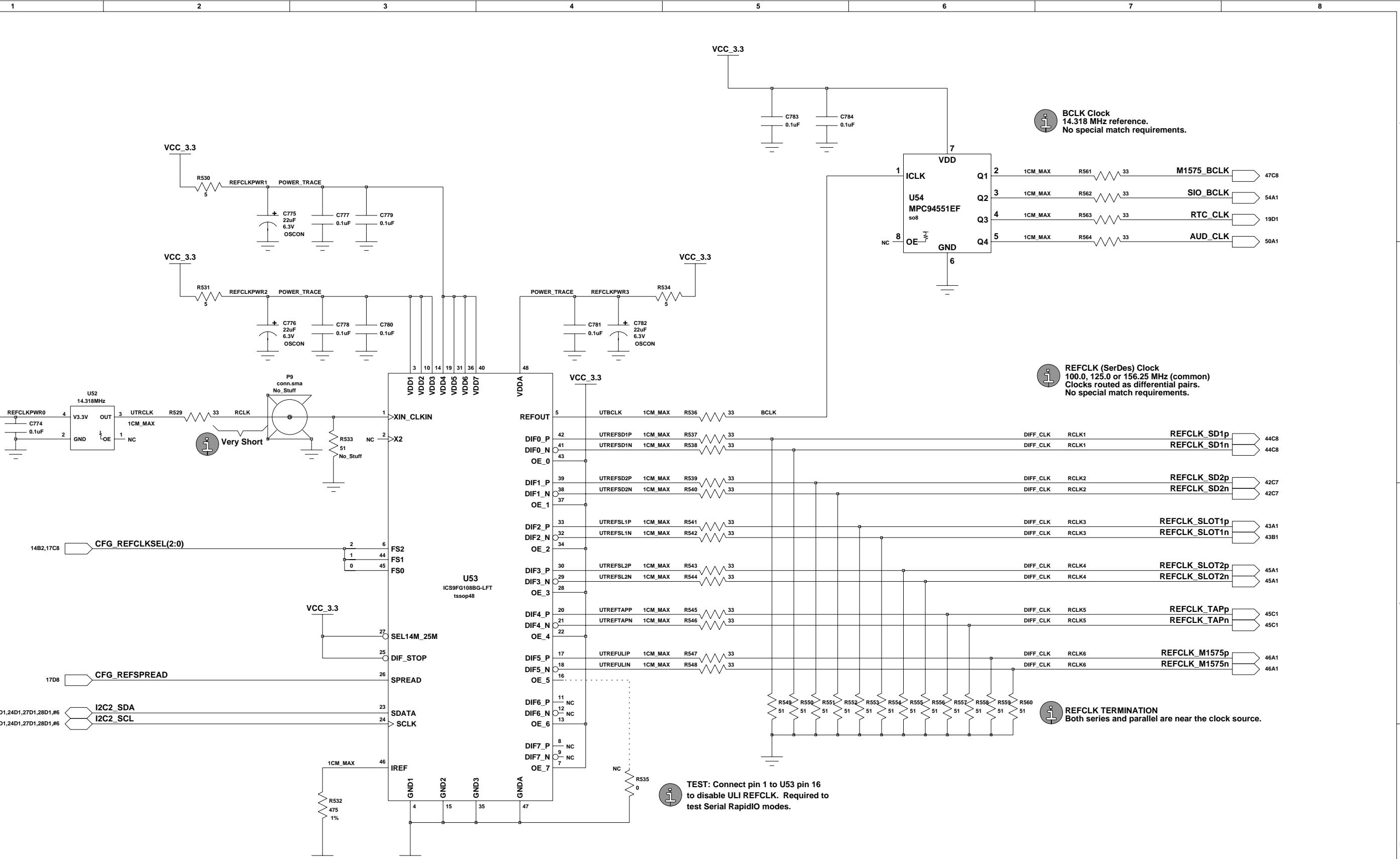


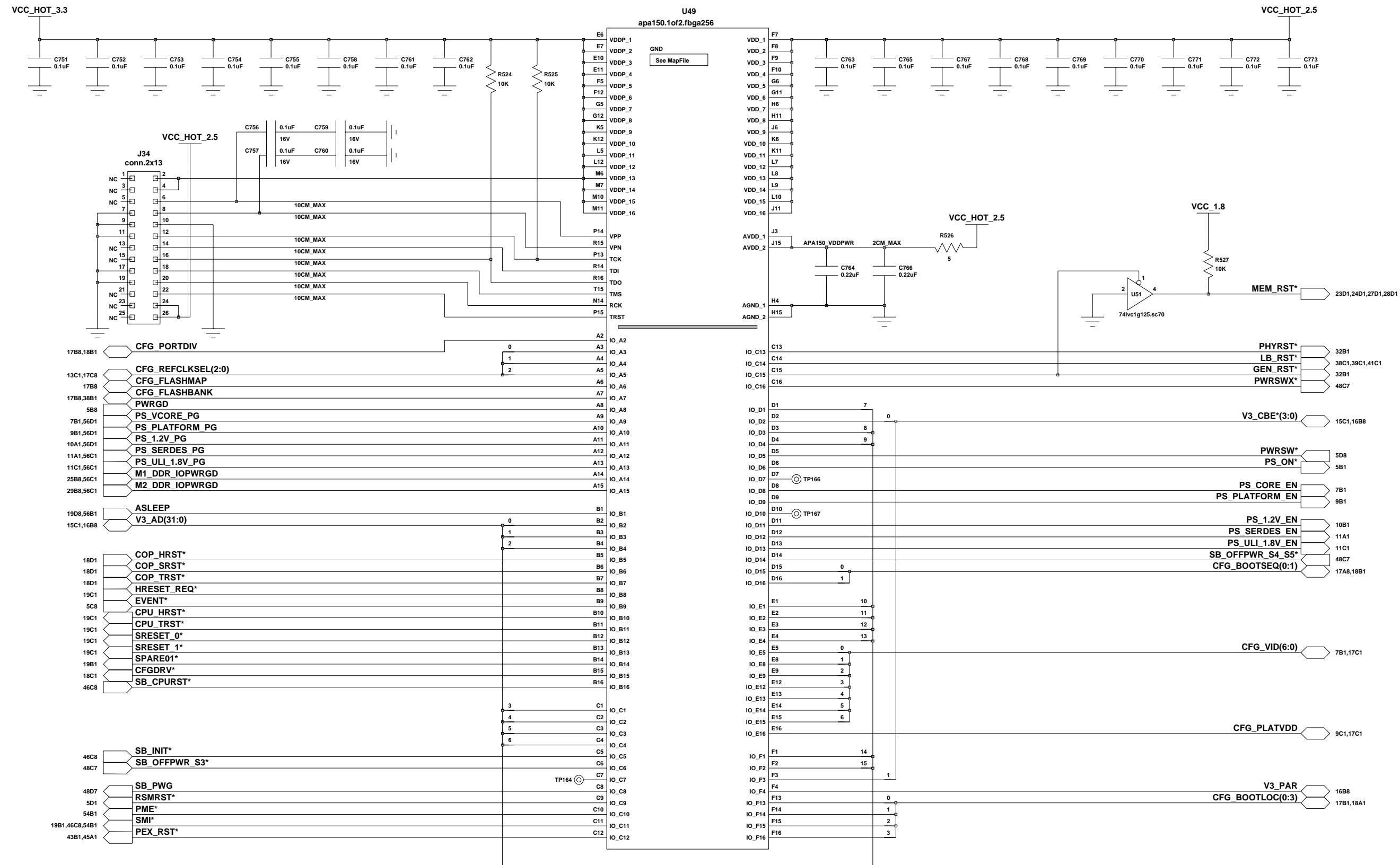
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1	2	3	4	5	6	7



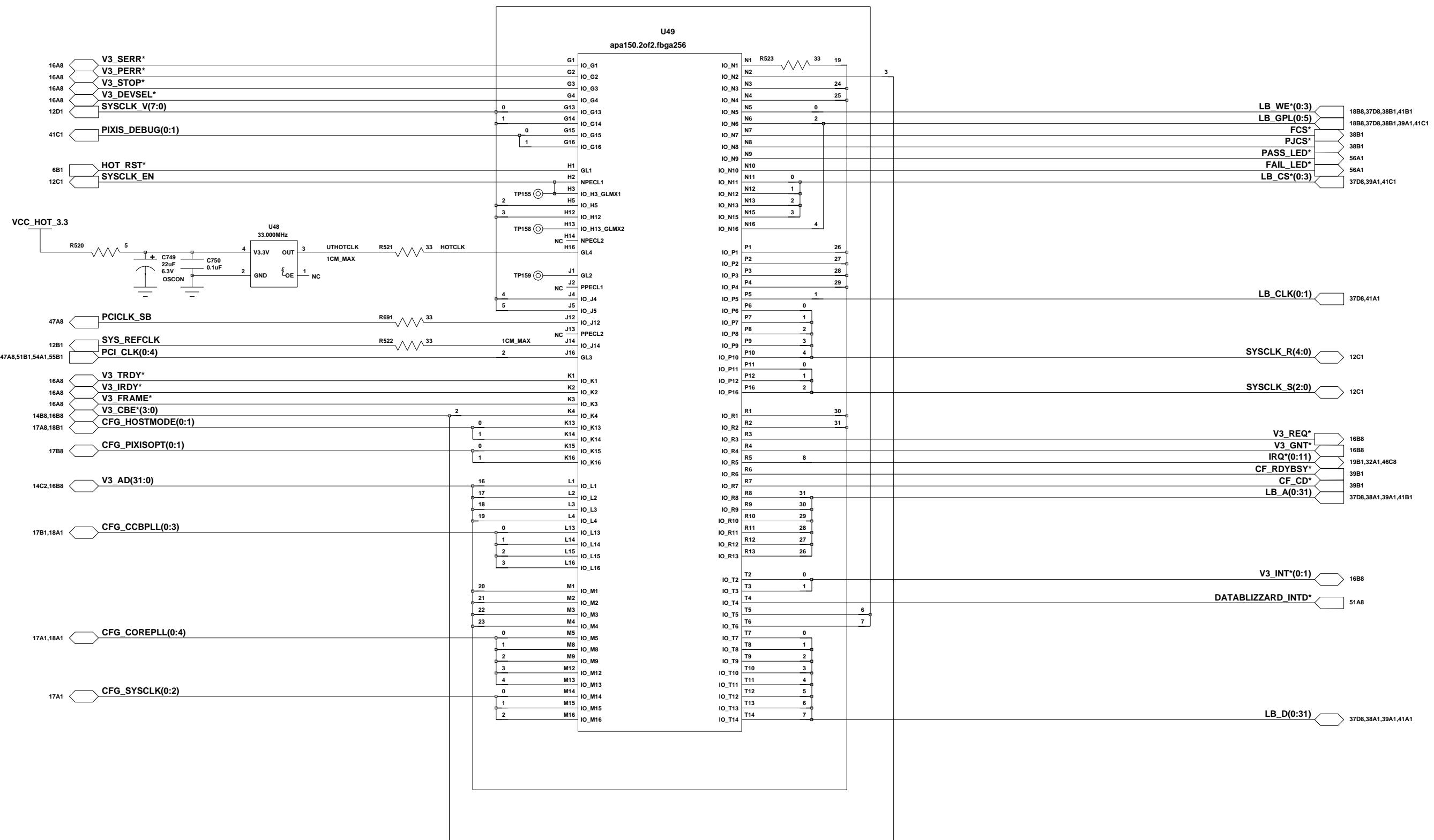
freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Cass Arnett	Date Changed: Thursday, February 1, 2007 Time Changed: 2:08:11 pm	Title: SERDES 1.2V and PHY 1.8V Power	Page: 11
1	2	3	4	5	6	7



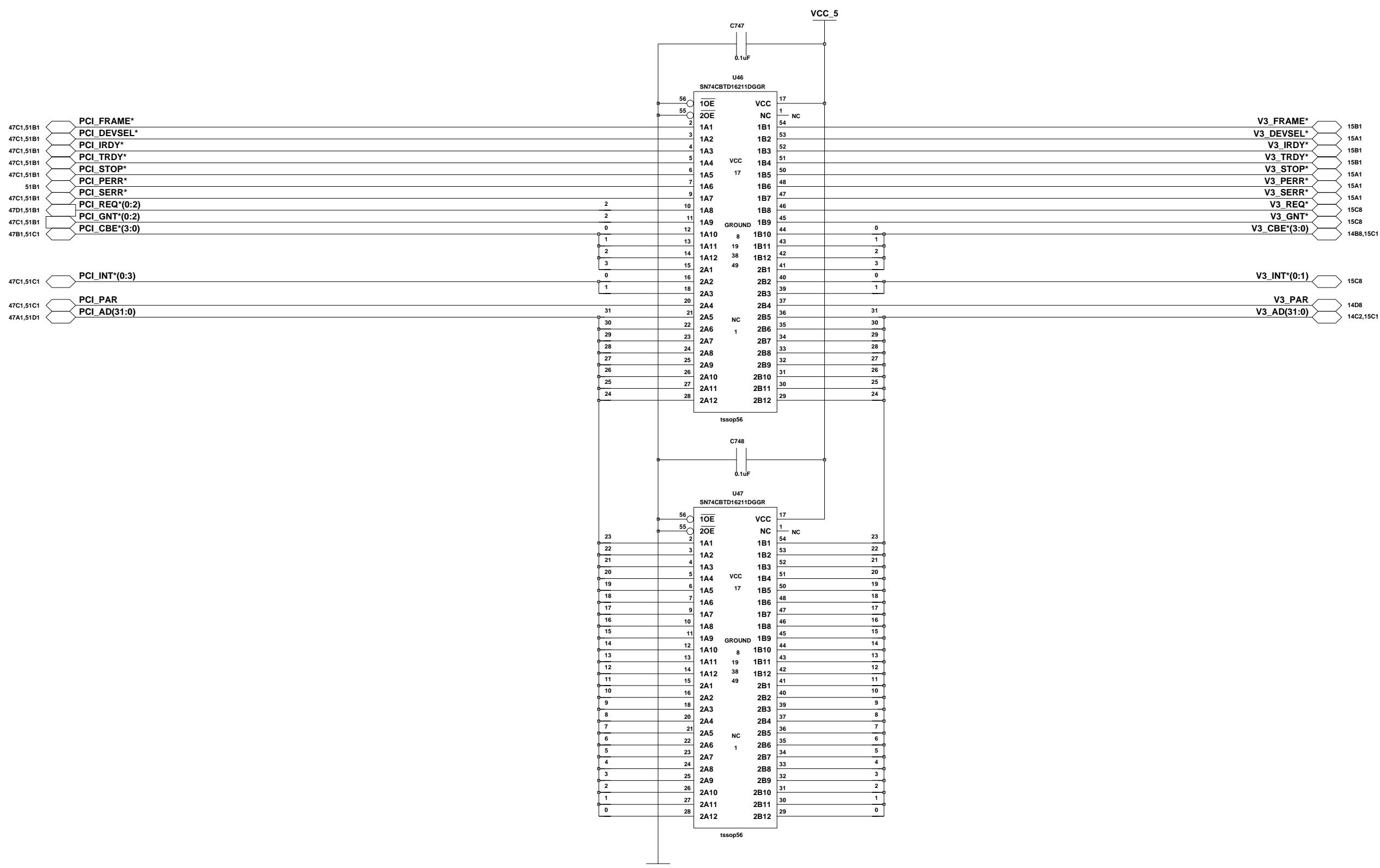


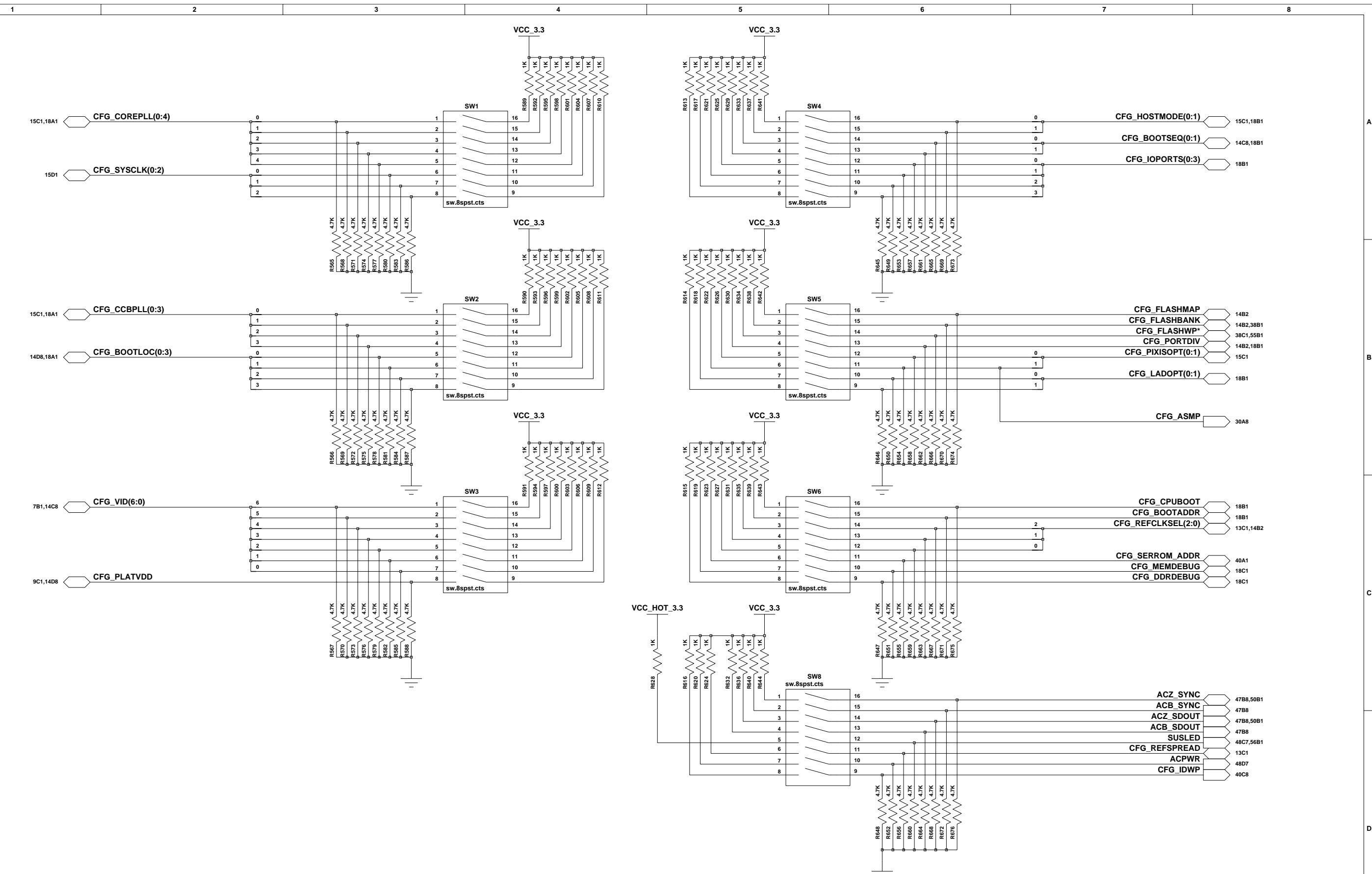


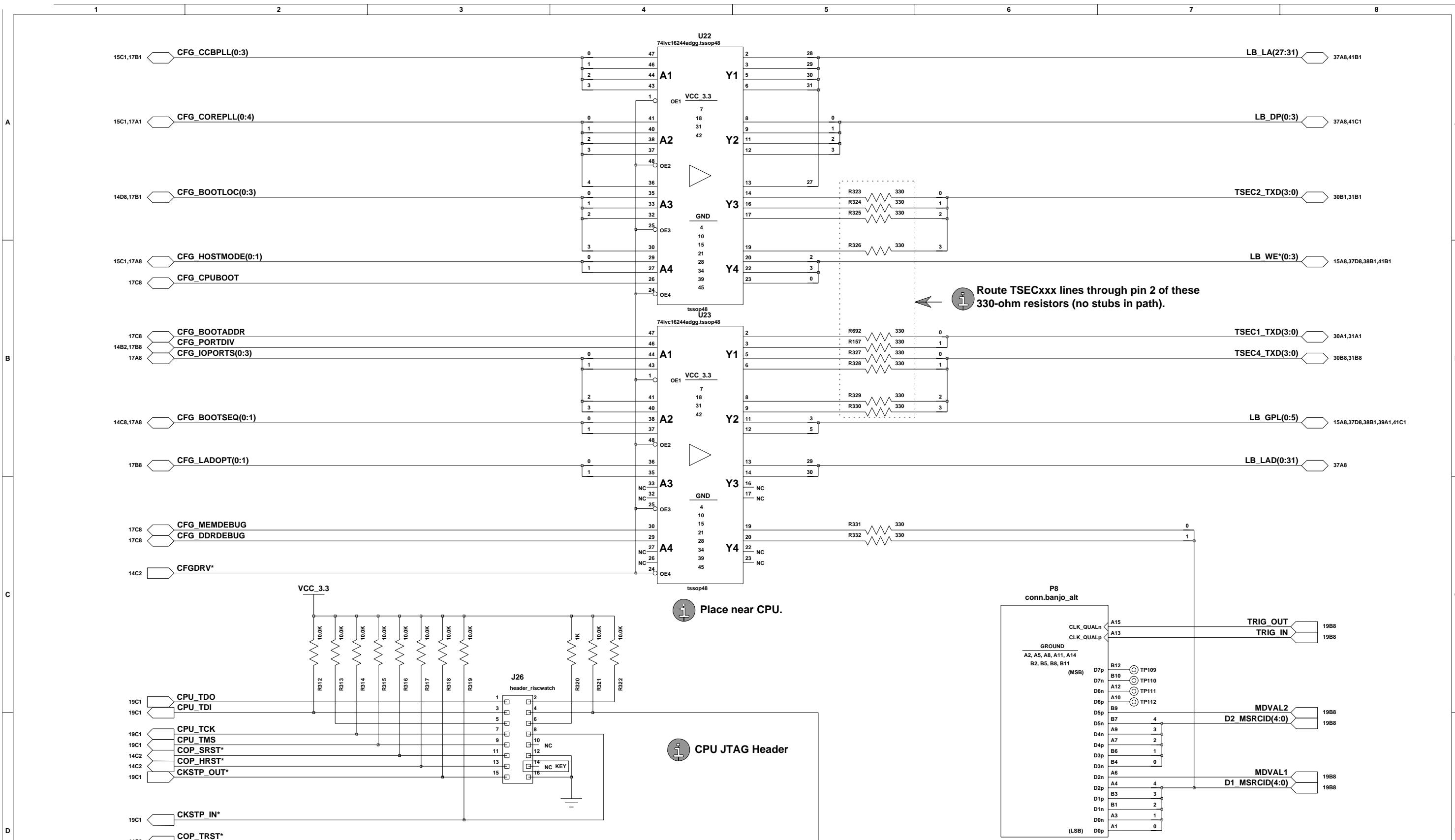
A



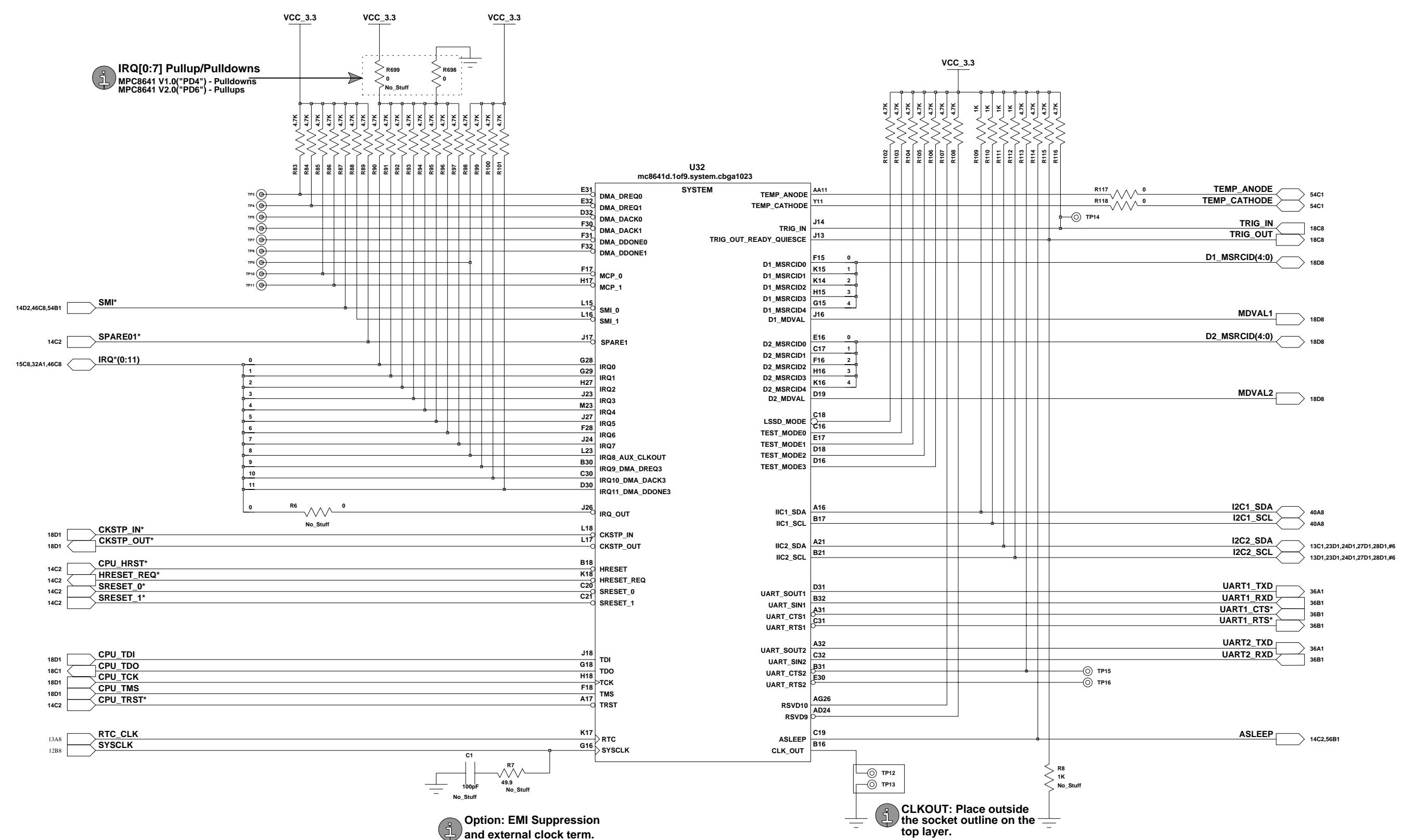
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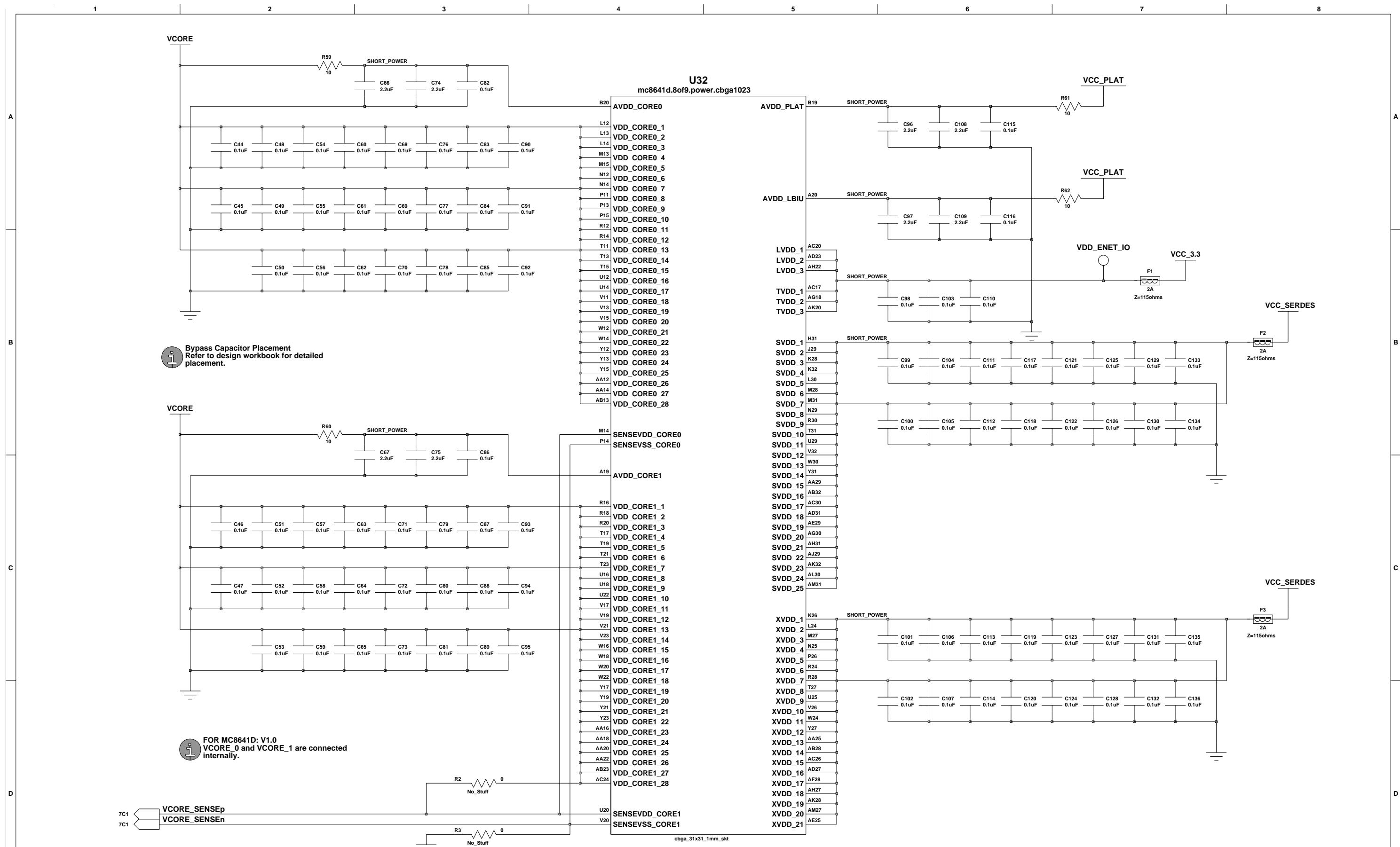


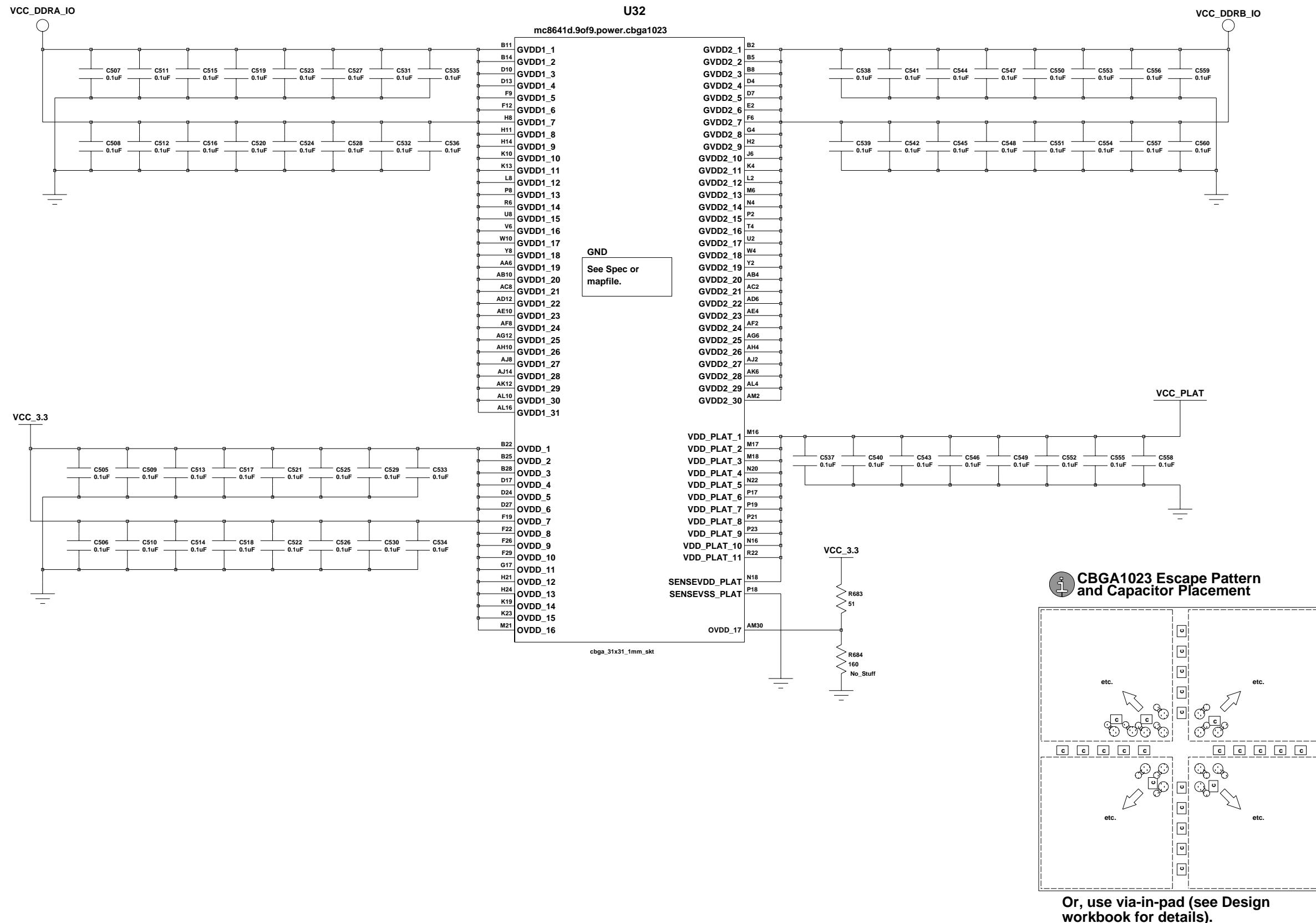




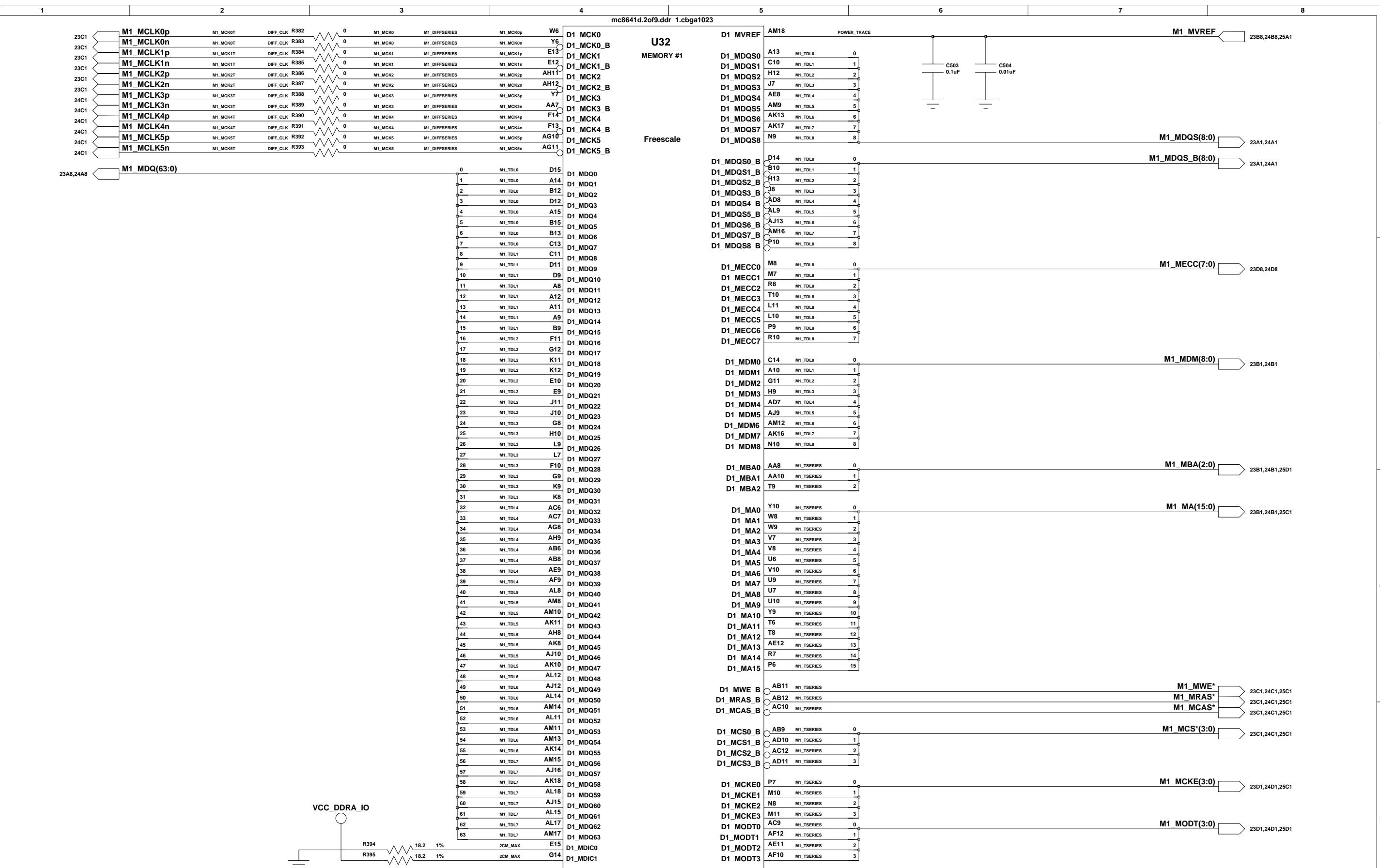
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1	2	3	4	5	6	7

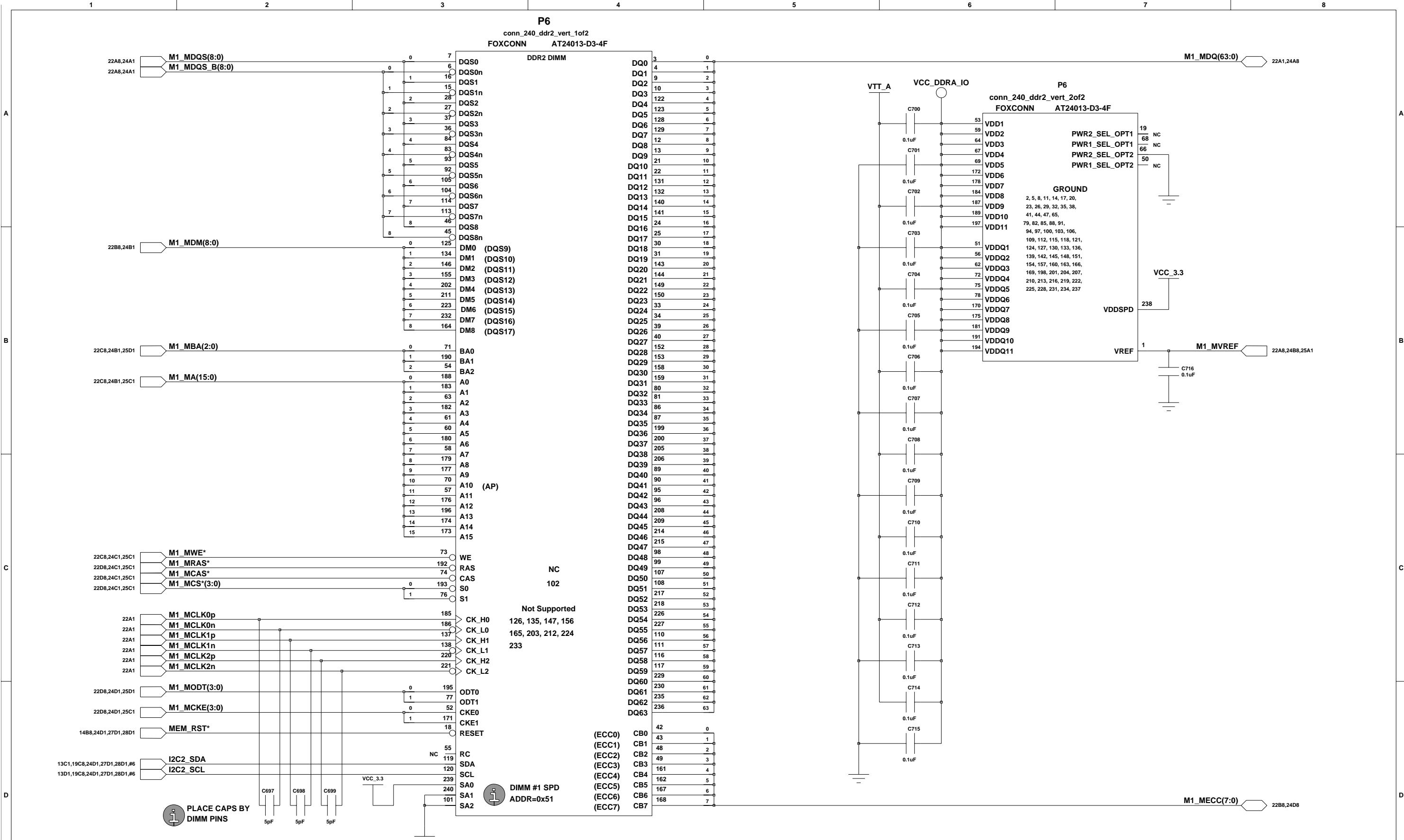


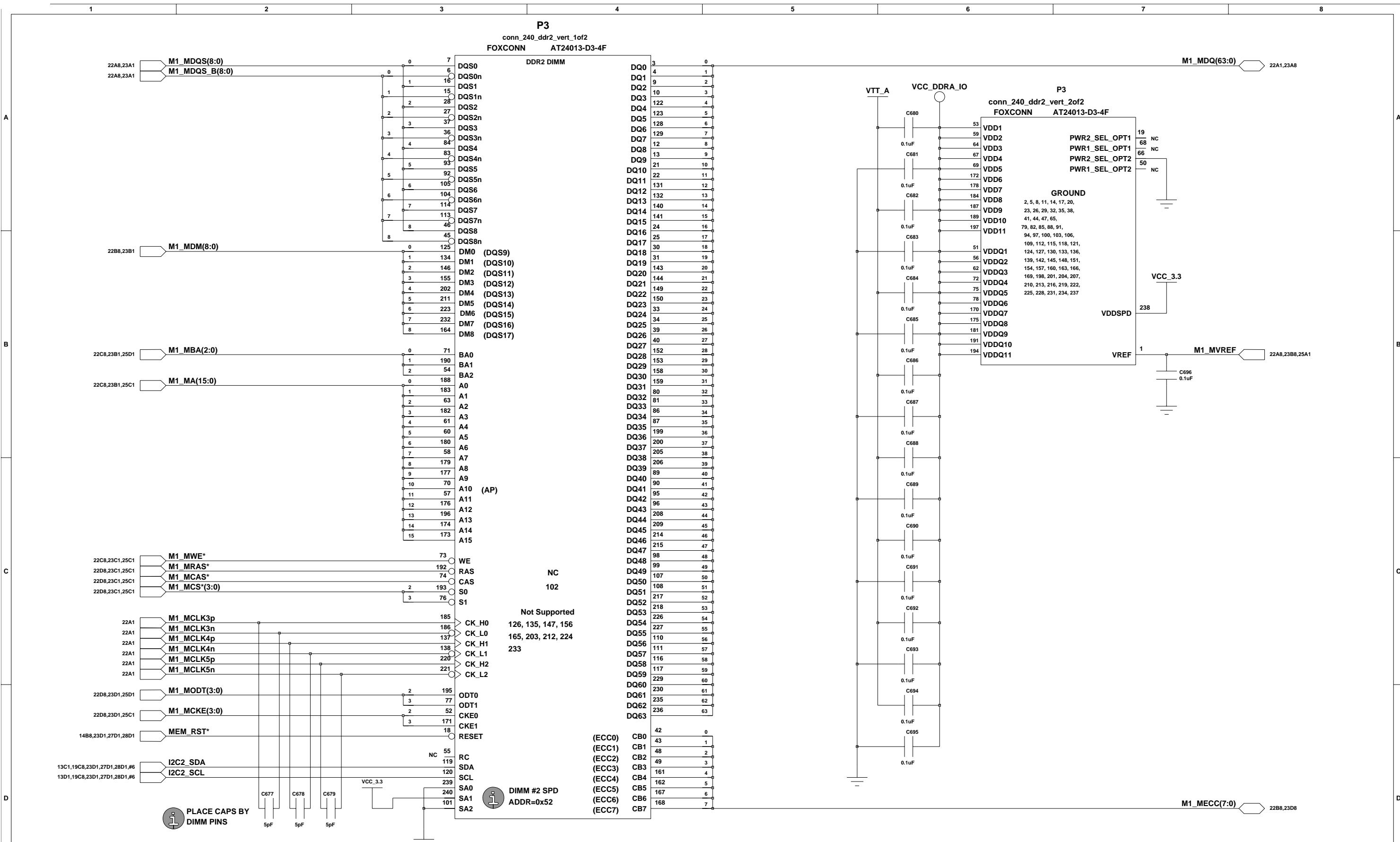


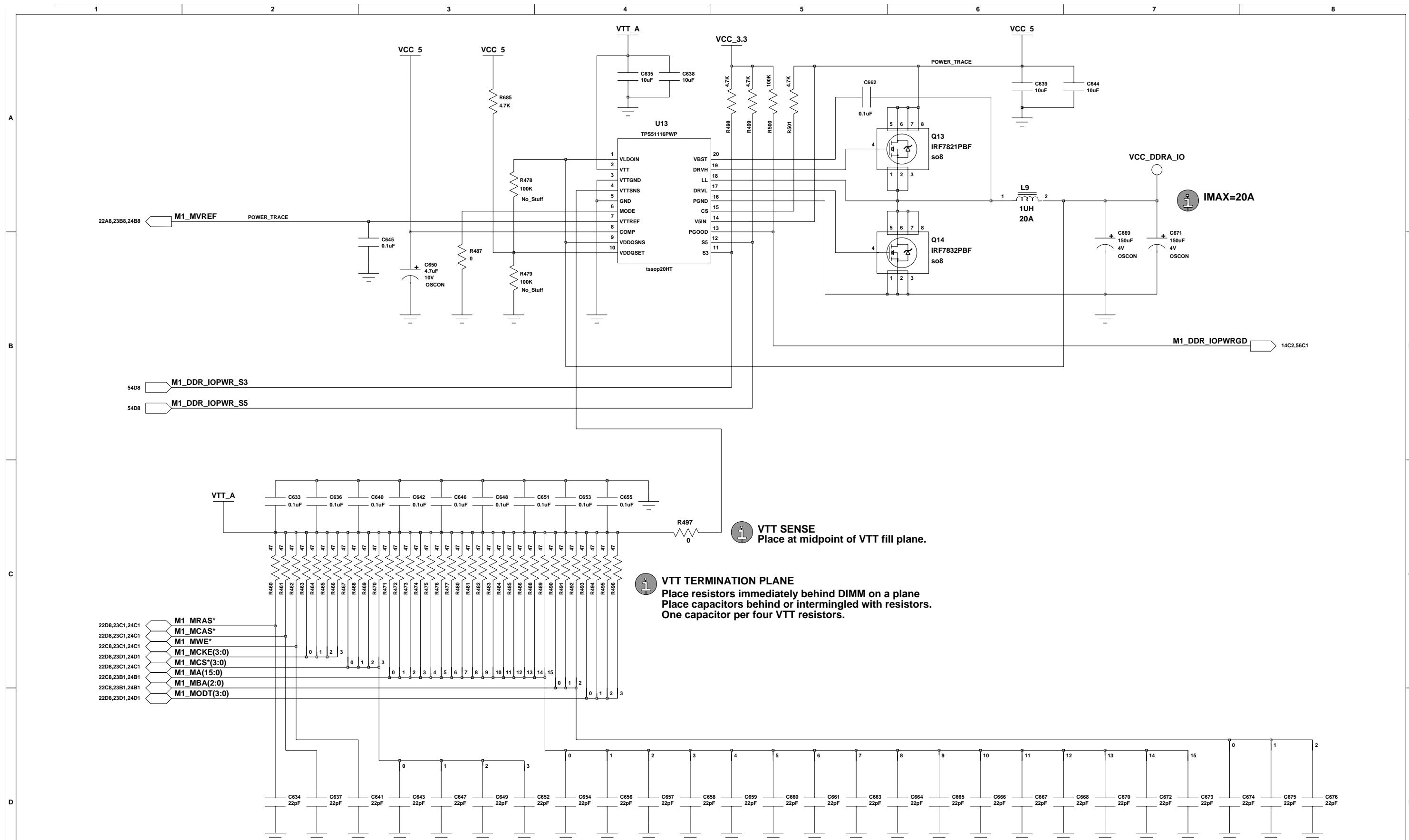


freescale™ semiconductor	Freescale Semiconductor 7700 W. Farmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Gary Milliorn	Date Changed: Thursday, February 1, 2007 Time Changed: 2:10:02 pm	Title: MC8641D Power, Part 2	Page: 21
1	2	3	4	5	6	7

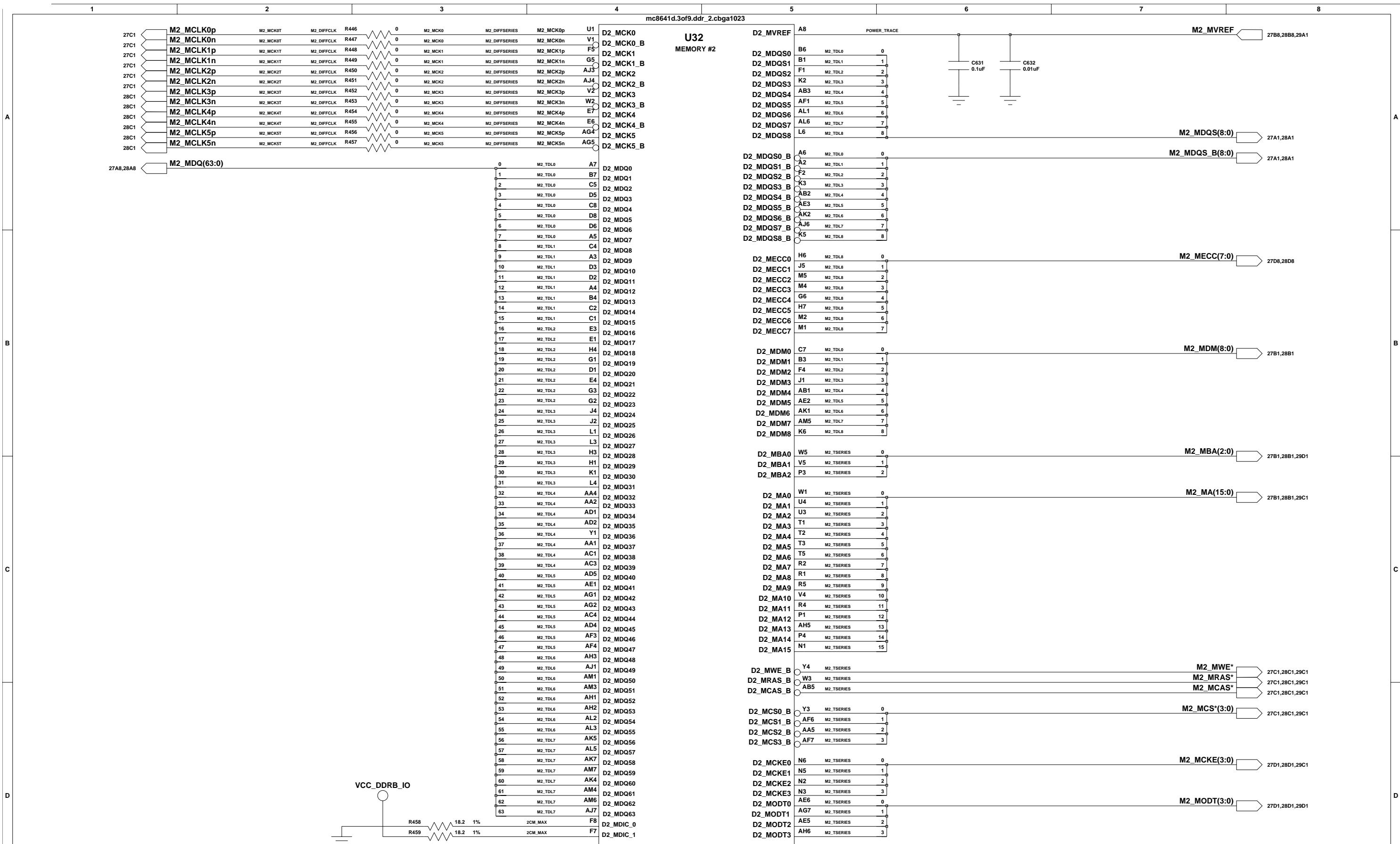


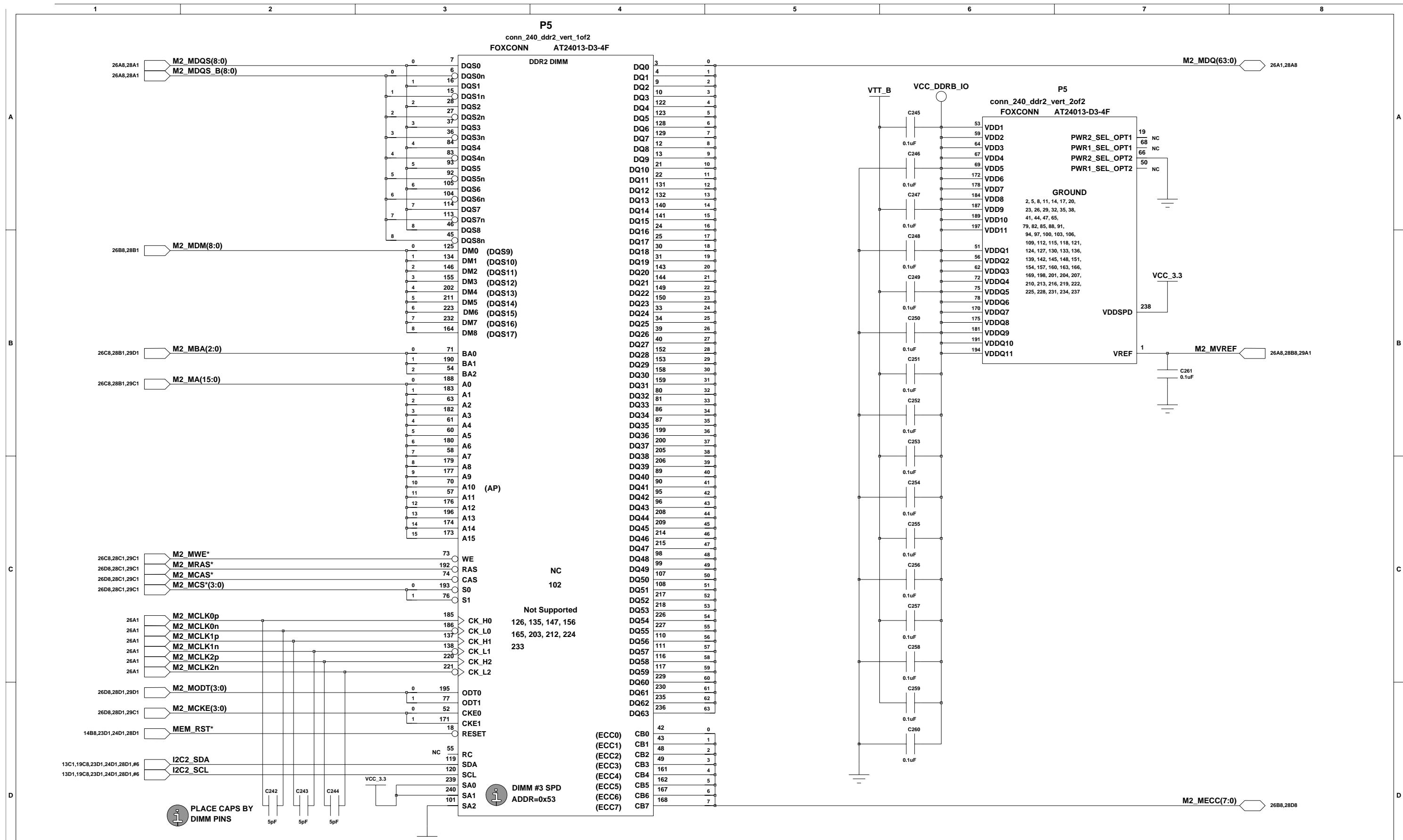


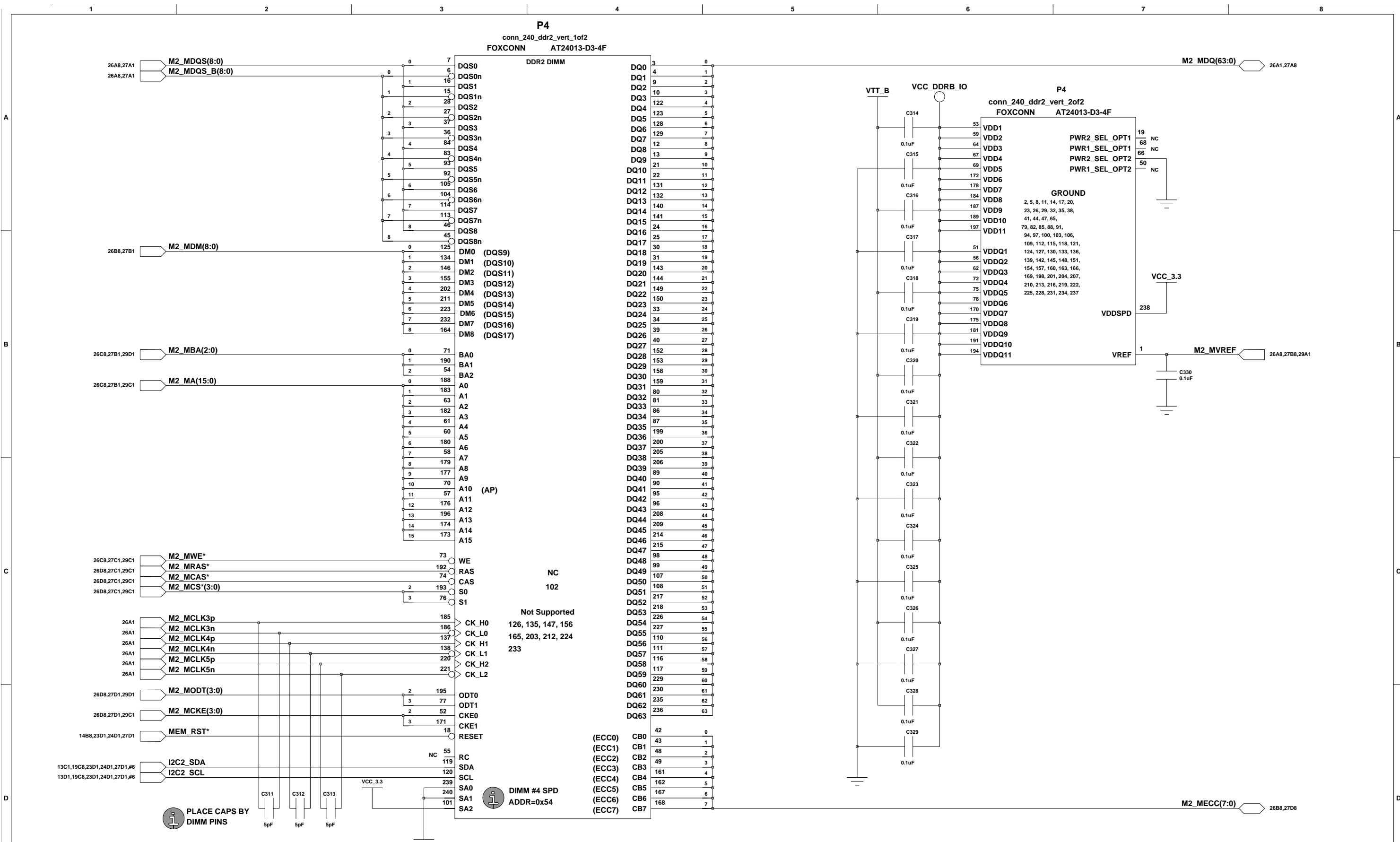


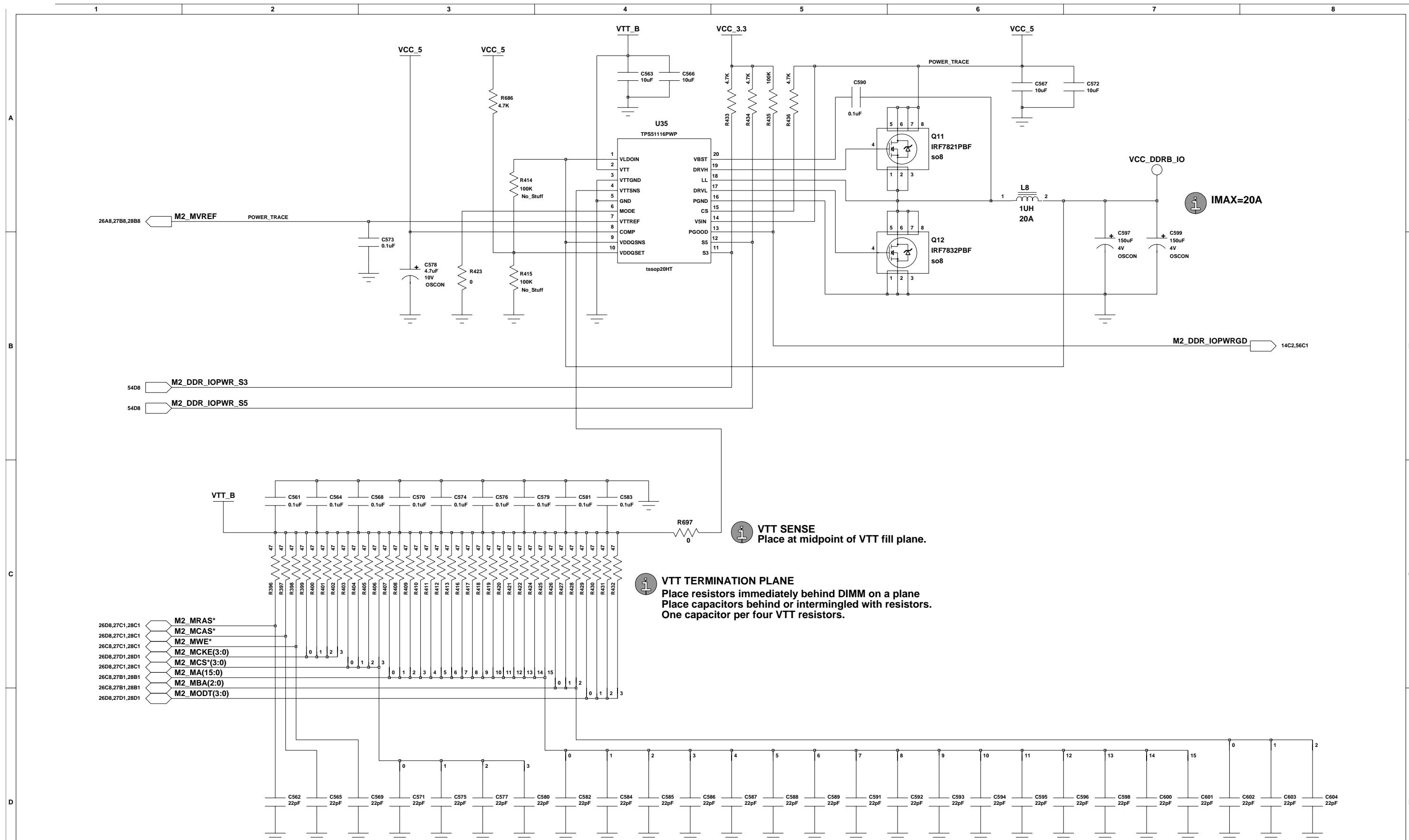


freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Gary Milliorn	Date Changed: Thursday, February 1, 2007 Time Changed: 2:10:39 pm	Title: DDR-II Interface #1 Power and Termination	Page: 25
1	2	3	4	5	6	7

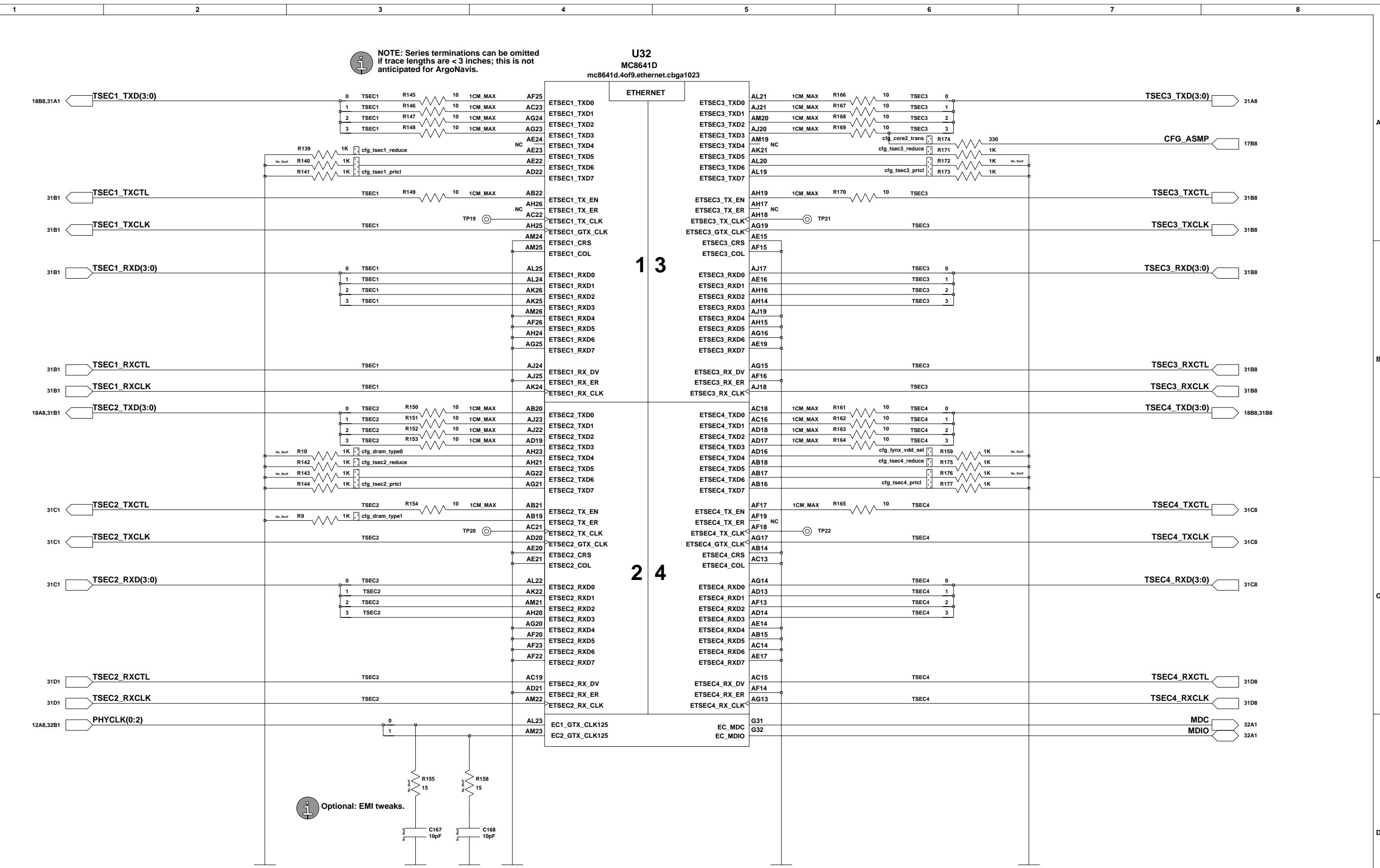




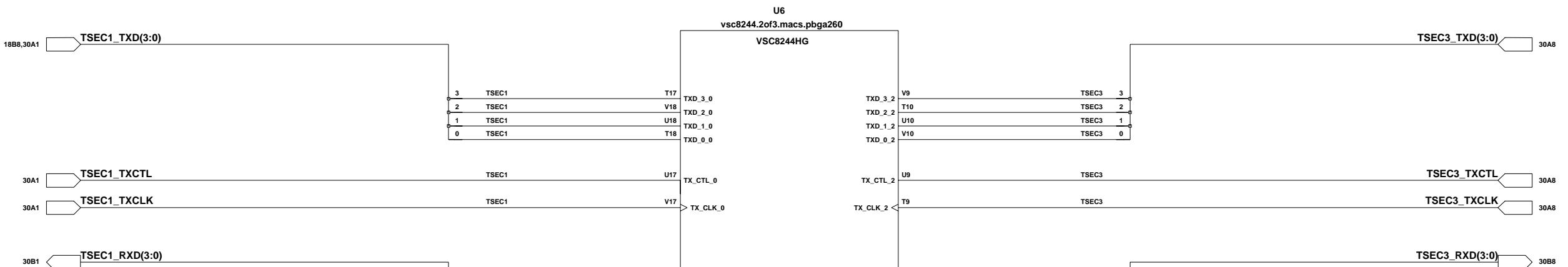




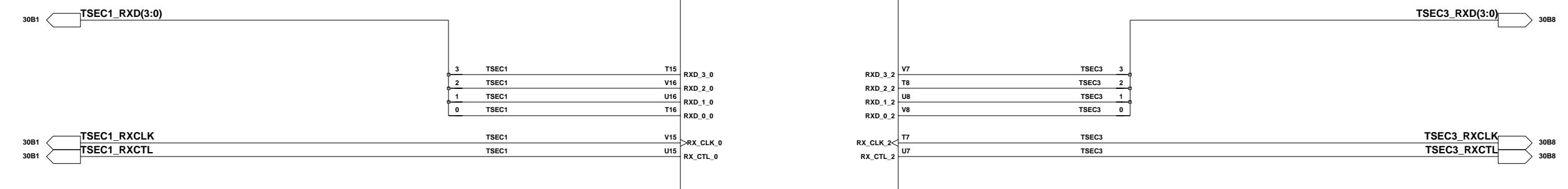
freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Gary Milliorn	Date Changed: Thursday, February 1, 2007 Time Changed: 2:11:16 pm	Title: DDR-II Interface #2 Power and Termination	Page: 29
1	2	3	4	5	6	7



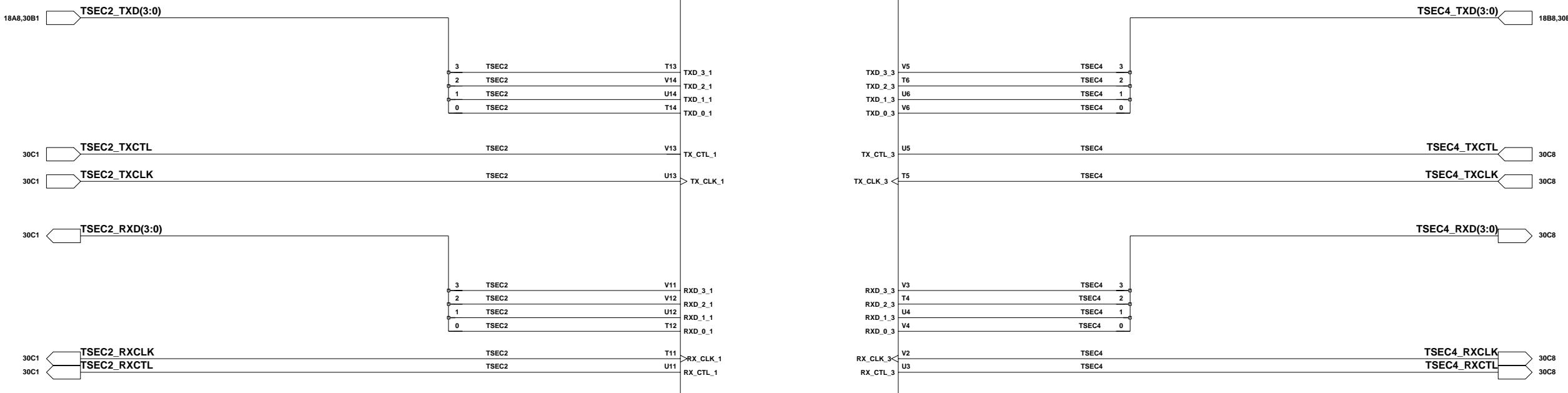
A



B

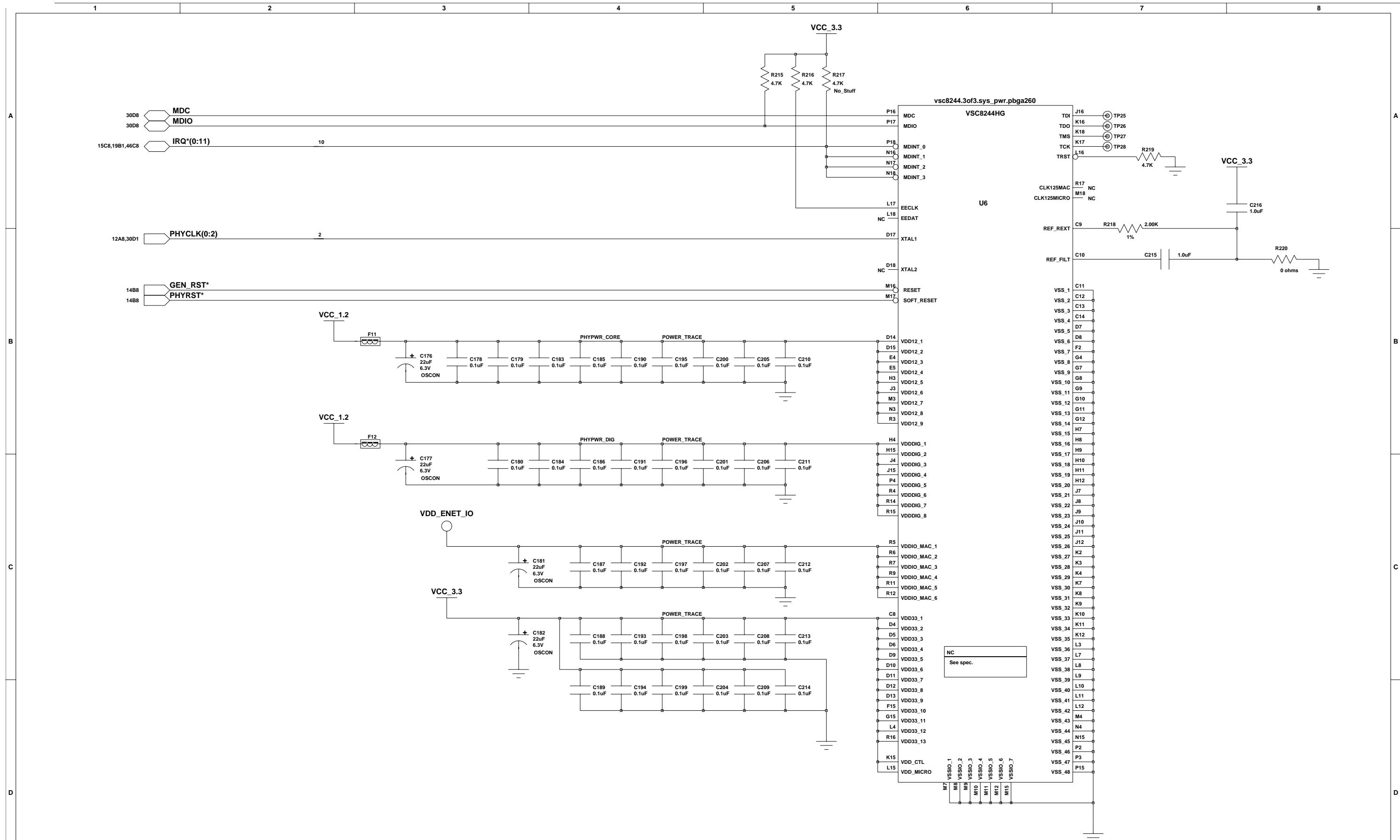


C

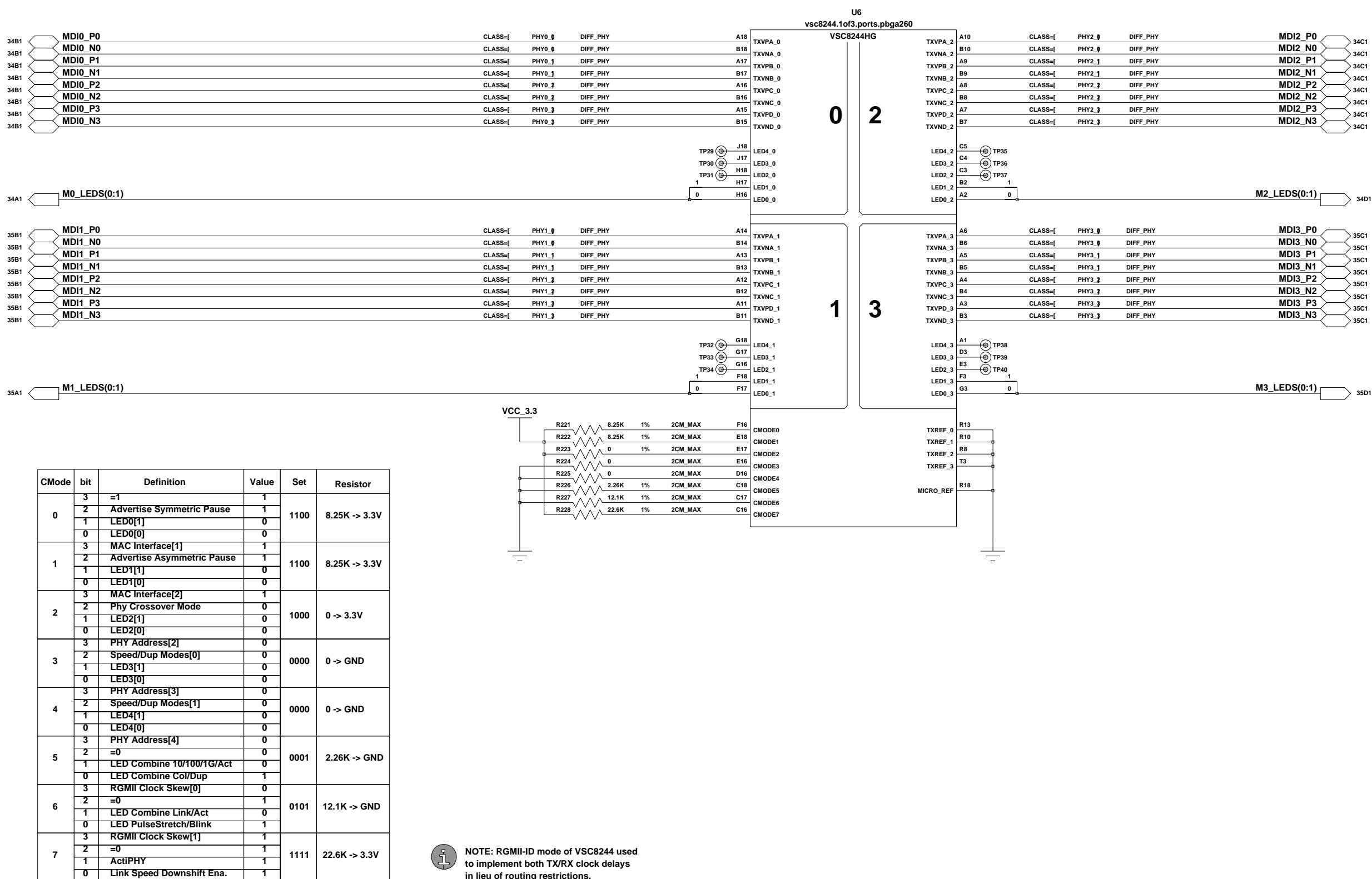


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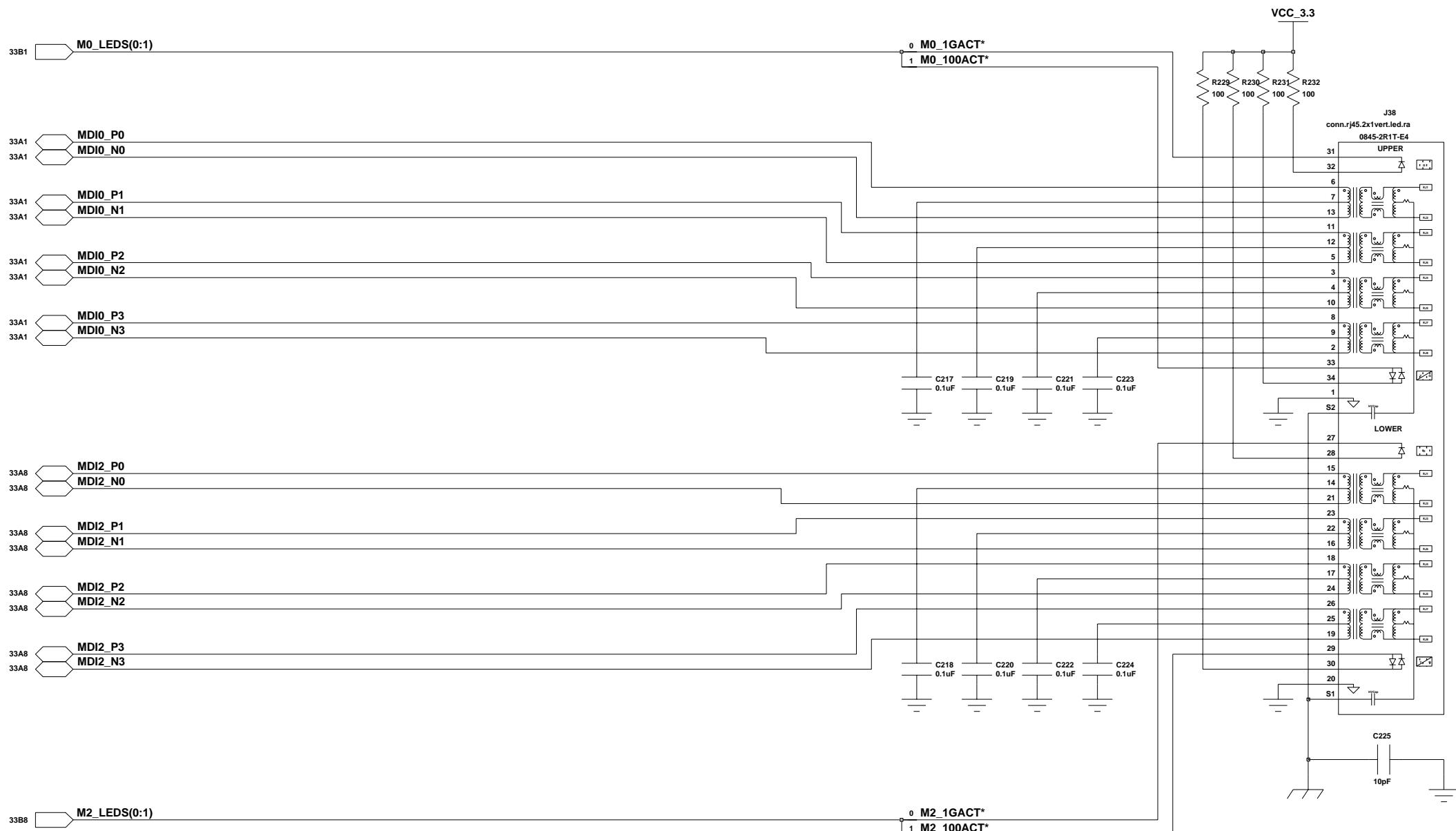
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1	2	3	4	5	6	7 8



freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Gary Milliorn	Date Changed: Thursday, February 1, 2007 Time Changed: 2:11:43 pm	Title: Quad Ethernet Port Power and Control	Page: 32
1	2	3	4	5	6	7



A



B

C

D

A

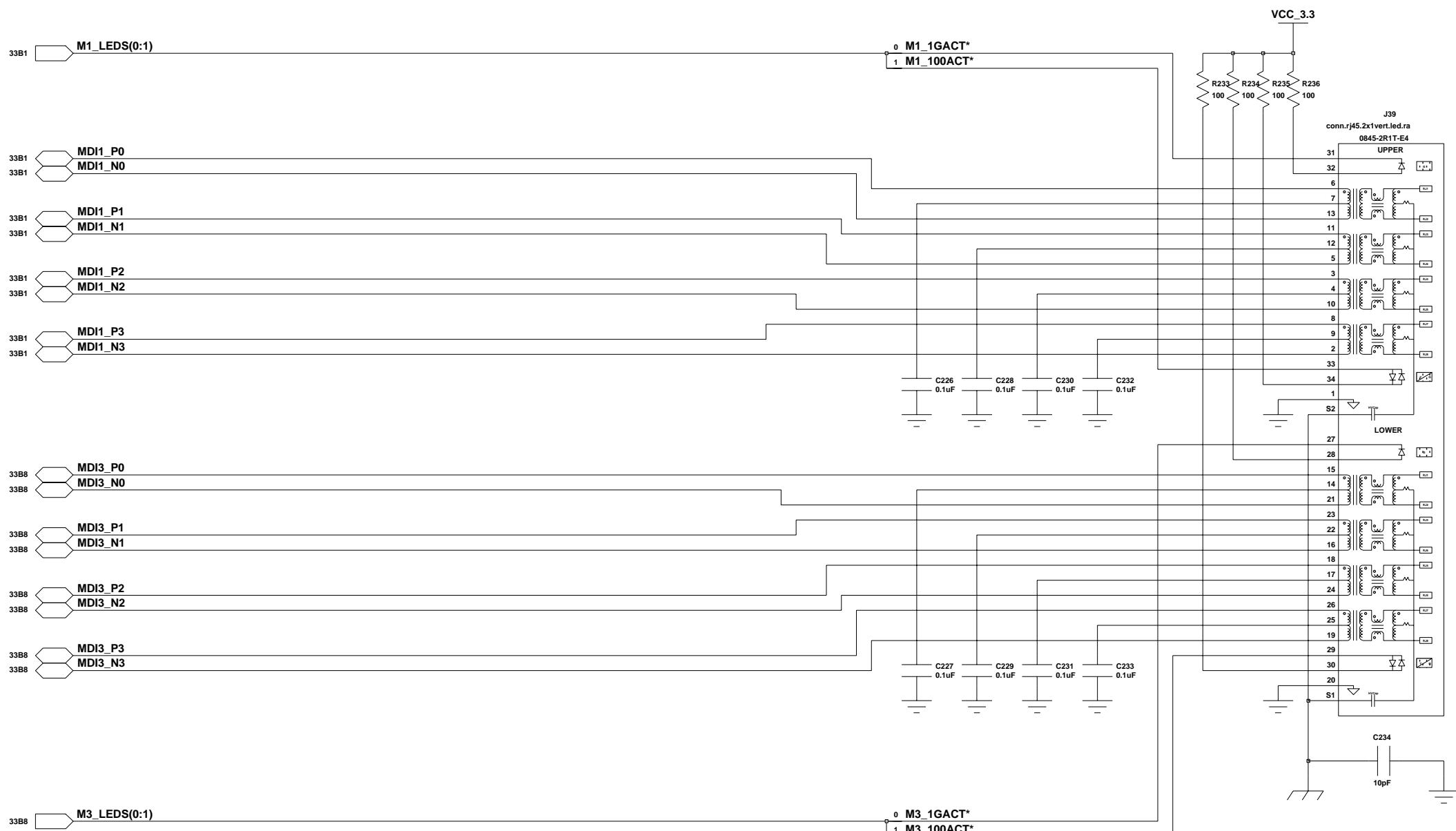
B

C

D

 freescale™ semiconductor	Freescale Semiconductor 7700 W. Farmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Gary Milliorn	Date Changed: Thursday, February 1, 2007 Time Changed: 2:12:00 pm	Title: Ethernet Ports #1 and #3	Page: 34
1	2	3	4	5	6	7

A



A

B

B

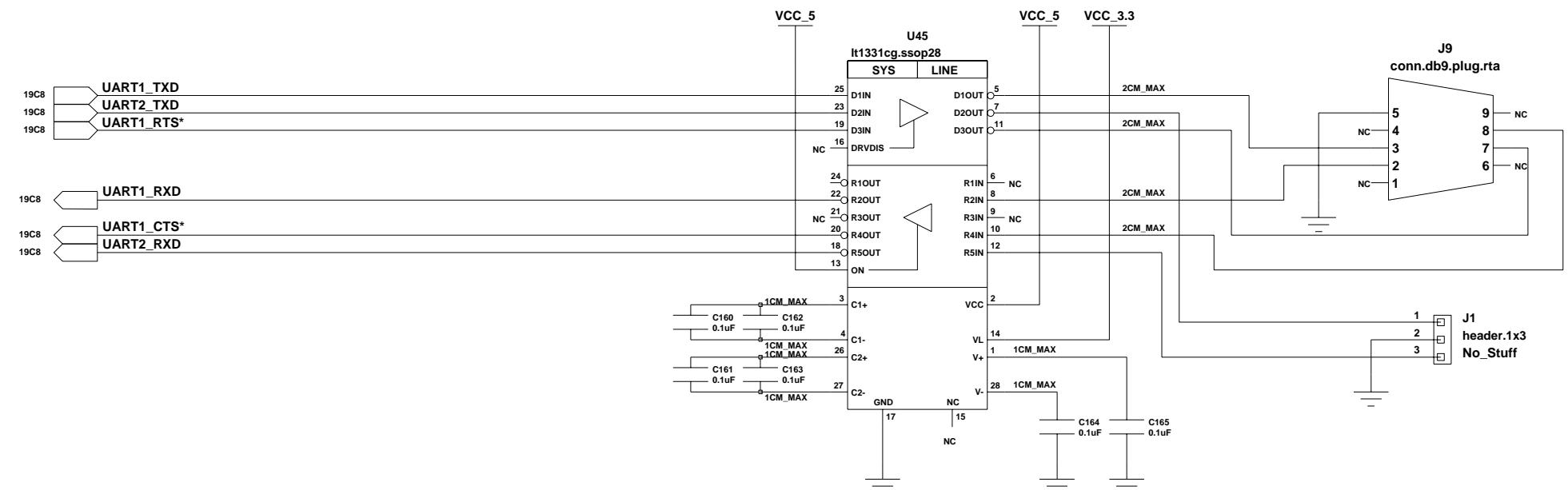
C

C

D

D

A



Serial Port #1

Serial Port #2
Requires custom cable.

B

C

D

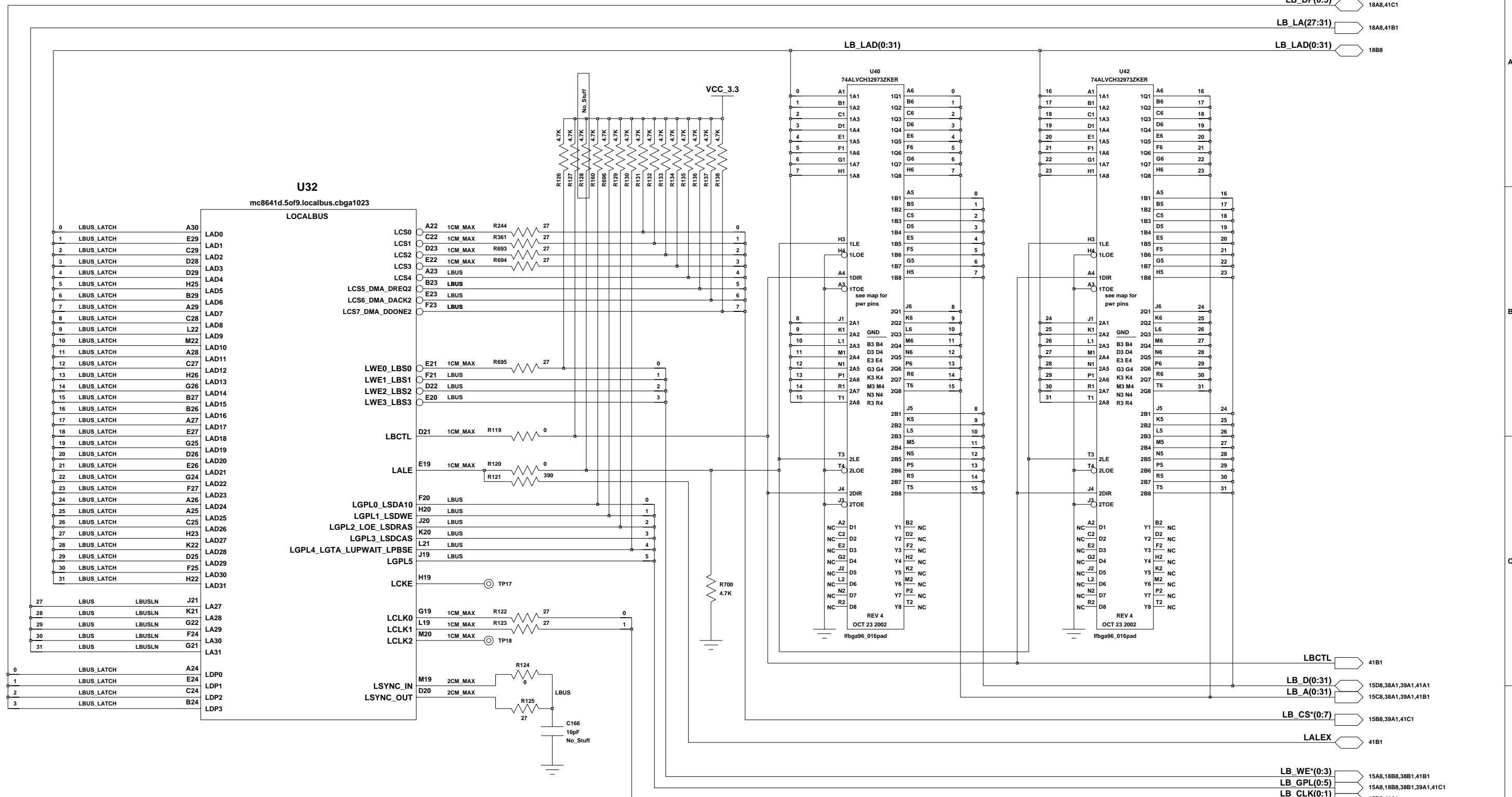
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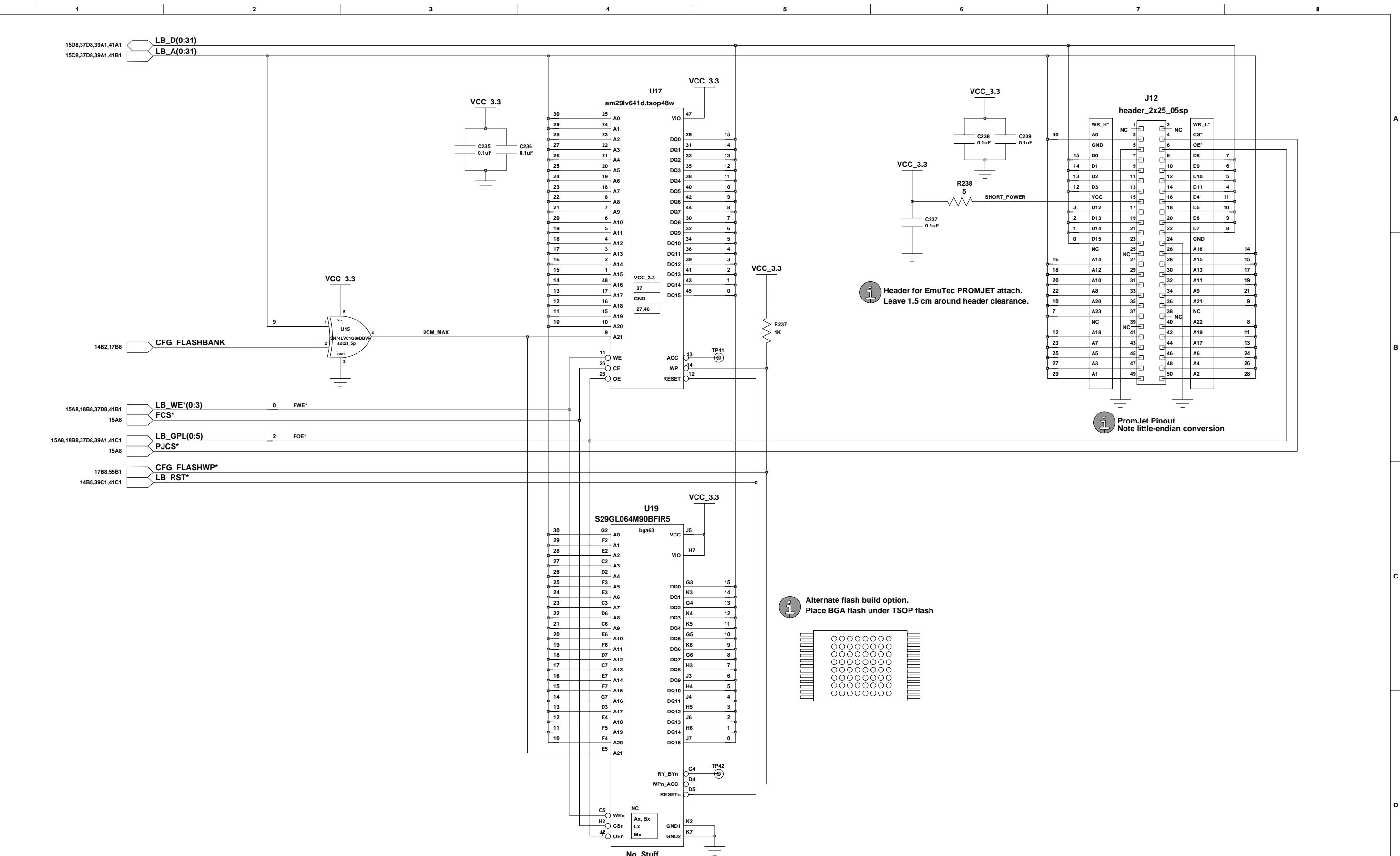
B

C

D

freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Gary Milliorn	Date Changed: Thursday, February 1, 2007 Time Changed: 2:12:20 pm	Title: Serial Ports	Page: 36
1	2	3	4	5	6	7





freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Gary Milliorn	Date Changed: Wednesday, November 8, 2006 Time Changed: 10:23:30 am	Title: Local Bus - Flash and Flash Emulator	Page: 38
1	2	3	4	5	6	7

A

15D8,37D8,38A1,41A1
15C8,37D8,38A1,41B1

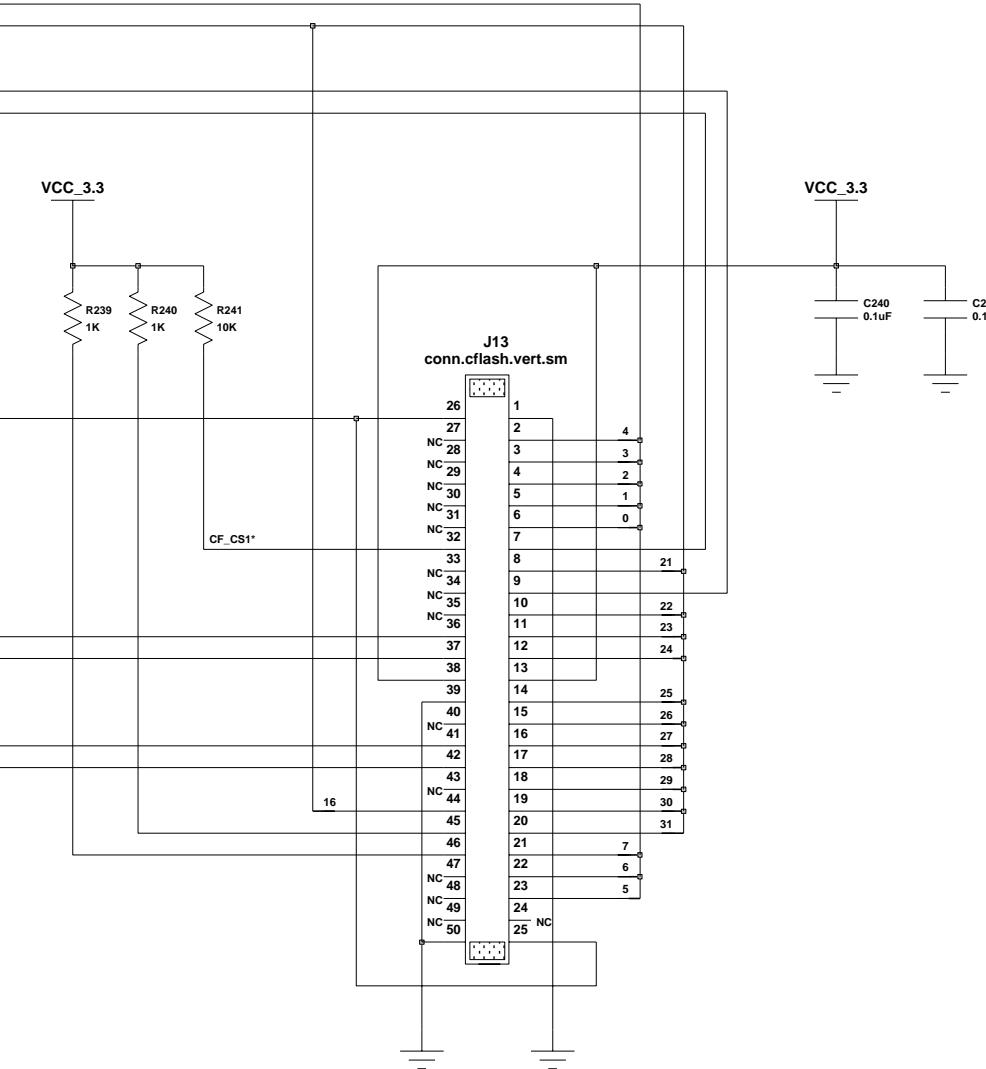
15A8,18B8,37D8,38B1,41C1
15B8,37D8,41C1

CF_CD*

CF_RDYBSY*

LB_RST*

CF_WAIT*



Compact Flash Mapping		
Pin	Function	Connection
2	D03	LB_D[4]
3	D04	LB_D[3]
4	D05	LB_D[2]
5	D06	LB_D[1]
6	D07	LB_D[0]
8	A10	LB_A[21]
10	A09	LB_A[22]
11	A08	LB_A[23]
12	A07	LB_A[24]
14	A06	LB_A[25]
15	A05	LB_A[26]
16	A04	LB_A[27]
17	A03	LB_A[28]
18	A02	LB_A[29]
19	A01	LB_A[30]
20	A00	LB_A[31]
21	D00	LB_D[7]
22	D01	LB_D[6]
23	D02	LB_D[5]
44	REG-	LB_A[16]

B

A

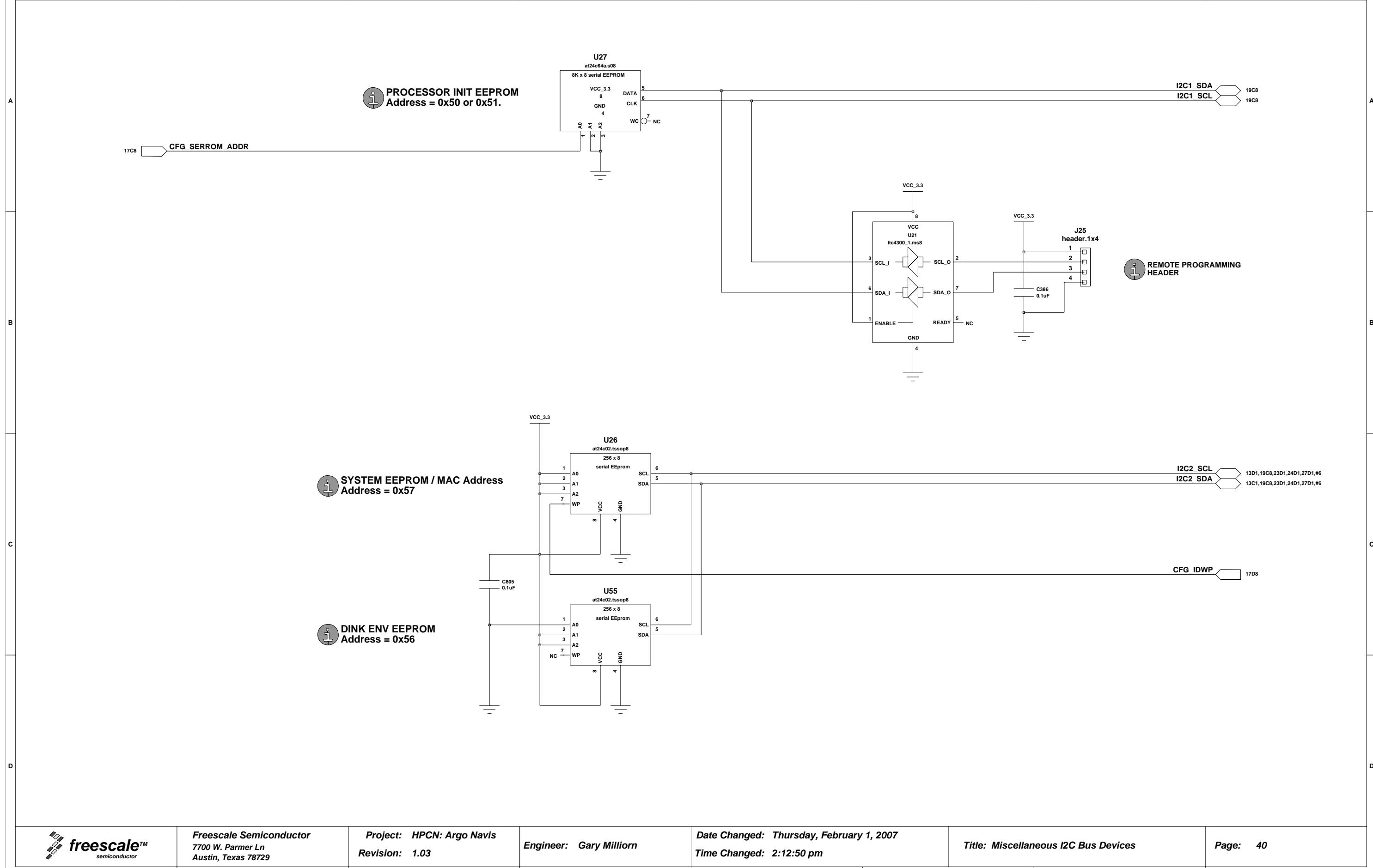
B

C

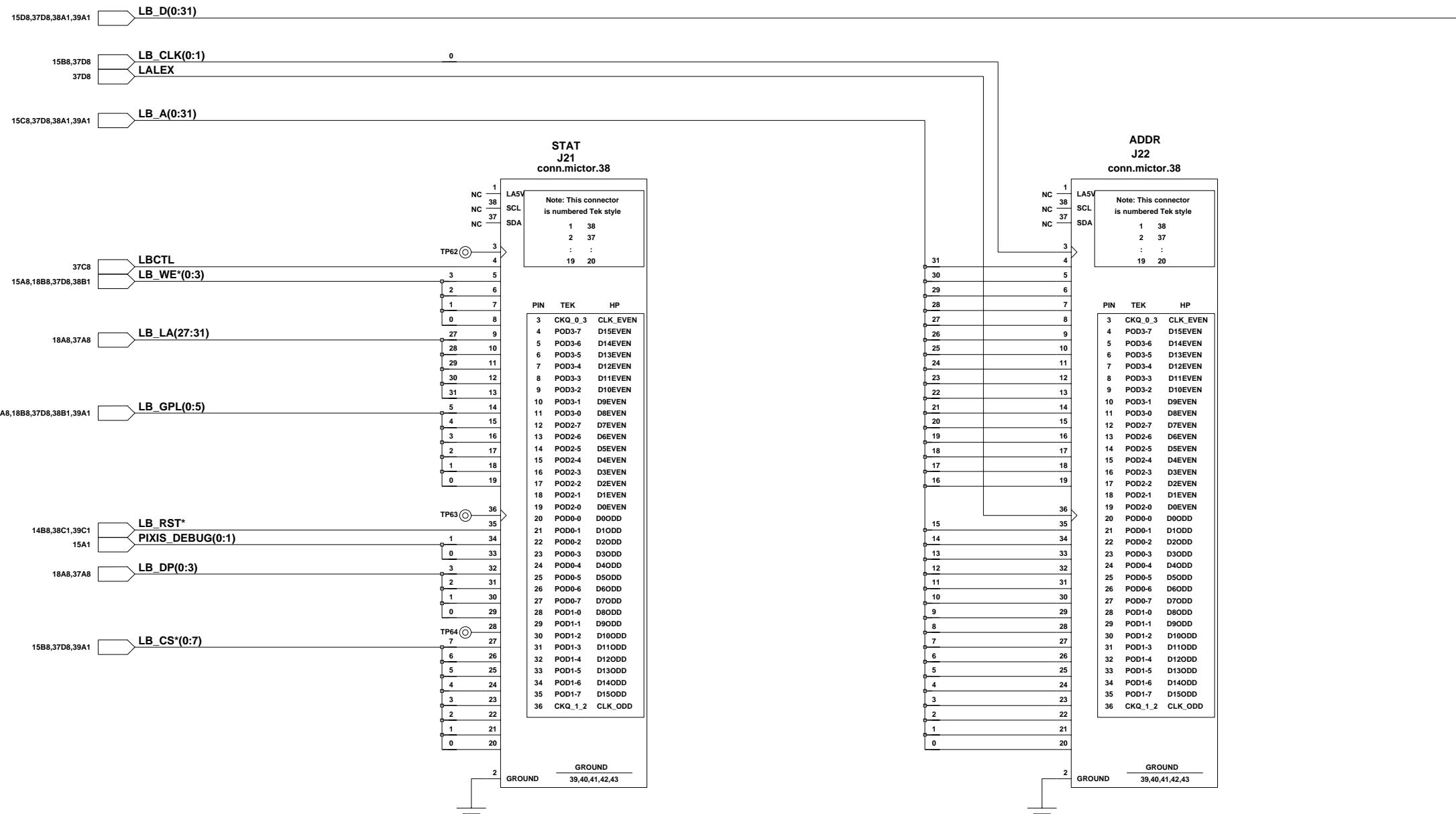
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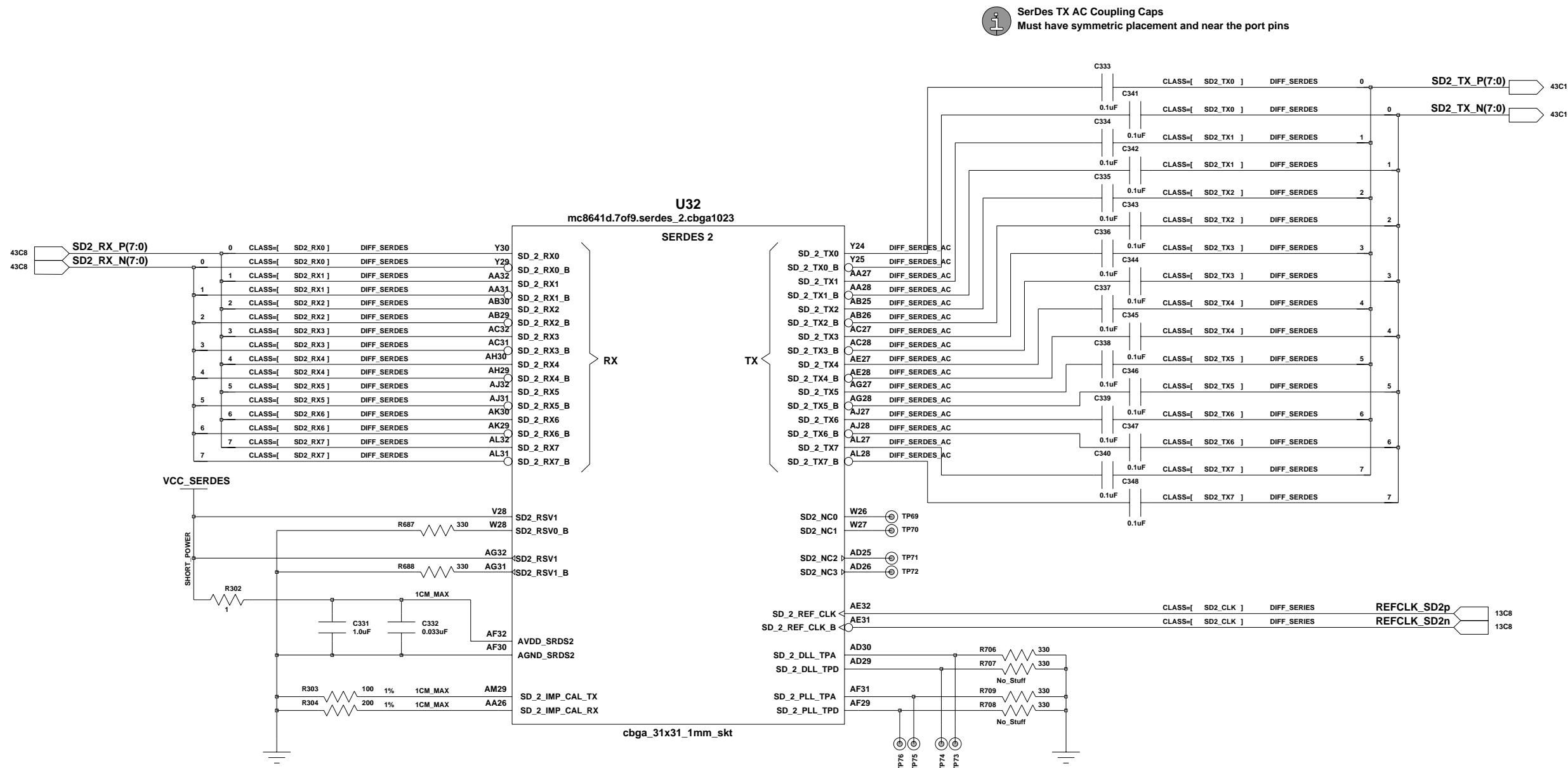
D

D



A

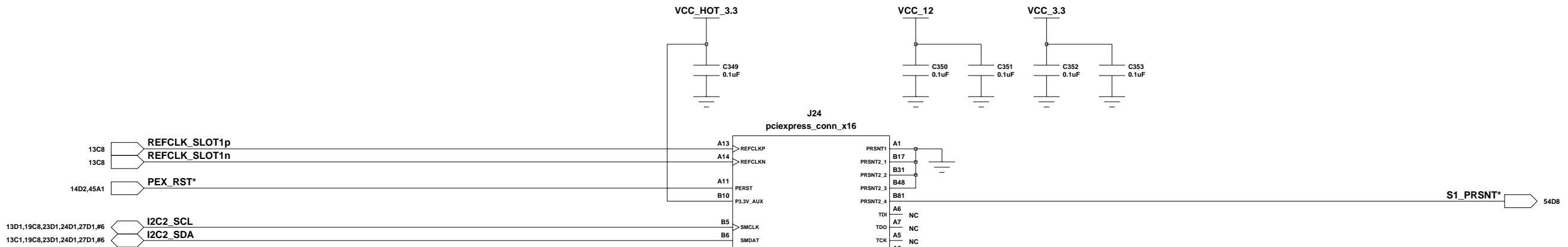




freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Gary Milliorn	Date Changed: Thursday, February 1, 2007 Time Changed: 2:13:09 pm	Title: MC8641D PCIExpress/SERDES/Lynx Port 2	Page: 42
1	2	3	4	5	6	7

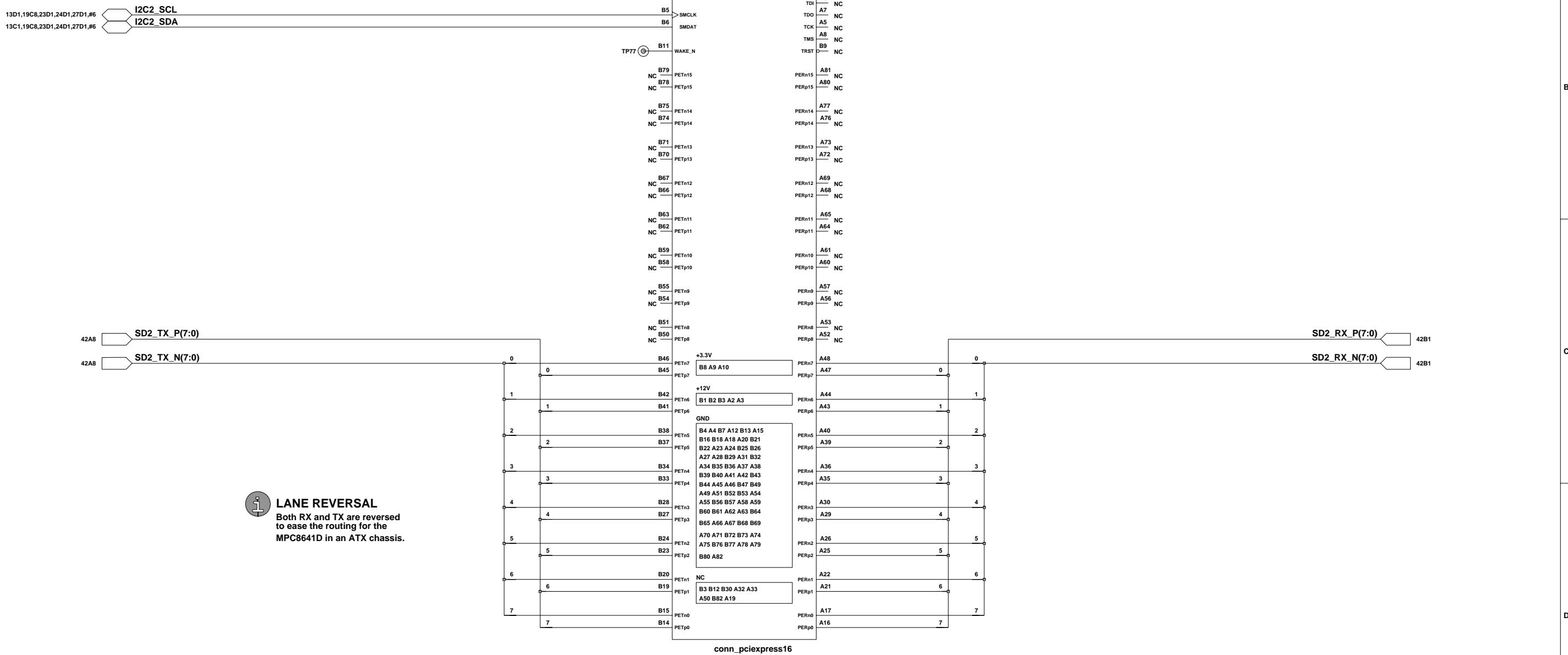
A

A



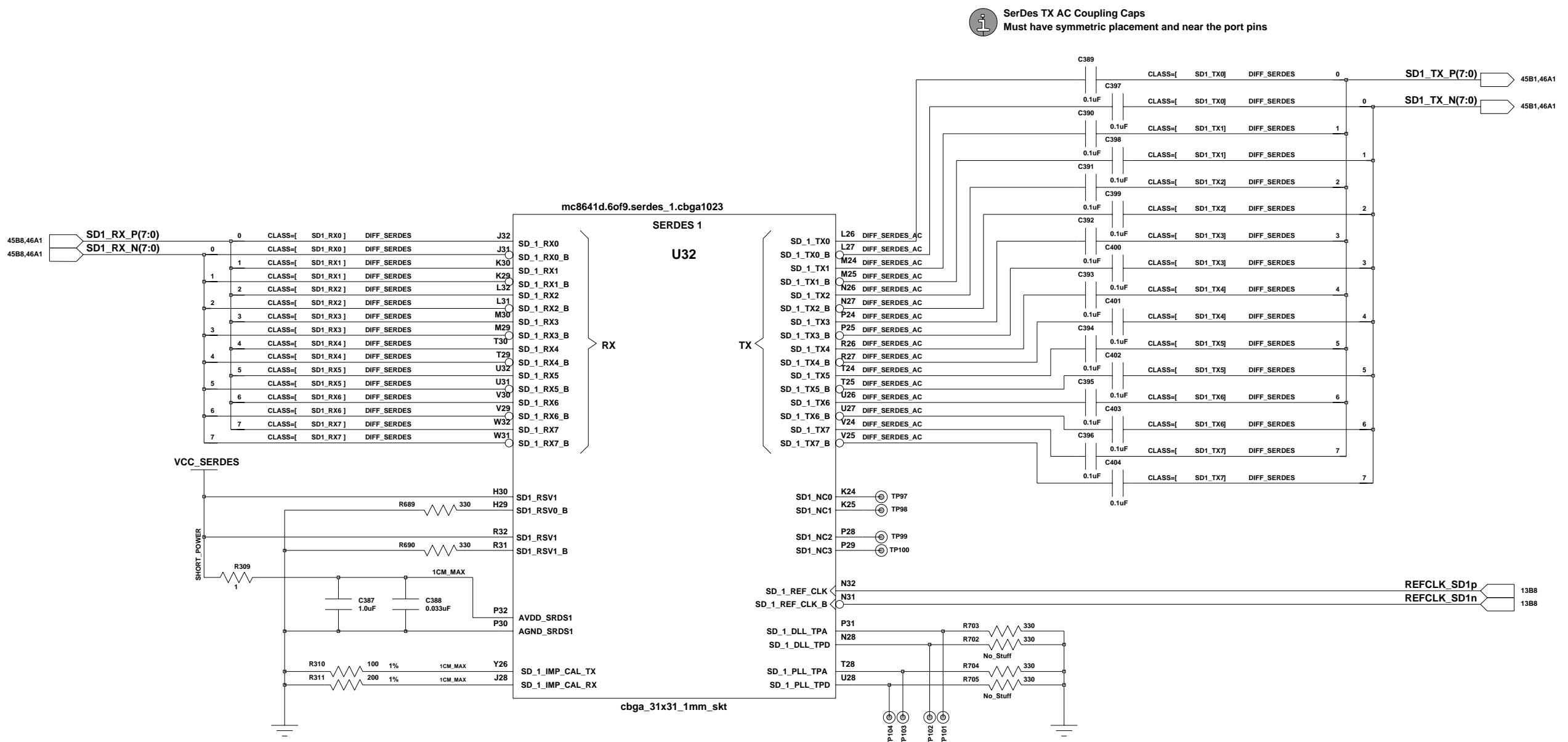
B

B

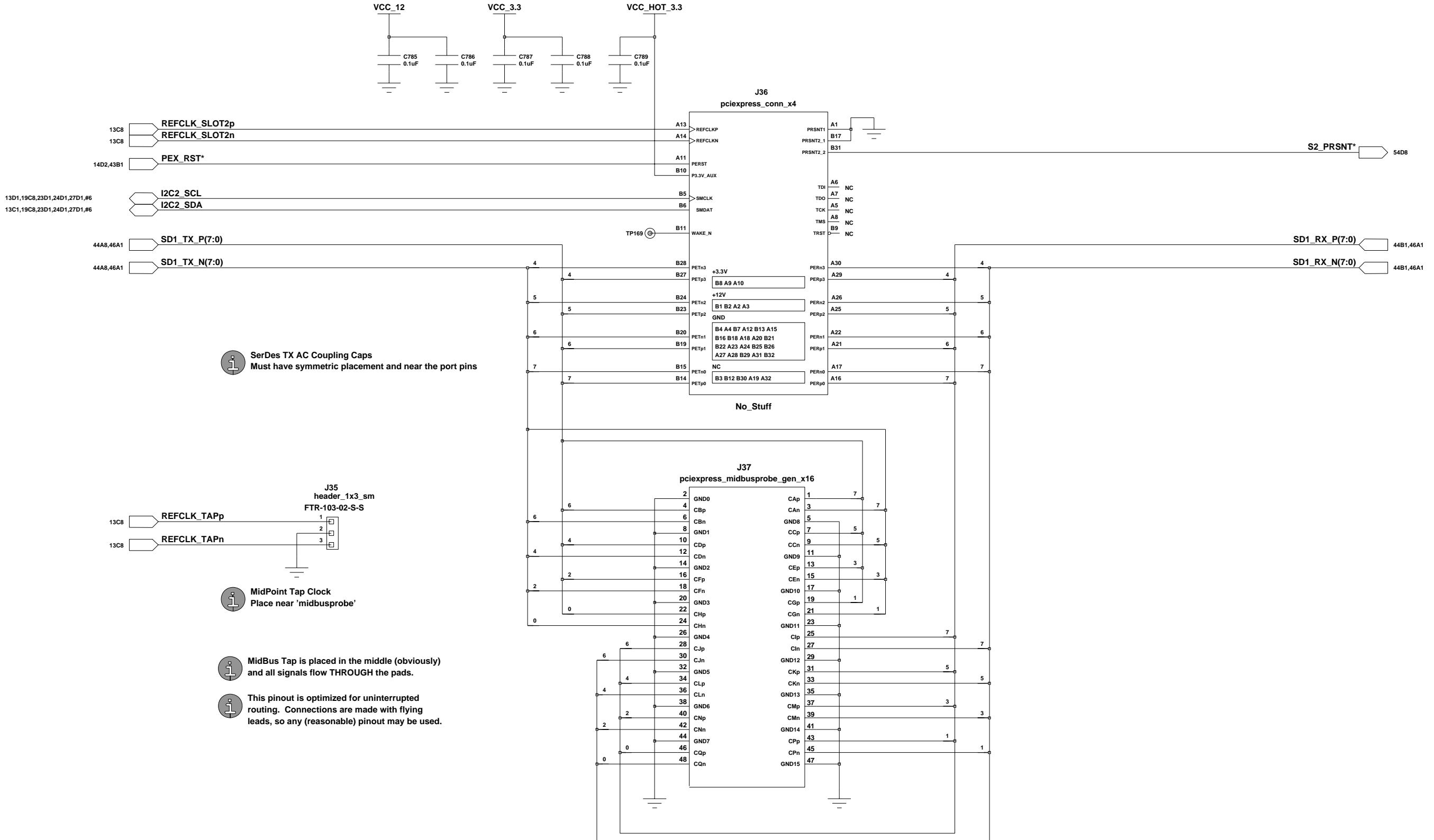
**LANE REVERSAL**

Both RX and TX are reversed
to ease the routing for the
MPC8641D in an ATX chassis.

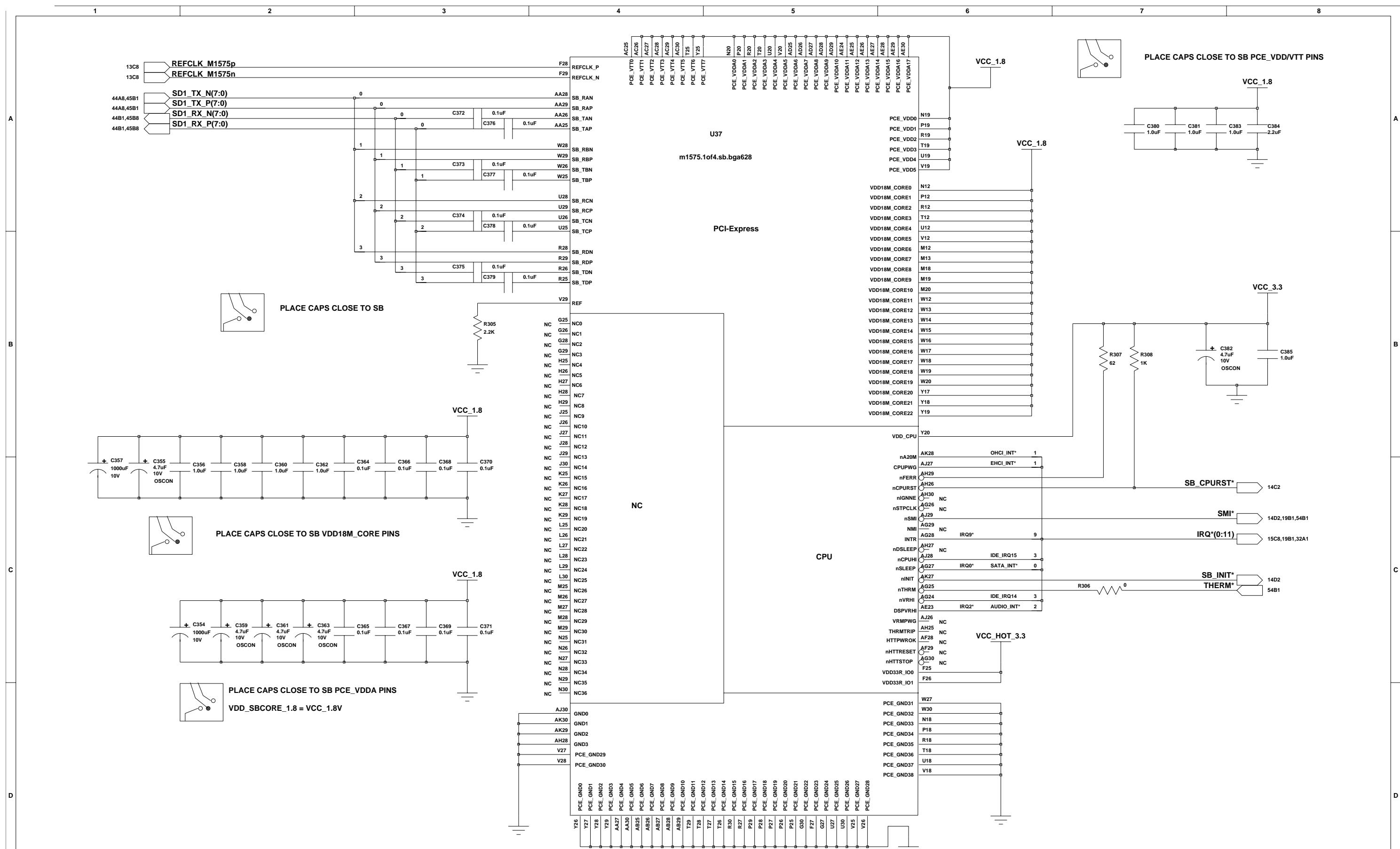
 freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Gary Milliorn	Date Changed: Thursday, February 1, 2007 Time Changed: 2:13:19 pm	Title: PCIExpress 8X Slot 1	Page: 43
1	2	3	4	5	6	7

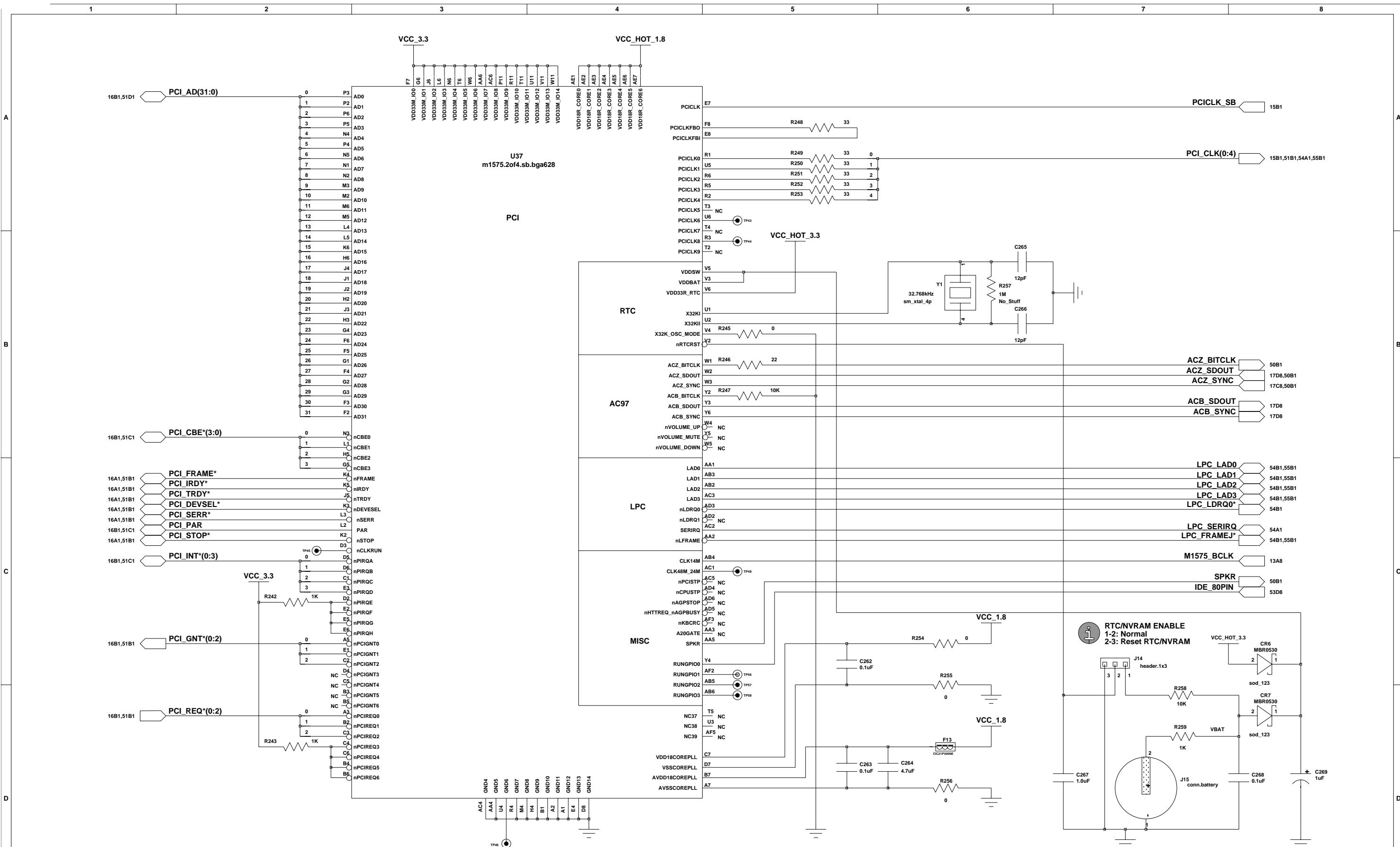


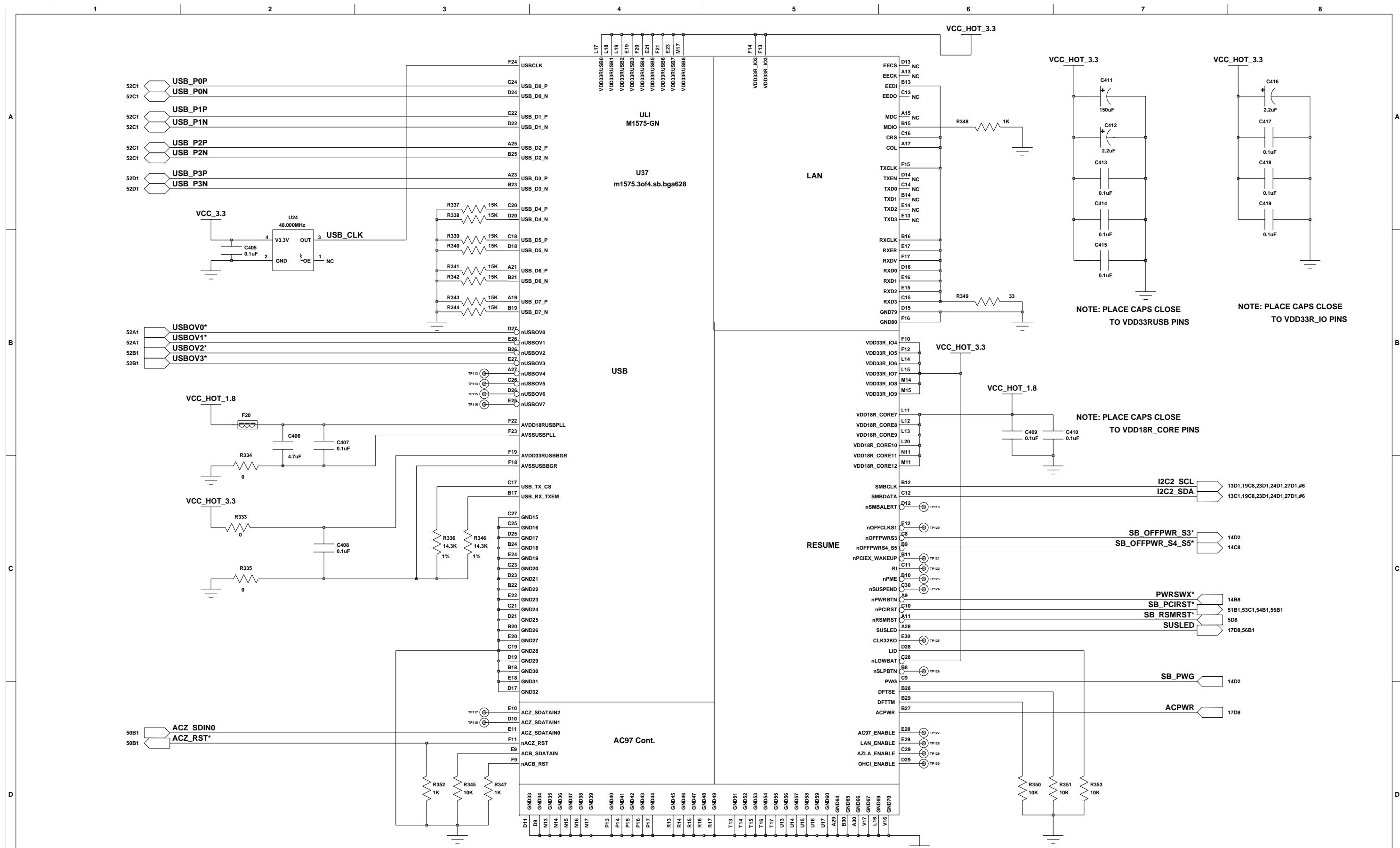
freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Gary Milliorn	Date Changed: Thursday, February 1, 2007 Time Changed: 2:13:27 pm	Title: MC8641D PCIExpress/SERDES/Lynx Port 1	Page: 44
1	2	3	4	5	6	7

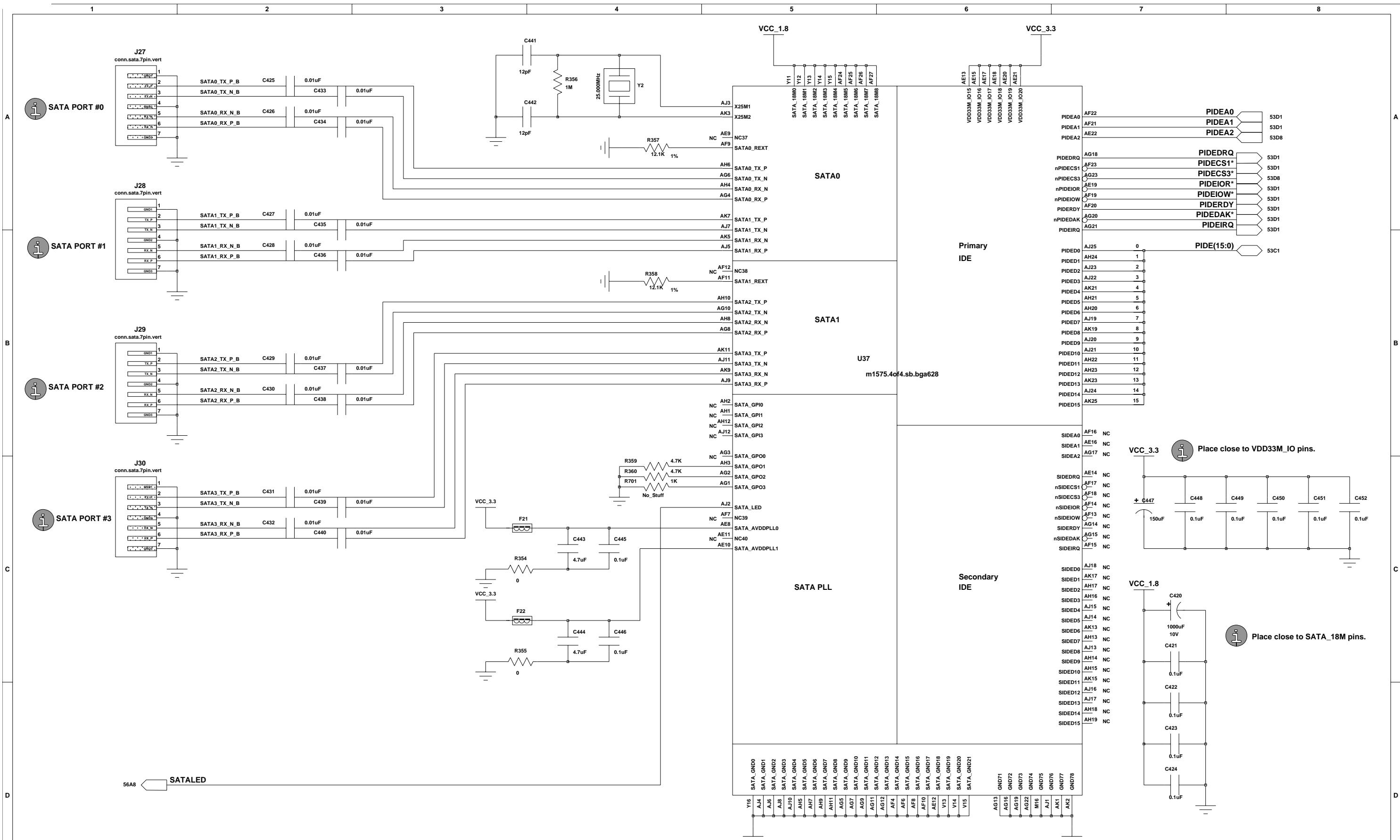


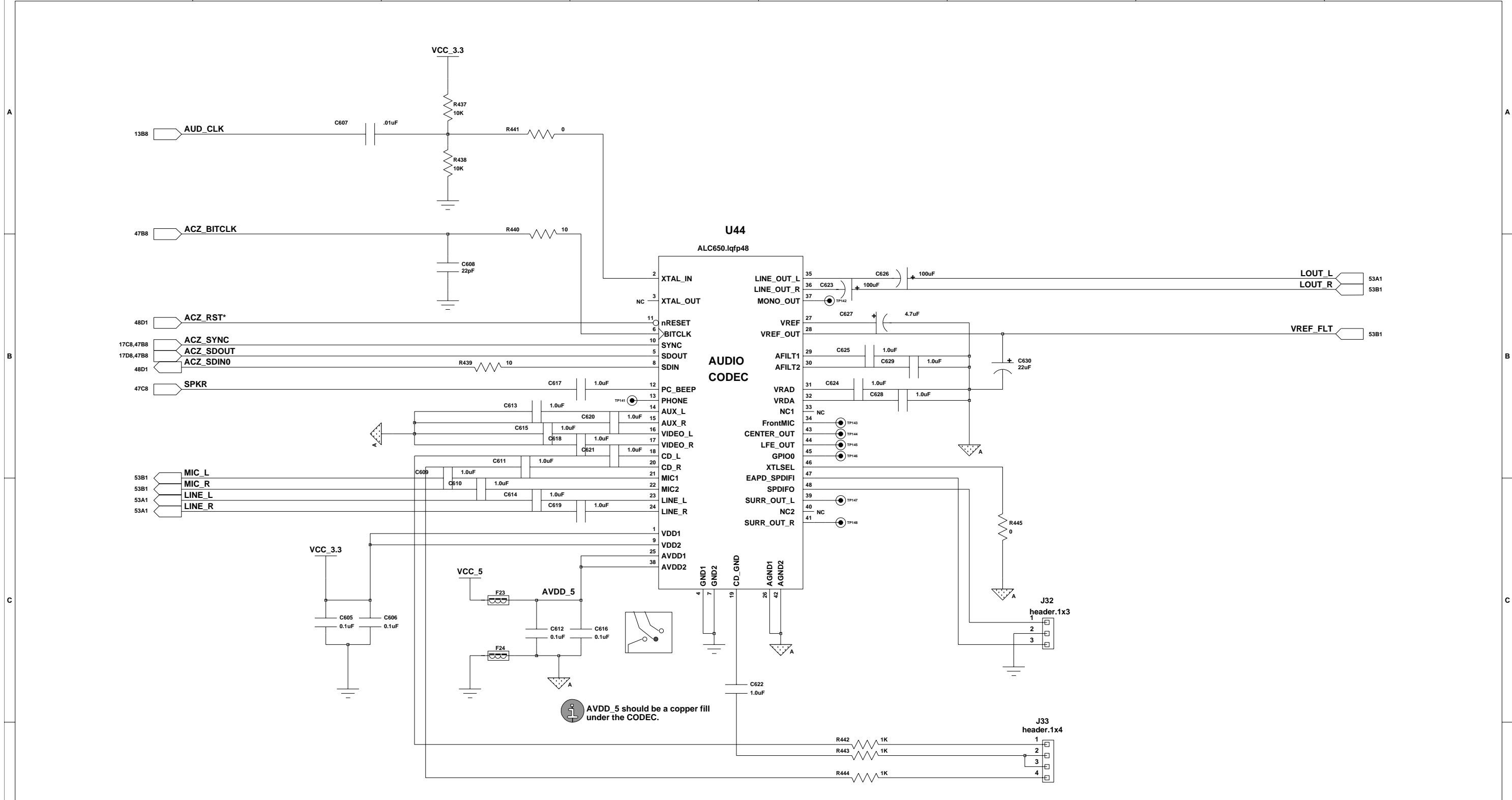
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1	2	3	4	5	6	7

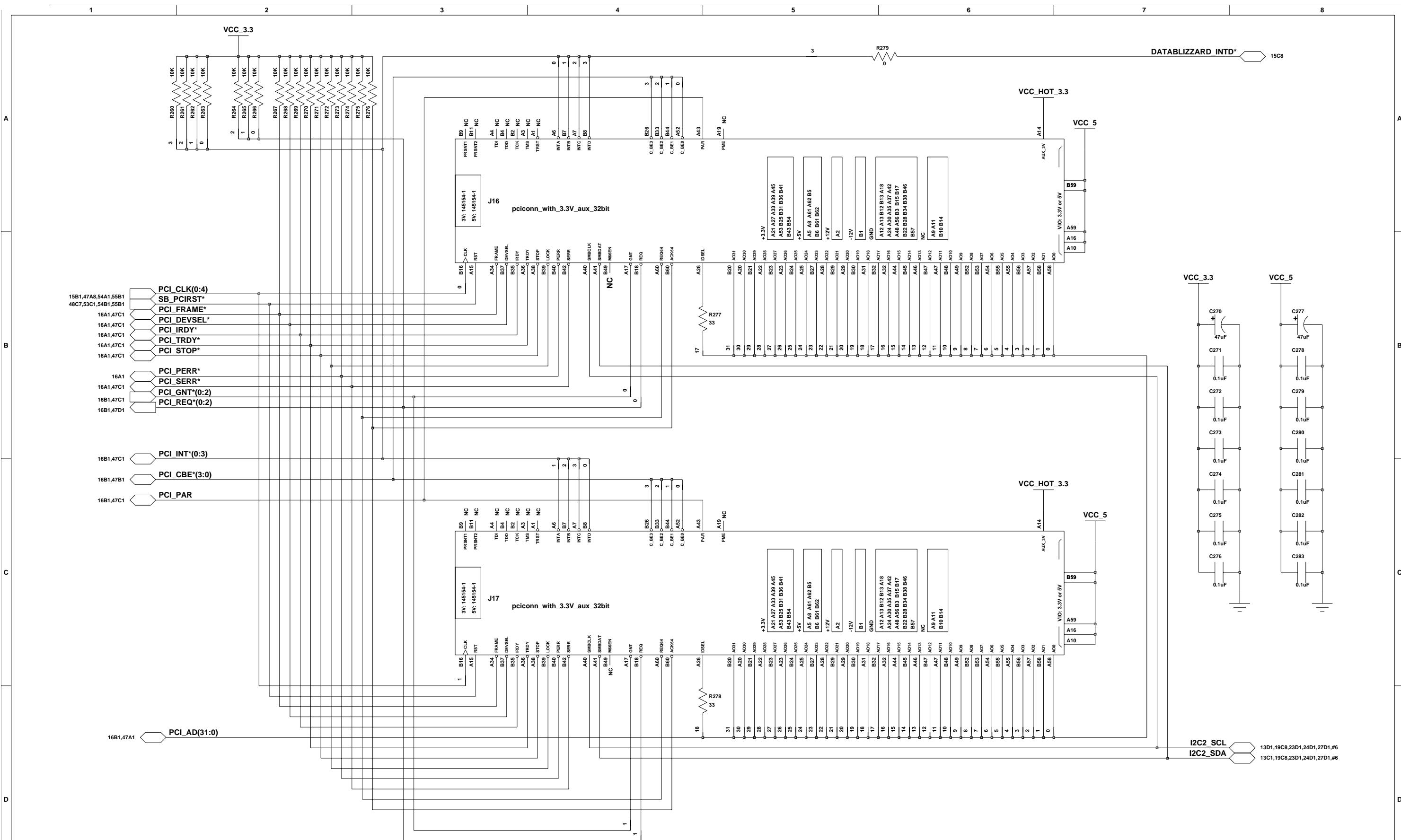


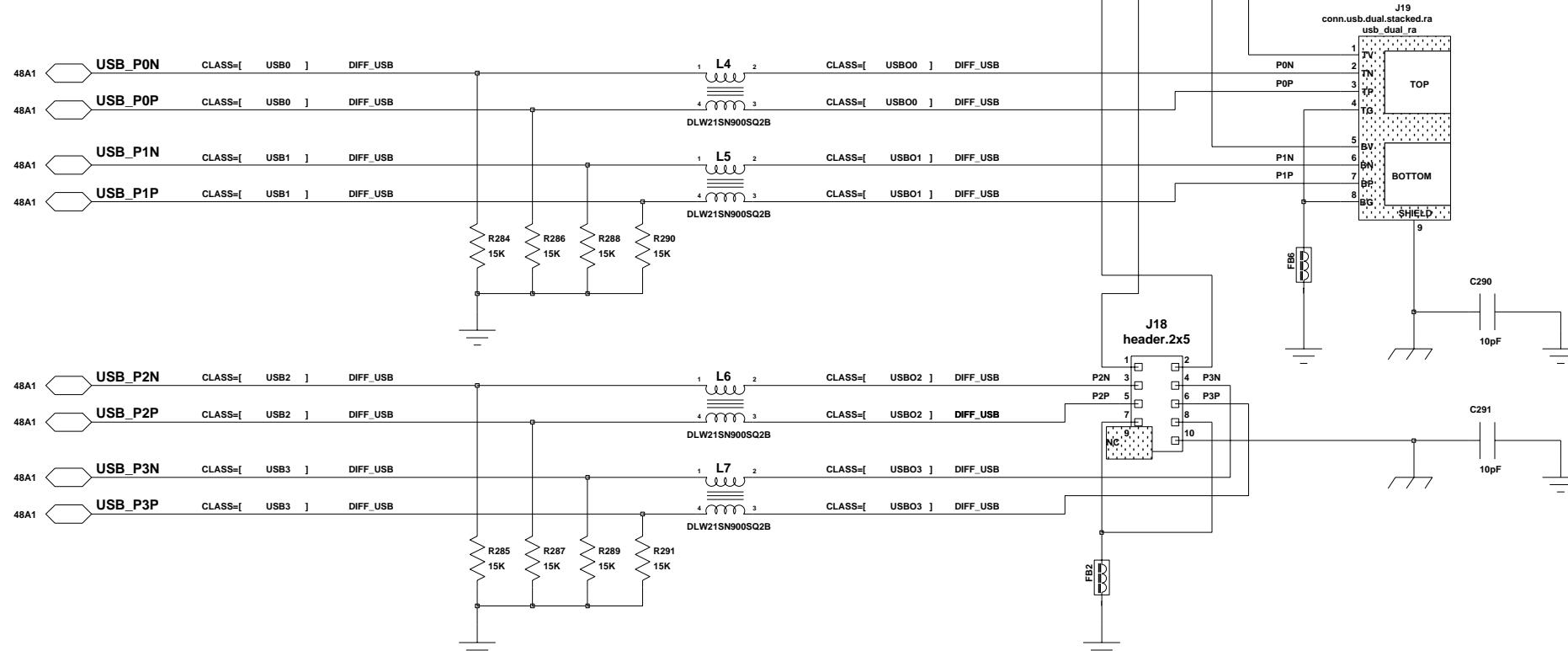
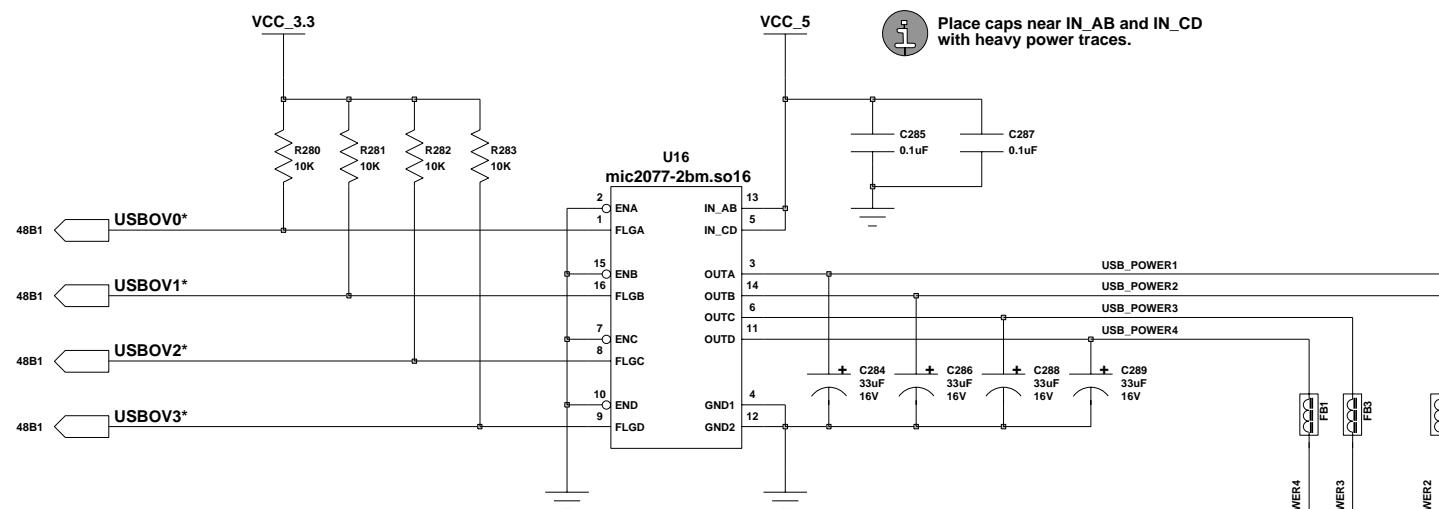




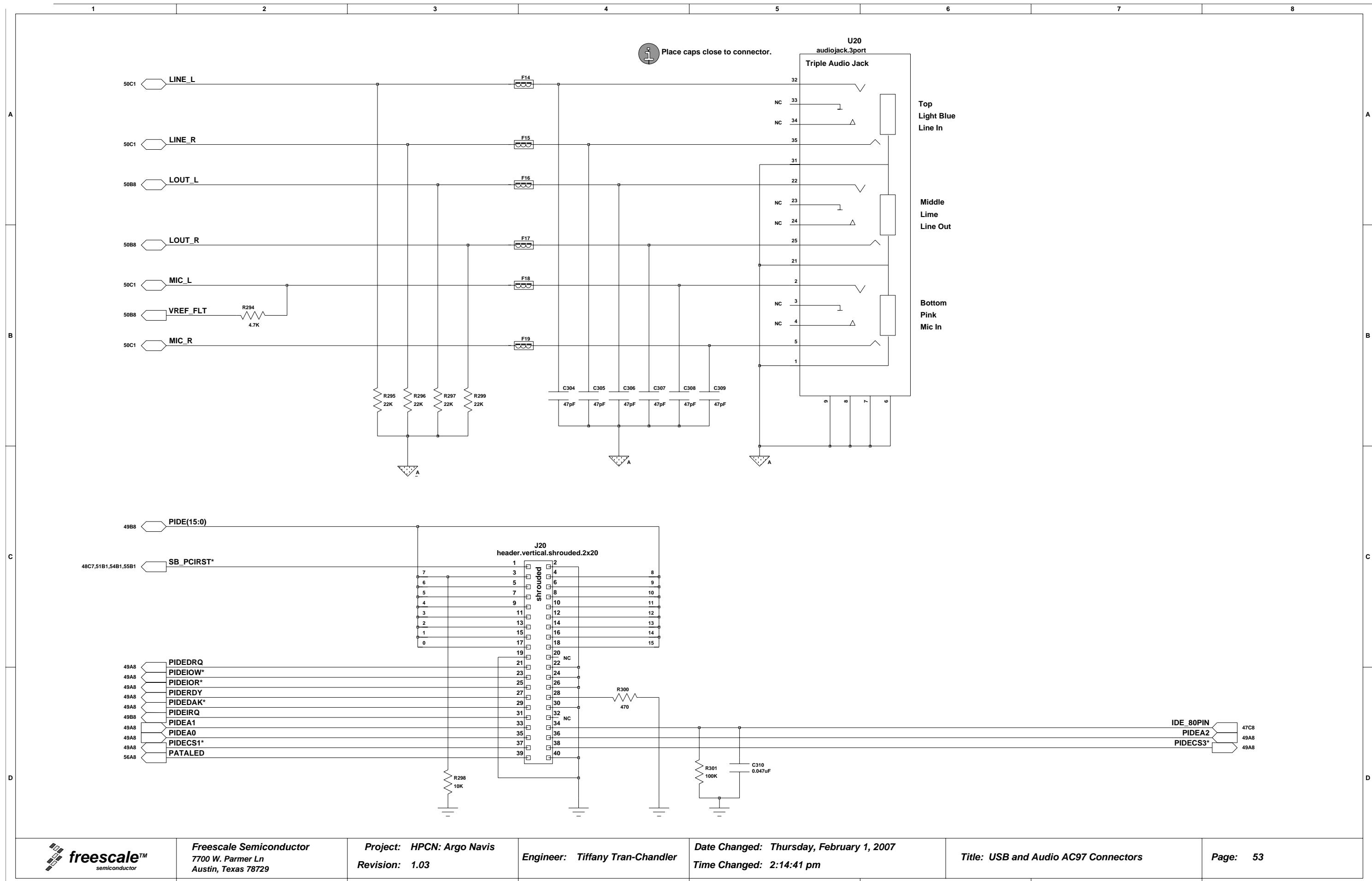


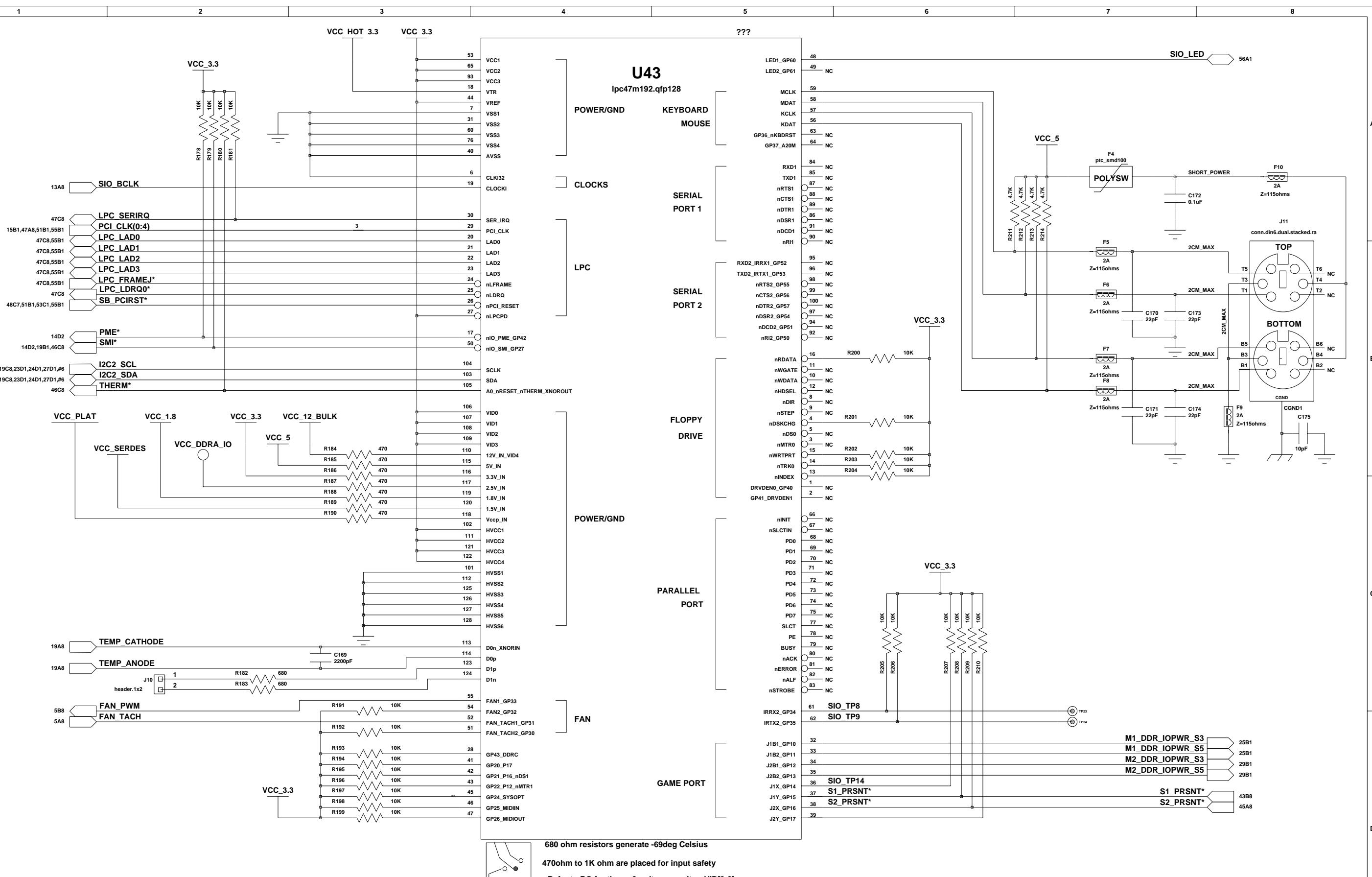






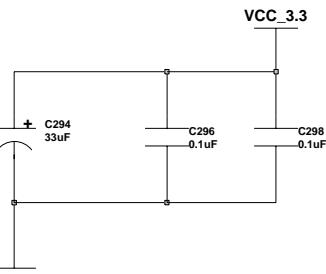
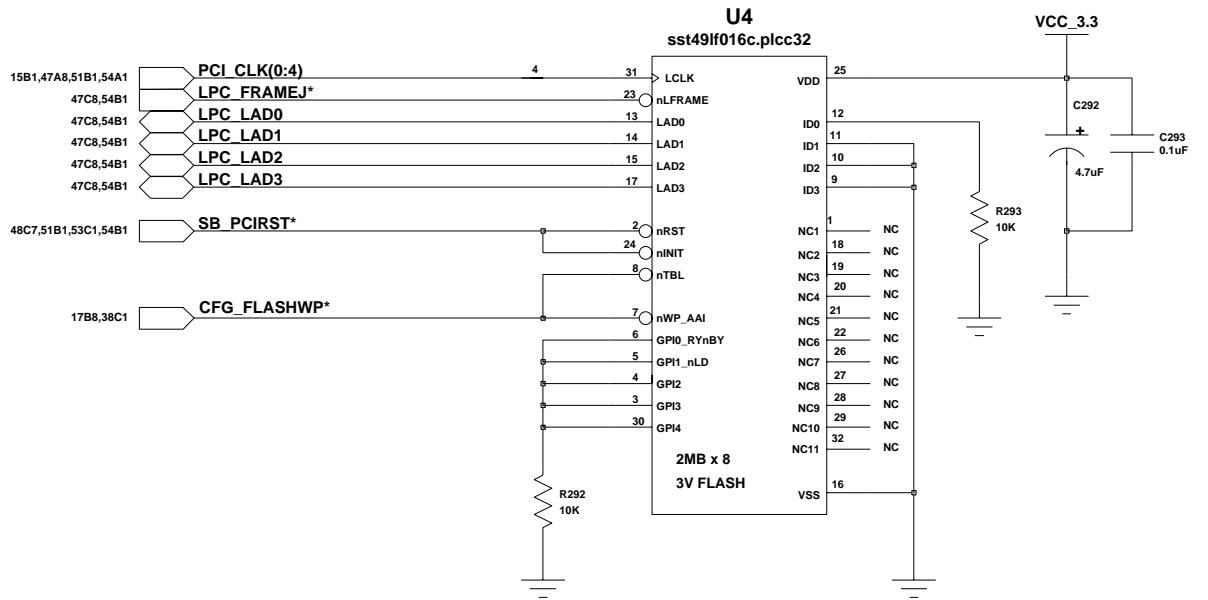
freescale™ semiconductor	Freescale Semiconductor 7700 W. Farmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Tiffany Tran-Chandler	Date Changed: Thursday, February 1, 2007 Time Changed: 2:14:34 pm	Title: USB Ports	Page: 52
1	2	3	4	5	6	7

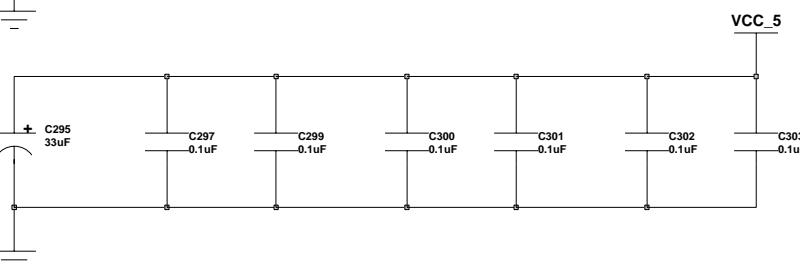




A


**Replace with socket:
21303602**

**Place these caps less than
1cm from VDD.**


Place caps close to SIO.


B

C

D

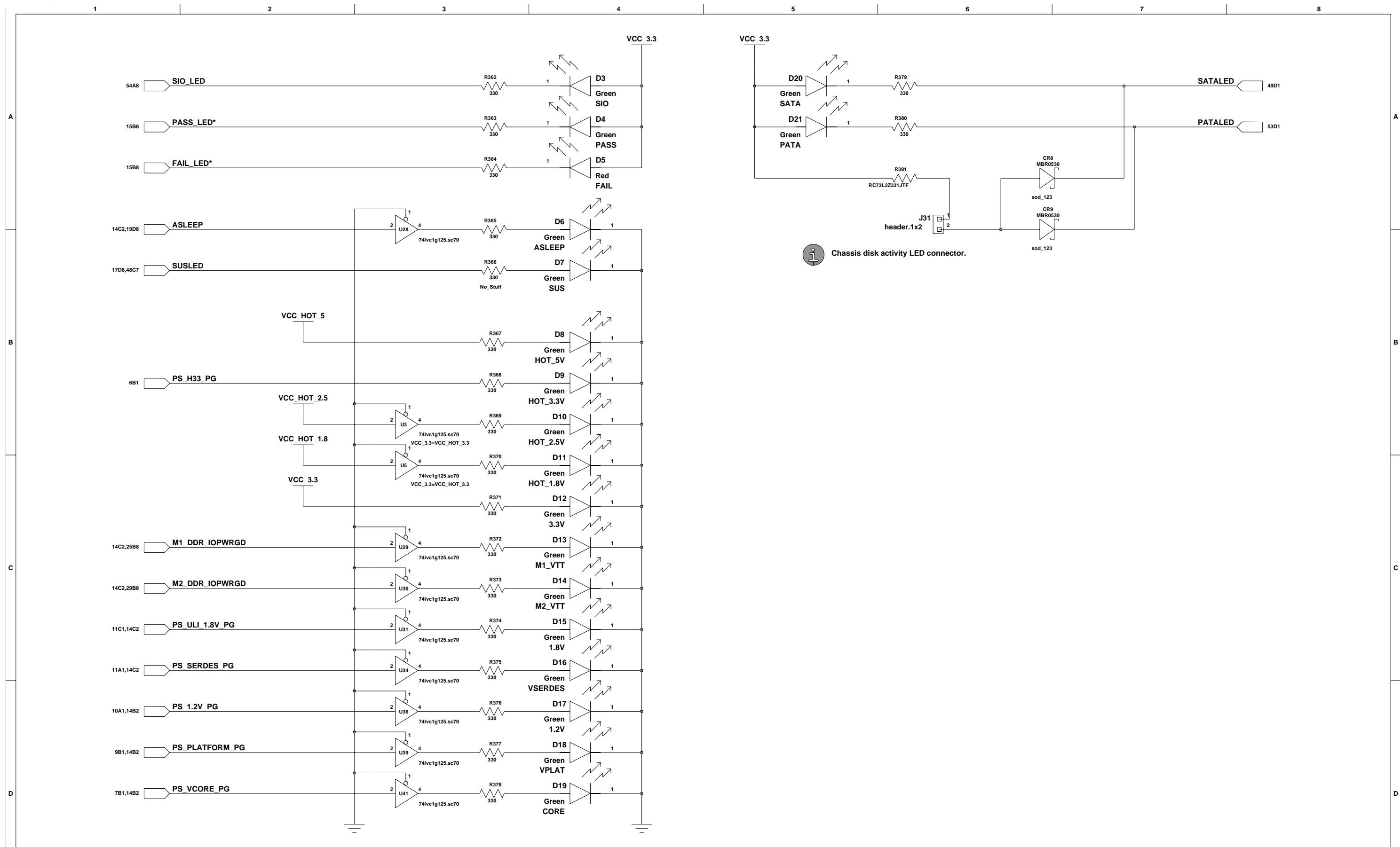
A

B

C

D

 freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: HPCN: Argo Navis Revision: 1.03	Engineer: Tiffany Tran-Chandler	Date Changed: Thursday, February 1, 2007 Time Changed: 2:14:57 pm	Title: LPC Boot Flash / ULI/AC97 Config	Page: 55
1	2	3	4	5	6	7



A

A



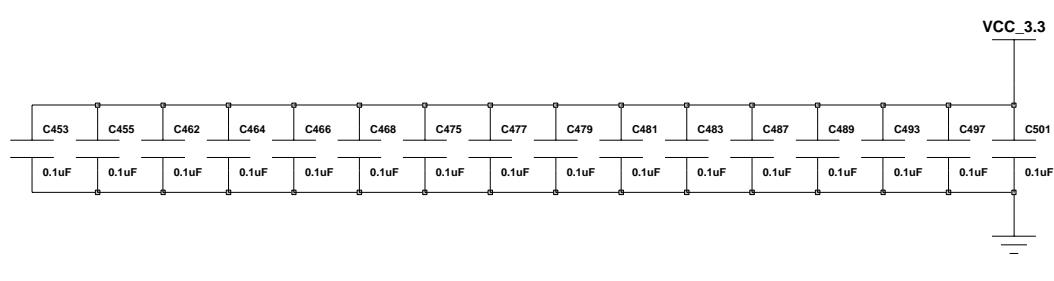
B

B



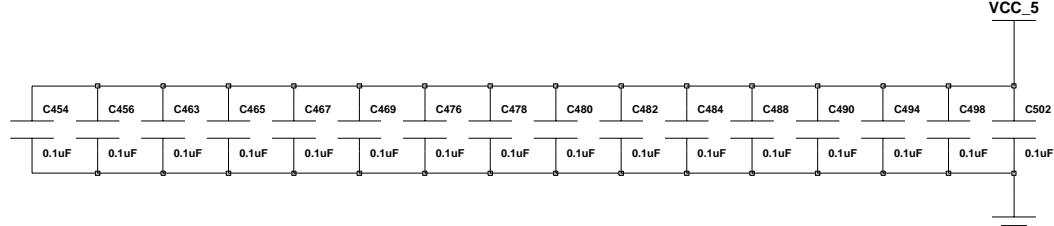
B

B



C

C

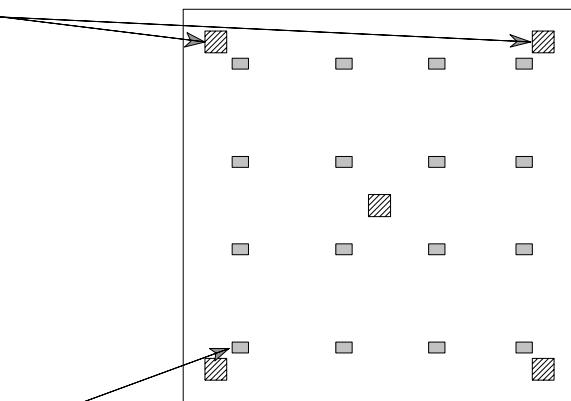


INTER POWER PLANE CAPACITANCE
Place ~2cm from each corner
and one in the center.

C

C

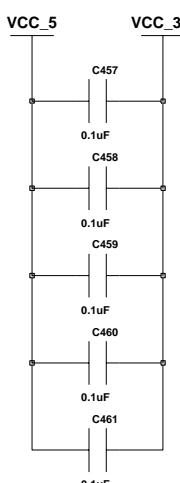
GLOBAL BULK CAPACITANCE
Place ~2cm from each corner
and one in the center.



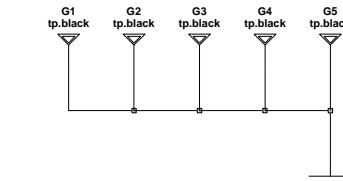
D

D

GLOBAL HF CAPACITANCE
Place in a grid ~5cm everywhere.



GROUND TEST POINTS
Place in each corner and center



CHASSIS MOUNTING HOLES
ATX/Micro-ATX Chassis: 7 holes.

