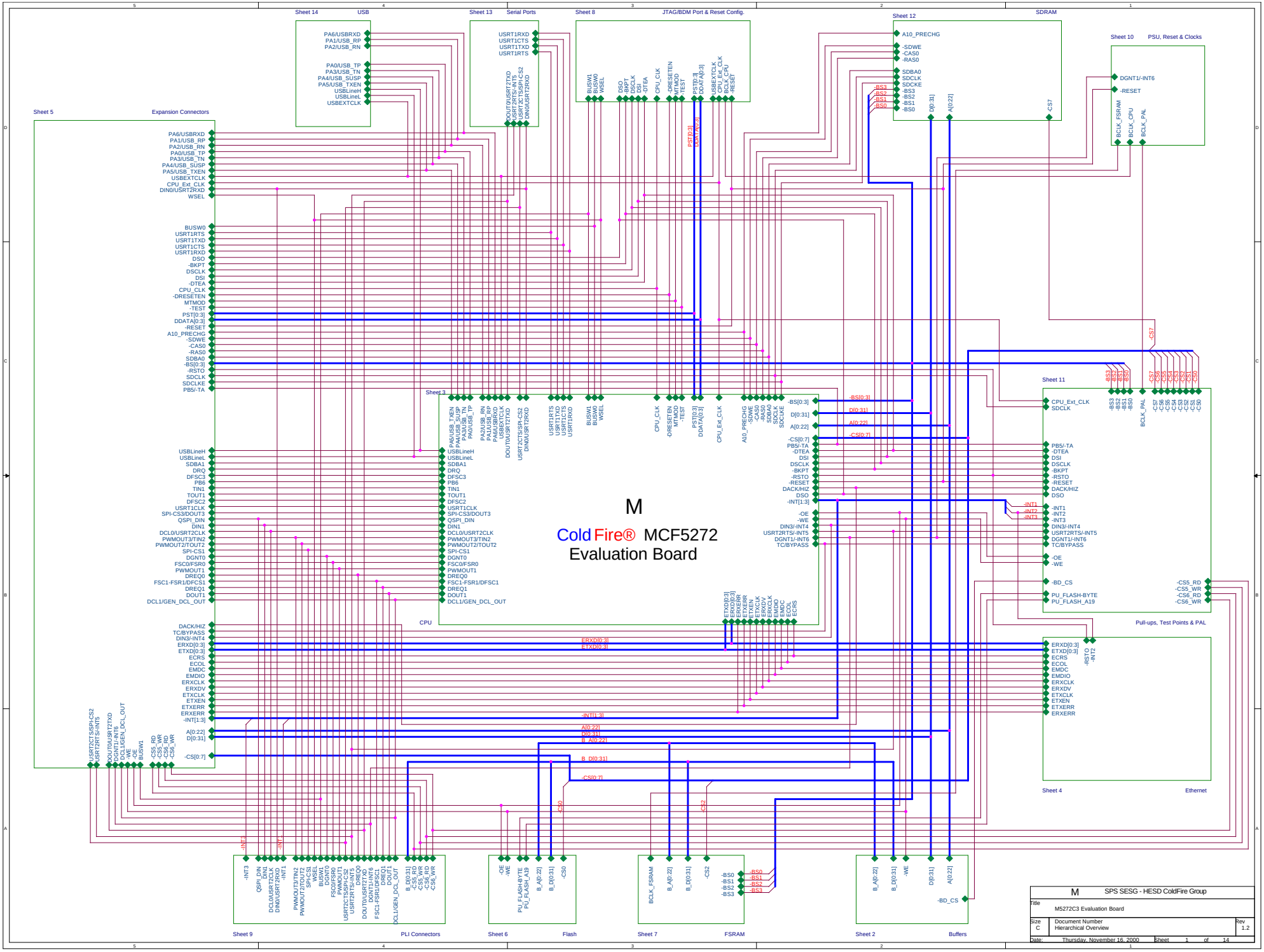
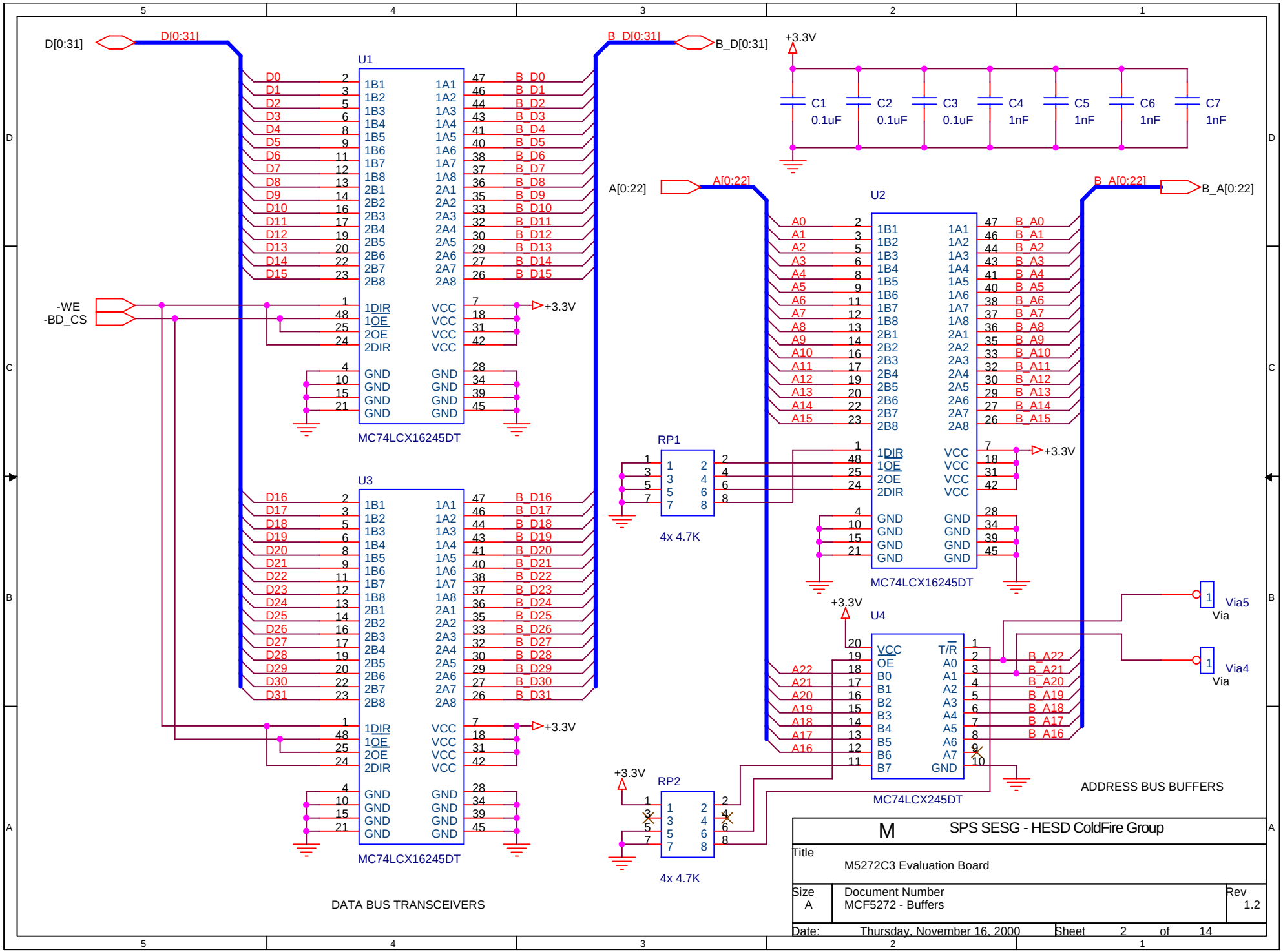
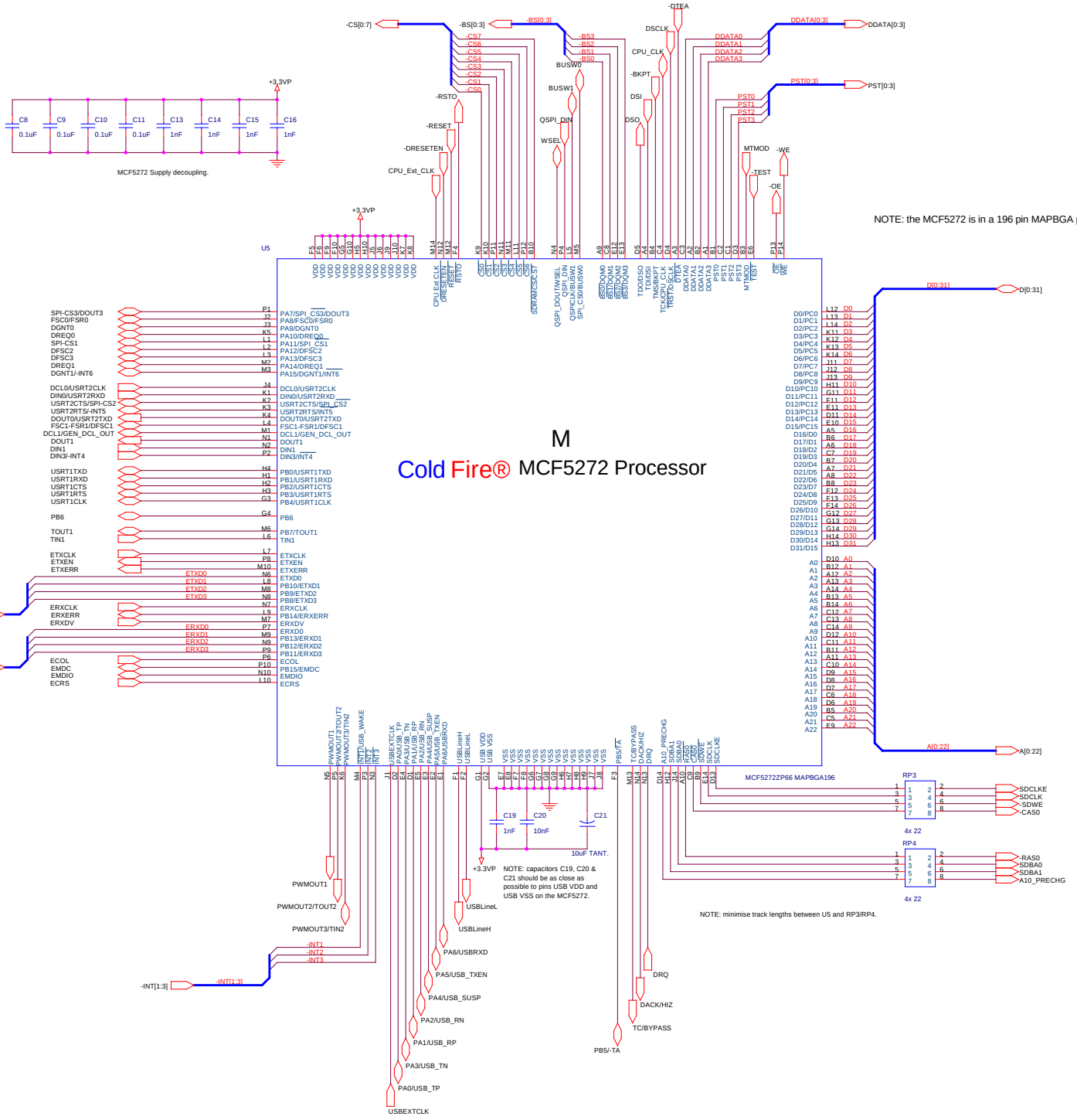
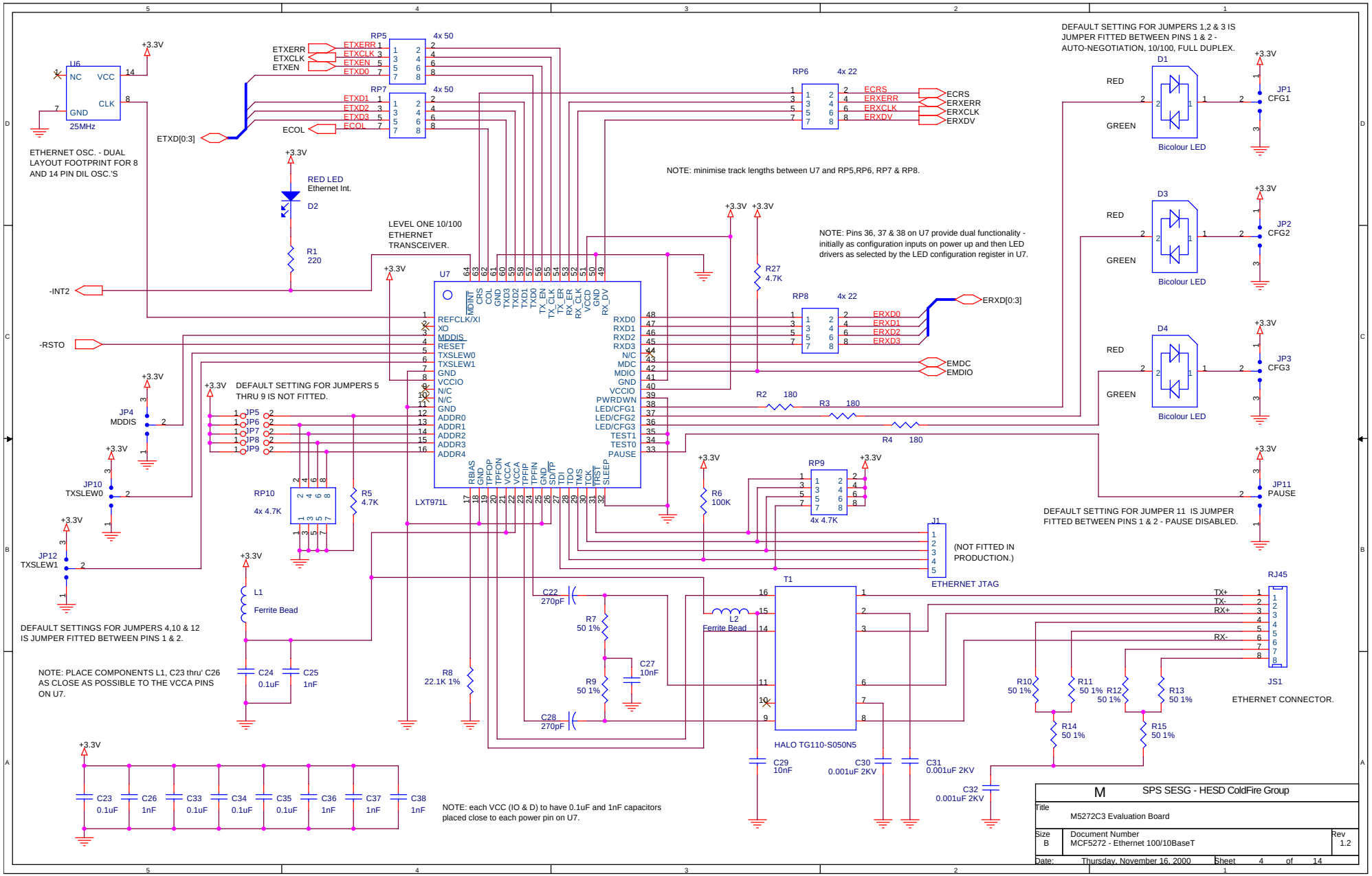

Sheet 14 USB
Sheet 13 Serial Ports
Sheet 8 JTAG/BDM Port & Reset Config.
Sheet 12 SDRAM
Sheet 10 PSU, Reset & Clocks
Sheet 5 Expansion Connectors
Sheet 3
M
ColdFire® MCF5272
Evaluation Board
CPU
Sheet 11
Pull-ups, Test Points & PAL
Sheet 4 Ethernet
Sheet 9 PLI Connectors
Sheet 6 Flash
Sheet 7 FSRAM
Sheet 2 Buffers
M SPS SESG - HESD ColdFire Group
Title M5272C3 Evaluation Board
Size C
Document Number Hierarchical Overview
Rev 1.2
Date: Thursday, November 16, 2000
Sheet 1 of 14


D[0:31]
B_D[0:31]
A[0:22]
B_A[0:22]
-WE
-BD_CS
+3.3V
U1
MC74LCX16245DT
U2
MC74LCX16245DT
U3
MC74LCX16245DT
U4
MC74LCX245DT
RP1
4x 4.7K
RP2
4x 4.7K
C1 0.1uF
C2 0.1uF
C3 0.1uF
C4 1nF
C5 1nF
C6 1nF
C7 1nF
Via5
Via4
DATA BUS TRANSCEIVERS
ADDRESS BUS BUFFERS
M
SPS SESG - HESD ColdFire Group
Title
M5272C3 Evaluation Board
Size A
Document Number
MCF5272 - Buffers
Rev 1.2
Date: Thursday, November 16, 2000
Sheet 2 of 14


MCF5272 Supply decoupling.
NOTE: the MCF5272 is in a 196 pin MAPBGA package.
M
Cold Fire® MCF5272 Processor
MCF5272ZP66 MAPBGA196
NOTE: capacitors C19, C20 & C21 should be as close as possible to pins USB VDD and USB VSS on the MCF5272.
NOTE: minimise track lengths between U5 and RP3/RP4.
M
SPS SESG - HESD ColdFire Group
Title
M5272C3 Evaluation Board
Size C
Document Number MCF5272 - CPU
Rev 1.2
Date: Thursday, November 16, 2000
Sheet 3 of 14


U6
NC
VCC
CLK
GND
25MHz
+3.3V
ETHERNET OSC. - DUAL LAYOUT FOOTPRINT FOR 8 AND 14 PIN DIL OSC.'S
RP5
4x 50
ETXERR
ETXCLK
ETXEN
ETXD0
RP7
ETXD1
ETXD2
ETXD3
ECOL
ETXD[0:3]
RP6
4x 22
ECRS
ERXERR
ERXCLK
ERXDV
NOTE: minimise track lengths between U7 and RP5,RP6, RP7 & RP8.
DEFAULT SETTING FOR JUMPERS 1,2 & 3 IS JUMPER FITTED BETWEEN PINS 1 & 2 - AUTO-NEGOTIATION, 10/100, FULL DUPLEX.
D1
RED
GREEN
Bicolour LED
JP1
CFG1
D3
JP2
CFG2
D4
JP3
CFG3
RED LED
Ethernet Int.
D2
R1
220
-INT2
-RSTO
LEVEL ONE 10/100 ETHERNET TRANSCEIVER.
U7
REFCLK/XI
XO
MDDIS
RESET
TXSLEW0
TXSLEW1
GND
VCCIO
N/C
ADDR0
ADDR1
ADDR2
ADDR3
ADDR4
RXD0
RXD1
RXD2
RXD3
MDC
MDIO
PWRDWN
LED/CFG1
LED/CFG2
LED/CFG3
TEST1
TEST0
PAUSE
LXT971L
NOTE: Pins 36, 37 & 38 on U7 provide dual functionality - initially as configuration inputs on power up and then LED drivers as selected by the LED configuration register in U7.
R27
4.7K
RP8
4x 22
ERXD0
ERXD1
ERXD2
ERXD3
ERXD[0:3]
EMDC
EMDIO
R2
180
R3
180
R4
180
JP4
MDDIS
DEFAULT SETTING FOR JUMPERS 5 THRU 9 IS NOT FITTED.
JP5
JP6
JP7
JP8
JP9
JP10
TXSLEW0
JP12
TXSLEW1
RP10
4x 4.7K
R5
4.7K
R6
100K
RP9
4x 4.7K
J1
(NOT FITTED IN PRODUCTION.)
ETHERNET JTAG
JP11
PAUSE
DEFAULT SETTING FOR JUMPER 11 IS JUMPER FITTED BETWEEN PINS 1 & 2 - PAUSE DISABLED.
L1
Ferrite Bead
DEFAULT SETTINGS FOR JUMPERS 4,10 & 12 IS JUMPER FITTED BETWEEN PINS 1 & 2.
NOTE: PLACE COMPONENTS L1, C23 thru' C26 AS CLOSE AS POSSIBLE TO THE VCCA PINS ON U7.
C24
0.1uF
C25
1nF
R8
22.1K 1%
C22
270pF
R7
50 1%
R9
50 1%
C27
10nF
C28
270pF
L2
Ferrite Bead
T1
HALO TG110-S050N5
C29
10nF
C30
0.001uF 2KV
C31
0.001uF 2KV
C32
0.001uF 2KV
RJ45
TX+
TX-
RX+
RX-
JS1
ETHERNET CONNECTOR.
R10
50 1%
R11
50 1%
R12
50 1%
R13
50 1%
R14
50 1%
R15
50 1%
C23
0.1uF
C26
1nF
C33
0.1uF
C34
0.1uF
C35
0.1uF
C36
1nF
C37
1nF
C38
1nF
NOTE: each VCC (IO & D) to have 0.1uF and 1nF capacitors placed close to each power pin on U7.
M
SPS SESG - HESD ColdFire Group
Title
M5272C3 Evaluation Board
Size
B
Document Number
MCF5272 - Ethernet 100/10BaseT
Rev
1.2
Date:
Thursday, November 16, 2000
Sheet
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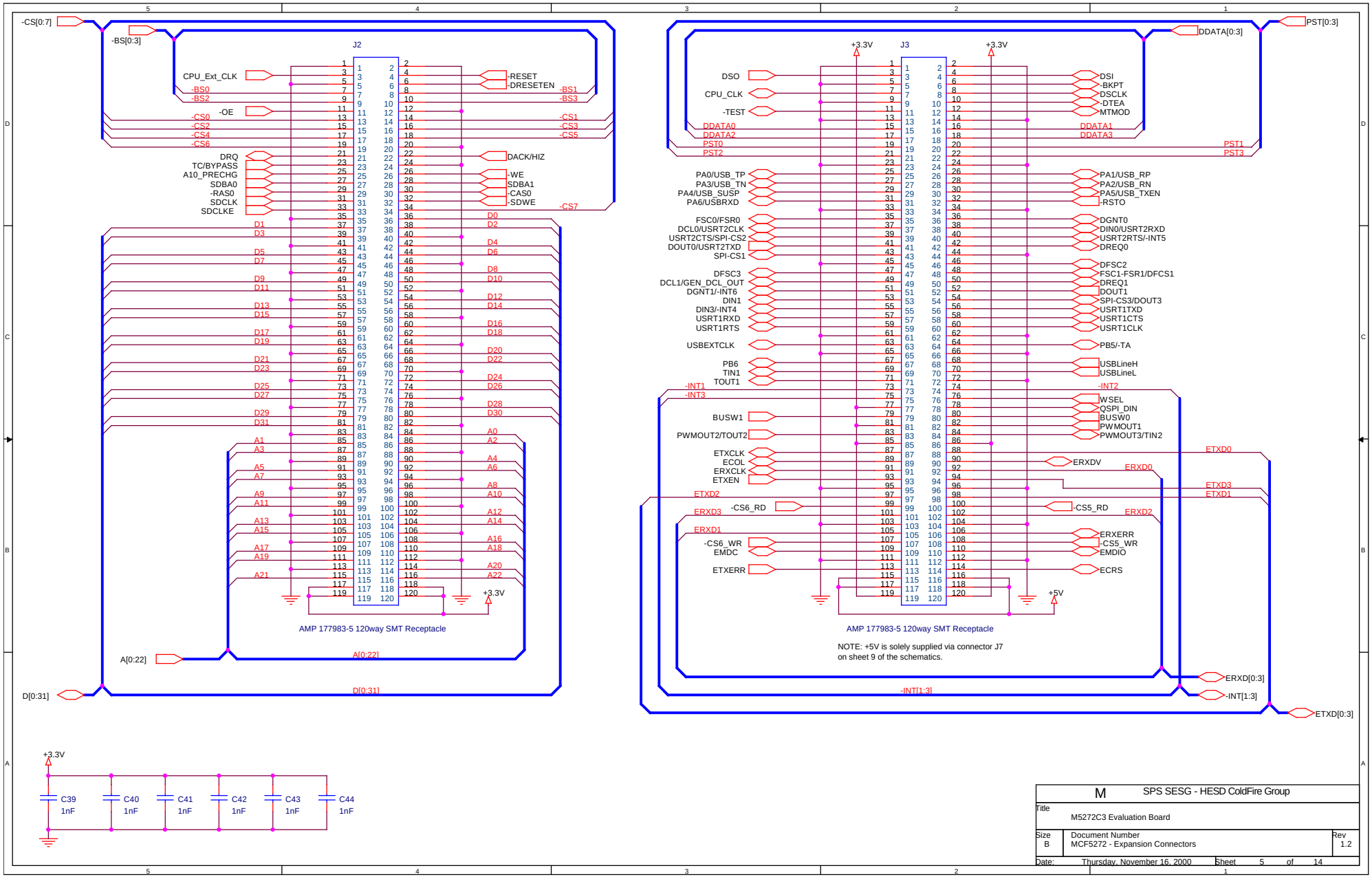
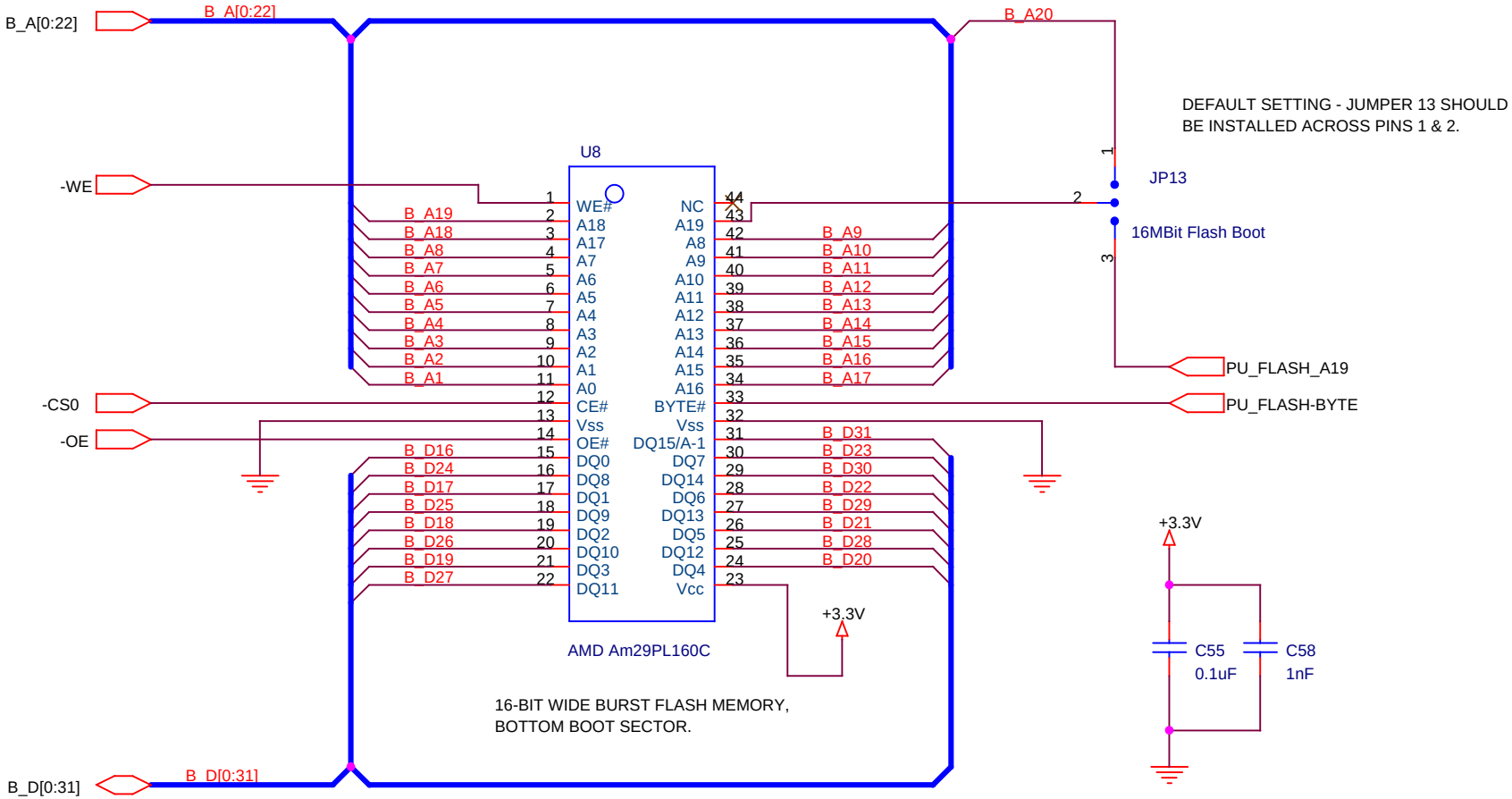
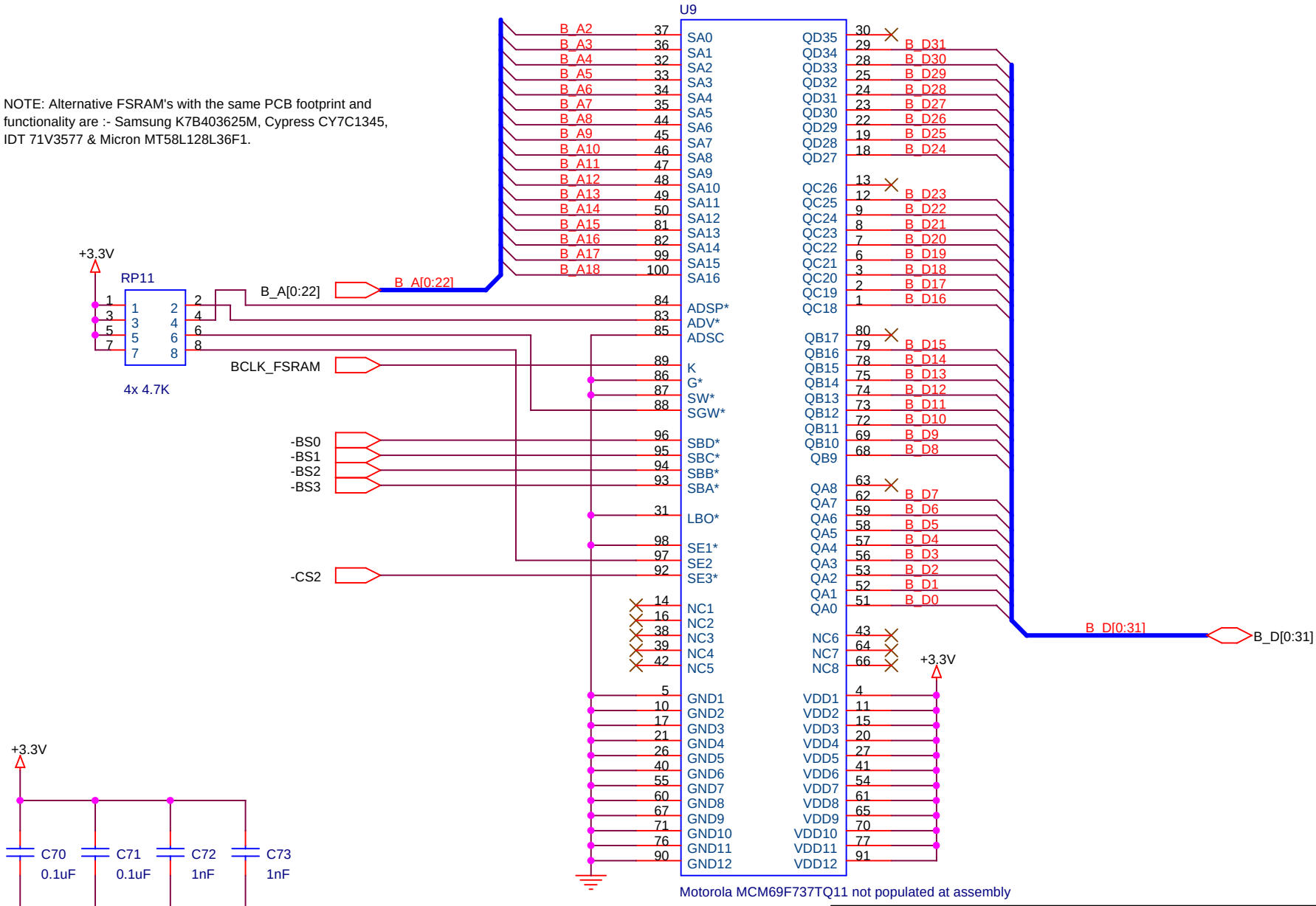
of
14



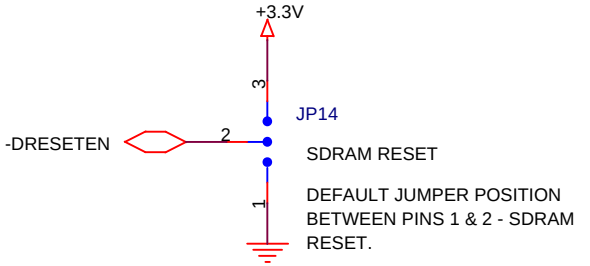
M	SPS SESG - HESD ColdFire Group	
Title	M5272C3 Evaluation Board	
Size B	Document Number MCF5272 - Expansion Connectors	Rev 1.2
Date: Thursday, November 16, 2000	Sheet 5 of 14	

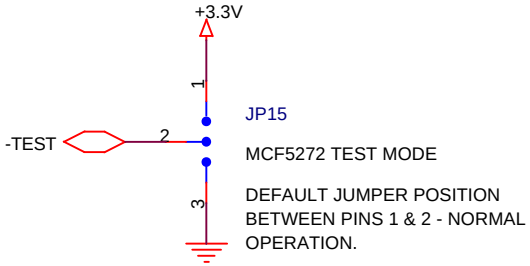


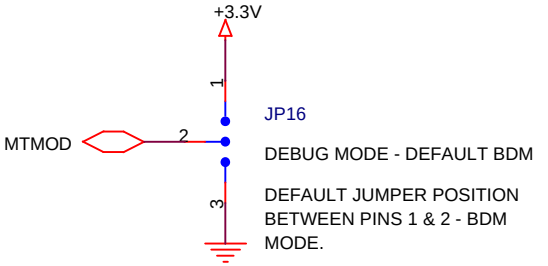
M	SPS SESG - HESD ColdFire Group	
Title	M5272C3 Evaluation Board	
Size A	Document Number MCF5272 - Flash Memory	Rev 1.2
Date: Thursday, November 16, 2000	Sheet 6 of 14	

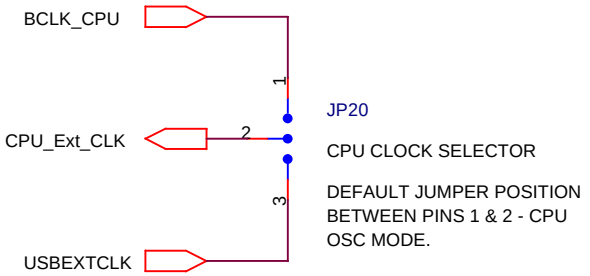


M	SPS SESG - HESD ColdFire Group	
Title	M5272C3 Evalution Board	
Size A	Document Number MCF5272 - FSRAM	Rev 1.2
Date: Thursday, November 16, 2000	Sheet 7 of 14	

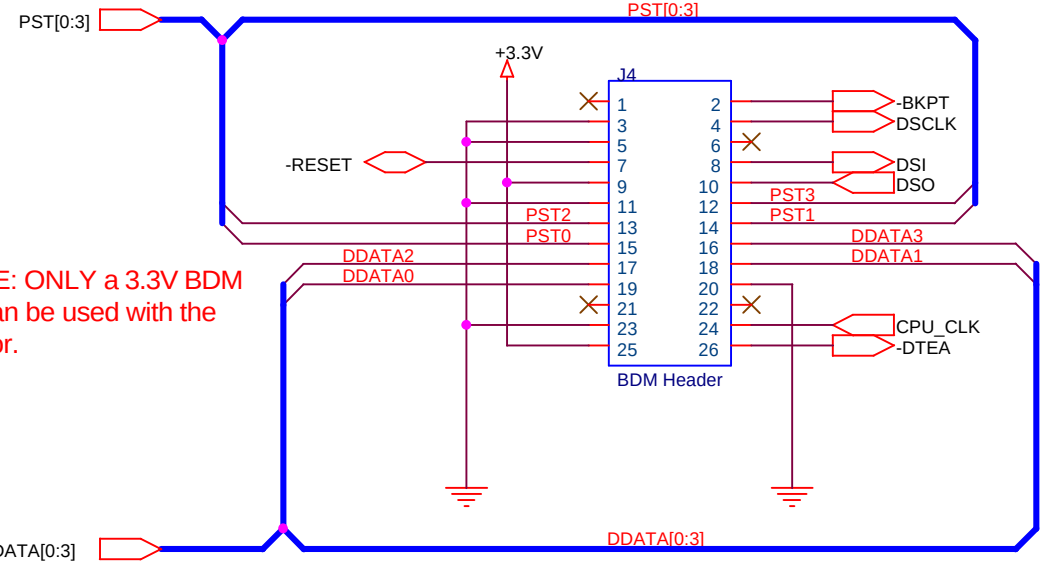








IMPORTANT NOTE: ONLY a 3.3V BDM debugging cable can be used with the MCF5272 processor.

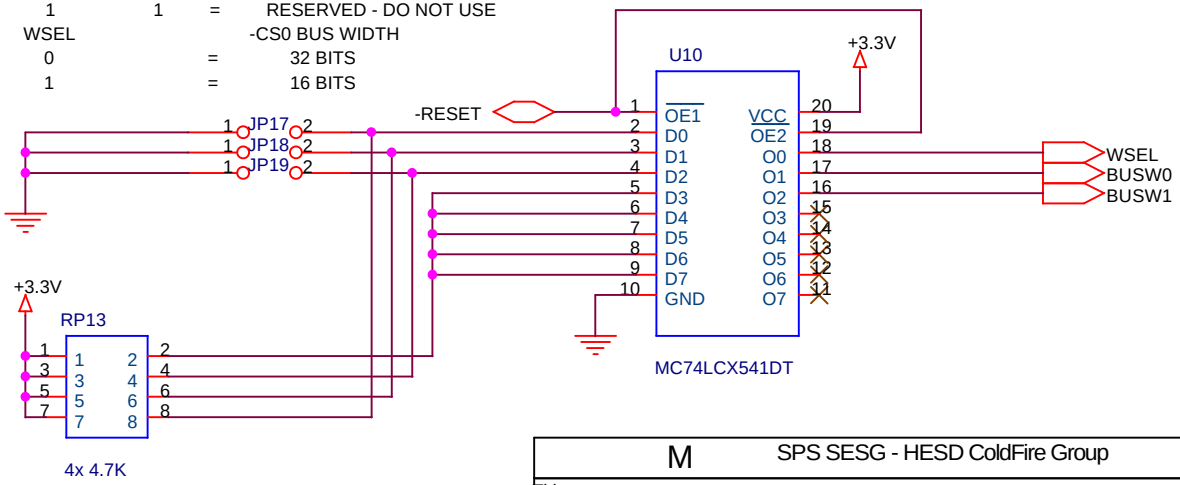


NOTE: 4.7K pull up resistors are used on signals -BKPT, DSCLK, DSI, DSO, -RESET & -DTEA. See page 11 of the schematics.

DEFAULT FOR JP17/WSEL IS FITTED (0).
DEFAULT FOR JP18/BUSW0 IS FITTED (0).
DEFAULT FOR JP19/BUSW1 IS NOT FITTED (1).

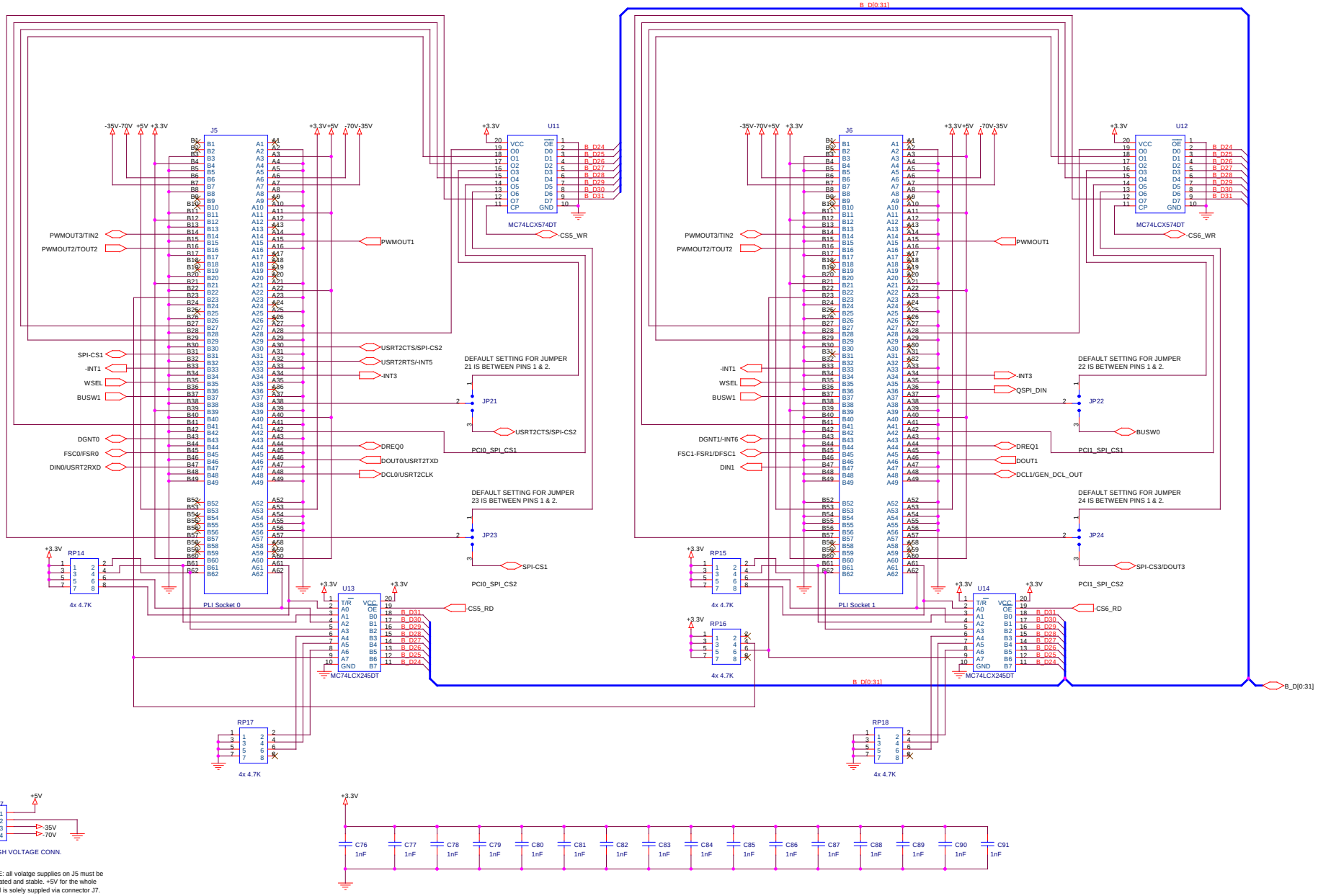
BUSW1	BUSW0		DATA BUS WIDTH
0	0	=	32 BITS
0	1	=	8 BITS
1	0	=	16 BITS
1	1	=	RESERVED - DO NOT USE

WSEL		-CS0 BUS WIDTH
0	=	32 BITS
1	=	16 BITS

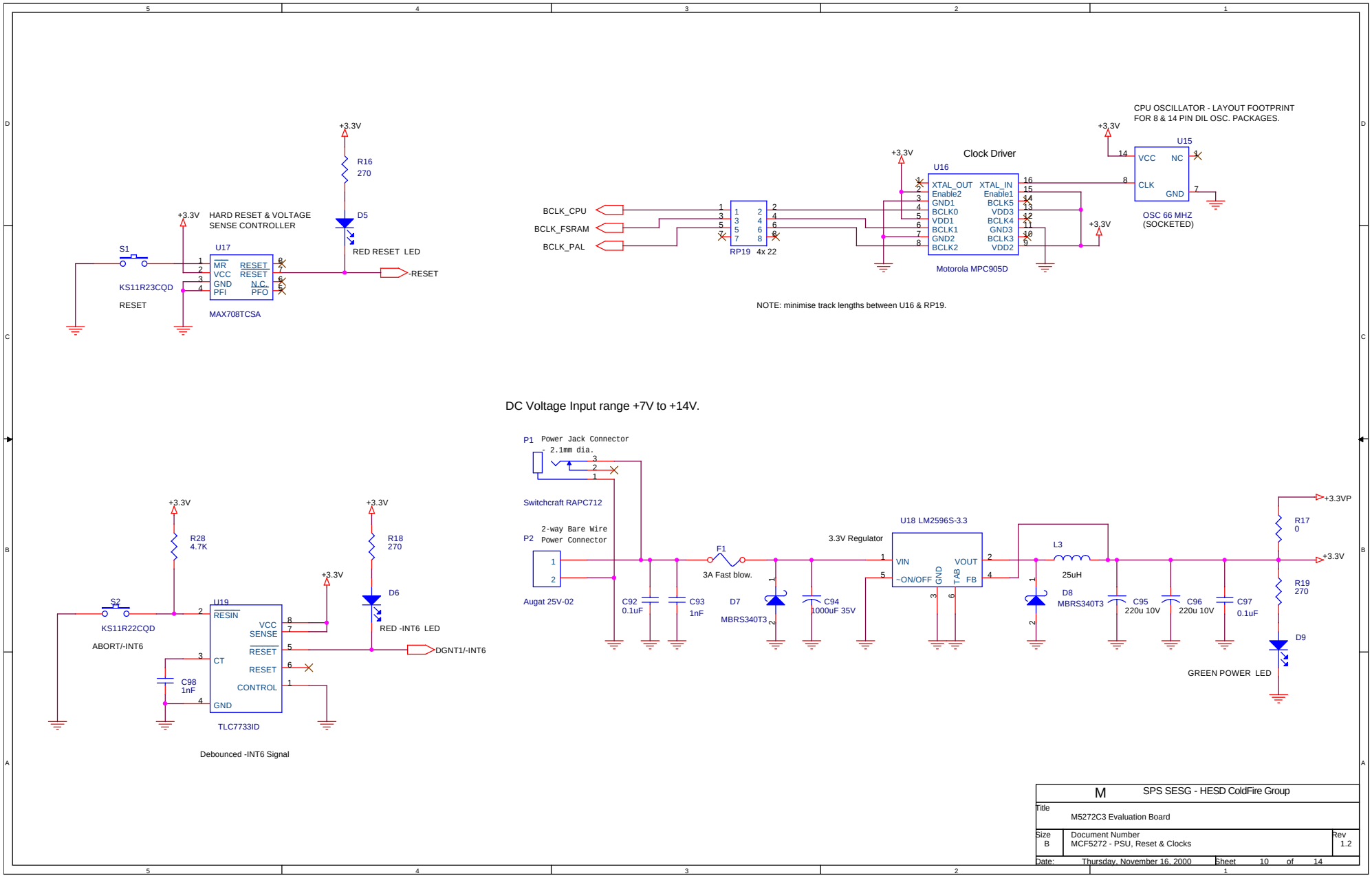


M	SPS SESG - HESD ColdFire Group	
Title	M5272C3 Evaluation Board	
Size A	Document Number MCF5272 Background Debug Mode (BDM) Port & Reset Config.	Rev 1.2
Date: Thursday, November 16, 2000	Sheet 8 of 14	

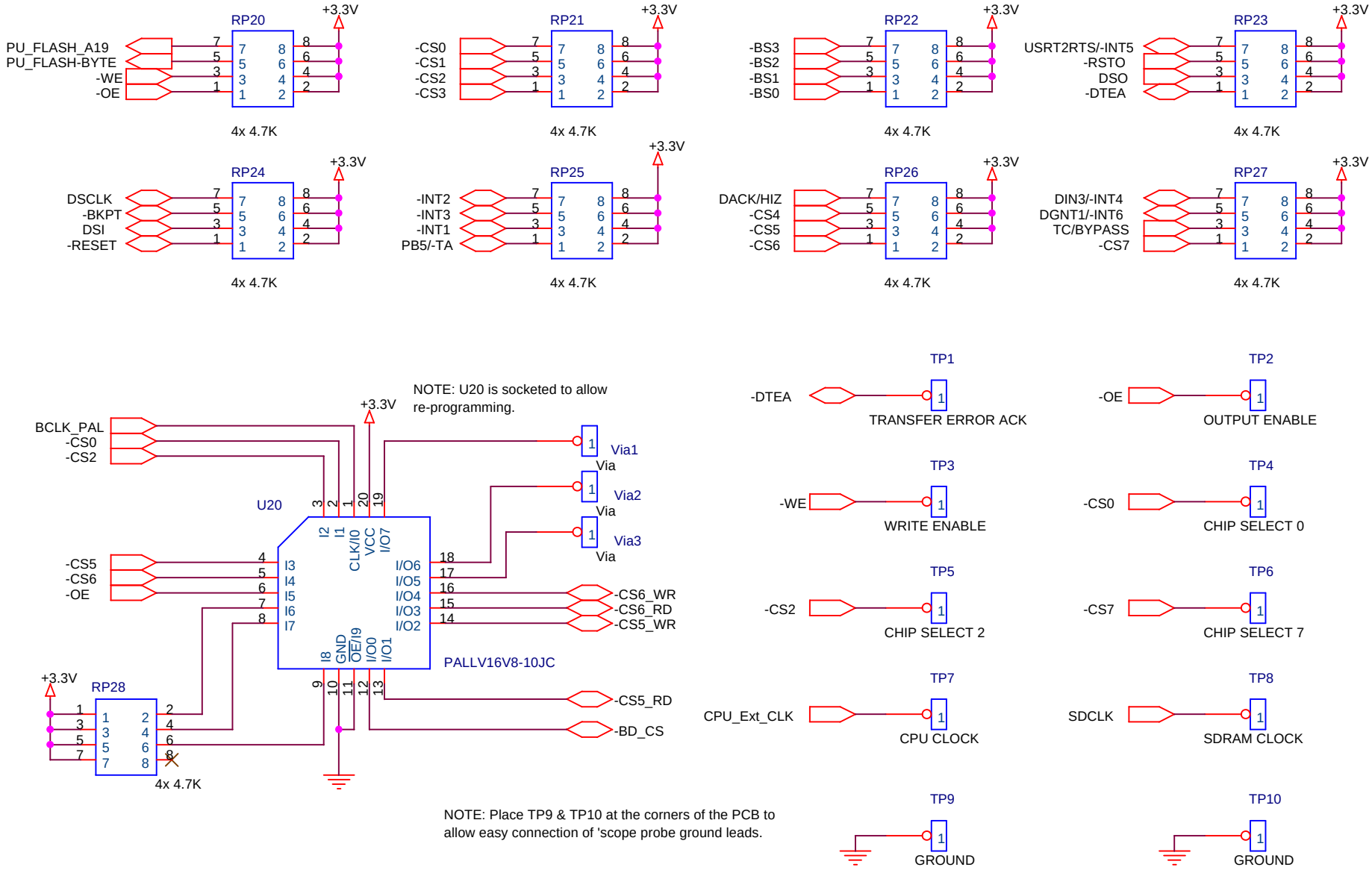
NOTE: PLI Sockets 0 & 1 are not populated during assembly.



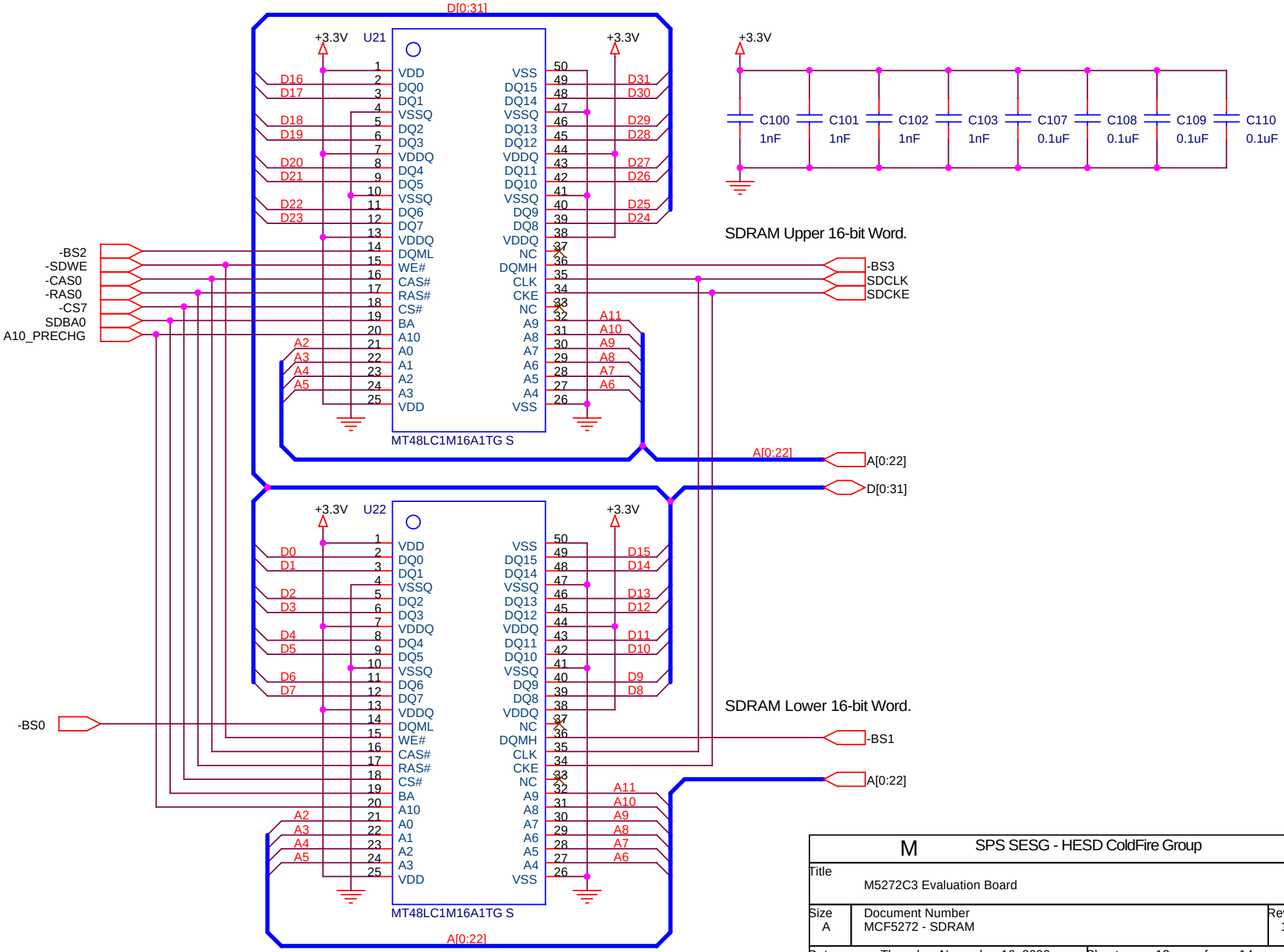
M	SPS SESG - HESD ColdFire Group	
Title	M5272C3 Evaluation Board	
Size C	Document Number MCF5272 - PLI Connectors	Rev 1.2
Date: Thursday, November 16, 2000	Sheet 9 of 14	

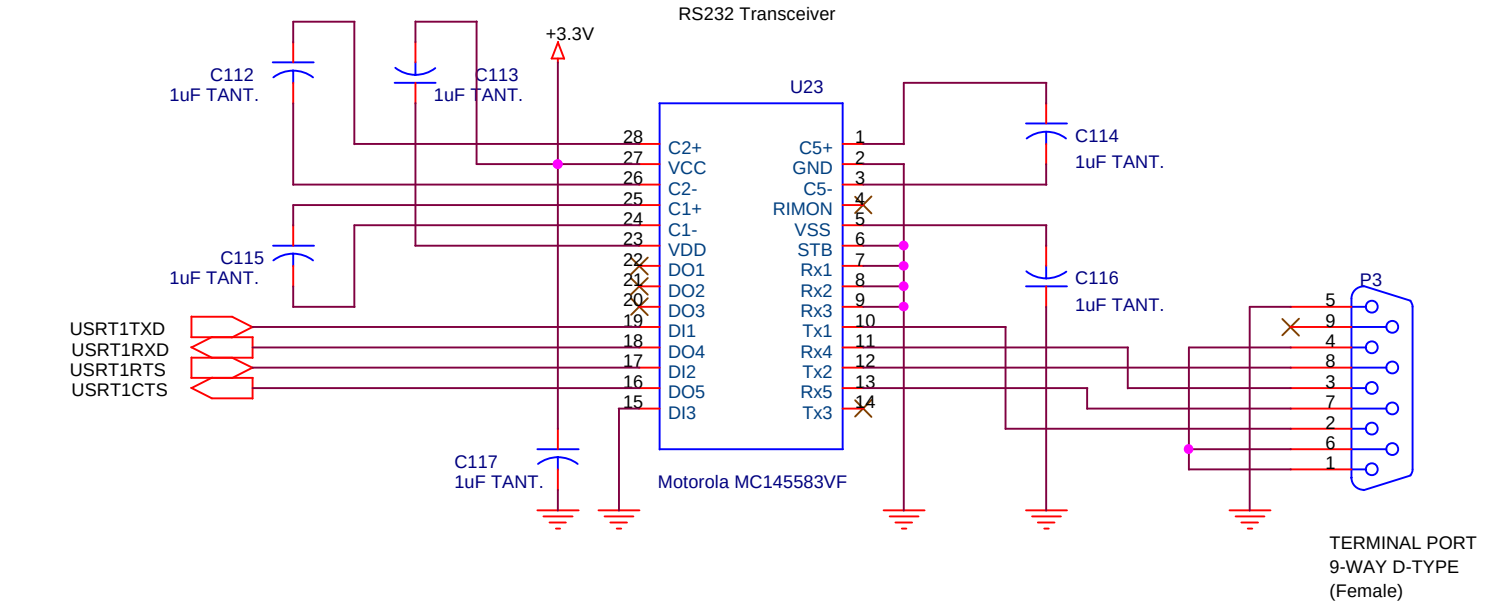


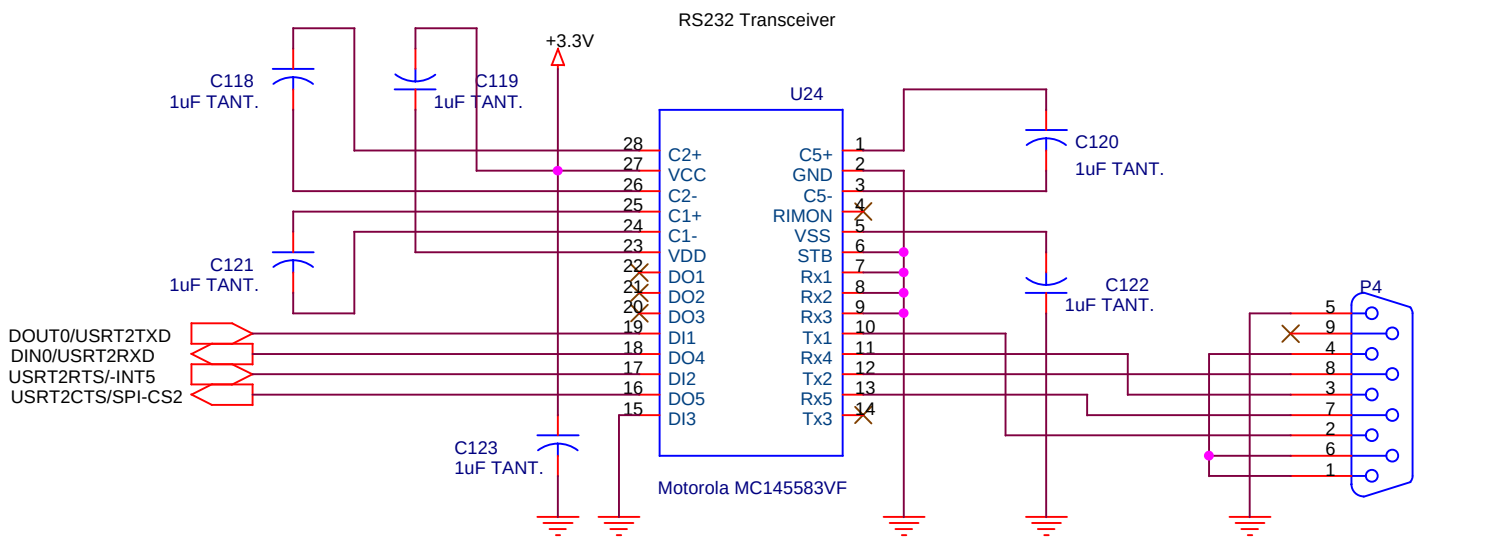
M	SPS SESG - HESD ColdFire Group	
Title	M5272C3 Evaluation Board	
Size B	Document Number MCF5272 - PSU, Reset & Clocks	Rev 1.2
Date: Thursday, November 16, 2000	Sheet 10 of 14	



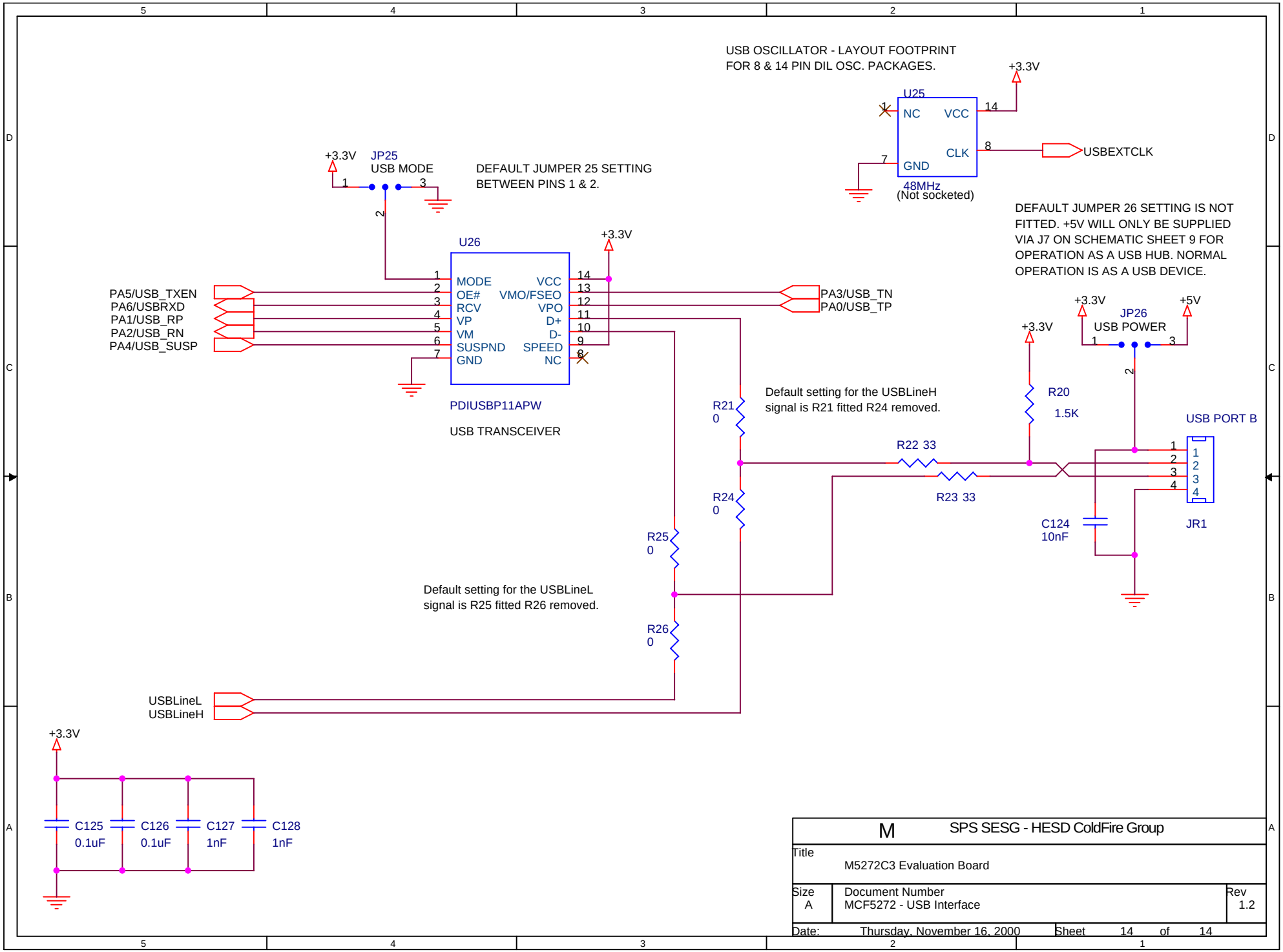
M	SPS SESG - HESD ColdFire Group	
Title	M5272C3 Evaluation Board	
Size A	Document Number MCF5272 Pull-ups, Test points and PAL.	Rev 1.2
Date: Thursday, November 16, 2000	Sheet 11 of 14	


D[0:31]
U21
+3.3V
VDD
DQ0
DQ1
VSSQ
DQ2
DQ3
VDDQ
DQ4
DQ5
VSSQ
DQ6
DQ7
VDDQ
DQML
WE#
CAS#
RAS#
CS#
BA
A10
A0
A1
A2
A3
VDD
VSS
DQ15
DQ14
VSSQ
DQ13
DQ12
VDDQ
DQ11
DQ10
VSSQ
DQ9
DQ8
VDDQ
NC
DQMH
CLK
CKE
NC
A9
A8
A7
A6
A5
A4
VSS
D16
D17
D18
D19
D20
D21
D22
D23
D31
D30
D29
D28
D27
D26
D25
D24
A2
A3
A4
A5
A11
A10
A9
A8
A7
A6
MT48LC1M16A1TG S
C100
1nF
C101
1nF
C102
1nF
C103
1nF
C107
0.1uF
C108
0.1uF
C109
0.1uF
C110
0.1uF
SDRAM Upper 16-bit Word.
-BS2
-SDWE
-CAS0
-RAS0
-CS7
SDBA0
A10_PRECHG
-BS3
SDCLK
SDCKE
A[0:22]
D[0:31]
U22
D0
D1
D2
D3
D4
D5
D6
D7
D15
D14
D13
D12
D11
D10
D9
D8
SDRAM Lower 16-bit Word.
-BS0
-BS1
A[0:22]
M
SPS SESG - HESD ColdFire Group
Title
M5272C3 Evaluation Board
Size
A
Document Number
MCF5272 - SDRAM
Rev
1.2
Date:
Thursday, November 16, 2000
Sheet
12
of
14





M	SPS SESG - HESD ColdFire Group	
Title	M5272C3 Evaluation Board	
Size A	Document Number MCF5272 - Serial Ports	Rev 1.2
Date: Thursday, November 16, 2000	Sheet 13 of 14	


USB OSCILLATOR - LAYOUT FOOTPRINT
FOR 8 & 14 PIN DIL OSC. PACKAGES.
+3.3V
U25
NC
VCC
CLK
GND
USBEXTCLK
48MHz
(Not socketed)
+3.3V
JP25
USB MODE
DEFAULT JUMPER 25 SETTING
BETWEEN PINS 1 & 2.
DEFAULT JUMPER 26 SETTING IS NOT
FITTED. +5V WILL ONLY BE SUPPLIED
VIA J7 ON SCHEMATIC SHEET 9 FOR
OPERATION AS A USB HUB. NORMAL
OPERATION IS AS A USB DEVICE.
U26
+3.3V
MODE
OE#
RCV
VP
VM
SUSPND
GND
VCC
VMO/FSEO
VPO
D+
D-
SPEED
NC
PA5/USB_TXEN
PA6/USBRXD
PA1/USB_RP
PA2/USB_RN
PA4/USB_SUSP
PA3/USB_TN
PA0/USB_TP
PDIUSBP11APW
USB TRANSCEIVER
+3.3V
JP26
USB POWER
+5V
+3.3V
R20
1.5K
USB PORT B
R21
0
Default setting for the USBLineH
signal is R21 fitted R24 removed.
R22 33
R23 33
R24
0
C124
10nF
JR1
R25
0
Default setting for the USBLineL
signal is R25 fitted R26 removed.
R26
0
USBLineL
USBLineH
+3.3V
C125
0.1uF
C126
0.1uF
C127
1nF
C128
1nF
M
SPS SESG - HESD ColdFire Group
Title
M5272C3 Evaluation Board
Size
A
Document Number
MCF5272 - USB Interface
Rev
1.2
Date:
Thursday, November 16, 2000
Sheet
14
of
14

Executive Summary of the M5272C3 Evaluation Board Schematics:

Page 1/14:

The top-level schematic depicts the major blocks and associated bus/signal interconnects for the evaluation board. Each major block/function has its own corresponding schematic page that goes into the detail of the design. This top-level schematic quickly indicates to the engineer the particular functional instantiation of the M5272C3 ColdFire reference design.

Page 2/14 [Buffers]:

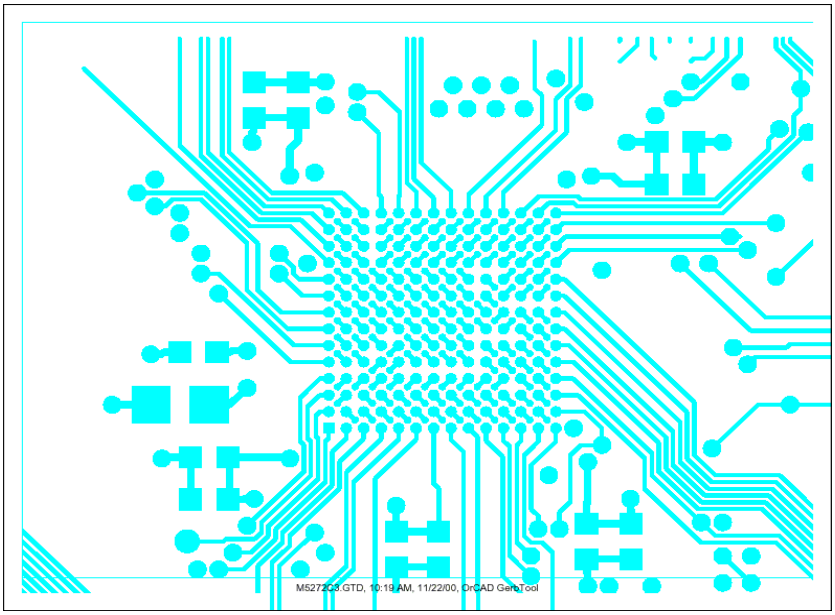
To reduce the bus loading on the processor and to ensure fast transition of the signals, buffers are used to increase the drive capability of the CPU as well as electrically isolate the processor from the peripherals. The signals that primarily tend to have extra loading on them in a system are the ADDRESS and DATA lines. Bi-directional buffers are used for both buses even though the ADDRESS bus is uni-directional. The bi-directional buffer was configured as a uni-directional buffer to reduce the number of parts in the BOM and potentially reduce the cost if high volumes were required.

- U1 and U3 are bi-directional buffers that add drive capability to the DATA signals during a write from the processor and isolate the processor from out of specification peripherals during reads. Note there are no external masters (other than the internal on-chip modules which include the core, DMA and ethernet) allowed when using the MCF5272. The control signals used to determine the direction of the bus and to enable the buffers are -WE (Write Enable (aka R/W)) and signal -BD_CS. -BD_CS is a logical OR'ing of the -CS0 (Chip Select 0; FLASH) and -CS2 (Chip Select 2; SRAM) and is generated by PAL U20 on page 11 of the schematics.
- U2 and U4 are configured as uni-directional buffers that add drive to the ADDRESS signals. Since both buffers are only required to be uni-directional in function, the -DIR and -OE signals to the buffers have been grounded (asserted) permanently.
- Capacitors C1 through C7 provide by-pass/decoupling for the buffers. The two values of capacitor selected, 0.1uF and 1nF, are self resonant at both the low and high frequencies for the clocks/oscillators, and harmonics thereof, on the board. This is true for all the schematic pages of this design, only the number of by-pass capacitors varying dependent on how much supply noise might be present.

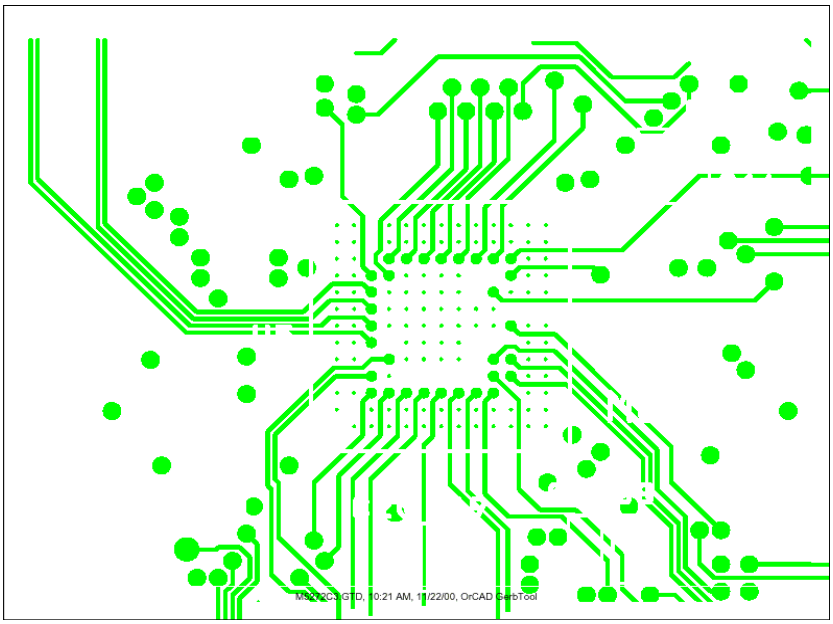
Page 3/14 [CPU]:

This is the ColdFire MCF5272 processor and all of the associated signals.

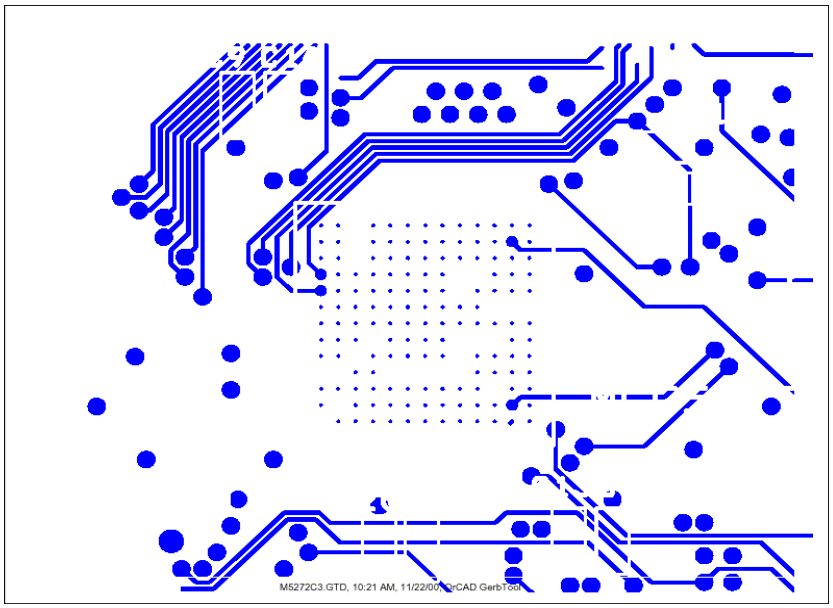
- Signals are grouped according to major function (i.e. DATA, ADDRESS, control, etc...)
- Processor by-pass capacitors are used to reduce supply noise at low & high board frequencies. If the designer looks at the Gerber files available on the Motorola SPS ColdFire website they will see that an isolated area of the power plane has been placed under the MCF5272. In each corner there are two values of by-pass/decoupling capacitor - 0.1uF and 1nF. This minimises any noise that might transfer from the rest of the printed circuit board (PCB) to the CPU supply.
- MCF5272 routing - all the track and space dimensions for this PCB are 8 thousandths of an inch. This tolerance was chosen deliberately as one that most PCB manufacturers ought to be happy to work with. Please study the next four diagrams which depict routing of the signals out of the processor carefully. This is a good way of routing out all the CPU signals on four layers of PCB within easy to manufacture tolerances.
- 196 MAPBGA, +3.3 V DC, 1 mm ball spacing, 15 mm x 15 mm package size



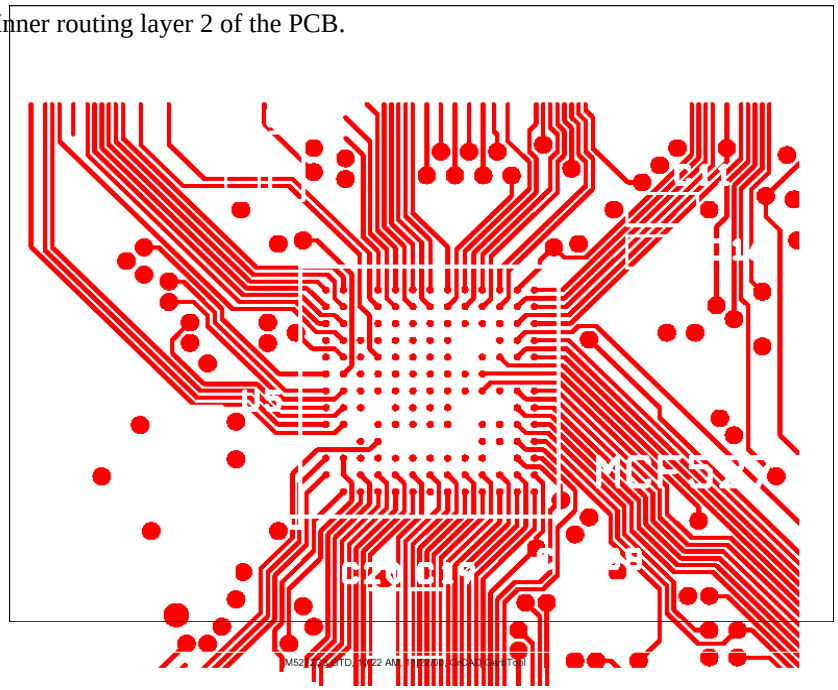
Top routing layer of the PCB detail around the MCF5272.



Inner routing layer 1 of the PCB.

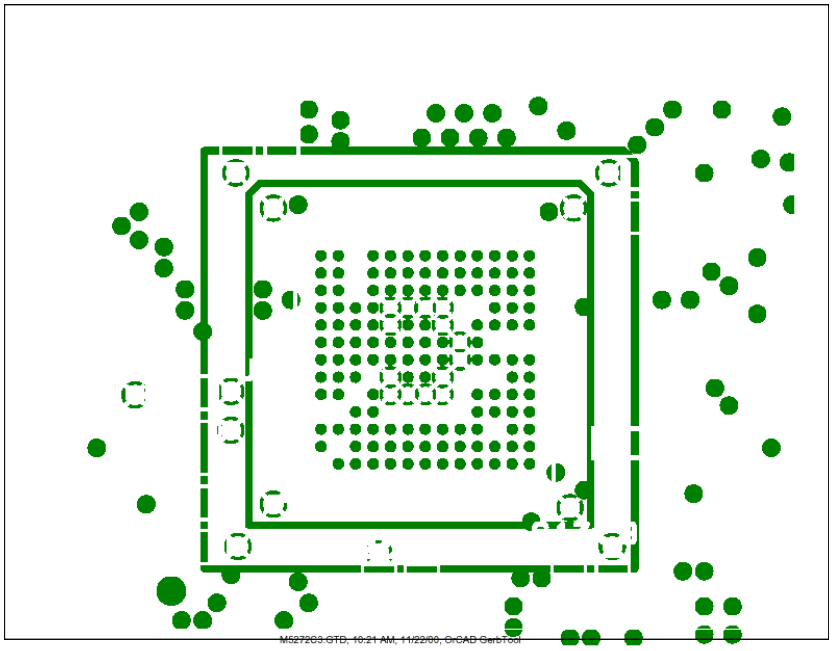


Inner routing layer 2 of the PCB.

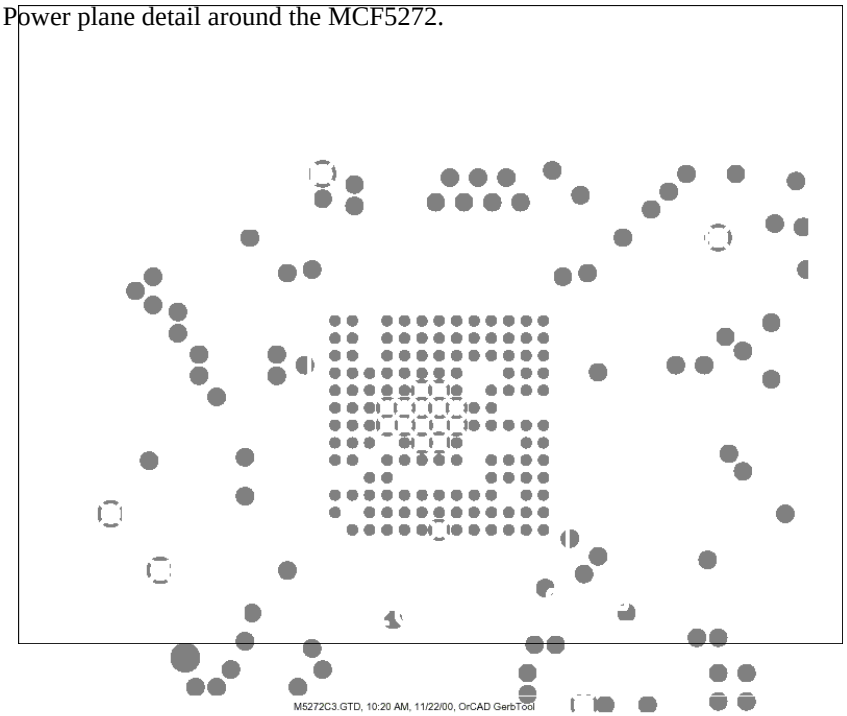


Bottom routing layer of the PCB.

The following two diagrams show the power and ground planes around the MCF5272. Please bear in mind that these are inverse color plots that is white represents copper. The main thing to note on the power plane is the isolation "square" of copper around the MCF5272 that isolates the power plane of the CPU from the rest of the board supply. By-pass/decoupling capacitors are placed at each corner of the CPU directly from the power to ground planes using via's.



Power plane detail around the MCF5272.



Ground plane detail around the MCF5272.

    - Special filtering on the +3.3 VP, USB VDD, and combined ground signals.
- Series termination on the SDRAM control signals of 22 Ohms minimises overshoot and undershoot on these critical signals.

Page 4/14 [Ethernet 100/10BaseT]:

A complicated looking page that can be broken into several smaller pieces to make it easier to understand . In general this page interfaces the ColdFire MCF5272 processor to an external 100/10BaseT ethernet transceiver and magnetic's (isolation transformer). The transceiver requires a 25 MHz OSC and several signals to be configured at reset for correct operation. Our schematics show the default settings for full duplex 10 or 100baseT auto negotiated operation .

- U6 is the 25MHz ethernet OSC.
- Special note for the resistor packs RP5 and RP7 as they are 50 Ohms where most other RP's are 22 or 4.7K Ohm. The Level One ethernet transceiver prefers to drive in to an impedance of 50 ohms and so resistor packs RP5 & RP7 are 50 ohms, whereas the MCF5272 drives most effectively in to 22 ohms hence RP6.
- Bi-color LED's [D1, D3 and D4] are helpful to indicate the status of the ethernet transceiver U7. The meaning of each LED is software configurable via the LED configuration register in U7. See page 67 of the LXT971 data sheet. They are also nice as you get to see color whether the signal is low or high!
- LED D2 illuminates to indicate when an ethernet interrupt (-INT2) is asserted.
- JP2, JP3, JP4, JP10, JP11 and JP12 are used to configure the ethernet default operational mode which is: auto-negotiation of 10 or 100baseT full duplex operation.
- Note 4.7K pull-up on U7 pin 42. You might miss it otherwise!
- There are several filters used with the ethernet transmit and receive channels. It is highly recommended that this exact filtering scheme be used - as we know it works.
- Several notes on the page indicate that the placement of the capacitors is important. Please heed them!
- Yes, the 100K R6 is really that value. It is a JTAG defined resistor and we are listening to them.

Page 5/14 [Expansion Connectors]:

Not much to say here but if you want to have expansion connectors, this is one way to do it. We do have a reference design of a daughter card that is on the ColdFire web site (http://www.mot.com/ColdFire) for those folks that wish to create their own. Our reference design daughter card takes the processor signals to mictor connectors to allow Tektronix Logic Analyzers to interface to our evaluation boards.

- Two 120 pin expansion connectors as you can see.
- These signals are not buffered.
- Note the by-pass caps though. They help to decouple/by-pass the boards power supply noise from any customer hardware.
- One special note, the + 5V DC is supplied by connector J7 (page 9). Since our evaluation board is 100% +3.3V DC, if +5V DC is required, the user must supply this from a regulated supply.

Page 6/14 [Flash Memory]:

The AMD flash is used to store our ROM Monitor dBUG and allow users to store applications or data. The flash ADDRESS and DATA signals are buffered. Chip Select 0 (-CS0) is the *global chip select*. It is active for ALL external memory accesses after reset until the chip selects have been programmed by the user's initialisation code.
A handy feature is implemented with JP13. The user may flash application code in to upper flash memory, change the jumper setting of JP13 to pins 2&3 and then reset the board and have their code boot up and run on the board. Neat feature as the ROM Monitor remains intact!

- This is a 16-bit wide flash memory and therefore the ADDRESS signals that connect from the MCF5272 start with B_A1. A common mistake is for the user to connect B_A0 of the processor to the A0 of the flash.

Page 7/14 [FSRAM]:

Fast Static RAM (FSRAM) is not populated on the evaluation board to keep the cost of the system down. We have provided the foot print on the board to allow those customers who wish to implement 512K of fast memory for benchmarking.

- Special care for proper byte lane enabling is required to prevent the infamous blue wiring so please note the configuration of the -BS[3:0] signals connections to the FSRAM.

- The FSRAM ADDRESS and DATA signals are buffered.
- This is a synchronous FSRAM so a bus clock is required.
- Alternate devices are mentioned on the schematic page as Motorola does not recommend this part any longer for new designs.

Page 8/14 [Background Debug Mode (BDM) Port & Reset Config.]:

The BDM connector is extremely important for every ColdFire design. This connector allows a host development system the ability to control the processor. This is so important that some people forget to implement it! The reason it is so important is that being able to control the processor via the BDM port and development tool allows the user to debug their hardware very quickly and use the same tool chain for code development. This is not the place to detail all the features of the ColdFire debug module but do remember that it allows development tools of all price/performance ratio's to speed your design to market quickly. Whether you only need access to the registers and memory or require instruction trace capabilities, it all is enabled because of the debug module. The debug module + third party tool can also be used in the manufacturing stage to program system flash. Other customers will use the JTAG to do system component verification during manufacturing. Both features are very useful and powerful to the ColdFire family. Sorry, will get off the stump now :<).

- J4 is the BDM connector defined by Motorola and detailed specifically in each ColdFire processor User's Manual Debug section.
- JP14 resets the SDRAM contoller on CPU reset when in default configuration between pins 1 & 2.
- JP15 should always be configured for pins 2&3 as the other mode is a Motorola only test mode and the operation of the processor is not guaranteed if configured incorrectly.
- JP16 defaults to 1&2 for BDM operation. 2&3 allow JTAG mode once the processor goes through a power-on or system reset exception processing.
- JP20 selects which operating frequency the users desires. The default mode of operation is 66 MHz when JP20 is between pins 1&2 and for 48 MHz when pins 2&3 are connected. If the lower frequency suffices for the user application, then an OSC can be eliminated from the BOM.
- U10 is used to configure the MCF5272 default mode of operation at power-on and push button reset times. The -RESET signal enables the buffer to drive the desired signal levels on the WSEL, BUSW0 and BUSW1 ColdFire pins. The -RESET signal is an open drain pin on the MCF5272 processor and therefore can be wired OR'ed to several sources. We have the -RESET wired to the reset button (S1; page 10) and to the BDM connector J4 (this page).

Page 9/14 [PLI Connector]:

Not populated. These interfaces allow ISDN (Integrated Services Digital Network) and POTS (Plain Old Telephone Service) capabilities via the NON-STANDARD PCI interface. Currently the support of these functions is left as an exercise for the user! Please consult your Motorola representative for details.

- The U11, U12, U13, and U14 buffers are activated by PAL U20 (page 11) signals -CS5_WR, -CS6_WR, -CS5_RD, and -CS6_RD respectively.
- If POTS service functions are used with the PLI interface and - 35V and -70V DC are required, the user must supply the correct regulated voltages on connector J7.
- Just a few by-pass capacitors mentioned at the bottom of the page. Again these are used to minimise transmission of power supply noise from the M5272C3 board to any PLI plug-in cards.

Page 10/14 [PSU, Reset & Clock]:

Only four functions on one page so this should be a snap! Both the Reset and Abort buttons are straightforward, well almost. The Reset logic is dual function. It not only allows for manual resetting of the evaluation board but also senses the voltage and if it drops below + 3.08 V DC, U17 will hold the processor and board in reset. The Abort switch, S2, allows the user a manual debounced method to generate an external interrupt, IRQ6. The clock drive circuitry (U16) adds drive capability and fans out the system processor clock. Since the board is designed with +3.3V DC parts only, only one voltage regulator is required. We chose a robust regulator to allow a wide range of input voltages (+ 5V to 14V DC). We also used extra power filtering to ensure proper voltage for the board and minimise EMI radiation.

- U17 is the dual manual Reset and voltage sense circuitry.
- U19 is the manual Abort switch circuitry that asserts the -IRQ6 signal of the MCF5272 processor
- LED's D5 and D6 allow the users to quickly determine that the board is powered up correctly and to indicate the assertion of their respective switches

- F1 is a fast blow fuse to aid in the protection of the sensitive microelectronics devices on the evaluation board in the case where a short occurs (i.e. prevents massive amount of current blasting through the board).
- Diode D7 is used for reverse polarity protection where either the user connected bare wires to connector P2 incorrectly or had incorrect polarity on barrel connector P1.

Page 11 [Pull-ups, Test points and PAL]:

The resistor packs are convenient packages for pull-up and -down of signals and help to clean up the design. This page has pull-ups on signals that should default to logic high or for noise immunity. This page also has a PAL (note that this PAL is not in circuit programmable and therefore socketed to allow for future programming if desired) that is used for buffer management and memory mapped I/O signals for the PLI connectors, as well as Test Points (TP[10:0]) for handy signal monitoring.

- Resistor pack values are 4.7 K to provide a relatively strong pull up on signals to aid in noise rejection and to hold signals in a default state during reset.
- TP[10:0] are just that; test points. The TP's go without much fanfare until you have to debug a system. Bringing out a few key signals and having a place to clip on a ground makes the whole process go that much more smoothly and doesn't cost much in the process.
- U20 (PAL) provides the control signals for buffer management, but also has several I/O pins available for the user.

Page 12/14 [SDRAM]:

A very powerful and marketable feature of the MCF5272 is the integrated SDRAM controller as the system memory industry has been shifting from ADRAM to SDRAM for price/performance. The MCF5272 SDRAM controller is easily programmed to control single banks of memory for 16-bit or 32-bit port sizes.

- The trickiest part of SDRAM is not connecting the proper control signals (all though it does help to do this correctly) but connecting the ADDRESS signals as per the SDRAM and MCF5272 specifications. Please read each SDRAM datasheet very carefully or use the same memory that our evaluation board does to ensure first time functionality.

Page 13/14 [Serial Ports]:

The serial port drivers are a necessity as the UART's provide a simple I/O connection that is common to every PC. The dBUG ROM Monitor uses one of the internal UART's for its access to the world. A great base line tool as you'll see.

- We have essentially used this design on multiple ColdFire evaluation boards with great success. Don't re-invent the wheel, use this design to make life simple.

Page 14/14 [USB Interface]:

The MCF5272 is the first ColdFire integrated processor to have USB. The USB is device/slave mode only and will connect to a host or hub as a device. We will provide a simple low level driver and example/demo on our ColdFire web site for those who wish to experiment with this new peripheral.

- The integrated USB controller on ColdFire requires a 48 MHz OSC (U25). This interface is asynchronous to the processor clock and data/communication is internally synchronized.
- U26 is the external transceiver. ColdFire may use its internal transceiver or use an external transceiver to be USB 1.0 compliant. We will choose which later.
- Note the resistor network on the D+ and D- signals and especially the 1.5 K (R20) resistor which is defined in the USB specification.
- JP26 should not be jumpered as a slave/device does not supply power to the host but receives it if needed.