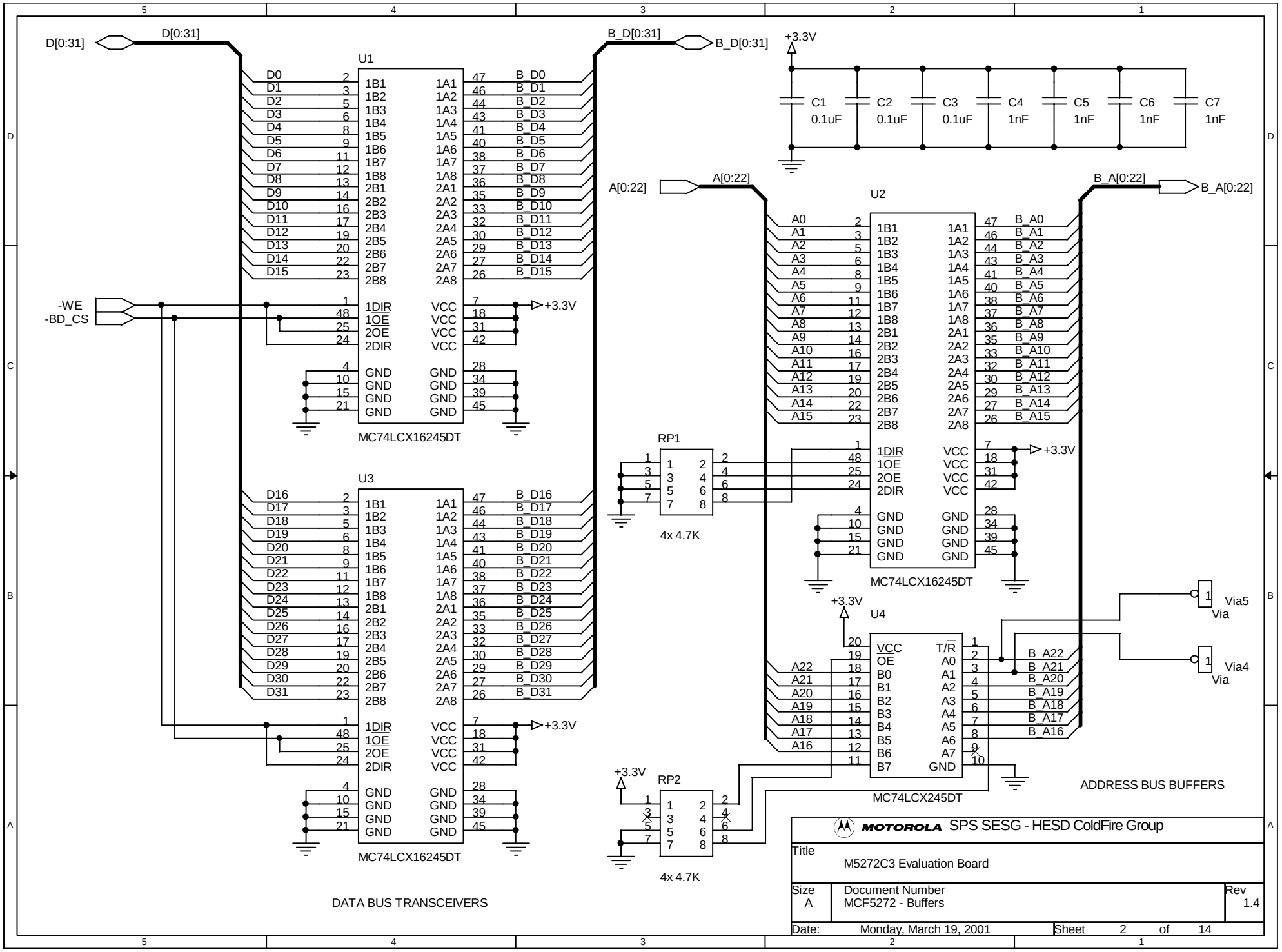
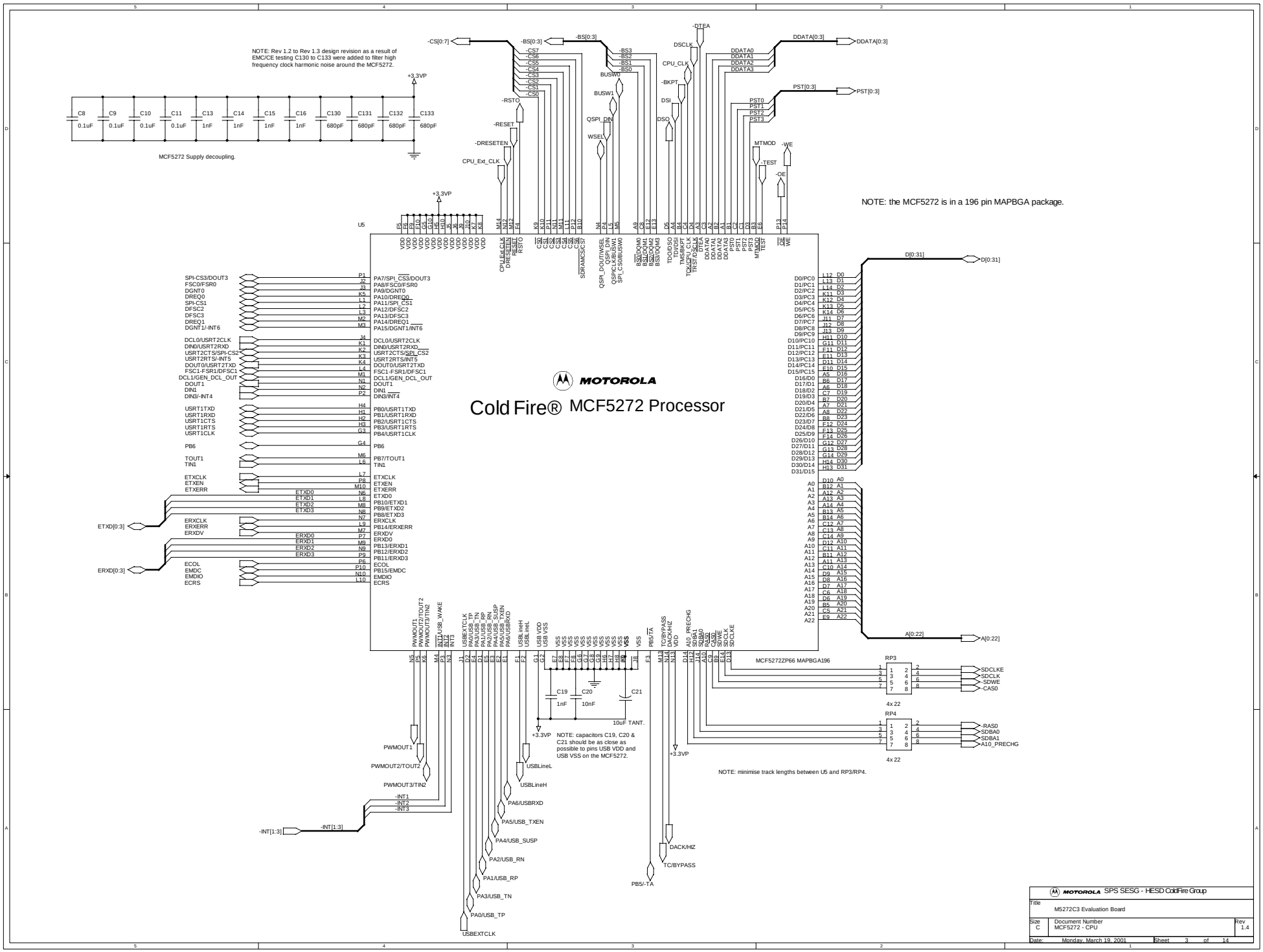
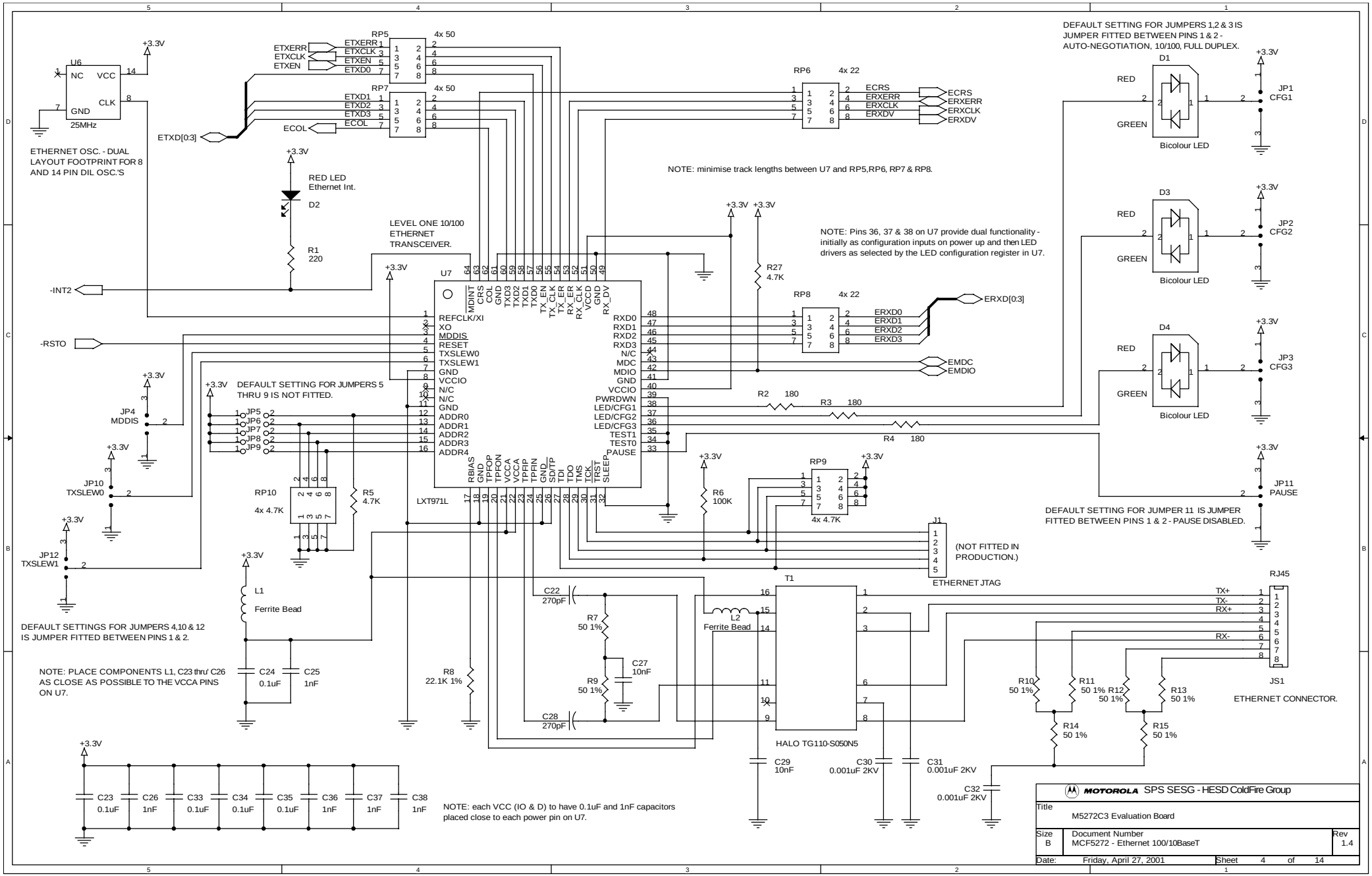
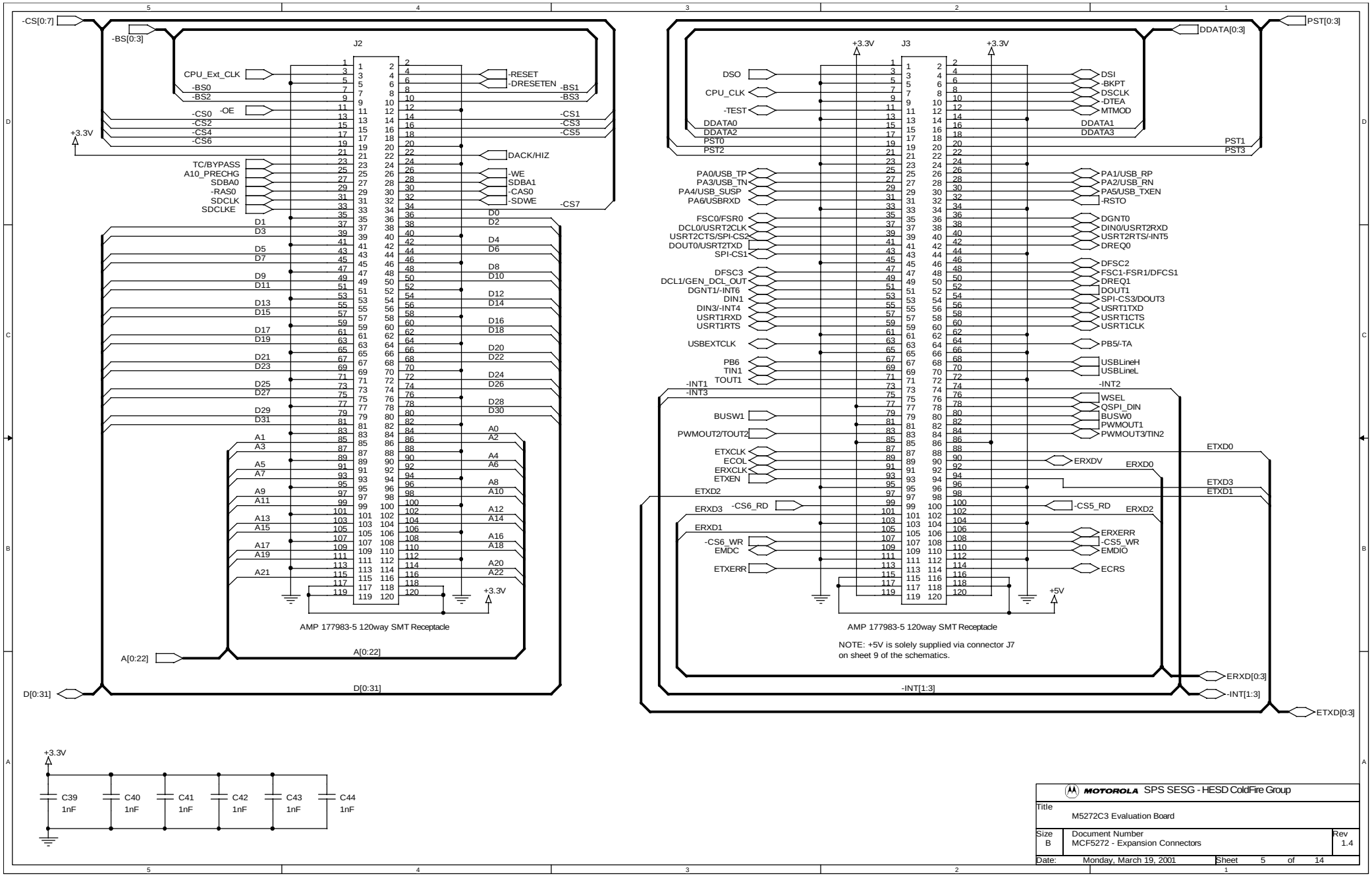
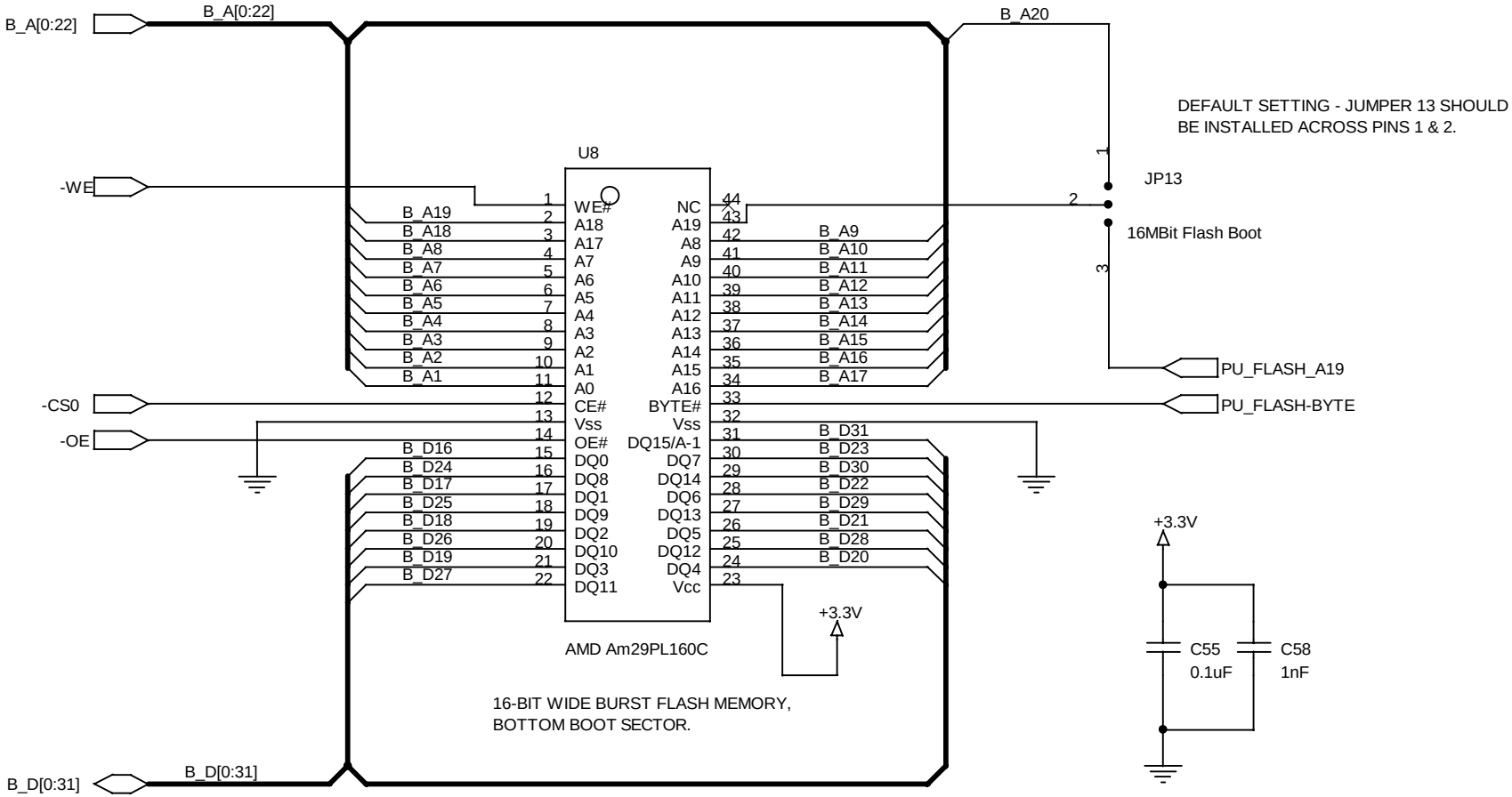
Sheet 14 USB
Sheet 13 Serial Ports
Sheet 8 JTAG/BDM Port & Reset Config.
Sheet 12 SDRAM
Sheet 10 PSU, Reset & Clocks
Sheet 5 Expansion Connectors
Sheet 3 CPU
Sheet 11 Pull-ups, Test Points & PAL
Sheet 4 Ethernet
Sheet 9 PLI Connectors
Sheet 6 Flash
Sheet 7 FSRAM
Sheet 2 Buffers
MOTOROLA
ColdFire® MCF5272
Evaluation Board
MOTOROLA SPS SESG - HESD ColdFire Group
Title
M5272C3 Evaluation Board
Size C
Document Number
Hierarchical Overview
Rev 1.4
Date: Monday, March 19, 2001
Sheet 1 of 14


D[0:31]
B_D[0:31]
A[0:22]
B_A[0:22]
+3.3V
C1 0.1uF
C2 0.1uF
C3 0.1uF
C4 1nF
C5 1nF
C6 1nF
C7 1nF
U1
U2
U3
U4
-WE
-BD_CS
MC74LCX16245DT
MC74LCX245DT
RP1
RP2
4x 4.7K
Via5
Via4
Via
DATA BUS TRANSCEIVERS
ADDRESS BUS BUFFERS
MOTOROLA SPS SESG - HESD ColdFire Group
Title
M5272C3 Evaluation Board
Size A
Document Number
MCF5272 - Buffers
Rev 1.4
Date: Monday, March 19, 2001
Sheet 2 of 14

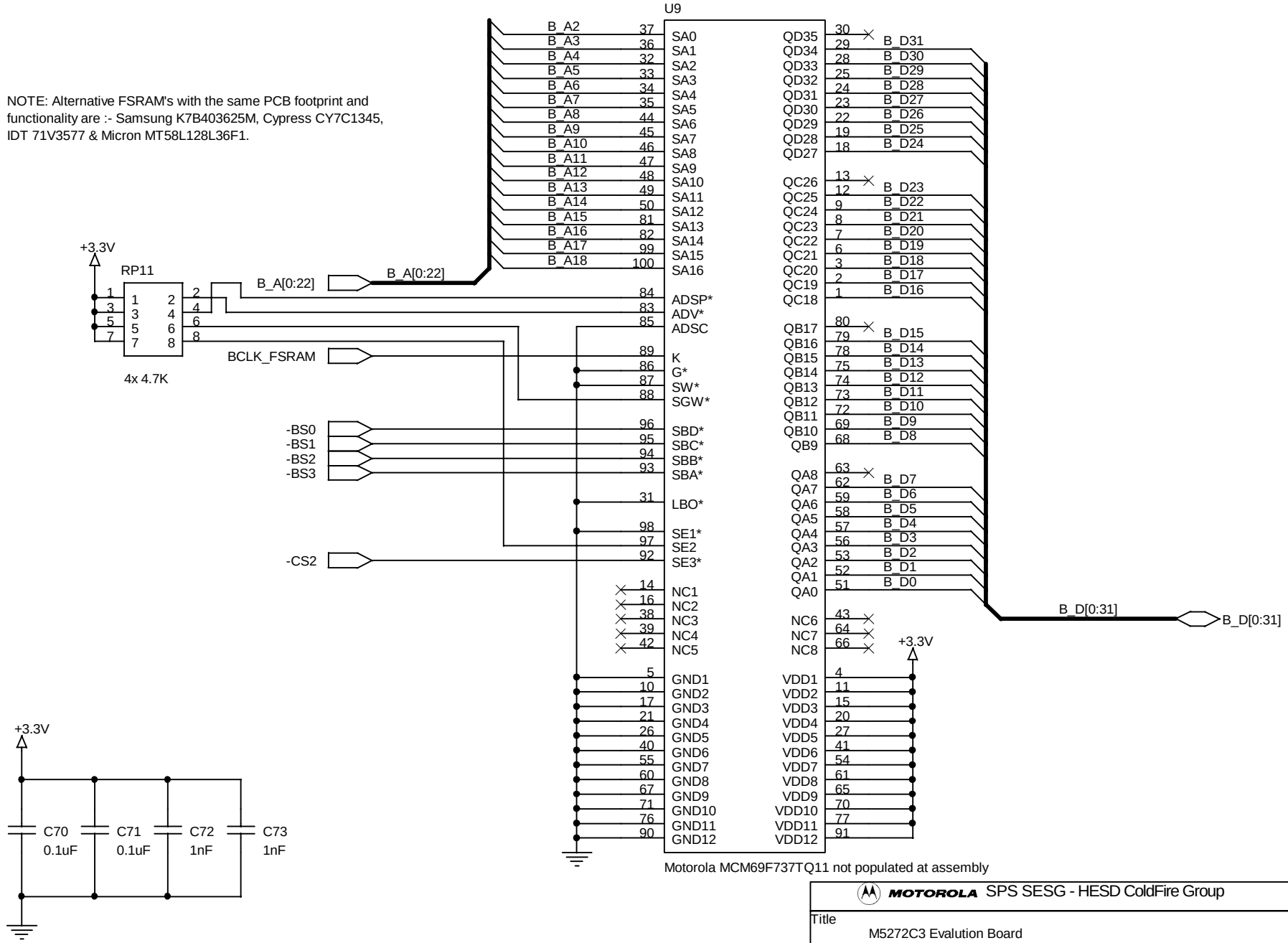

NOTE: Rev 1.2 to Rev 1.3 design revision as a result of EMC/CE testing C130 to C133 were added to filter high frequency clock harmonic noise around the MCF5272.
+3.3VP
C8 0.1uF
C9 0.1uF
C10 0.1uF
C11 0.1uF
C13 1nF
C14 1nF
C15 1nF
C16 1nF
C130 680pF
C131 680pF
C132 680pF
C133 680pF
MCF5272 Supply decoupling.
NOTE: the MCF5272 is in a 196 pin MAPBGA package.
U5
MOTOROLA
Cold Fire® MCF5272 Processor
MCF5272ZP66 MAPBGA196
RP3
RP4
4x 22
C19 1nF
C20 10nF
C21 10uF TANT.
NOTE: capacitors C19, C20 & C21 should be as close as possible to pins USB VDD and USB VSS on the MCF5272.
NOTE: minimise track lengths between U5 and RP3/RP4.
-INT[1:3]
ETXD[0:3]
ERXD[0:3]
D[0:31]
A[0:22]
DDATA[0:3]
PST[0:3]
-CS[0:7]
-BS[0:3]
SDCLKE
SDCLK
-SDWE
-CAS0
-RAS0
SDBA0
SDBA1
A10_PRECHG
USBLineL
USBLineH
PWMOUT1
PWMOUT2/TOUT2
PWMOUT3/TIN2
PA6/USBRXD
PA5/USB_TXEN
PA4/USB_SUSP
PA2/USB_RN
PA1/USB_RP
PA3/USB_TN
PA0/USB_TP
USBEXTCLK
DACK/HIZ
TC/BYPASS
PB5/-TA
SPI-CS3/DOUT3
FSC0/FSR0
DGNT0
DREQ0
SPI-CS1
DFSC2
DFSC3
DREQ1
DGNT1/-INT6
DCL0/USRT2CLK
DIN0/USRT2RXD
USRT2CTS/SPI-CS2
USRT2RTS/-INT5
DOUT0/USRT2TXD
FSC1-FSR1/DFSC1
DCL1/GEN_DCL_OUT
DOUT1
DIN1
DIN3/-INT4
USRT1TXD
USRT1RXD
USRT1CTS
USRT1RTS
USRT1CLK
PB6
TOUT1
TIN1
ETXCLK
ETXEN
ETXERR
ERXCLK
ERXERR
ERXDV
ECOL
EMDC
EMDIO
ECRS
PA7/SPI_CS3/DOUT3
PA8/FSC0/FSR0
PA9/DGNT0
PA10/DREQ0
PA11/SPI_CS1
PA12/DFSC2
PA13/DFSC3
PA14/DREQ1
PA15/DGNT1/INT6
DCL0/USRT2CLK
DIN0/USRT2RXD
USRT2CTS/SPI_CS2
USRT2RTS/INT5
DOUT0/USRT2TXD
FSC1-FSR1/DFSC1
DCL1/GEN_DCL_OUT
DOUT1
DIN1
DIN3/INT4
PB0/USRT1TXD
PB1/USRT1RXD
PB2/USRT1CTS
PB3/USRT1RTS
PB4/USRT1CLK
PB6
PB7/TOUT1
TIN1
ETXCLK
ETXEN
ETXERR
ETXD0
PB10/ETXD1
PB9/ETXD2
PB8/ETXD3
ERXCLK
PB14/ERXERR
ERXDV
ERXD0
PB13/ERXD1
PB12/ERXD2
PB11/ERXD3
ECOL
PB15/EMDC
EMDIO
ECRS
D0/PC0
D1/PC1
D2/PC2
D3/PC3
D4/PC4
D5/PC5
D6/PC6
D7/PC7
D8/PC8
D9/PC9
D10/PC10
D11/PC11
D12/PC12
D13/PC13
D14/PC14
D15/PC15
D16/D0
D17/D1
D18/D2
D19/D3
D20/D4
D21/D5
D22/D6
D23/D7
D24/D8
D25/D9
D26/D10
D27/D11
D28/D12
D29/D13
D30/D14
D31/D15
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
MOTOROLA SPS SESG - HESD ColdFire Group
Title
M5272C3 Evaluation Board
Size C
Document Number MCF5272 - CPU
Rev 1.4
Date: Monday, March 19, 2001
Sheet 3 of 14


U6
NC
VCC
CLK
GND
25MHz
+3.3V
ETHERNET OSC. - DUAL LAYOUT FOOTPRINT FOR 8 AND 14 PIN DIL OSC.'S
RP5
4x 50
ETXERR
ETXCLK
ETXEN
ETXD0
RP7
4x 50
ETXD1
ETXD2
ETXD3
ECOL
ETXD[0:3]
RP6
4x 22
ECRS
ERXERR
ERXCLK
ERXDV
NOTE: minimise track lengths between U7 and RP5,RP6, RP7 & RP8.
DEFAULT SETTING FOR JUMPERS 1,2 & 3 IS JUMPER FITTED BETWEEN PINS 1 & 2 - AUTO-NEGOTIATION, 10/100, FULL DUPLEX.
D1
RED
GREEN
Bicolour LED
JP1
CFG1
D3
JP2
CFG2
D4
JP3
CFG3
RED LED
Ethernet Int.
D2
R1
220
-INT2
-RSTO
LEVEL ONE 10/100 ETHERNET TRANSCEIVER.
U7
REFCLK/XI
XO
MDDIS
RESET
TXSLEW0
TXSLEW1
GND
VCCIO
N/C
ADDR0
ADDR1
ADDR2
ADDR3
ADDR4
MDINT
CRS
COL
TXD3
TXD2
TXD1
TXD0
TX_EN
TX_CLK
TX_ER
RX_ER
RX_CLK
RX_DV
RXD0
RXD1
RXD2
RXD3
MDC
MDIO
PWRDWN
LED/CFG1
LED/CFG2
LED/CFG3
TEST1
TEST0
PAUSE
RBIAS
TPFOP
TPFON
VCCA
TPFIP
TPFIN
SD/TP
TDI
TDO
TMS
TCK
TRST
SLEEP
LXT971L
NOTE: Pins 36, 37 & 38 on U7 provide dual functionality - initially as configuration inputs on power up and then LED drivers as selected by the LED configuration register in U7.
R27
4.7K
RP8
4x 22
ERXD0
ERXD1
ERXD2
ERXD3
ERXD[0:3]
EMDC
EMDIO
R2 180
R3 180
R4 180
JP11
PAUSE
DEFAULT SETTING FOR JUMPER 11 IS JUMPER FITTED BETWEEN PINS 1 & 2 - PAUSE DISABLED.
JP4
MDDIS
JP10
TXSLEW0
JP12
TXSLEW1
DEFAULT SETTING FOR JUMPERS 5 THRU 9 IS NOT FITTED.
JP5
JP6
JP7
JP8
JP9
RP10
4x 4.7K
R5
4.7K
R6
100K
RP9
4x 4.7K
J1
(NOT FITTED IN PRODUCTION.)
ETHERNET JTAG
DEFAULT SETTINGS FOR JUMPERS 4,10 & 12 IS JUMPER FITTED BETWEEN PINS 1 & 2.
L1
Ferrite Bead
NOTE: PLACE COMPONENTS L1, C23 thru' C26 AS CLOSE AS POSSIBLE TO THE VCCA PINS ON U7.
C24
0.1uF
C25
1nF
R8
22.1K 1%
C22
270pF
R7
50 1%
R9
50 1%
C27
10nF
C28
270pF
L2
Ferrite Bead
T1
HALO TG110-S050N5
C29
10nF
C30
0.001uF 2KV
C31
0.001uF 2KV
C32
0.001uF 2KV
RJ45
TX+
TX-
RX+
RX-
JS1
ETHERNET CONNECTOR.
R10
50 1%
R11
50 1%
R12
50 1%
R13
50 1%
R14
50 1%
R15
50 1%
C23
0.1uF
C26
1nF
C33
0.1uF
C34
0.1uF
C35
0.1uF
C36
1nF
C37
1nF
C38
1nF
NOTE: each VCC (IO & D) to have 0.1uF and 1nF capacitors placed close to each power pin on U7.
MOTOROLA SPS SESG - HESD ColdFire Group
Title
M5272C3 Evaluation Board
Size B
Document Number
MCF5272 - Ethernet 100/10BaseT
Rev 1.4
Date: Friday, April 27, 2001
Sheet 4 of 14


-CS[0:7]
-BS[0:3]
J2
CPU_Ext_CLK
-BS0
-BS2
-OE
-CS0
-CS2
-CS4
-CS6
+3.3V
TC/BYPASS
A10_PRECHG
SDBA0
-RAS0
SDCLK
SDCLKE
-RESET
-DRESETEN
-BS1
-BS3
-CS1
-CS3
-CS5
DACK/HIZ
-WE
SDBA1
-CAS0
-SDWE
-CS7
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
AMP 177983-5 120way SMT Receptacle
A[0:22]
D[0:31]
DDATA[0:3]
PST[0:3]
J3
DSO
CPU_CLK
-TEST
DDATA0
DDATA2
PST0
PST2
DSI
-BKPT
DSCLK
-DTEA
MTMOD
DDATA1
DDATA3
PST1
PST3
PA0/USB_TP
PA3/USB_TN
PA4/USB_SUSP
PA6/USBRXD
PA1/USB_RP
PA2/USB_RN
PA5/USB_TXEN
-RSTO
FSC0/FSR0
DCL0/USRT2CLK
USRT2CTS/SPI-CS2
DOUT0/USRT2TXD
SPI-CS1
DGNT0
DIN0/USRT2RXD
USRT2RTS/-INT5
DREQ0
DFSC3
DCL1/GEN_DCL_OUT
DGNT1/-INT6
DIN1
DIN3/-INT4
USRT1RXD
USRT1RTS
DFSC2
FSC1-FSR1/DFCS1
DREQ1
DOUT1
SPI-CS3/DOUT3
USRT1TXD
USRT1CTS
USRT1CLK
USBEXTCLK
PB5/-TA
PB6
TIN1
TOUT1
USBLineH
USBLineL
-INT1
-INT3
-INT2
BUSW1
WSEL
QSPI_DIN
BUSW0
PWMOUT1
PWMOUT2/TOUT2
PWMOUT3/TIN2
ETXCLK
ECOL
ERXCLK
ETXEN
ERXDV
ETXD0
ERXD0
ETXD3
ETXD1
ETXD2
ERXD3
-CS6_RD
-CS5_RD
ERXD2
ERXD1
-CS6_WR
EMDC
ERXERR
-CS5_WR
EMDIO
ETXERR
ECRS
+5V
AMP 177983-5 120way SMT Receptacle
NOTE: +5V is solely supplied via connector J7
on sheet 9 of the schematics.
ERXD[0:3]
-INT[1:3]
ETXD[0:3]
C39
1nF
C40
1nF
C41
1nF
C42
1nF
C43
1nF
C44
1nF
MOTOROLA SPS SESG - HESD ColdFire Group
Title
M5272C3 Evaluation Board
Size
B
Document Number
MCF5272 - Expansion Connectors
Rev
1.4
Date: Monday, March 19, 2001
Sheet 5 of 14

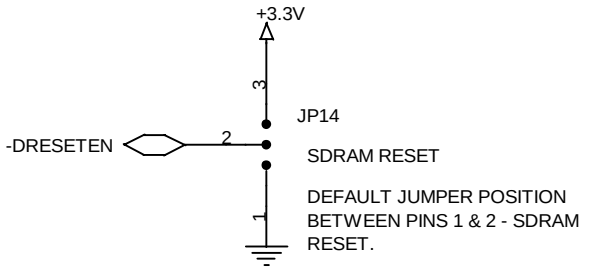


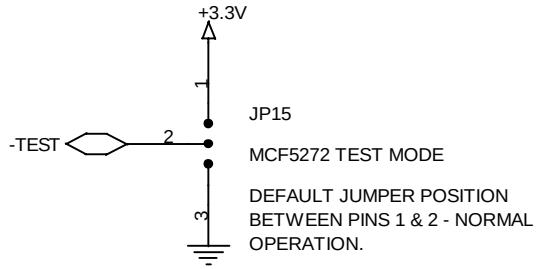
MOTOROLA SPS SESG - HESD ColdFire Group		
Title M5272C3 Evaluation Board		
Size A	Document Number MCF5272 - Flash Memory	Rev 1.4
Date: Monday, March 19, 2001	Sheet 6 of 14	

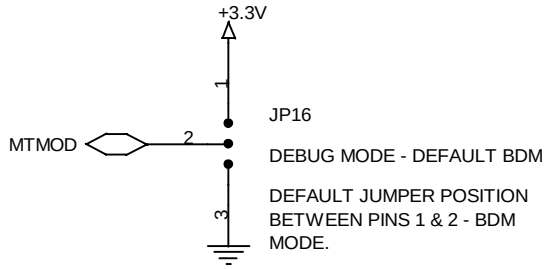


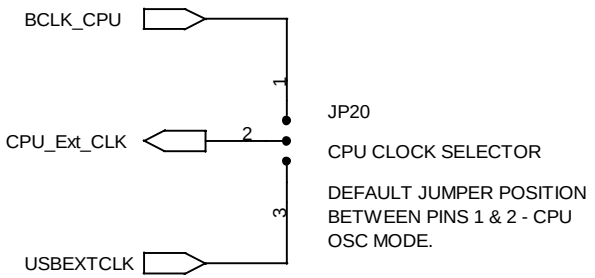
MOTOROLA SPS SESG - HESD ColdFire Group

Title	M5272C3 Evalution Board	
Size A	Document Number MCF5272 - FSRAM	Rev 1.4
Date: Monday, March 19, 2001	Sheet 7 of 14	



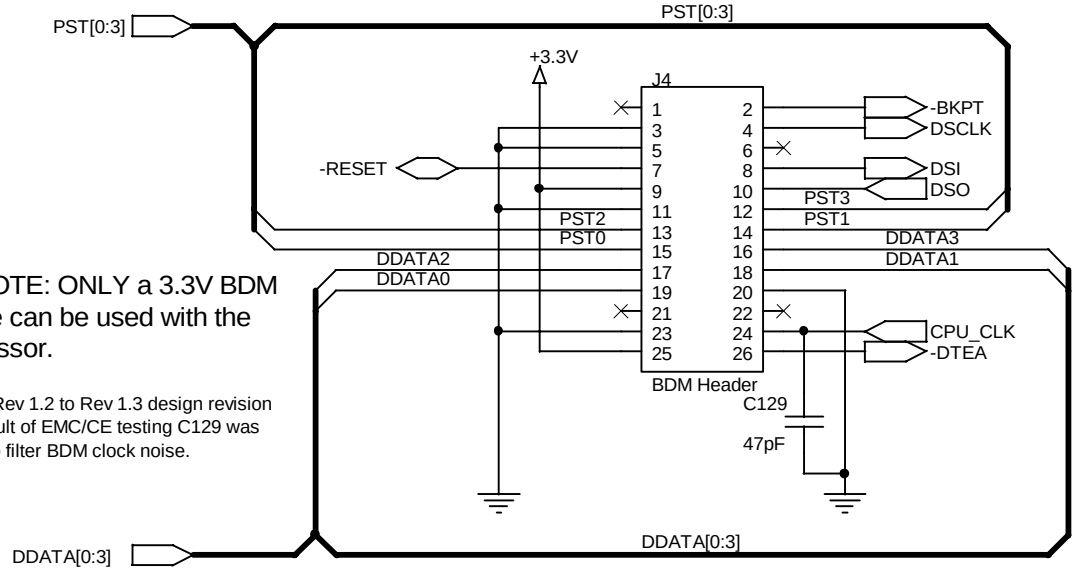






IMPORTANT NOTE: ONLY a 3.3V BDM debugging cable can be used with the MCF5272 processor.

NOTE: Rev 1.2 to Rev 1.3 design revision as a result of EMC/CE testing C129 was added to filter BDM clock noise.



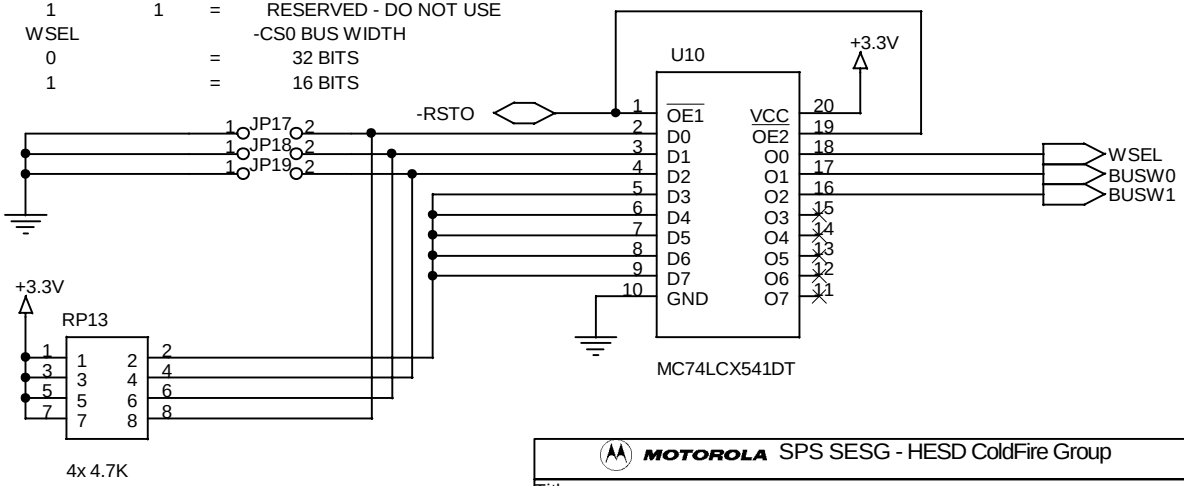
NOTE: 4.7K pull up resistors are used on signals -BKPT, DSCLK, DSI, DSO, -RESET & -DTEA. See page 11 of the schematics.

DEFAULT FOR JP17/WSEL IS FITTED (0).
DEFAULT FOR JP18/BUSW0 IS FITTED (0).
DEFAULT FOR JP19/BUSW1 IS NOT FITTED (1).

BUSW1	BUSW0		DATA BUS WIDTH
0	0	=	32 BITS
0	1	=	8 BITS
1	0	=	16 BITS
1	1	=	RESERVED - DO NOT USE

WSEL		-CS0 BUS WIDTH
0	=	32 BITS
1	=	16 BITS

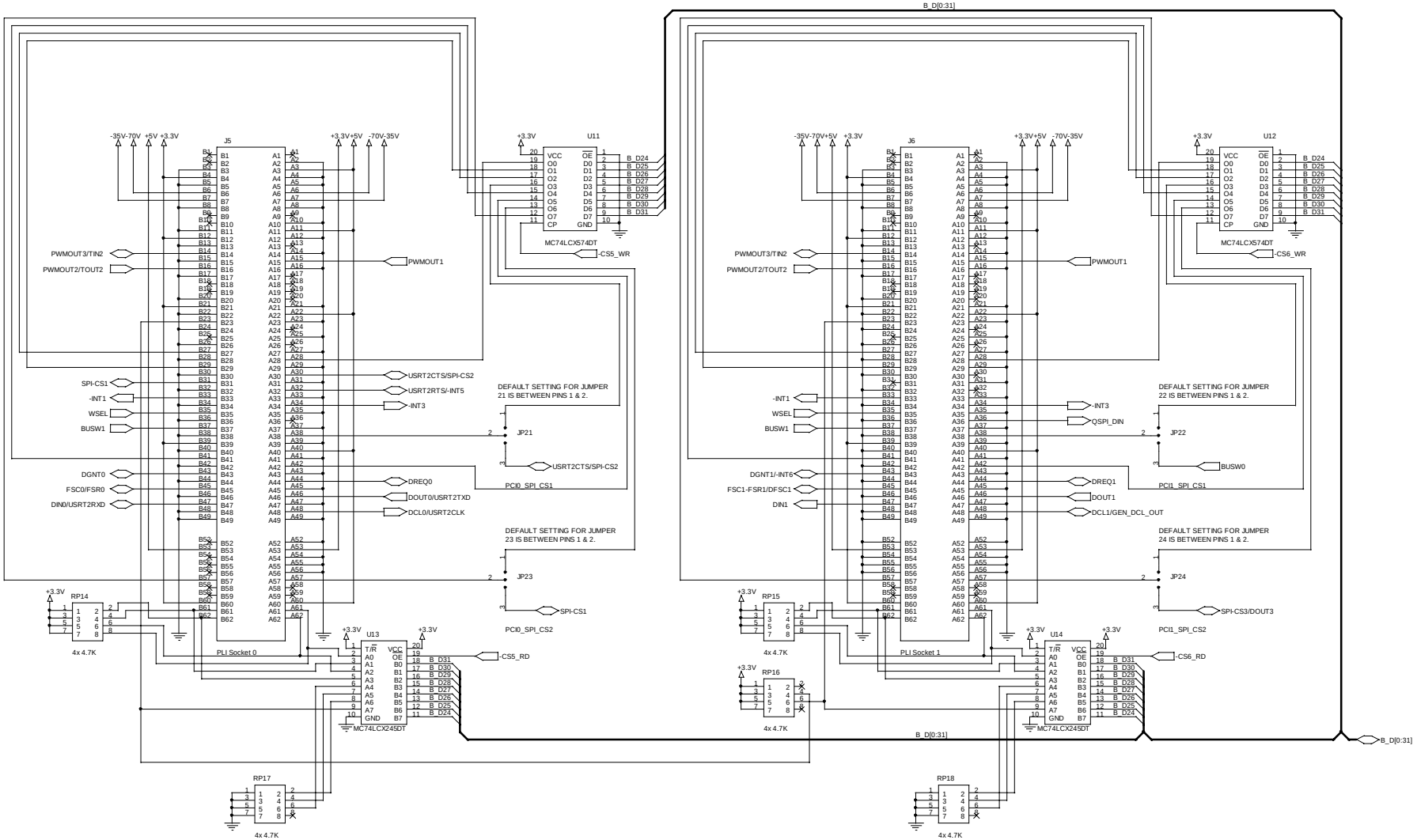
IMPORTANT NOTE: THE -RSTO SIGNAL MUST BE USED TO DRIVE THE OUTPUT ENABLE PINS OF U10 TO ALLOW THE WSEL, BUSW0 & BUSW1 SIGNALS TO BE LATCHED CORRECTLY BY THE MCF5272 - U5.

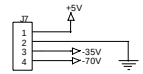


MOTOROLA SPS SESG - HESD ColdFire Group

Title	M5272C3 Evaluation Board	
Size A	Document Number MCF5272 Background Debug Mode (BDM) Port & Reset Config.	Rev 1.4
Date: Monday, March 19, 2001	Sheet 8 of 14	

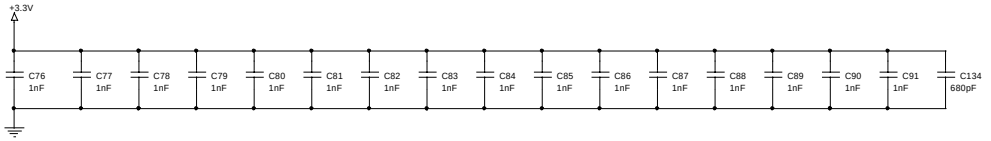
NOTE: PLI Sockets 0 & 1 are not populated during assembly.





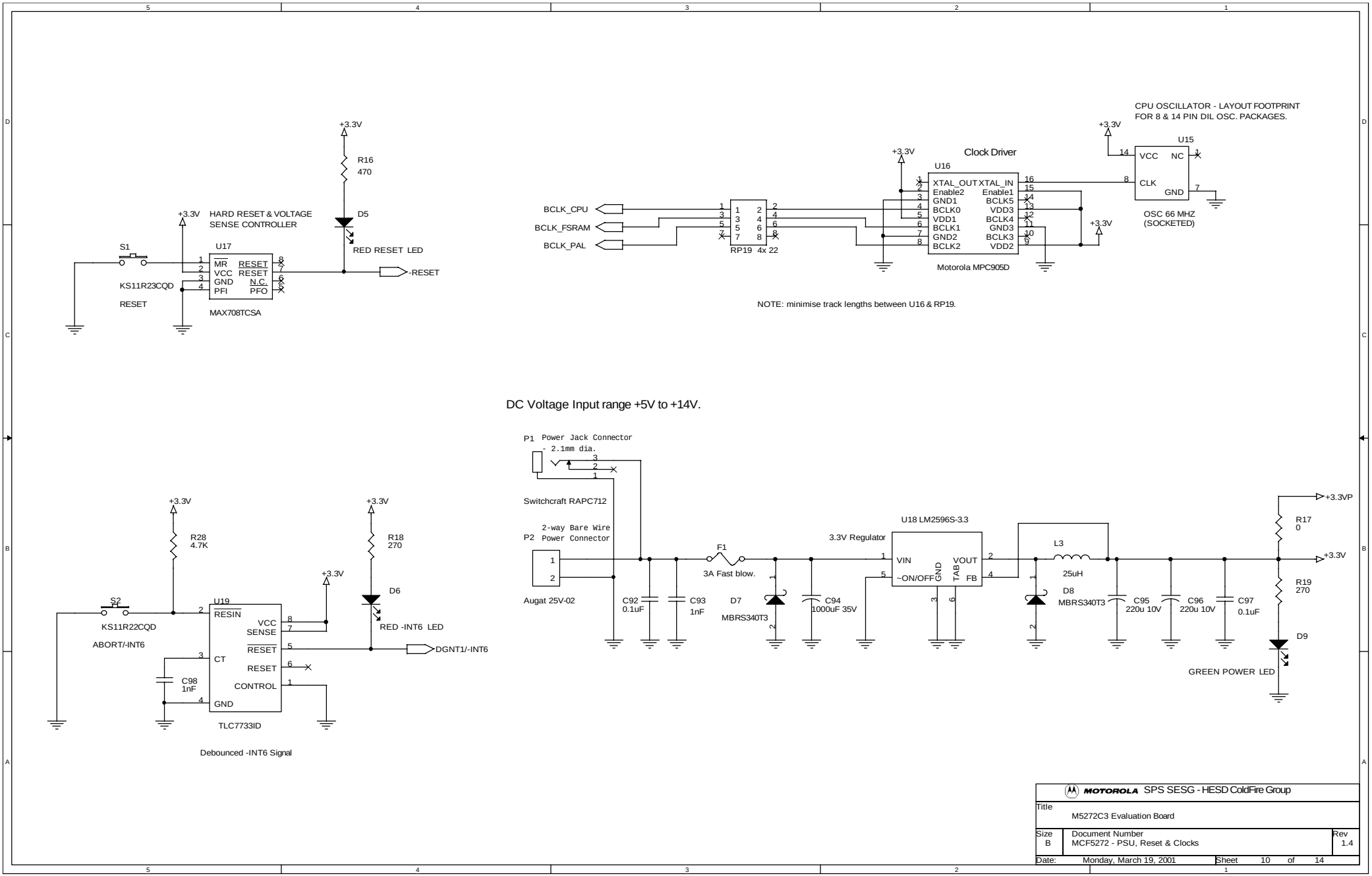
+5V & HIGH VOLTAGE CONN.

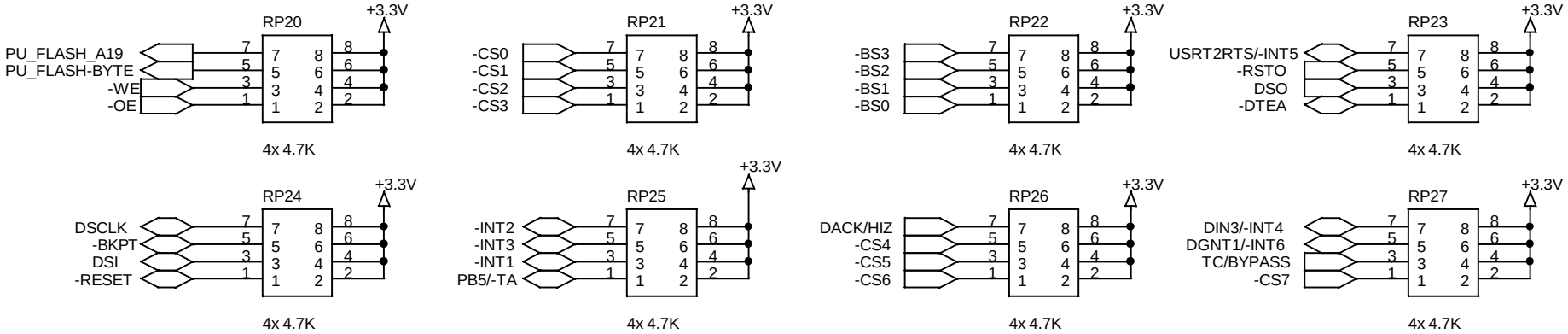
NOTE: all volatge supplies on J5 must be regulated and stable. +5V for the whole board is solely suppled via connector J7.

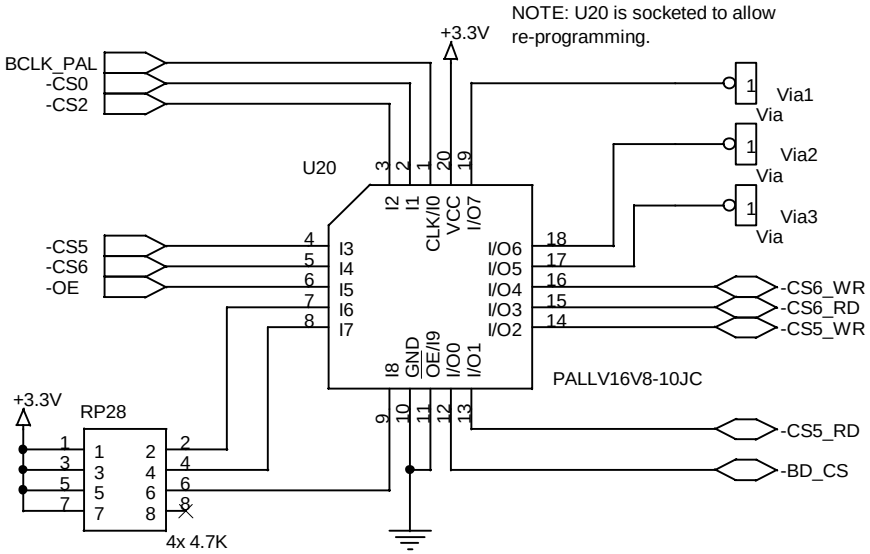


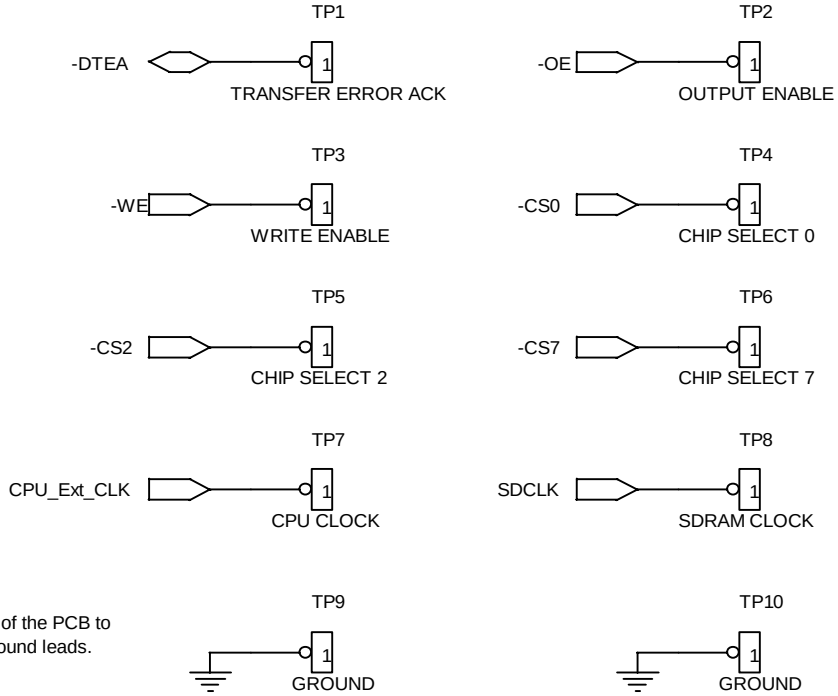
NOTE: Rev 1.2 to Rev 1.3 design revision as a result of EMC/CE testing C134 was added to filter high frequency clock harmonic noise near U16 (See schematic sheet 10).

MOTOROLA SPS SESG - HESD ColdFire Group		
Title: M5272C3 Evaluation Board		
Size: C	Document Number: MCF5272 - PLI Connectors	Rev: 1.4
Date: Monday, March 19, 2001	Sheet 9 of 14	


HARD RESET & VOLTAGE SENSE CONTROLLER
+3.3V
R16 470
D5
RED RESET LED
S1
U17
MR RESET
VCC RESET
GND N.C.
PFI PFO
KS11R23CQD
RESET
MAX708TCSA
-RESET
CPU OSCILLATOR - LAYOUT FOOTPRINT FOR 8 & 14 PIN DIL OSC. PACKAGES.
U15
VCC NC
CLK
GND
OSC 66 MHZ (SOCKETED)
Clock Driver
U16
XTAL_OUT XTAL_IN
Enable2 Enable1
GND1 BCLK5
BCLK0 VDD3
VDD1 BCLK4
BCLK1 GND3
GND2 BCLK3
BCLK2 VDD2
Motorola MPC905D
BCLK_CPU
BCLK_FSRAM
BCLK_PAL
RP19 4x 22
NOTE: minimise track lengths between U16 & RP19.
DC Voltage Input range +5V to +14V.
P1 Power Jack Connector - 2.1mm dia.
Switchcraft RAPC712
2-way Bare Wire Power Connector
P2
Augat 25V-02
C92 0.1uF
C93 1nF
F1
3A Fast blow.
D7 MBRS340T3
C94 1000uF 35V
U18 LM2596S-3.3
3.3V Regulator
VIN VOUT
~ON/OFF FB
GND TAB
L3 25uH
D8 MBRS340T3
C95 220u 10V
C96 220u 10V
C97 0.1uF
R17 0
R19 270
+3.3VP
D9
GREEN POWER LED
R28 4.7K
S2
KS11R22CQD
ABORT/-INT6
U19
RESIN
VCC
SENSE
RESET
CT
RESET
CONTROL
GND
C98 1nF
TLC7733ID
R18 270
D6
RED -INT6 LED
DGNT1/-INT6
Debounced -INT6 Signal
MOTOROLA SPS SESG - HESD ColdFire Group
Title
M5272C3 Evaluation Board
Size B
Document Number
MCF5272 - PSU, Reset & Clocks
Rev 1.4
Date: Monday, March 19, 2001
Sheet 10 of 14

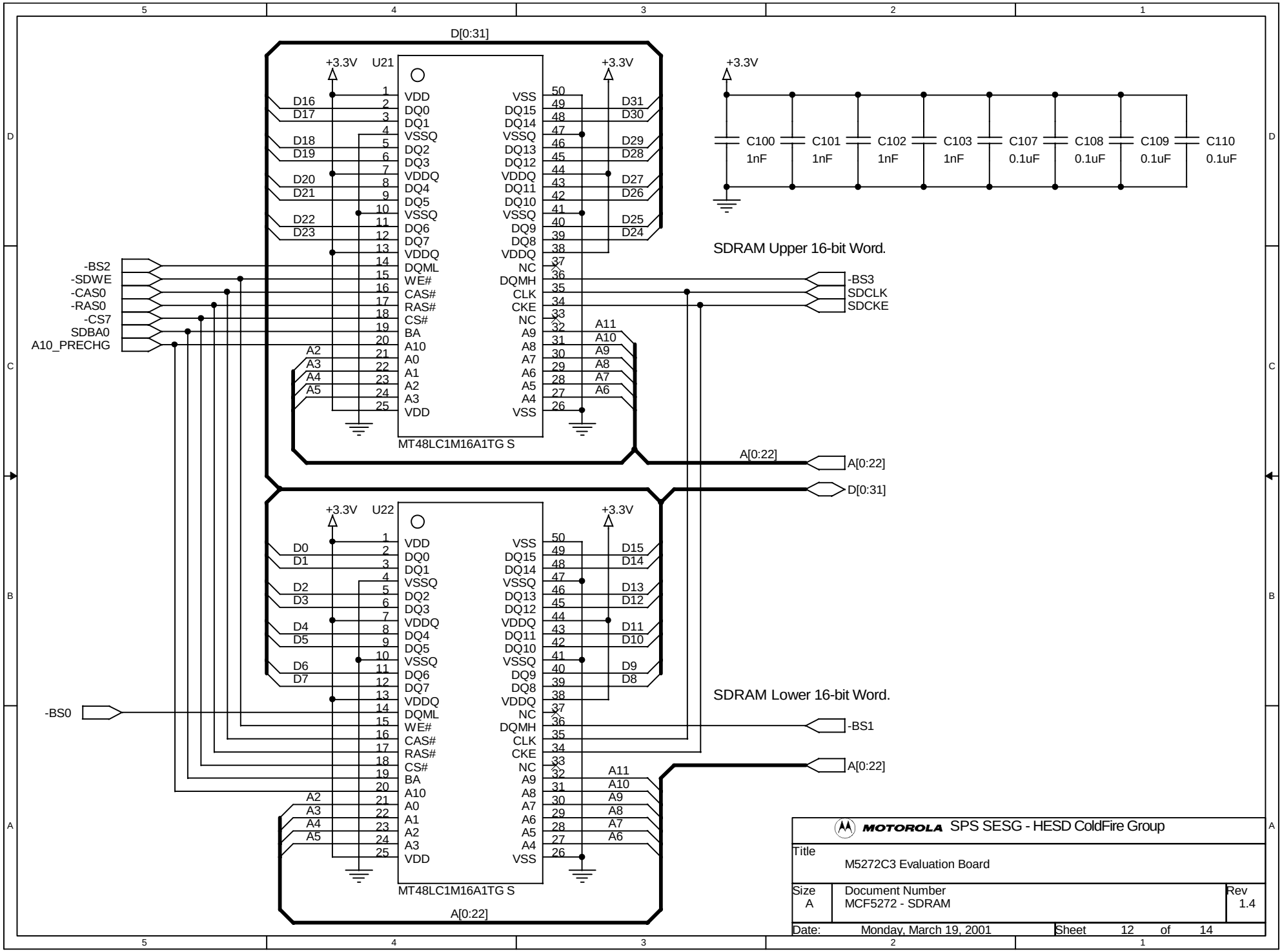






NOTE: Place TP9 & TP10 at the corners of the PCB to allow easy connection of 'scope probe ground leads.

MOTOROLA SPS SESG - HESD ColdFire Group		
Title M5272C3 Evaluation Board		
Size A	Document Number MCF5272 Pull-ups, Test points and PAL.	Rev 1.4
Date: Monday, March 19, 2001	Sheet 11 of 14	


D[0:31]
U21
+3.3V
MT48LC1M16A1TG S
SDRAM Upper 16-bit Word.
C100 1nF
C101 1nF
C102 1nF
C103 1nF
C107 0.1uF
C108 0.1uF
C109 0.1uF
C110 0.1uF
-BS2
-SDWE
-CAS0
-RAS0
-CS7
SDBA0
A10_PRECHG
-BS3
SDCLK
SDCKE
A[0:22]
D[0:31]
U22
SDRAM Lower 16-bit Word.
-BS0
-BS1
A[0:22]
MOTOROLA SPS SESG - HESD ColdFire Group
Title
M5272C3 Evaluation Board
Size A
Document Number MCF5272 - SDRAM
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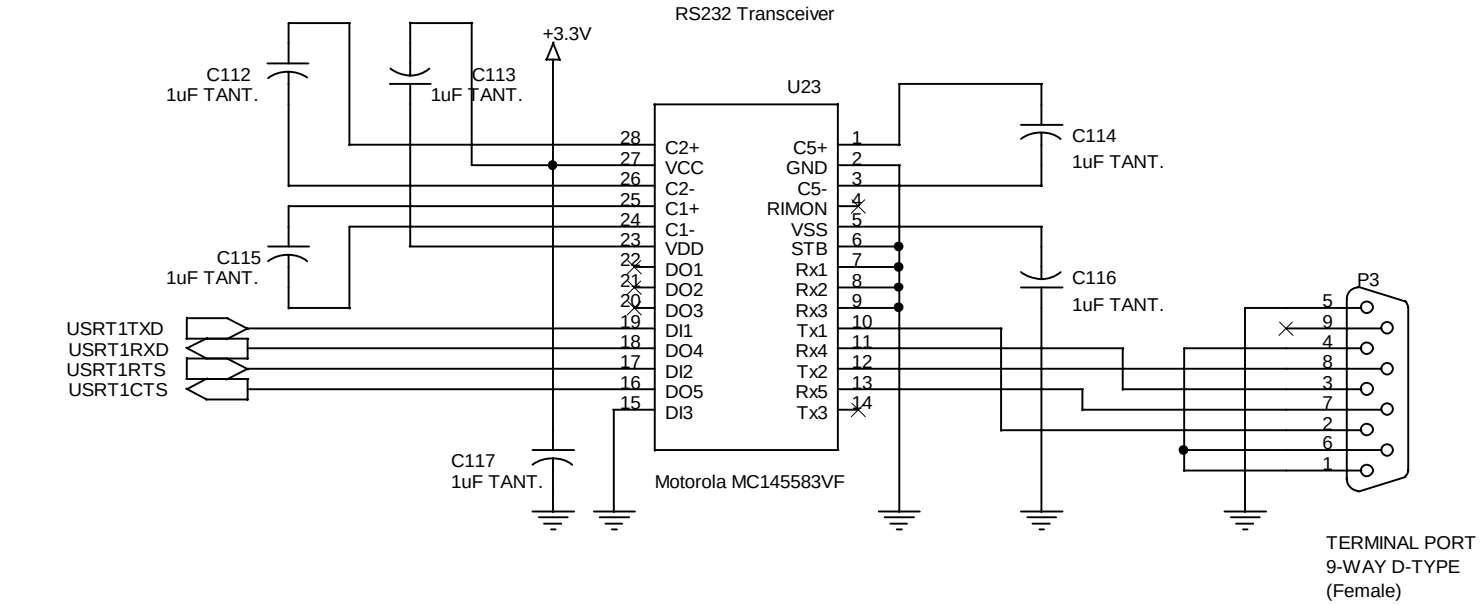
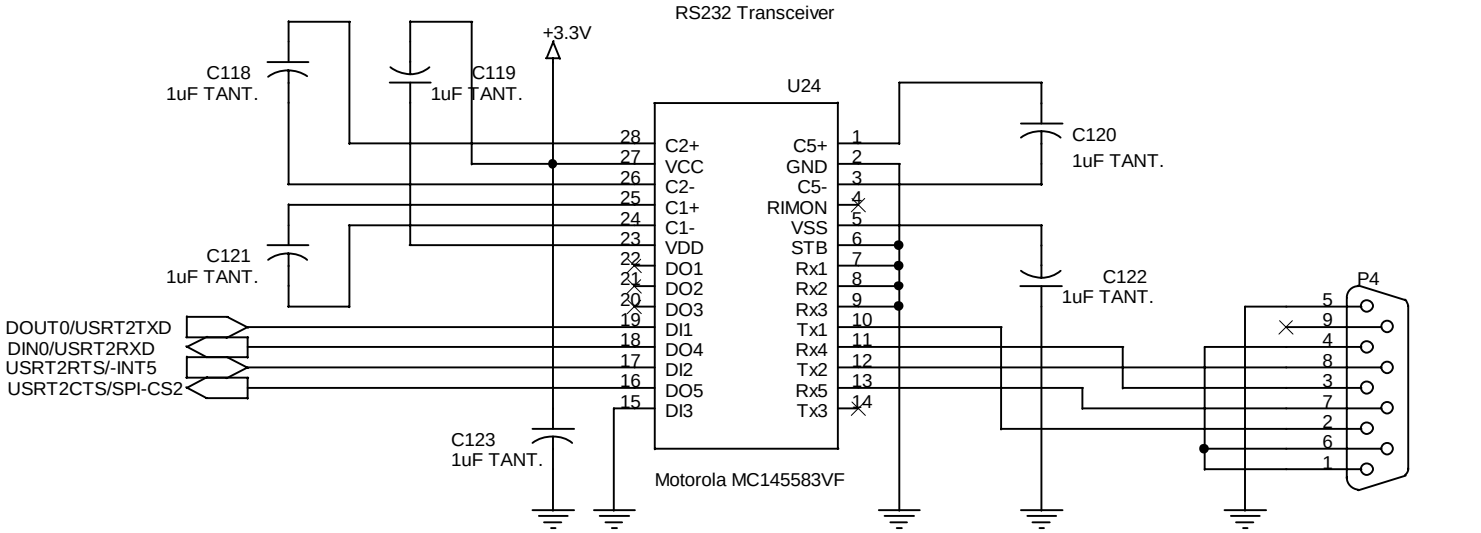


TERMINAL PORT
9-WAY D-TYPE
(Female)



AUXILARY PORT
9-WAY D-TYPE (Female)

MOTOROLA SPS SESG - HESD ColdFire Group		
Title M5272C3 Evaluation Board		
Size A	Document Number MCF5272 - Serial Ports	Rev 1.4
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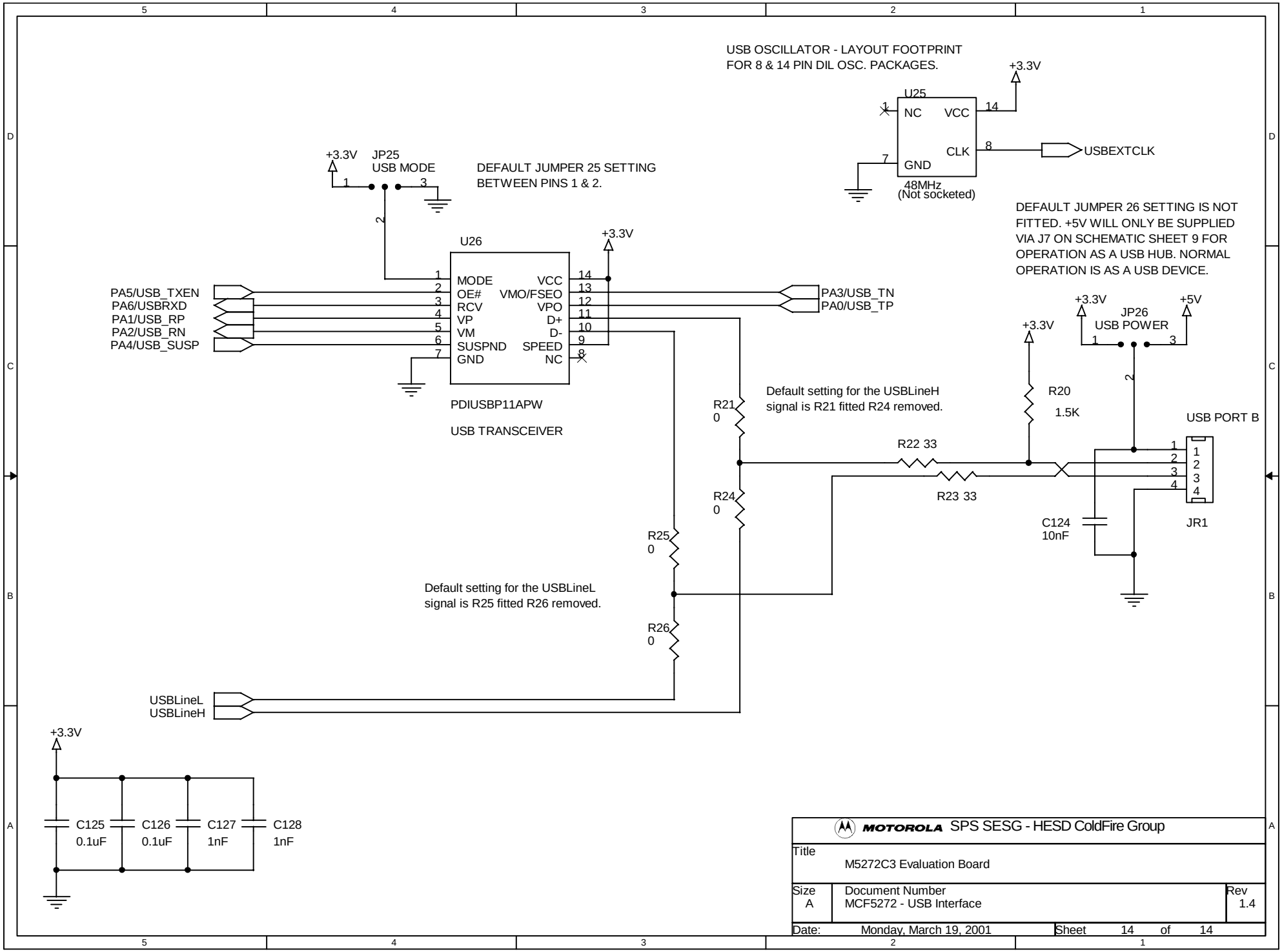
USB OSCILLATOR - LAYOUT FOOTPRINT
FOR 8 & 14 PIN DIL OSC. PACKAGES.
+3.3V
U25
NC
VCC
CLK
GND
USBEXTCLK
48MHz
(Not socketed)
+3.3V
JP25
USB MODE
DEFAULT JUMPER 25 SETTING
BETWEEN PINS 1 & 2.
DEFAULT JUMPER 26 SETTING IS NOT
FITTED. +5V WILL ONLY BE SUPPLIED
VIA J7 ON SCHEMATIC SHEET 9 FOR
OPERATION AS A USB HUB. NORMAL
OPERATION IS AS A USB DEVICE.
U26
+3.3V
MODE
OE#
RCV
VP
VM
SUSPND
GND
VCC
VMO/FSEO
VPO
D+
D-
SPEED
NC
PA5/USB_TXEN
PA6/USBRXD
PA1/USB_RP
PA2/USB_RN
PA4/USB_SUSP
PA3/USB_TN
PA0/USB_TP
PDIUSBP11APW
USB TRANSCEIVER
+3.3V
JP26
USB POWER
+5V
+3.3V
R20
1.5K
USB PORT B
R21
0
Default setting for the USBLineH
signal is R21 fitted R24 removed.
R22 33
R23 33
R24
0
C124
10nF
JR1
R25
0
Default setting for the USBLineL
signal is R25 fitted R26 removed.
R26
0
USBLineL
USBLineH
+3.3V
C125
0.1uF
C126
0.1uF
C127
1nF
C128
1nF
MOTOROLA SPS SESG - HESD ColdFire Group
Title
M5272C3 Evaluation Board
Size
A
Document Number
MCF5272 - USB Interface
Rev
1.4
Date: Monday, March 19, 2001
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