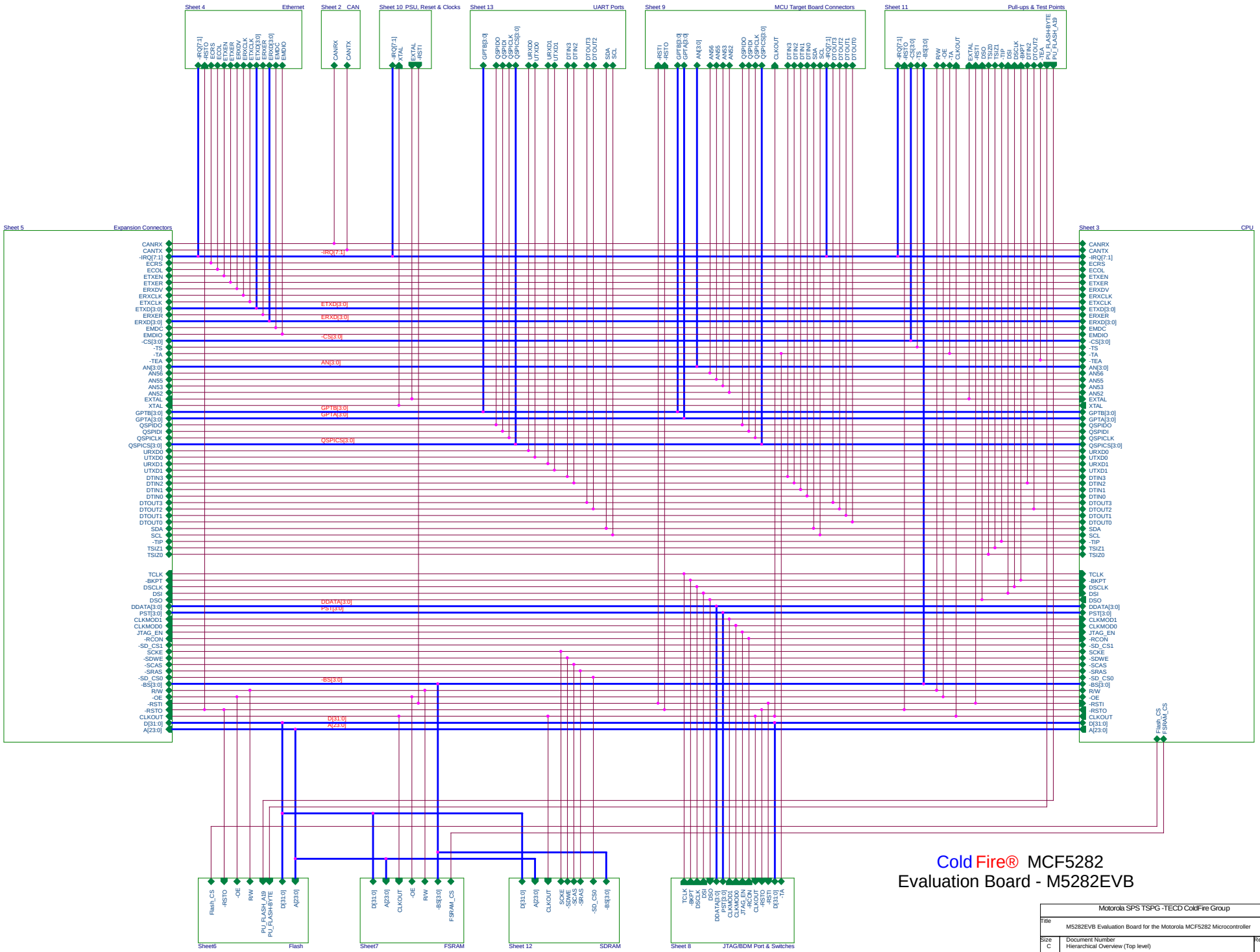

Cold Fire® MCF5282
Evaluation Board - M5282EVB

Motorola SPS TSPG -TECD ColdFire Group		
Title	M5282EVB Evaluation Board for the Motorola MCF5282 Microcontroller	
Size C	Document Number Hierarchical Overview (Top level)	Rev 1.0
Date: Tuesday, November 12, 2002	Sheet 1 of 13	

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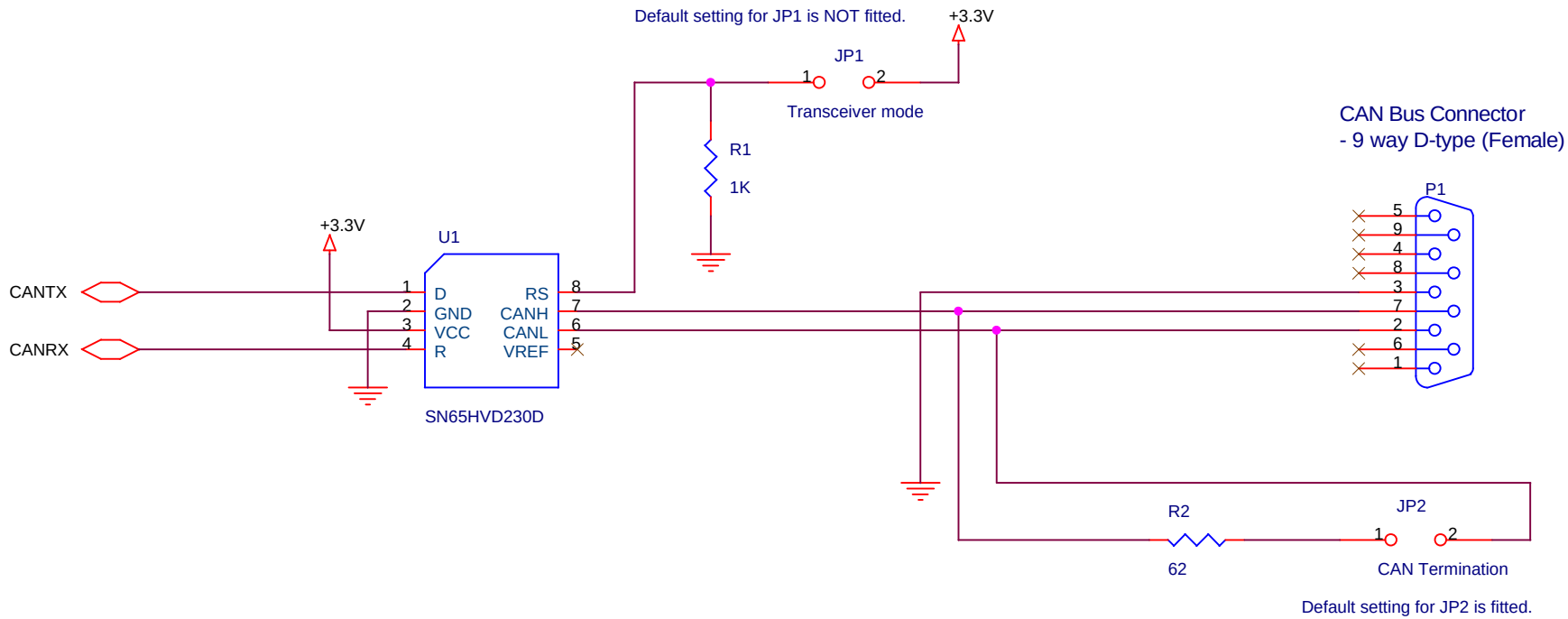

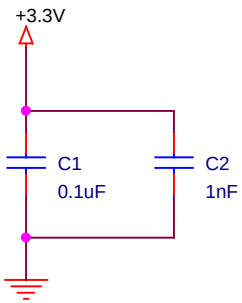

Motorola SPS TSPG -TECD ColdFire Group		
Title M5282EVB Evaluation Board for the Motorola MCF5282 Microcontroller		
Size A	Document Number CAN Transceiver/Connector	Rev 1.0
Date: Tuesday, November 12, 2002	Sheet 2 of 13	

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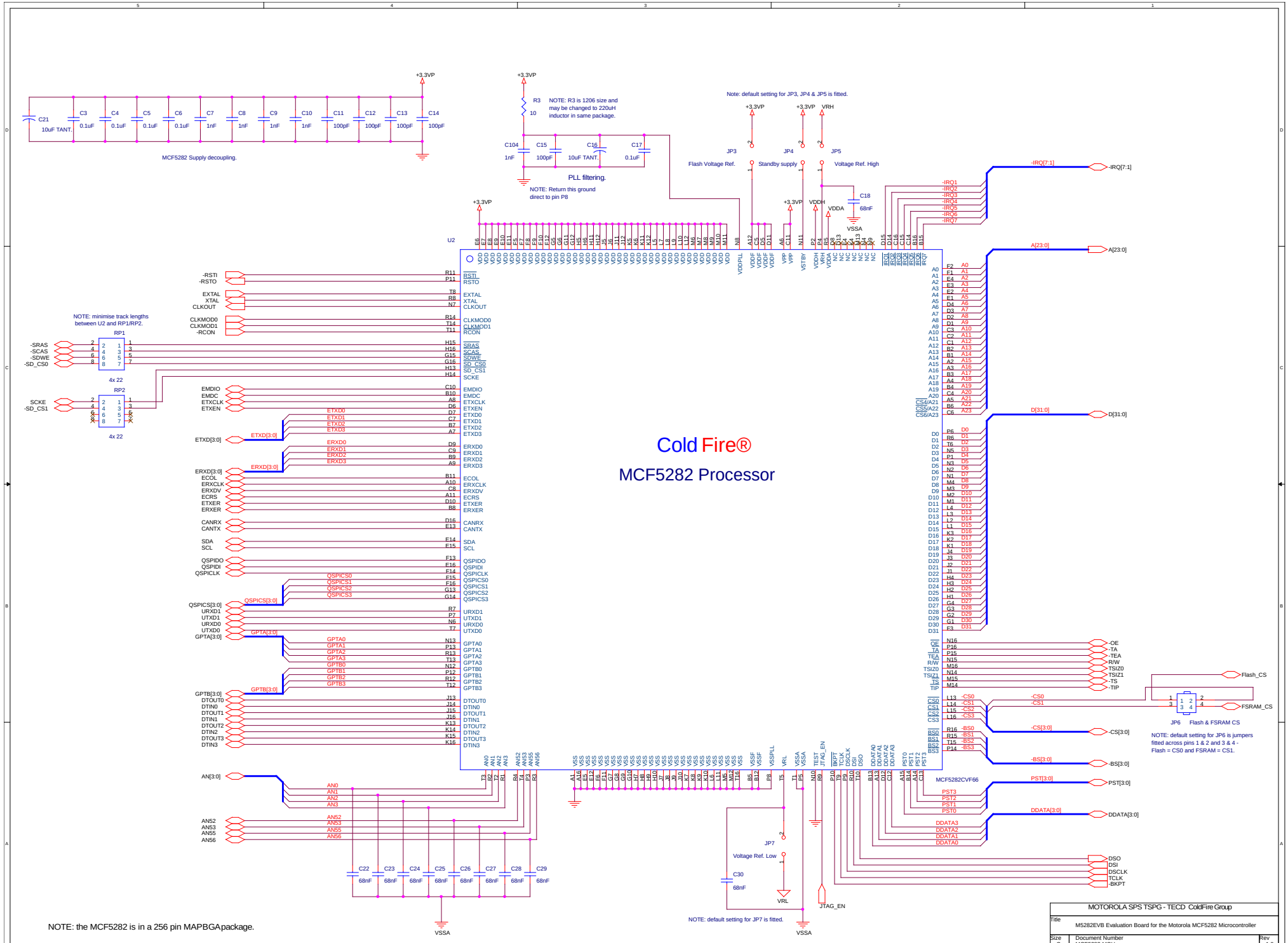

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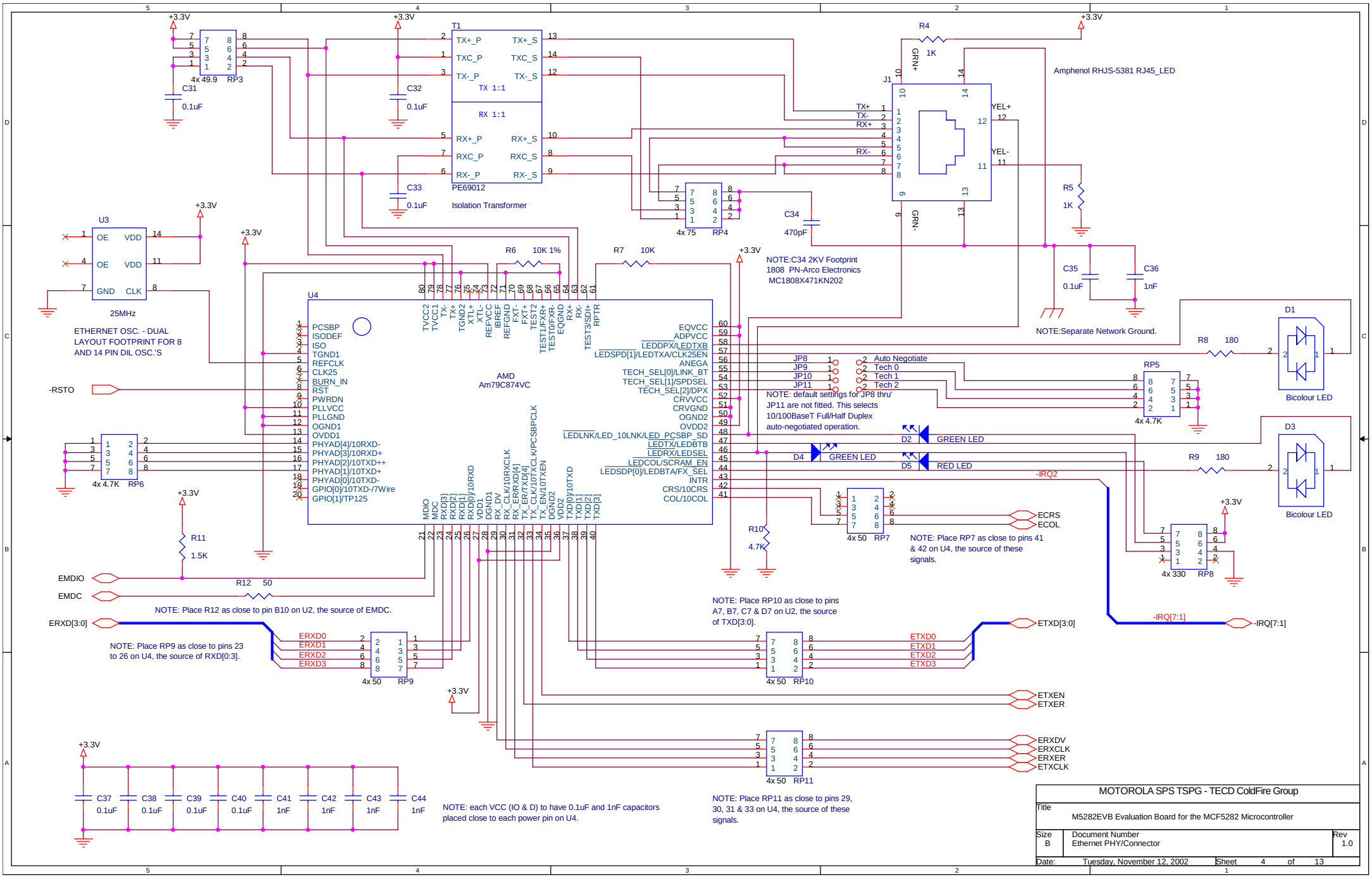

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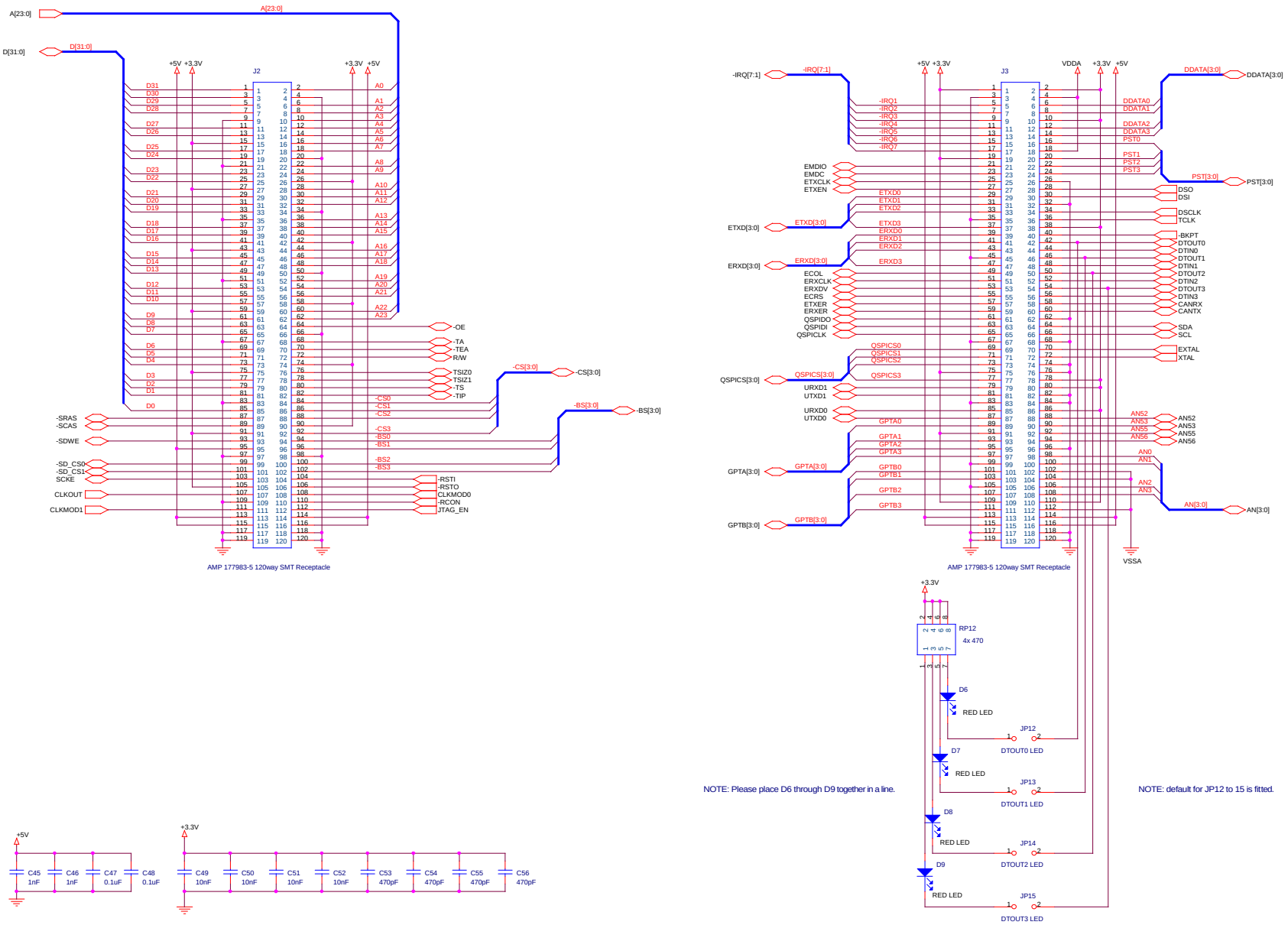
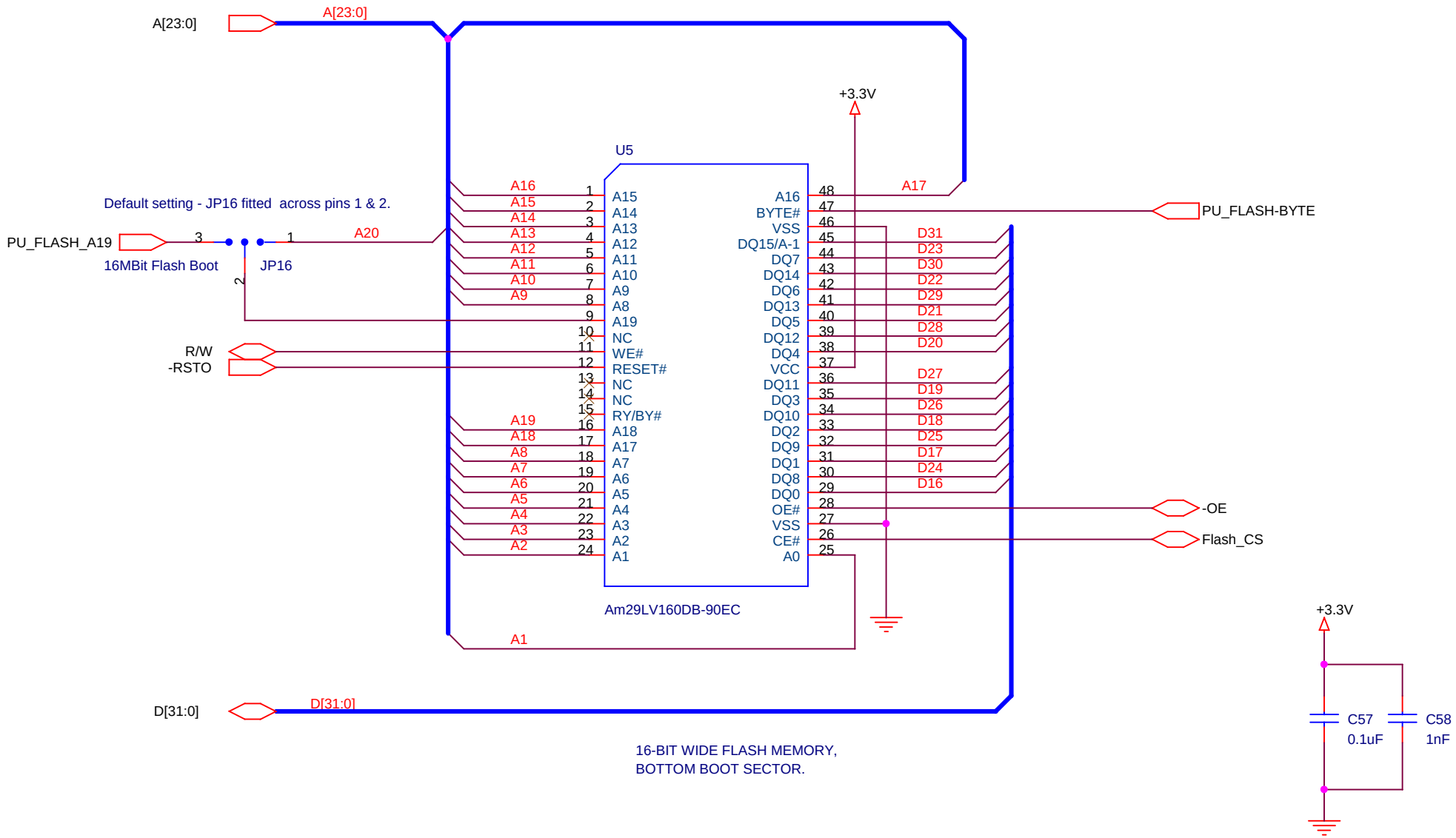


NOTE: Please place D6 through D9 together in a line.

NOTE: default for JP12 to 15 is fitted.

MOTOROLA SPS TSPG -TECD ColdFire Group	
Title	M5282EVB Evaluation Board for the Motorola MCF5282 Microcontroller
Size C	Document Number: Expansion Connectors
Rev	1.0
Date: Tuesday, November 12, 2002	Sheet 5 of 13

PDF created with FinePrint pdfFactory trial version http://www.fineprint.com



MOTOROLA SPS TSPG - TECD ColdFir e Group		
Title: M5282EVB Evaluation Board for the Motorola MCF5282 Microcontroller		
Size: A	Document Number: Flash Memory	Rev: 1.0
Date: Tuesday, November 12, 2002	Sheet 6 of 13	

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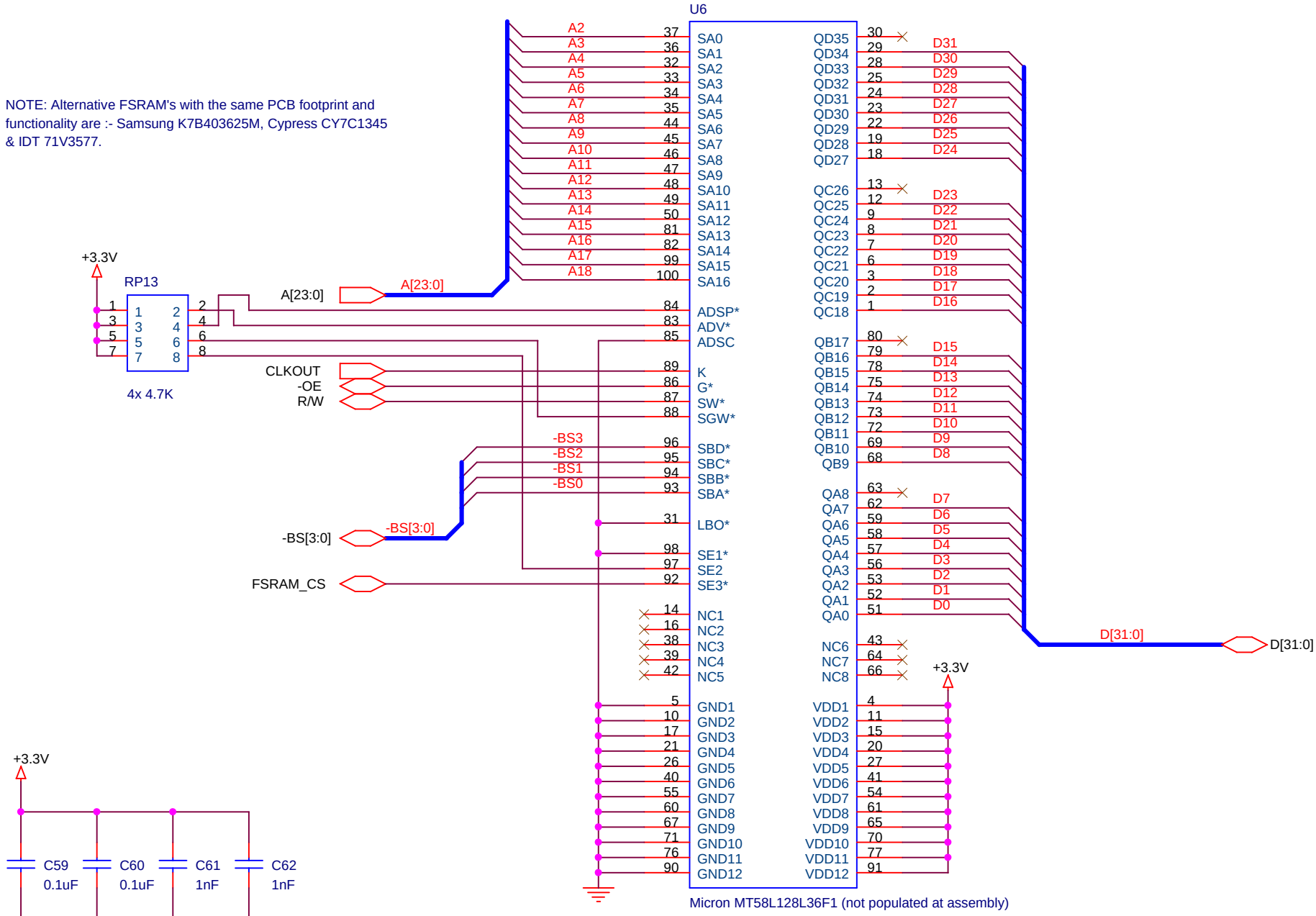

MOTOROLA SPS TSPG - TECD ColdFire Group		
Title: M5282EVB Evalution Board for the Motorola MCF5282 Microcontroller		
Size: A	Document Number: Static RAM	Rev: 1.0
Date: Tuesday, November 12, 2002	Sheet 7 of 13	

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OFF - SW1 - ON		
Chip Config. Off	1	Chip Config. On
JTAG Interface Enabled	2	BDM Interface Enabled
Encoded Clock Mode	3	Encoded Clock Mode
Encoded Clock Mode	4	Encoded Clock Mode
Encoded Oper. Mode	5	Encoded Oper. Mode
Encoded Oper. Mode	6	Encoded Oper. Mode
Encoded Oper. Mode	7	Encoded Oper. Mode
Encoded Boot Device	8	Encoded Boot Device
Encoded Boot Device	9	Encoded Boot Device
Partial Bus Drive	10	Full Bus Drive
Encoded Address Mode	11	Encoded Address Mode
Encoded Address Mode	12	Encoded Address Mode

Encoded Clock Mode

SW1-3	SW1-4	Mode
OFF	OFF	External Clock - (No PLL)
OFF	ON	1:1 PLL
ON	OFF	Normal PLL operation (Ext. Clock)
ON	ON	Normal PLL operation (Ext. Crystal)

Encoded Operating Mode

SW1-5	SW1-6	SW1-7	Mode
OFF	X	X	Reserved
ON	OFF	ON	Reserved
ON	OFF	OFF	Factory Test
ON	ON	OFF	Single Chip
ON	ON	ON	Master

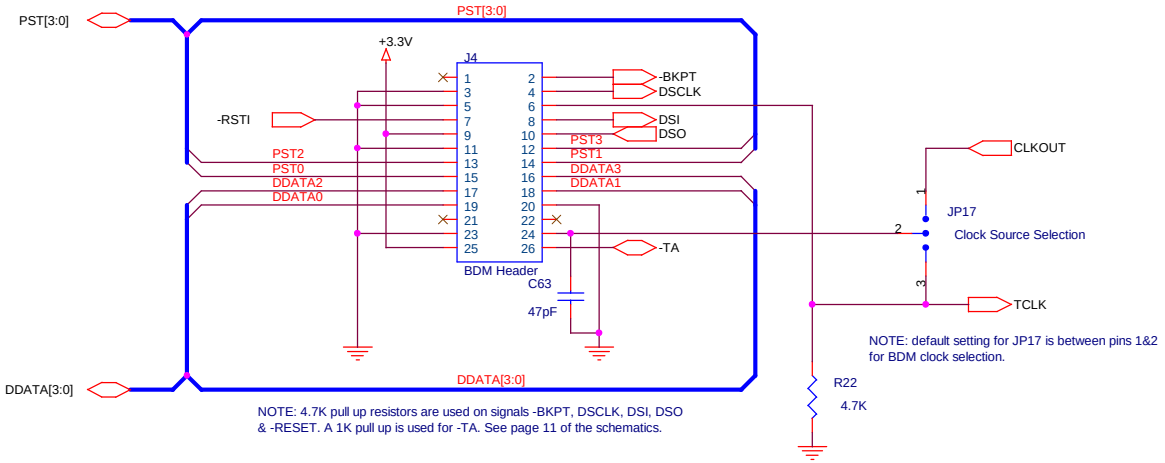
Encoded Boot Device (Port Size)

SW1-8	SW1-9	Mode
OFF	OFF	Internal (32-bit)
OFF	ON	External (16-bit)
ON	OFF	External (8-bit)
ON	ON	External (32-bit)

Encoded Address/Chip Select Mode

SW1-11	SW1-12	Mode
OFF	OFF	PF[7:5] = -CS[6:4]
OFF	ON	PF7 = -CS6, PF[6:5] = A[22:21]
ON	OFF	PF[7:6] = -CS[6:5], PF[5] = A21
ON	ON	PF[7:5] = A[23:21]

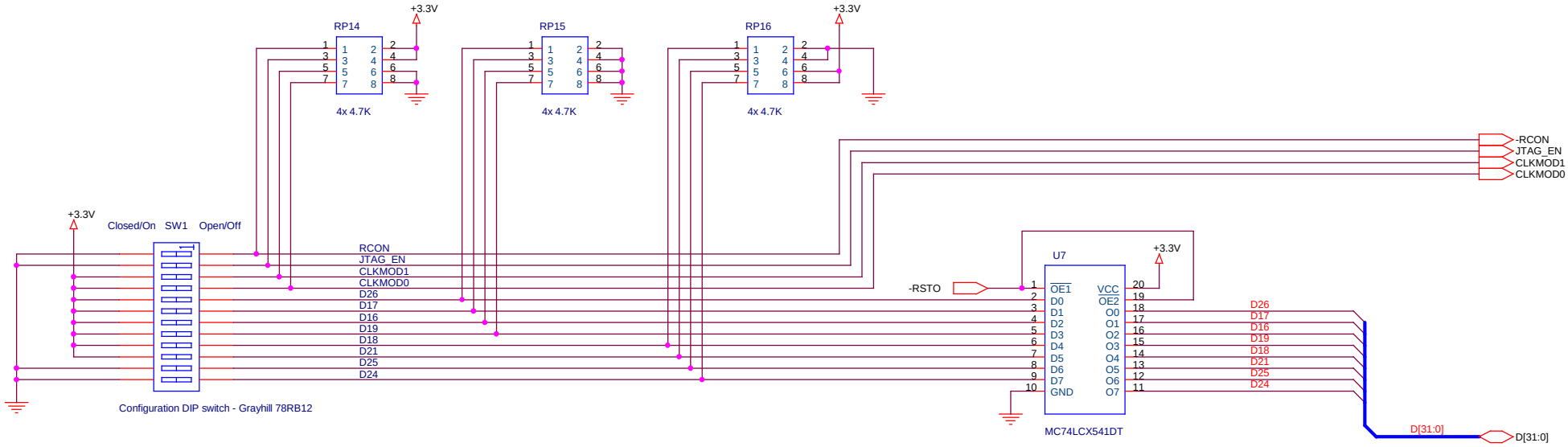
NOTE: Please place these tables on the silkscreen on the topside of the PCB close to SW1.



NOTE: default setting for JP17 is between pins 1&2 for BDM clock selection.

NOTE: 4.7K pull up resistors are used on signals -BKPT, DSCLK, DSI, DSO & -RESET. A 1K pull up is used for -TA. See page 11 of the schematics.

IMPORTANT NOTE: ONLY a 3.3V BDM debugging cable can be used with the MCF5282 processor.



Configuration DIP switch - Grayhill 78RB12

IMPORTANT NOTE: THE -RSTO SIGNAL MUST BE USED TO DRIVE THE OUTPUT ENABLE PINS OF U7 TO ALLOW THE D16, D17, D18, D19, D21, D24, D25 & D26 SIGNALS TO BE LATCHED CORRECTLY BY THE MCF5282 FOR CONFIGURATION AT RESET.

MOTOROLA SPS TSPG - TECD ColdFire Group		
Title	M5282EVB Evaluation Board for the Motorola MCF5282 Microcontroller	
Size B	Document Number BDM/JTAG Header and Chip Configuration.	Rev 1.0
Date: Tuesday, November 12, 2002	Sheet 8 of 13	

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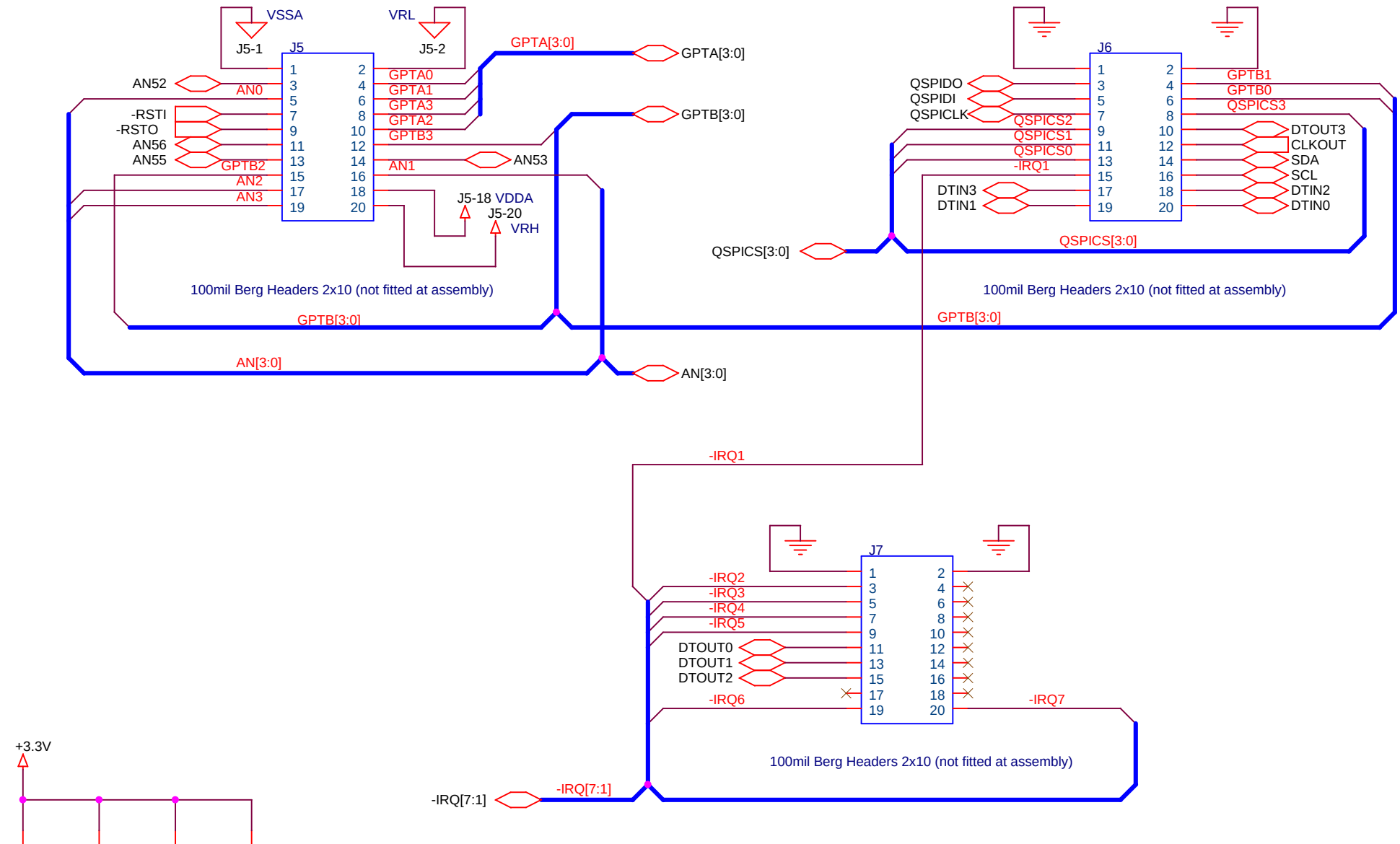

MOTOROLA SPS TSPG - TECD ColdFir e Group

Title
M5282EVB Evaluation Board for the Motorola MCF5282 Microcontroller

Size	Document Number	Rev
A	MCF5282 - Module Headers	1.0

Date: Tuesday, November 12, 2002 Sheet 9 of 13

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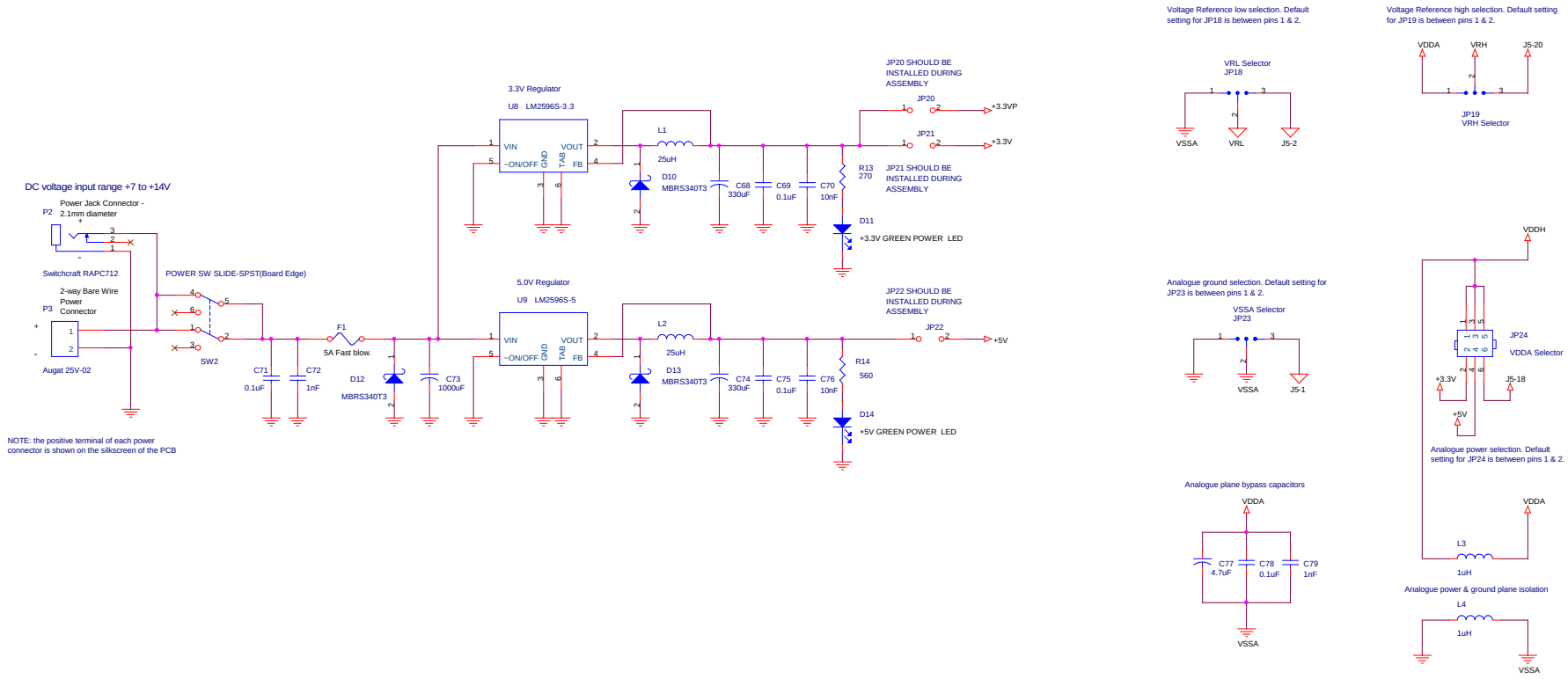
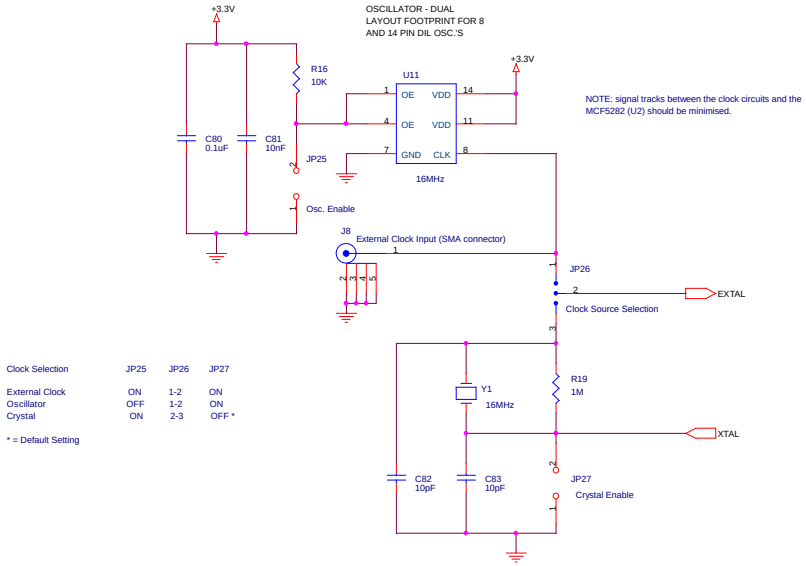
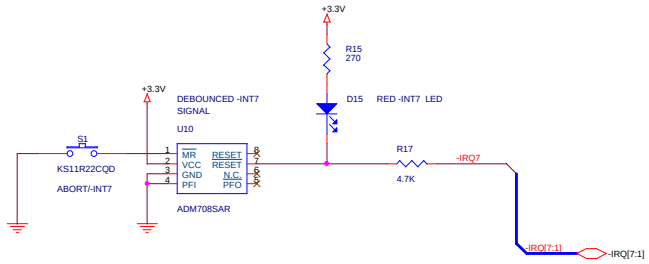
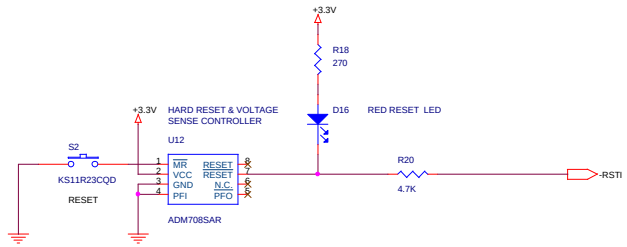




Clock Selection	JP25	JP26	JP27
External Clock	ON	1-2	ON
Oscillator	OFF	1-2	ON
Crystal	ON	2-3	OFF *

* = Default Setting





MOTORLA SPS TSPG - TECD ColdFire Group		
Title: M5282EVB Evaluation Board for the Motorola MCF5282 Microcontroller		
Size: C	Document Number: Power Supplies, Clocks and Reset/Abort Switches.	Rev: 1.0
Date: Tuesday, November 12, 2002	Sheet 10 of 13	

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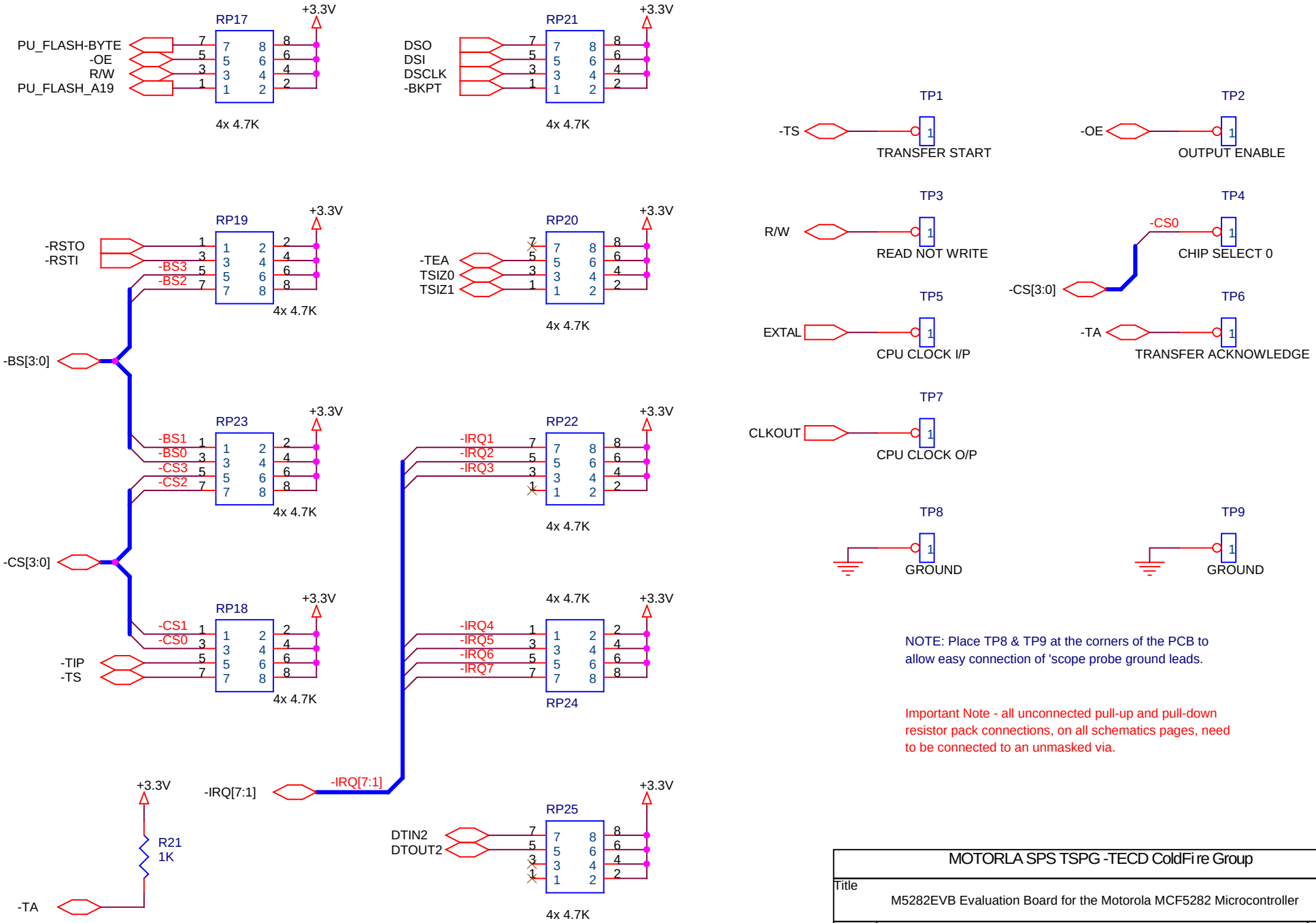

NOTE: Place TP8 & TP9 at the corners of the PCB to allow easy connection of 'scope probe ground leads.

Important Note - all unconnected pull-up and pull-down resistor pack connections, on all schematics pages, need to be connected to an unmasked via.

MOTORLA SPS TSPG -TECD ColdFi re Group		
Title: M5282EVB Evaluation Board for the Motorola MCF5282 Microcontroller		
Size: A	Document Number: Pull-ups and Test Points.	Rev: 1.0
Date: Tuesday, November 12, 2002	Sheet 11 of 13	

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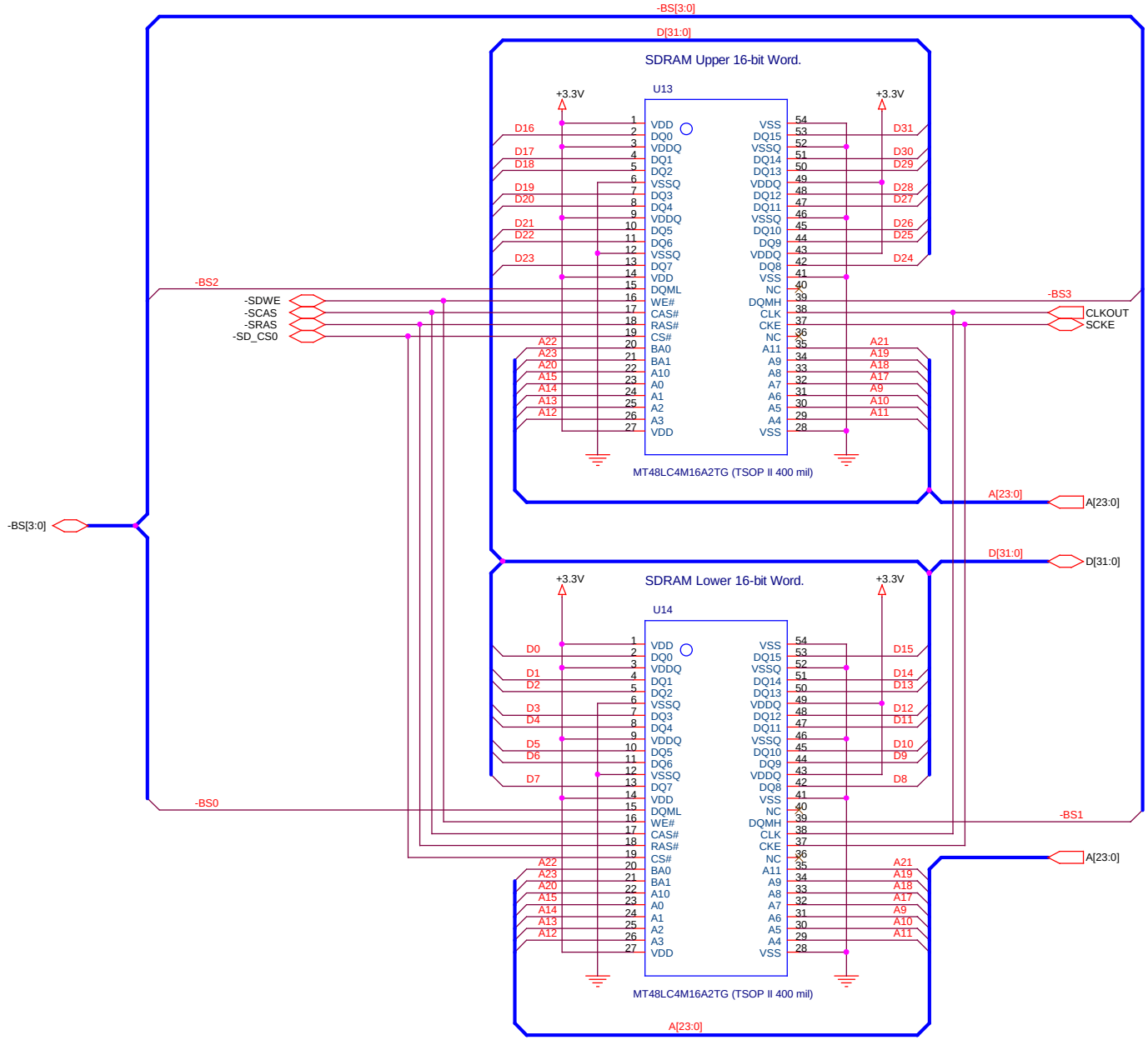

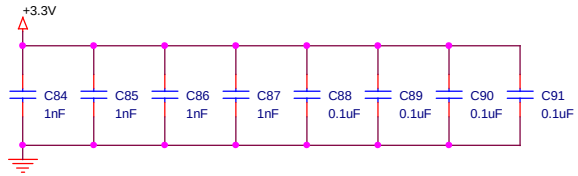

NOTE: Alternative SDRAM's with the same PCB footprint are :

Samsung K4S641632E
Hyundai HY57V641620HG
Toshiba TC59S6416CFT
Infineon HYB39S64160ET
Winbond W986416DH

MOTOROLA SPS TSPG - TECD ColdFire Group		
Title: M5282EVB Evaluation Board for the Motorola MCF5282 Microcontroller		
Size: B	Document Number: Synchronous DRAM	Rev: 1.0
Date: Tuesday, November 12, 2002	Sheet 12 of 13	

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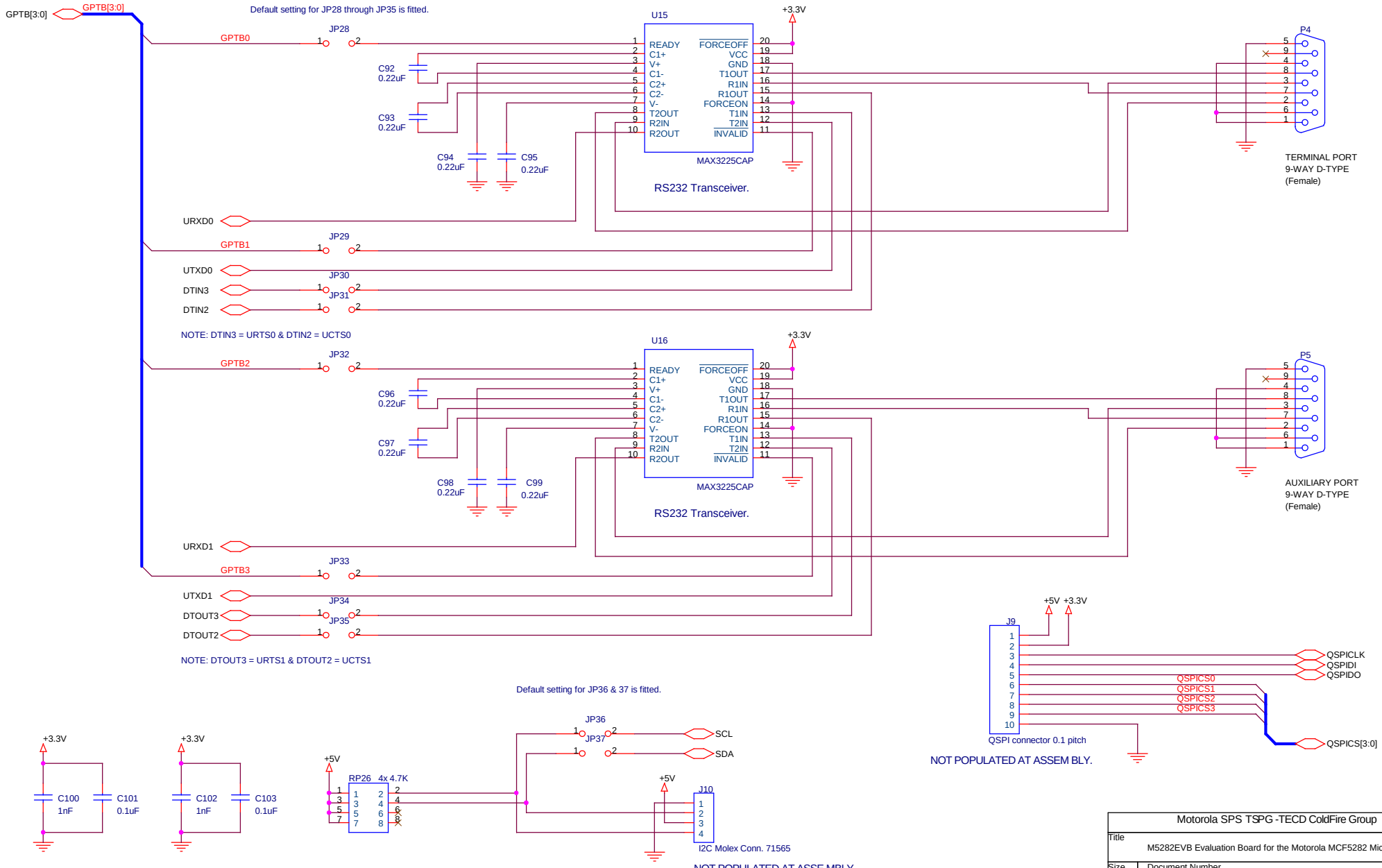

Motorola SPS TSPG -TECD ColdFire Group		
Title: M5282EVB Evaluation Board for the Motorola MCF5282 Microcontroller		
Size: B	Document Number: UART Transceivers/Connectors	Rev: 1.0
Date: Tuesday, November 12, 2002	Sheet 13 of 13	

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