Audio board 2

Contents

Revision history and contents	1
System block diagram	2
Power block diagram	3
ADC preamplifier	4
ADC codec	5
ADC power supply	6
DAC amplifier ch1-8	7
DAC amplifier ch9-16	8
DAC amplifier ch17-24	9
DAC codec 1	10
DAC codec 2	11
DAC codec 3	12
DAC power supply	13
Wireless subwoofer (BLE)	14
Ethernet PHY	15
SPDT & SD card slot & mFI	16
M.2 & PCIE clock	17
SPDIF	18
IMX HDMI	19
HDMI card & EXP	20
USB type-c	21
DSI interface	22
Level shifter for IMX	23
Remote debug	24
Remote debug isalation	25
DAC buffer	26
CPLD jtag	27
CPLD 1	28
CPLD 2	29
CPLD 3	30
B2B for 865	31
B2B for 845 & 815	32
Main power	33
Analog power	34
Digital power	35
IMX boot setting	36
IOMUX tabel 1	37
IOMUX tabel 2	38

Revision	Date	Changes
c	20191204	First release
c1	20200513	1. change C340 from 0.1uF to 0.22uF 2. change C2949,C2944,C3001 from 0.01uF to 0.22uF 3. change J2524 from TSW-102-07-T-S to b2b-xh-a 4. change R3157,R2820 and R452 from 100R to 1k 5. change R3146 from 100R to 10k 6. change U48 from PCA9617ADP to PCA9509ADP for better compatibility of HDMI monitors, and R185 needs to be populated
d	20200903	1. swap pcie tx and rx signal. 2. change sdio2's spdt switch U2447 part number. 3. add a gpio option for usb_id (only for 865). 4. modify spdif circuit. 5. change fixed hole from non-plated hole to plated hole, and add dnp resistors. 6. dnp U2508 and U2417

Subject to Change without Notice

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

General naming rule is [MASTER]_[BUS]_[SIGNAL]_[SLAVE]
>>, << and <<>> indicate the direction of the signal
#, _B or _N means low active
__NET_NAME is a single net, this name only for layout

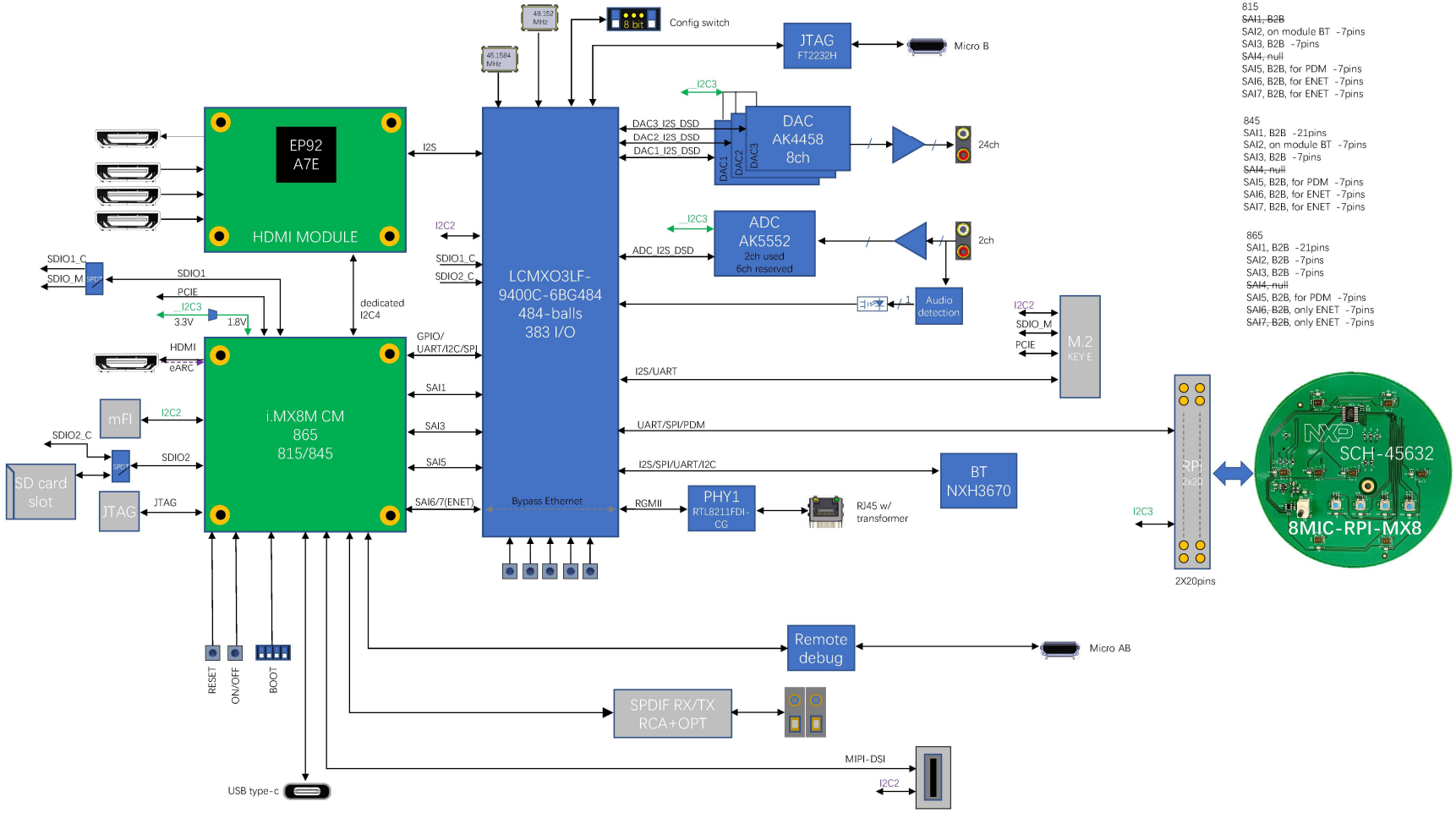
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: Revision and Contents		
Approved:	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 1 of 38	

System Block Diagram



815
~~SAI1, B2B~~
SAI2, on module BT -7pins
SAI3, B2B -7pins
~~SAI4, null~~
SAI5, B2B, for PDM -7pins
SAI6, B2B, for ENET -7pins
SAI7, B2B, for ENET -7pins

845
SAI1, B2B -21pins
SAI2, on module BT -7pins
SAI3, B2B -7pins
~~SAI4, null~~
SAI5, B2B, for PDM -7pins
SAI6, B2B, for ENET -7pins
SAI7, B2B, for ENET -7pins

865
SAI1, B2B -21pins
SAI2, B2B -7pins
SAI3, B2B -7pins
~~SAI4, null~~
SAI5, B2B, for PDM -7pins
~~SAI6, B2B~~, only ENET -7pins
~~SAI7, B2B~~, only ENET -7pins

I2C2 Slave table

Slave	PN	Address	Level
PCIE	OSC9FGV0241AKLF	1101 010x	3.3V
CPLD	LCMXO3LF	1000 000x/any	3.3V
CC	PTN5150A	0011 101x	3.3V
MFI	xxx	0001 000x	3.3V
		0001 001x	3.3V
M.2 I/F	xxx	TBD	1.8V
DSI I/F	xxx	TBD	1.8V
IO EXP	PCA6408ABS	0100 000x	1.8V
IO EXP	PCA6416AEV	0100 001x	1.8V

I2C3 Slave table

Slave	PN	Address	Level
ADC	AK5552VN	0010 011x	3.3V
DAC1	AK4458VN	0010 000x	3.3V
DAC2	AK4458VN	0010 010x	3.3V
DAC3	AK4458VN	0010 001x	3.3V
RPI	SCH-45632	0100 001x	3.3V
IO EXP	PCA6416AEV	0100 000x	1.8V

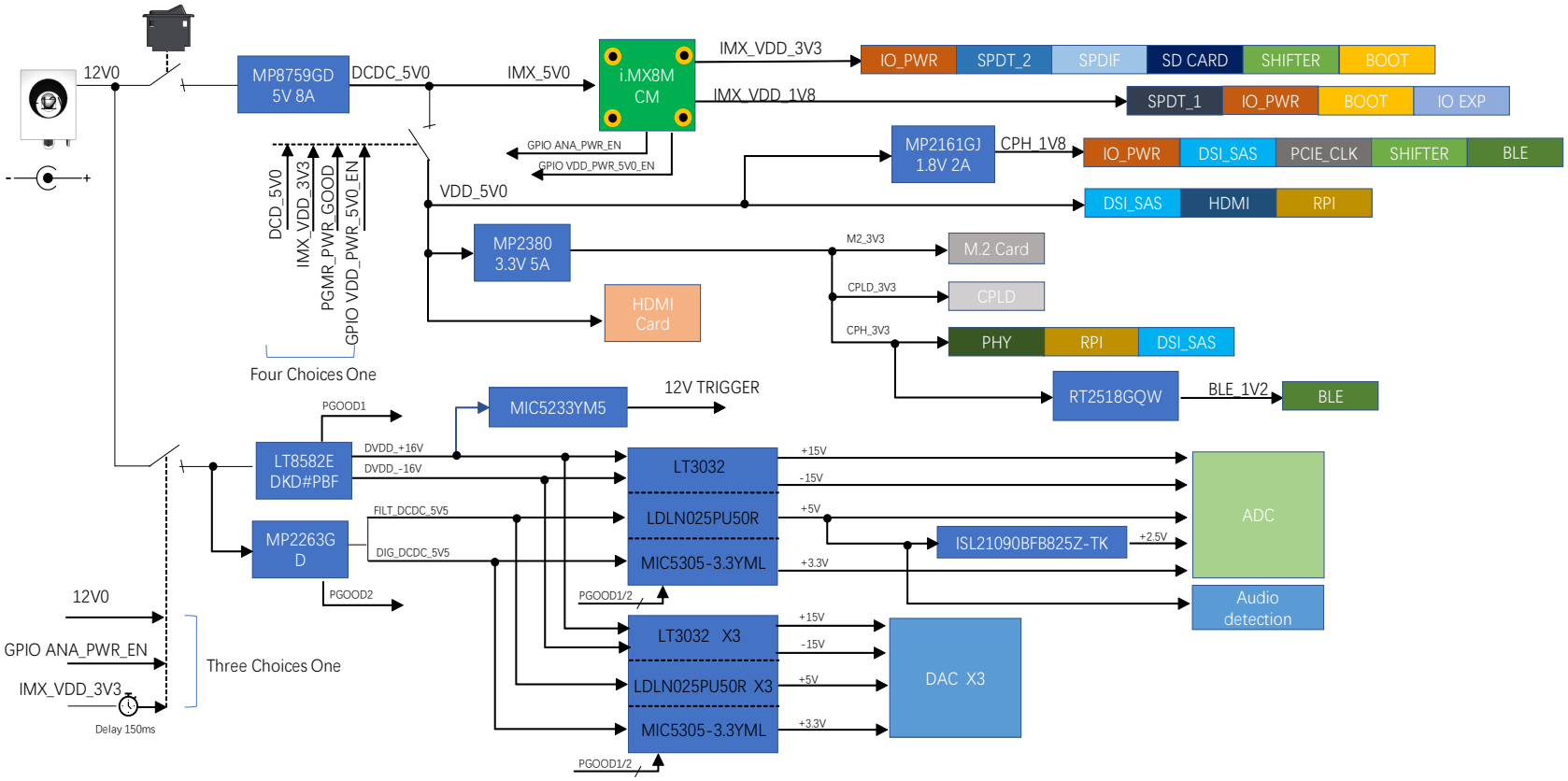
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

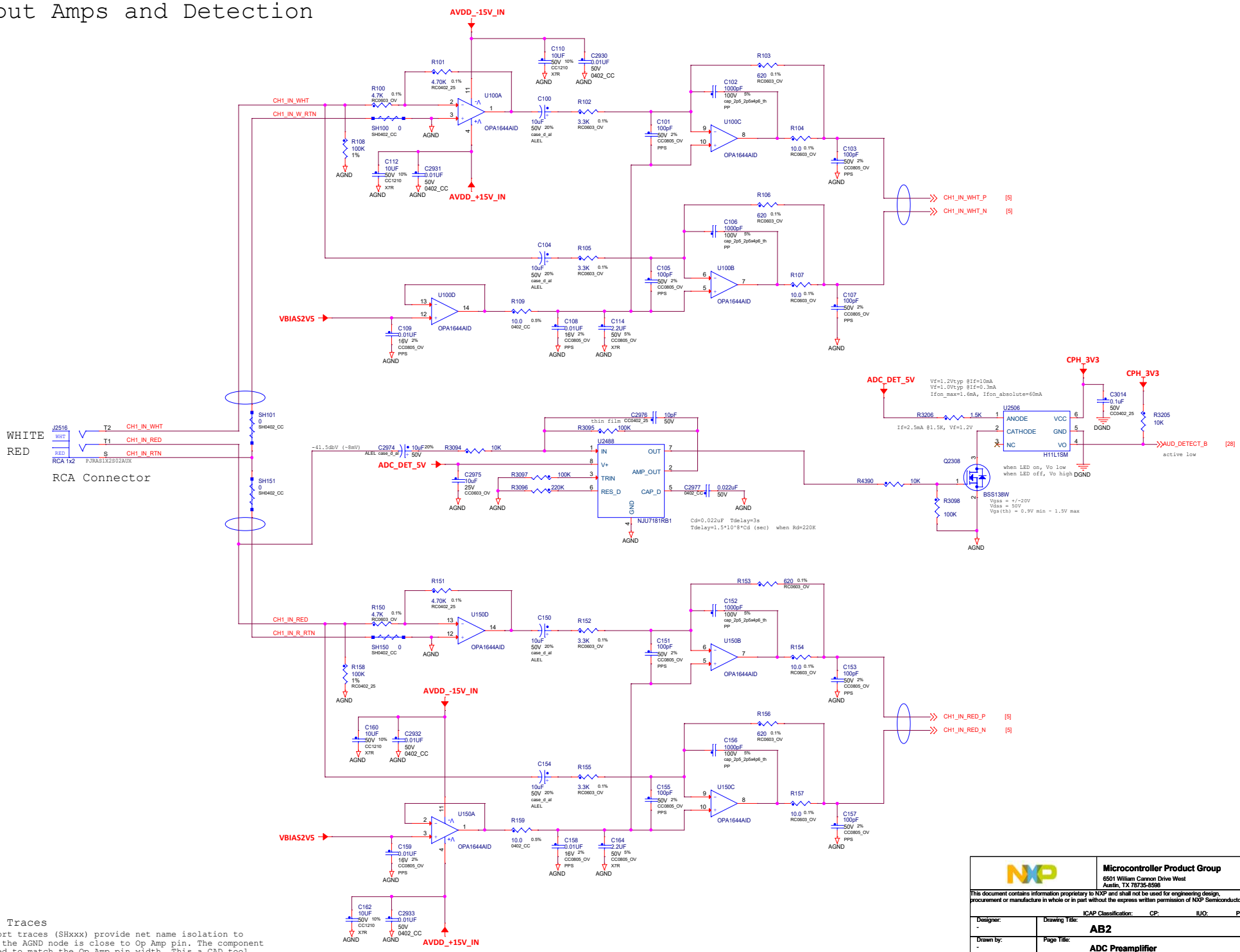
Designer: -	Drawing Title: **AB2**		
Drawn by: -	Page Title: **System Block Diagram**		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 2 of 38	

Power Block Diagram



NXP	**Microcontroller Product Group** 6501 William Cannon Drive West Austin, TX 78735-8598				
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.					
	ICAP Classification:	CP:	IUO:	PUBI:	X
Designer: -	Drawing Title: **AB2**				
Drawn by: -	Page Title: **Power Block Diagram**				
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616			Rev D
	Date: Wednesday, September 09, 2020		Sheet 3 of 38		

Input Amps and Detection



Short Traces

The short traces (SHxxx) provide net name isolation to insure the AGND node is close to Op Amp pin. The component is sized to match the Op Amp pin width. This a CAD tool item not an electrical item.

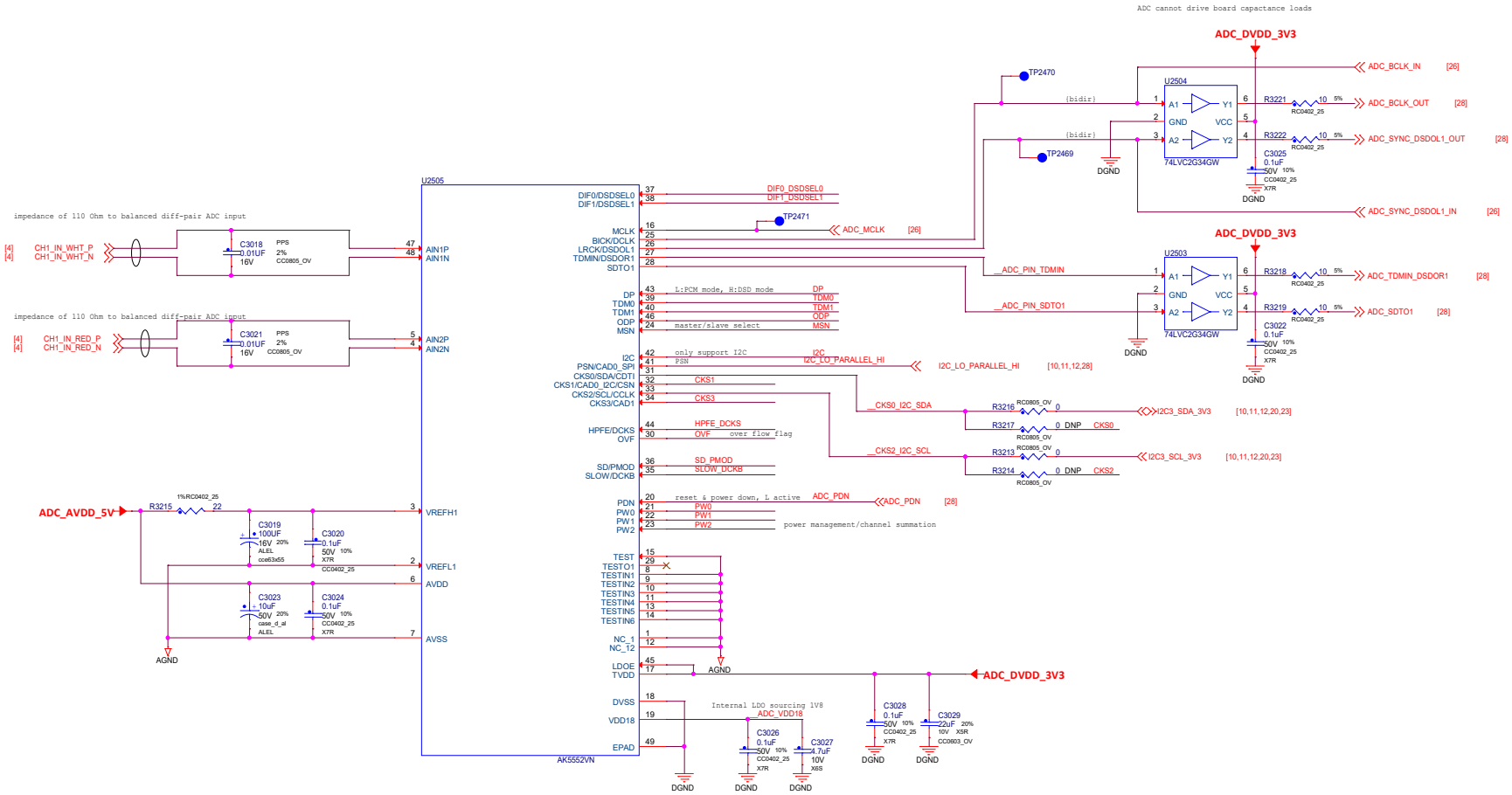
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: **AB2**		
Drawn by: -	Page Title: **ADC Preamplifier**		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 4 of 38	

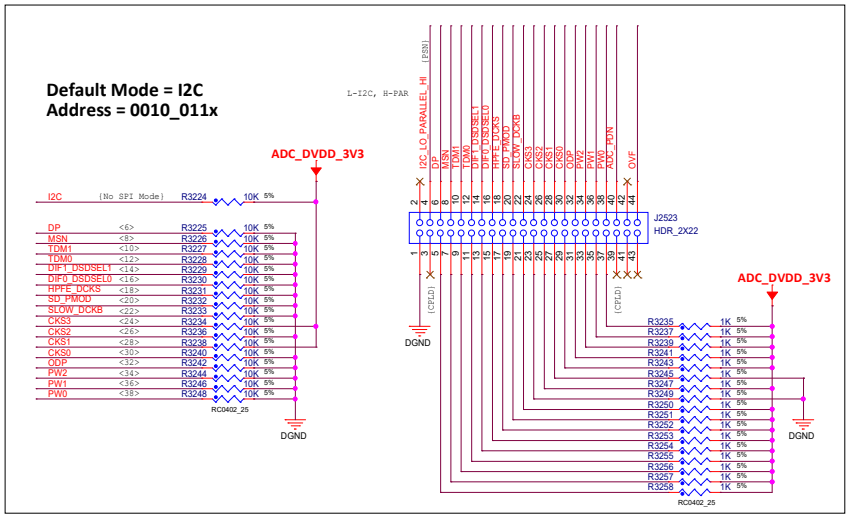
ADC



Optional Ground Plane Short

If installed, shorts under DACs should also be installed

Optional Configuration Header ADC



Output Format:
PCM mode: 24/32 - bit MSB justified, I2S or TDM
DSD mode: DSD Native 64, 128, 256

Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management1	PW8	PW7	PW6	PW5	PW4	PW3	PW2	PW1
01H	Power Management2	0	0	0	0	0	MONO2	MONO1	RSTN
02H	Control 1	0	CKS3	CKS2	CKS1	CKS0	DIF1	DIF0	HPFE
03H	Control 2	0	TDM1	TDM0	0	0	0	0	0
04H	Control 3	DP	0	0	0	0	0	SD	SLOW
05H	DSD	0	0	DCKS	0	PMOD	DCKB	DSDSEL1	DSDSEL0
06H	TEST1	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0
07H	TEST2	0	0	0	0	0	0	0	TRST

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

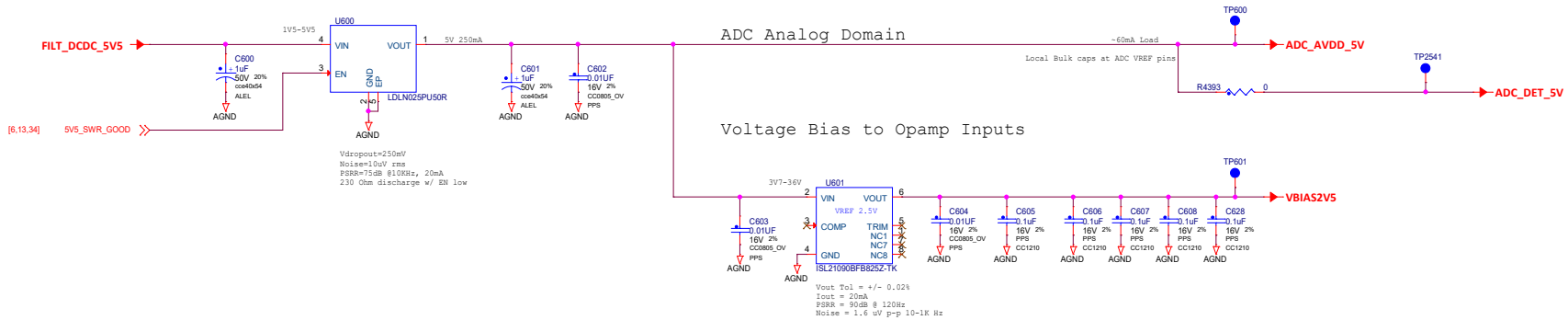
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

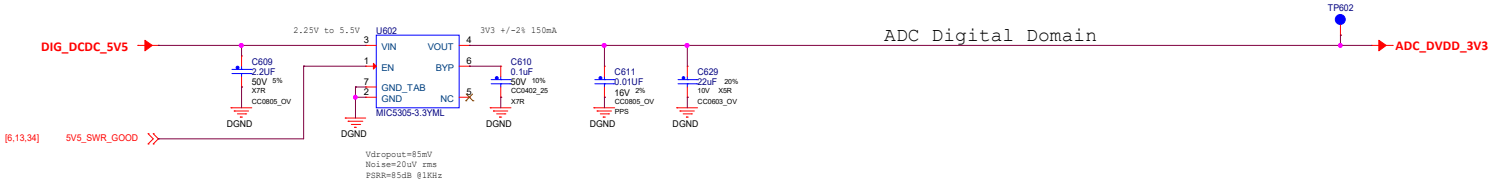
ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: ADC		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 5 of 38	

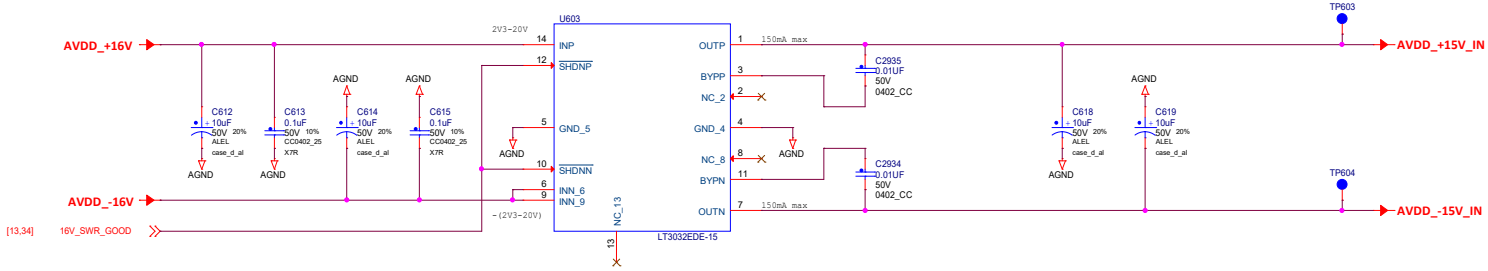
Audio Line In
Power Supplies

ADC Reference Voltages



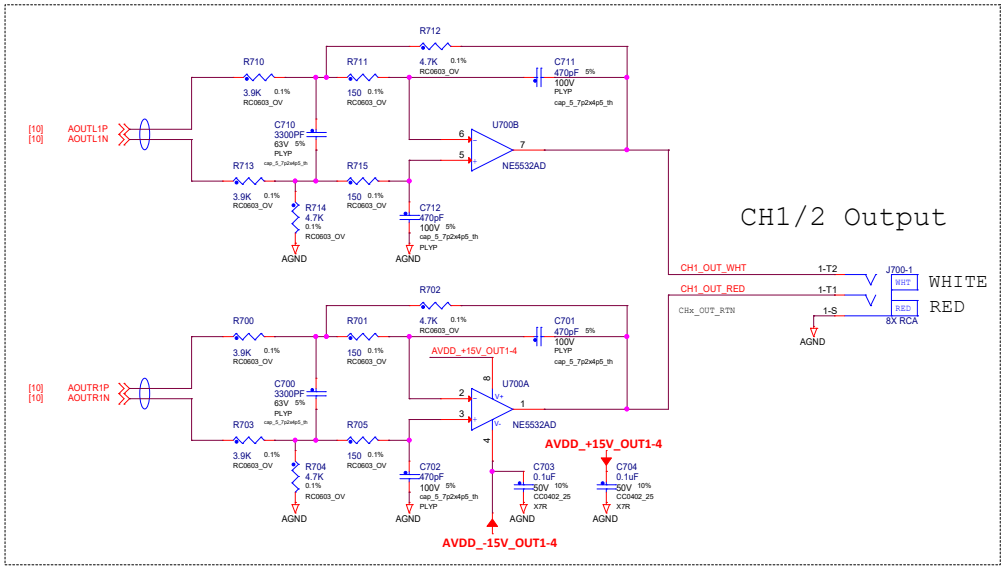


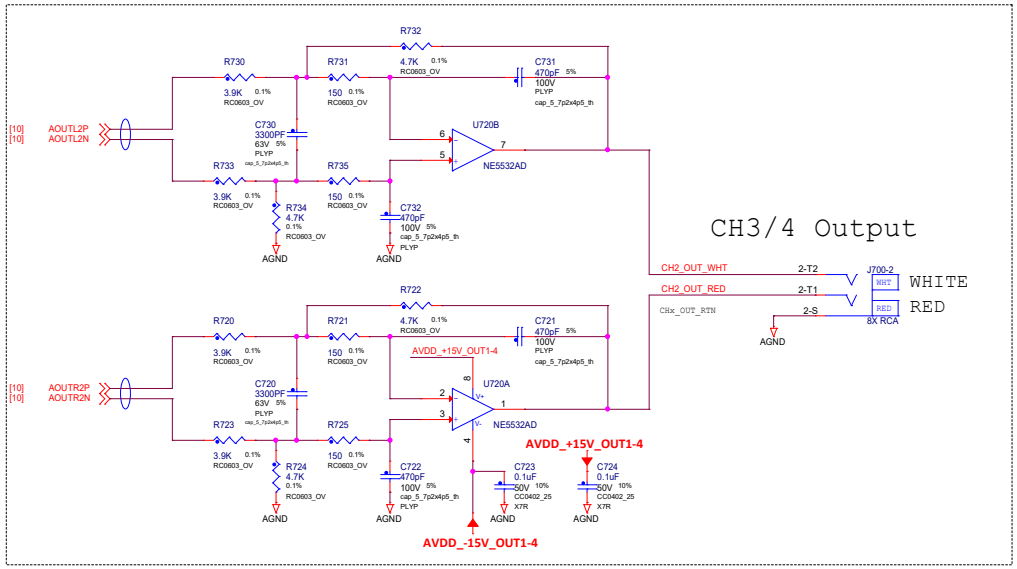
OpAmp +/- 15V Supply
OpAmps @ ~10-15mA each

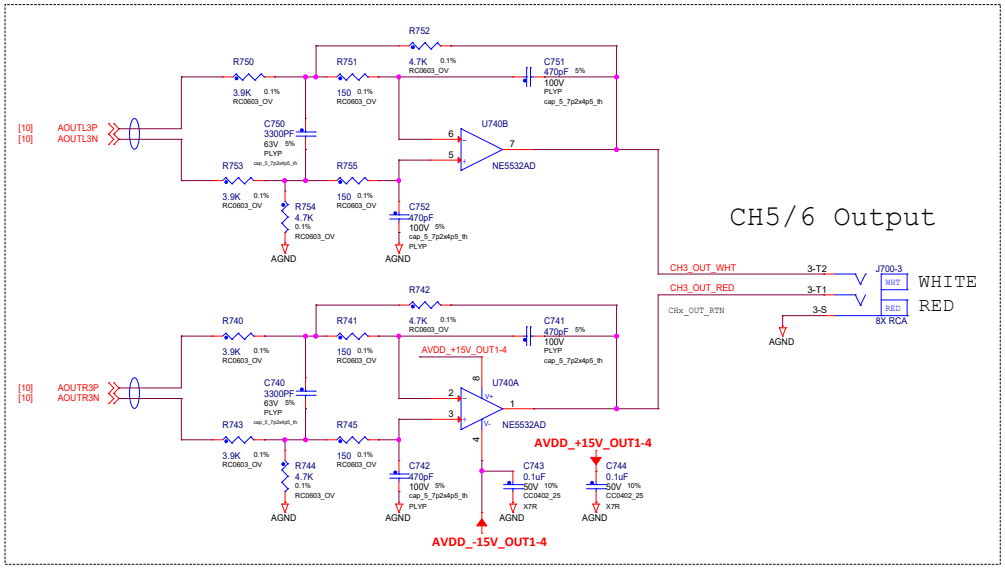


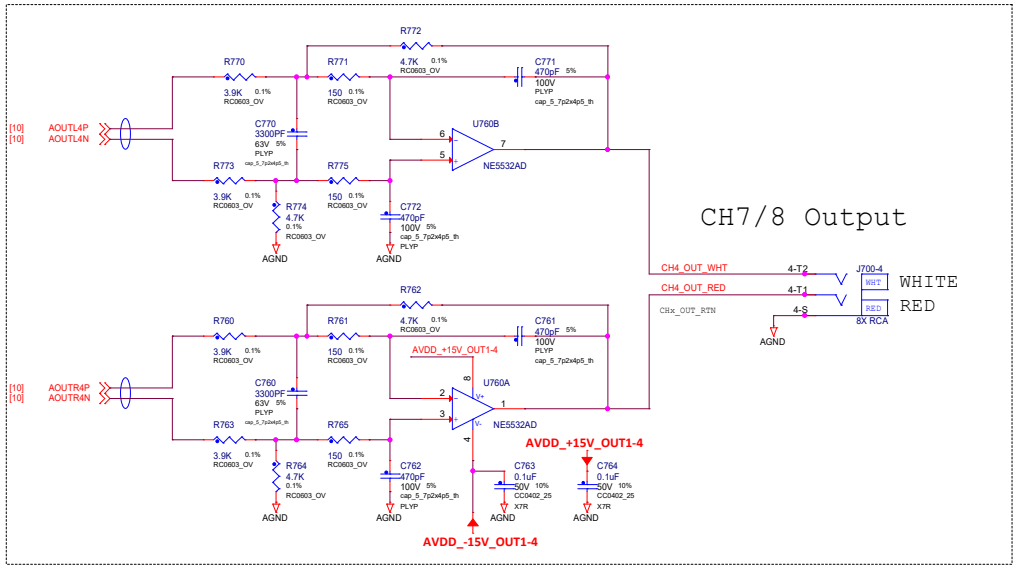
NXP	**Microcontroller Product Group** 6501 William Cannon Drive West Austin, TX 78735-8598		
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.			
	ICAP Classification: CP: IUO: PUBI: X		
Designer: -	Drawing Title: **AB2**		
Drawn by: -	Page Title: **ADC Power Supply**		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 6 of 38	

Output Amps - DAC 1 of 3
8 Channels per DAC
Output Channels 1 through 8
4x(R/L) Channels









The output circuit employs differential version of the MFB (Multi Feed Back) active filter. MFB is chosen since it has better attenuation characteristics at higher frequency to avoid aliasing.

Corner frequency (Fc), gain, Q and other transfer functions shown below. calculation uses CH1 output diagram and component references:

Gain = 20*log(Rf/Ri) = 20*log(4.7k/3.9k) = +1.621dB where Rf is R702 and Ri is R700

fc = 1/(2*pi*sqrt((2*C700)*C701*R701*R702)) = approx. 108kHz
C700 value is doubled since this MFB filter is a differential topology as opposed to the single ended implementation

Q = sqrt((2*C700)*C701*R702*R701)/(R702*C701 + R701*C701 + R701*C701*(-R702/R700)) = 0.673

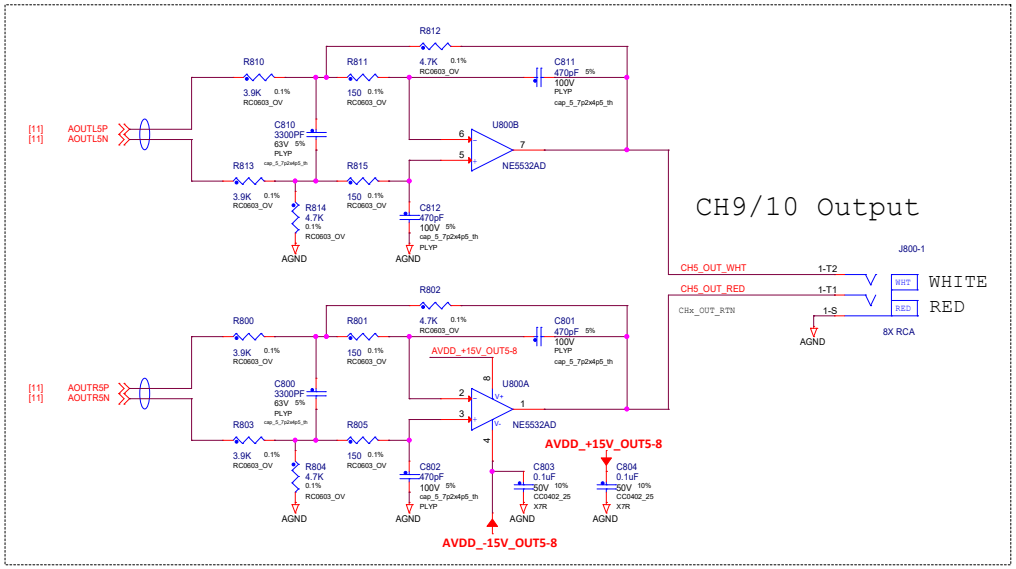
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

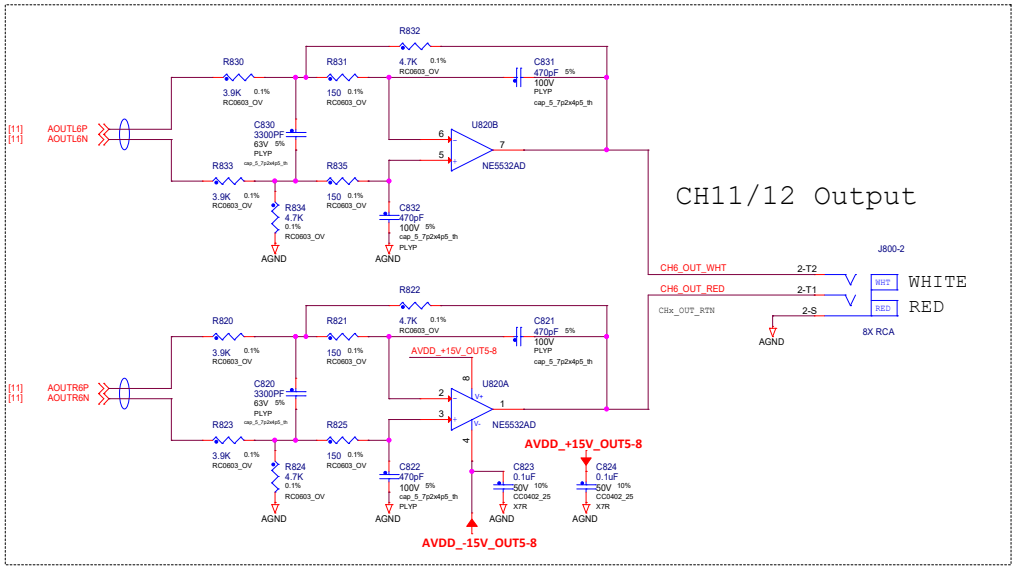
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

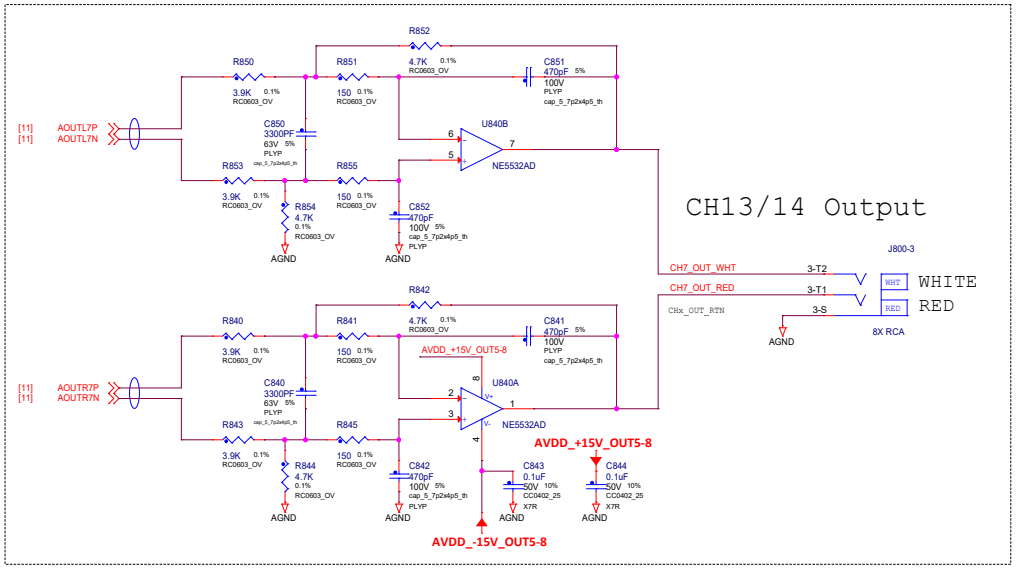
ICAP Classification: CP: IUO: PUBI: X

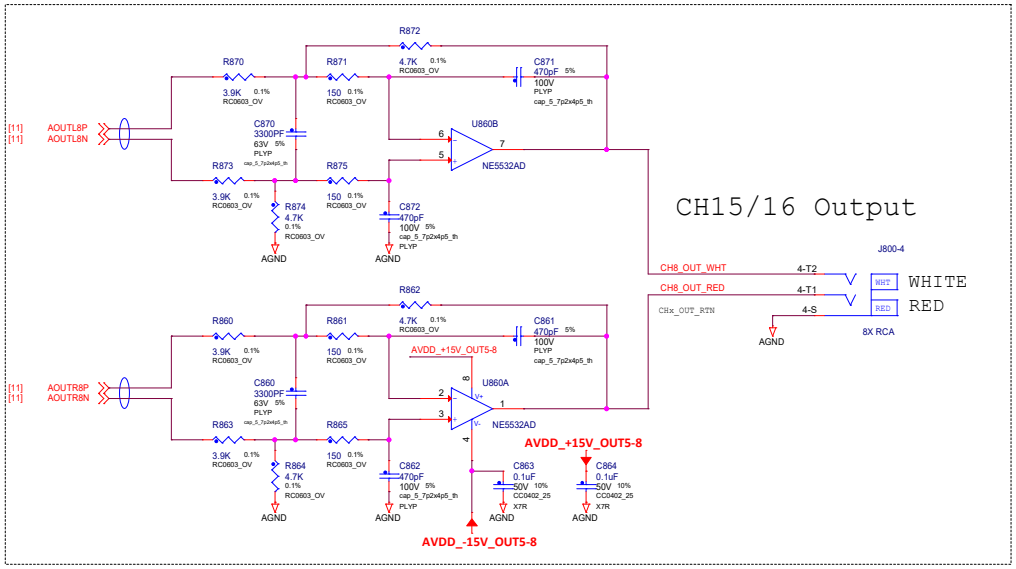
Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: DAC Amplifier CH1-8		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 7 of 38	

Output Amps - DAC 2 of 3
8 Channels per DAC
Output Channels 9 through 16
4x(R/L) Channels



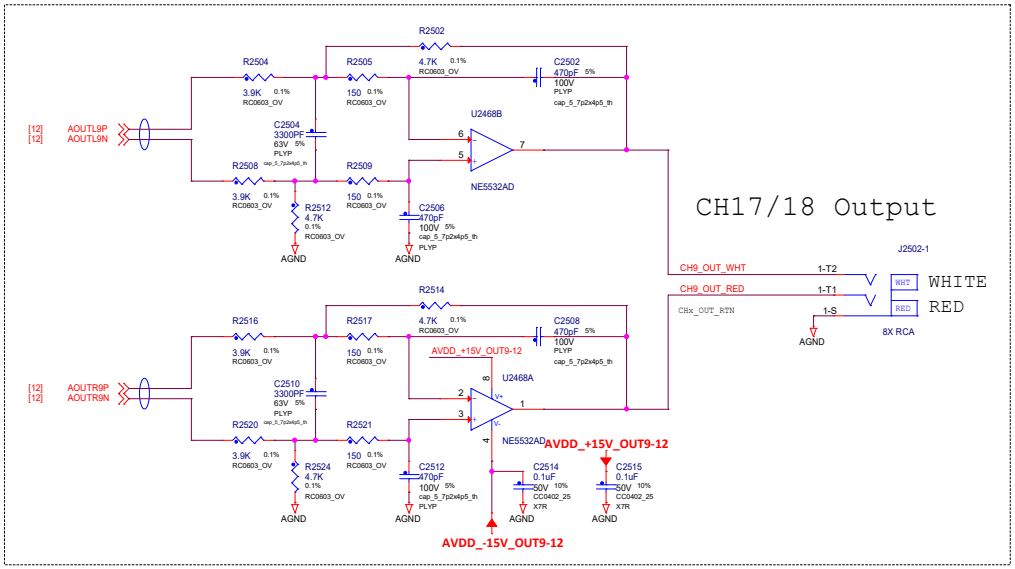


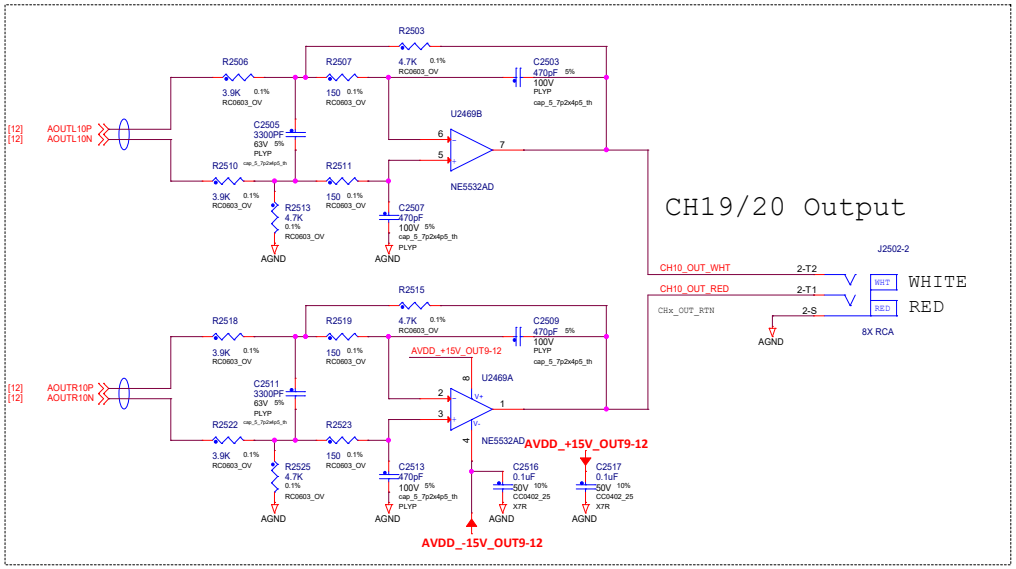


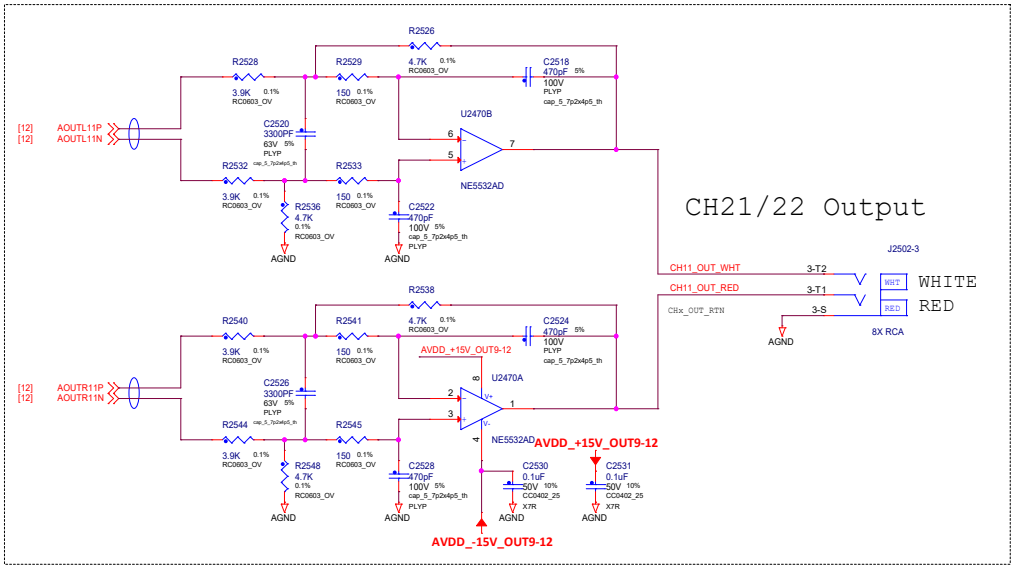


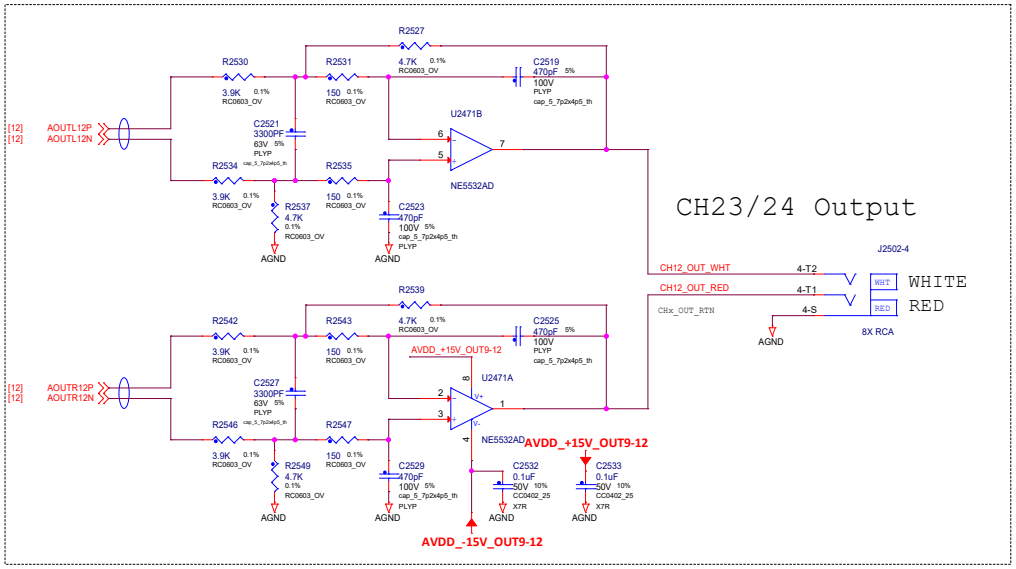
NXP	**Microcontroller Product Group** 6501 William Cannon Drive West Austin, TX 78735-8598		
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.			
	ICAP Classification:	CP:	IUO: PUBI: X
Designer: -	Drawing Title: **AB2**		
Drawn by: -	Page Title: **DAC Amplifier CH9-16**		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 8 of 38	

Output Amps - DAC 3 of 3
8 Channels per DAC
Output Channels 17 through 24
4x(R/L) Channels









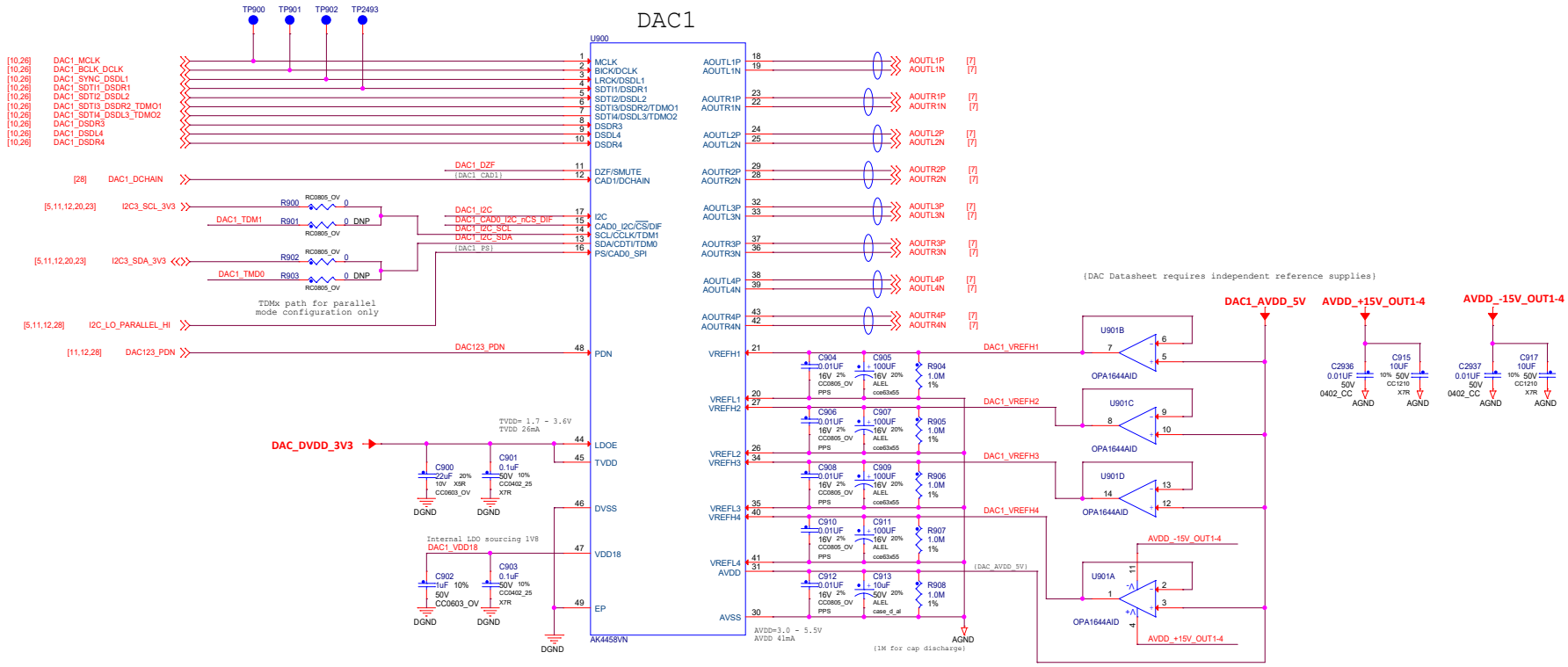
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: **AB2**		
Drawn by: -	Page Title: **DAC Amplifier CH17-24**		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 9 of 38	

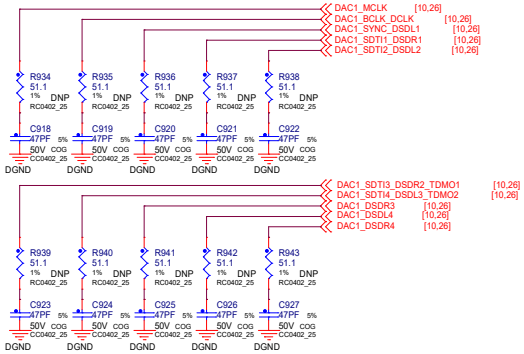
Audio Line Out
DAC 1 of 3



Optional Ground Plane Short

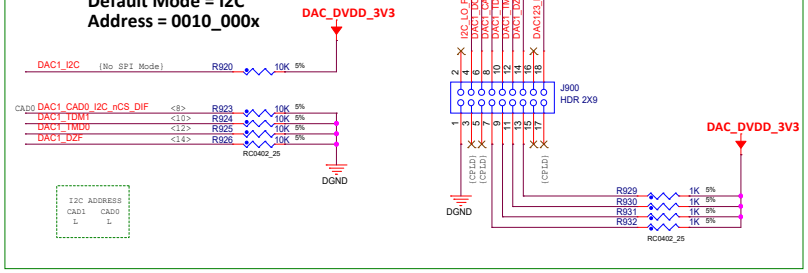
If installed, shorts under DACs should also be installed

Optional Bus Termination



Optional Configuration Header DAC 1

Default Mode = I2C
Address = 0010_000x



Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	0	0	SD	DFS1	DFS0	DEM11	DEM10	SMUTE
02H	Control 3	DP	0	DCKS	DCKB	MONO1	DZFB	SELLR1	SLOW
03H	L1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	R1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	Control 4	INVL1	INVR1	INVL2	INVR2	SELLR2	0	DFS2	SSLOW
06H	DSD1	DDM	DML1	DMR1	DMC	DMRE	0	DSDD	DSDSEL0
07H	Control 5	L3	R3	L4	R4	0	0	1	SYNCE
08H	Sound Control	L1	R1	L2	R2	0	0	SC1SC1	SC0
09H	DSD2	DML2	DMR2	DML3	DMR3	DML4	DMR4	DSDF	DSDSEL1
0AH	Control 6	TDM1	TDM0	SDS1	SDS2	PW2	PW1	DEM 21	DEM20
0BH	Control 7	ATS1	ATS0	0	SDS0	PW4	PW3	DCHAIN	0
0CH	Control 8	INVR4	INVL4	INVR3	INVL3	0	FIR2	FIR1	FIR0
0DH	Control 9	MONO4	MONO3	MONO2	0	SELLR4	SELLR3	0	0
0EH	Control 10	DEM41	DEM40	DEM31	DEM30	0	0	0	0
0FH	L2ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
10H	R2ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
11H	L3ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
12H	R3ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
13H	L4ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
14H	R4ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

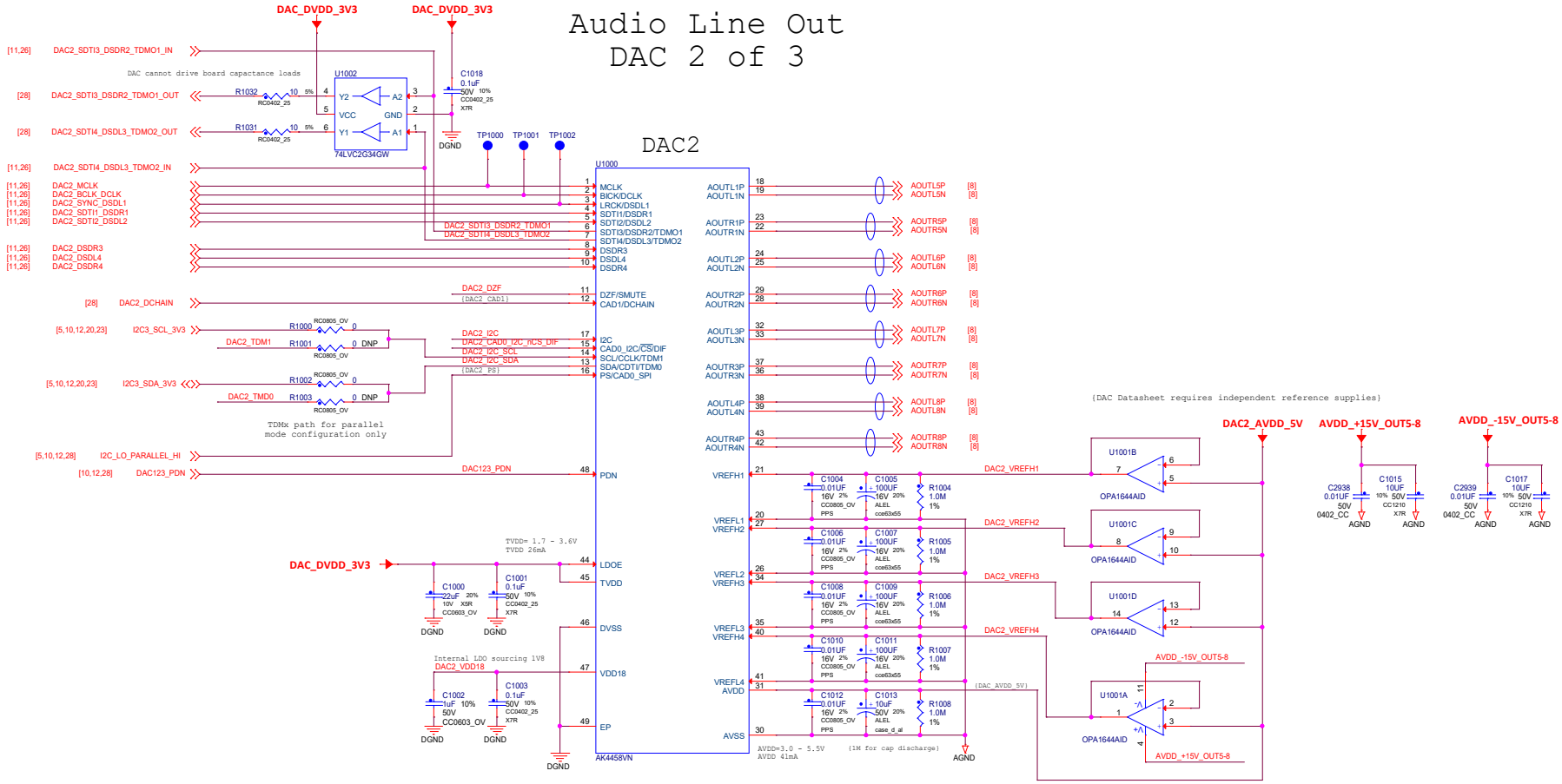
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: DAC 1		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 10 of 38	

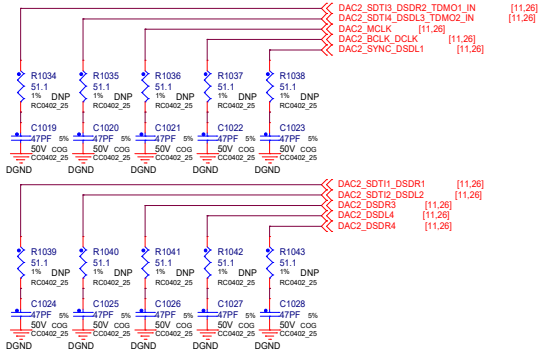
Audio Line Out
DAC 2 of 3



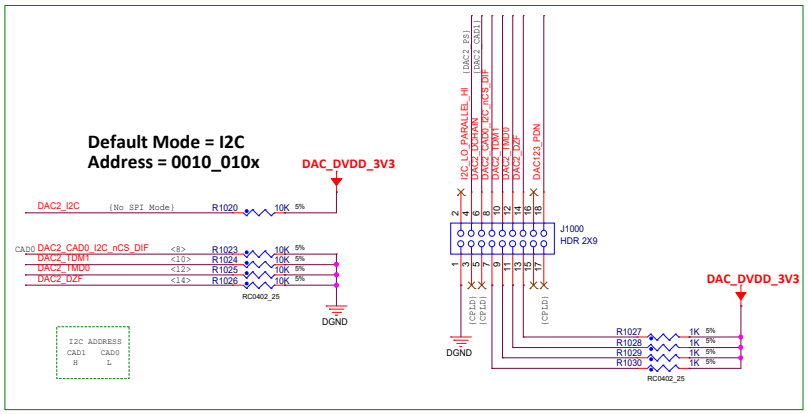
Optional Ground Plane Short

If installed, shorts under DACs should also be installed

Optional Bus Termination



Optional Configuration Header DAC 2



Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	0	0	SD	DFS1	DFS0	DEM11	DEM10	SMUTE
02H	Control 3	DP	0	DCKS	DCKB	MONO1	DZFB	SELLR1	SLOW
03H	L1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	R1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	Control 4	INVL1	INVR1	INVL2	INVR2	SELLR2	0	DFS2	SSLOW
06H	DSD1	DDM	DML1	DMR1	DMC	DMRE	0	DSDD	DSDSEL0
07H	Control 5	L3	R3	L4	R4	0	0	1	SYNCE
08H	Sound Control	L1	R1	L2	R2	0	0	SC1SC1	SC0
09H	DSD2	DML2	DMR2	DML3	DMR3	DML4	DMR4	DSDF	DSDSEL1
0AH	Control 6	TDM1	TDM0	SDS1	SDS2	PW2	PW1	DEM 21	DEM20
0BH	Control 7	ATS1	ATS0	0	SDS0	PW4	PW3	DCHAIN	0
0CH	Control 8	INVR4	INVL4	INVR3	INVL3	0	FIR2	FIR1	FIR0
0DH	Control 9	MONO4	MONO3	MONO2	0	SELLR4	SELLR3	0	0
0EH	Control 10	DEM41	DEM40	DEM31	DEM30	0	0	0	0
0FH	L2ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
10H	R2ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
11H	L3ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
12H	R3ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
13H	L4ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
14H	R4ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

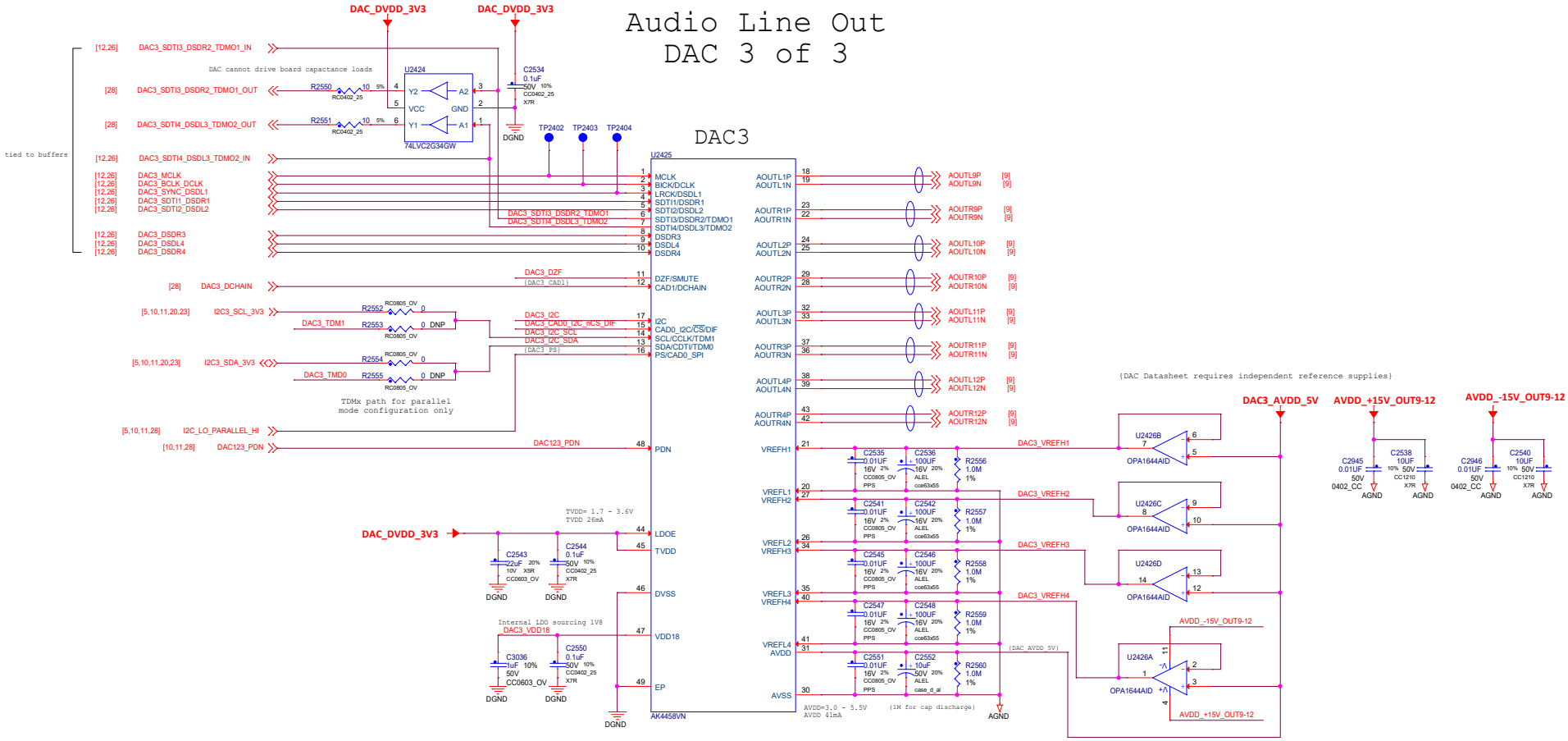
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: **AB2**		
Drawn by: -	Page Title: **DAC 2**		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 11 of 38	

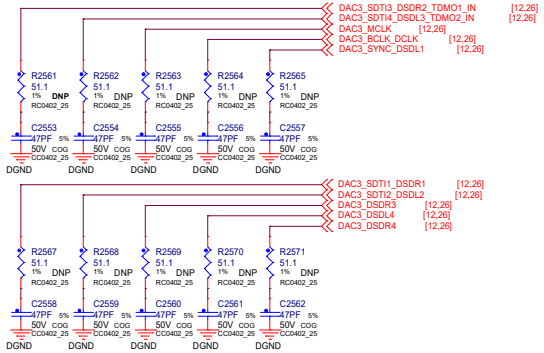
Audio Line Out
DAC 3 of 3



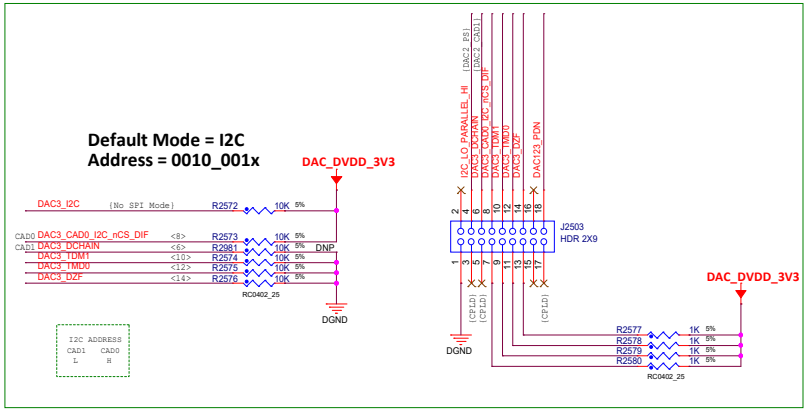
Optional Ground Plane Short

If installed, shorts under DACs should also be installed

Optional Bus Termination



Optional Configuration Header DAC 3



Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	0	0	SD	DFS1	DFS0	DEM11	DEM10	SMUTE
02H	Control 3	DP	0	DCKS	DCKB	MONO1	DZFB	SELLR1	SLOW
03H	L1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	R1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	Control 4	INVL1	INVR1	INVL2	INVR2	SELLR2	0	DFS2	SSLOW
06H	DSD1	DDM	DML1	DMR1	DMC	DMRE	0	DSDD	DSDSEL0
07H	Control 5	L3	R3	L4	R4	0	0	1	SYNCE
08H	Sound Control	L1	R1	L2	R2	0	0	SC1SC1	SC0
09H	DSD2	DML2	DMR2	DML3	DMR3	DML4	DMR4	DSDF	DSDSEL1
0AH	Control 6	TDM1	TDM0	SDS1	SDS2	PW2	PW1	DEM 21	DEM20
0BH	Control 7	ATS1	ATS0	0	SDS0	PW4	PW3	DCHAIN	0
0CH	Control 8	INVR4	INVL4	INVR3	INVL3	0	FIR2	FIR1	FIR0
0DH	Control 9	MONO4	MONO3	MONO2	0	SELLR4	SELLR3	0	0
0EH	Control 10	DEM41	DEM40	DEM31	DEM30	0	0	0	0
0FH	L2ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
10H	R2ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
11H	L3ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
12H	R3ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
13H	L4ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
14H	R4ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

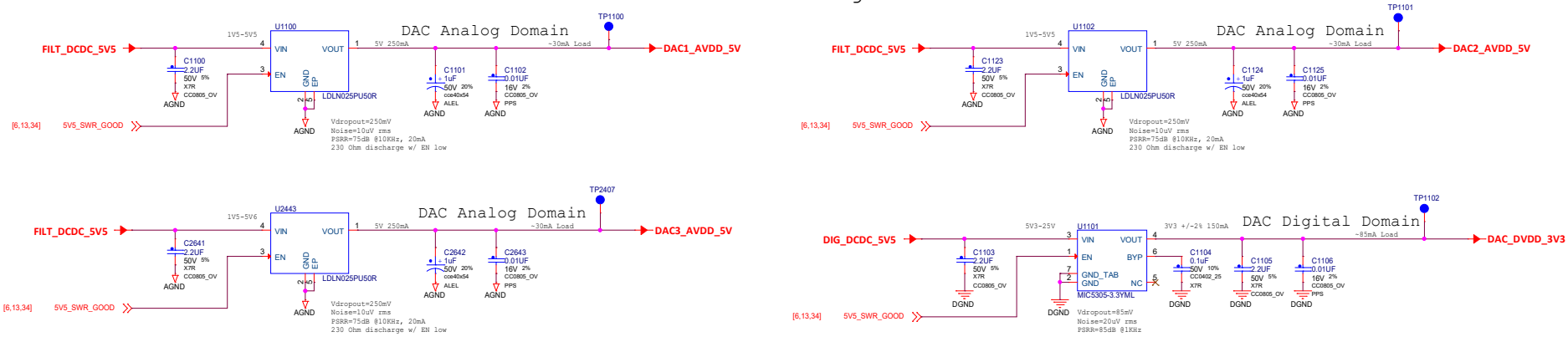
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

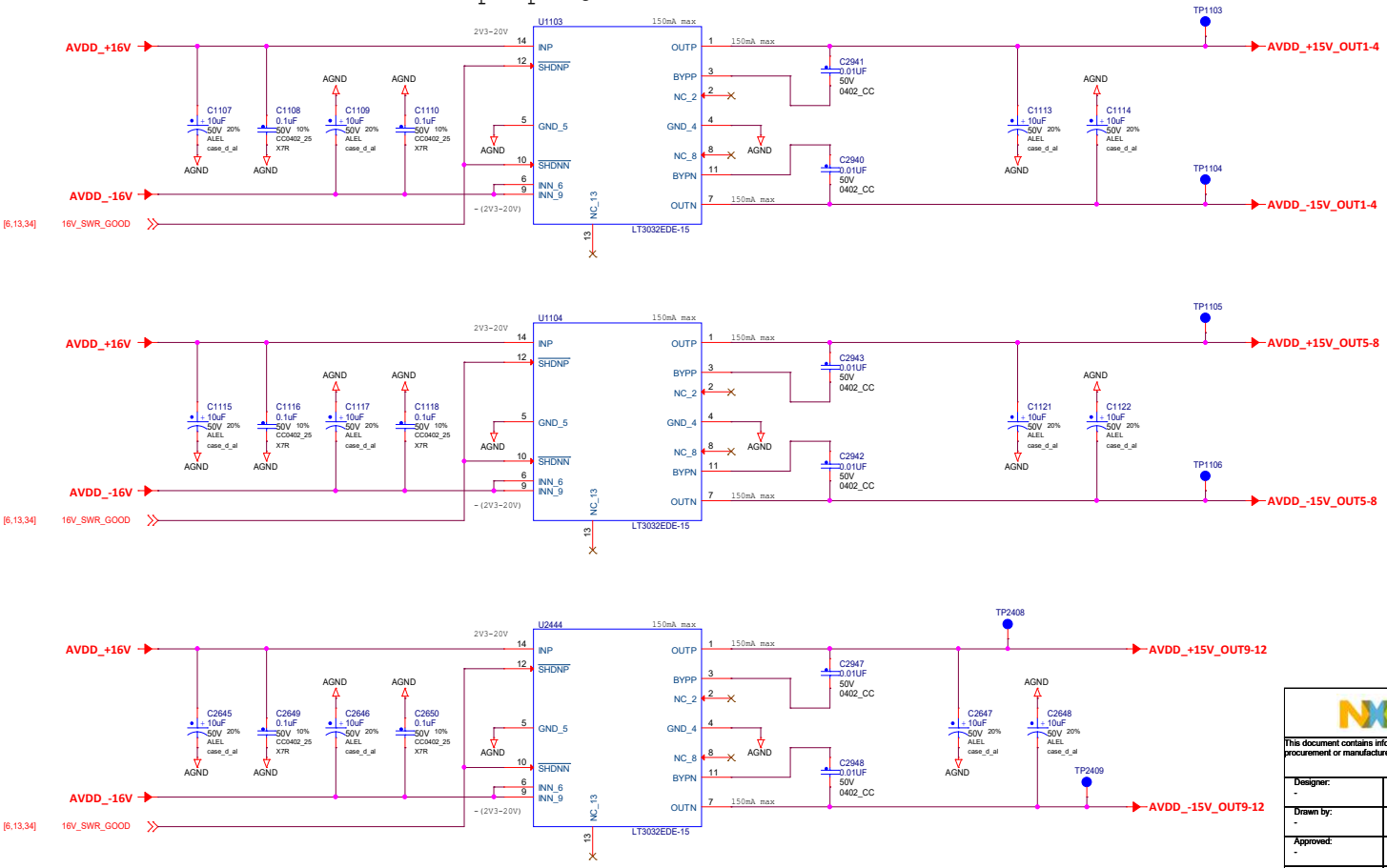
Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: DAC 3		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 12 of 38	

Audio Line Ouput - DAC 1, DAC2 & DAC3 Power Supplies

DAC Reference Voltages

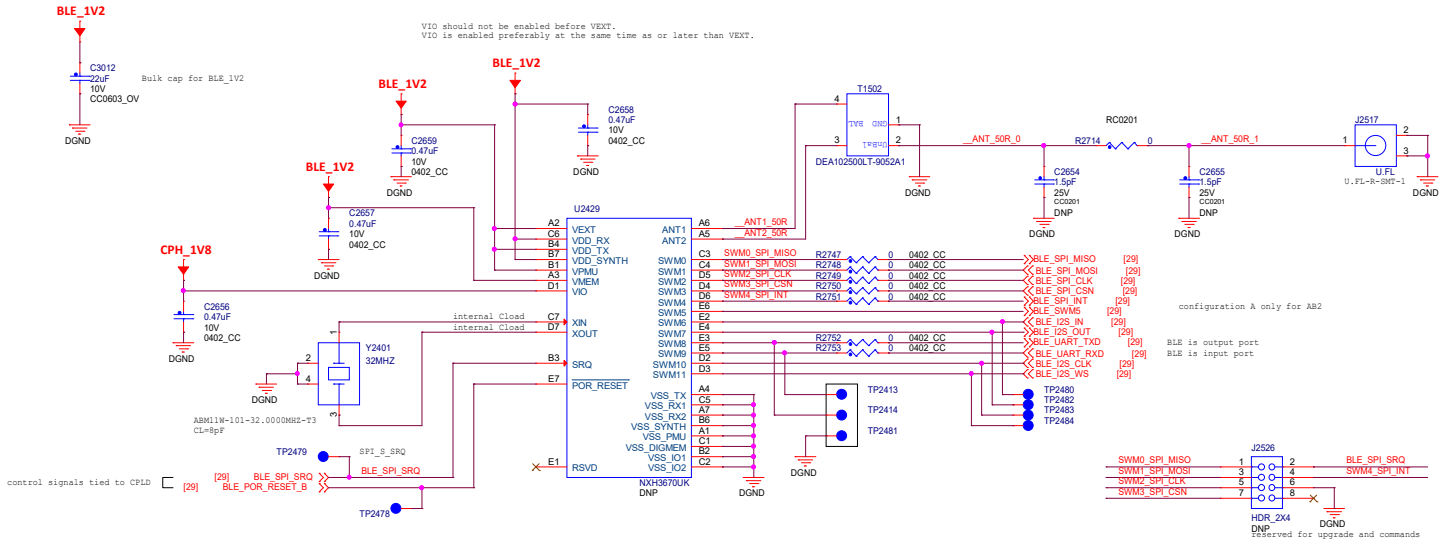


OpAmp +/- 15V Supply
4 OpAmps @ ~10-15mA each



NXP	Microcontroller Product Group 6501 William Cannon Drive West Austin, TX 78735-8598		
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.			
	ICAP Classification: CP: IUO: PUBI: X		
Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: DAC Power Supply		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 13 of 38	

Wireless Subwoofer



Pin	Default	Configuration A	Configuration B	Configuration C	Configuration D
SWM00	SPI_S_MISO	SPI_S_MISO	SPI_S_MISO	SPI_S_MISO	SPI_S_MISO
SWM01	SPI_S_MOSI	SPI_S_MOSI	SPI_S_MOSI	SPI_S_MOSI	SPI_S_MOSI
SWM02	SPI_S_CLK	SPI_S_CLK	SPI_S_CLK	SPI_S_CLK	SPI_S_CLK
SWM03	SPI_S_CSN	SPI_S_CSN	SPI_S_CSN	SPI_S_CSN	SPI_S_CSN
SWM04	SPI_S_INT	SPI_S_INT	SPI_S_INT	SPI_S_INT	SPI_S_INT
SWM05	tri-state	tri-state	tri-state	I2S SO	tri-state
SWM06	tri-state	I2S SI	I2S SI	I2S SI	UART RXD
SWM07	tri-state	I2S SO	I2S SO	UART TXD	UART TXD
SWM08	tri-state	UART TXD	EXT RXEN(CRX)	EXT RXEN(CRX)	EXT RXEN(CRX)
SWM09	tri-state	UART RXD	EXT PAEN(CTX)	EXT PAEN(CTX)	EXT PAEN(CTX)
SWM10	tri-state	I2S CLK	I2S CLK	I2S CLK	tri-state
SWM11	tri-state	I2S WS	I2S WS	I2S WS	tri-state
SRQ	SPI_S_SRQ	SPI_S_SRQ	SPI_S_SRQ	SPI_S_SRQ	SPI_S_SRQ

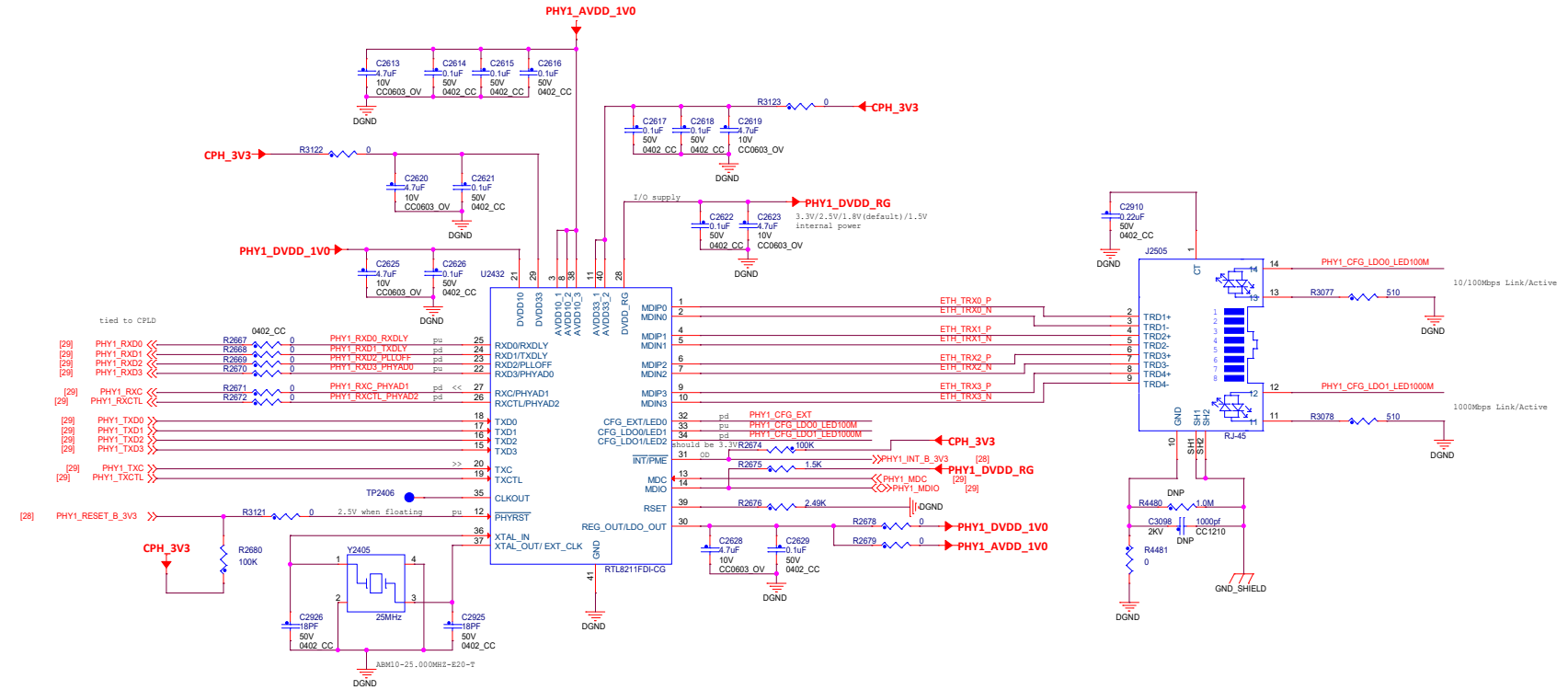
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

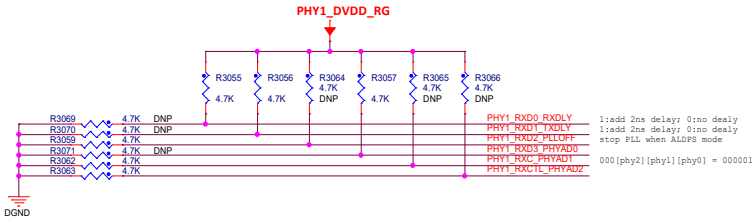
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

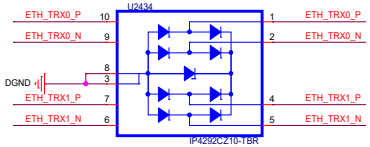
ICAP Classification: CP: IUO: PUBI: X

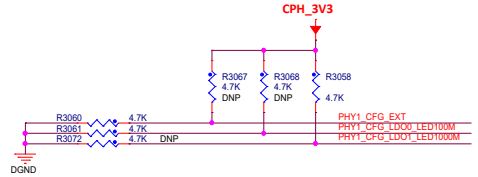
Designer: -	Drawing Title: **AB2**		
Drawn by: -	Page Title: **Wireless Subwoofer**		
Approved:	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 14 of 38	

Ethernet PHY

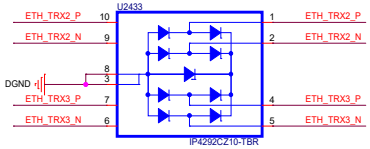








CFG_EXT	CFG_LDO1	CFG_LDO0	DVDD_RG
0	0	0	output reserved
	0	1	output 2.5V
	1	0	output 1.8V (default)
	1	1	output 1.5V
1	0	0	external supply 3.3V
	0	1	external supply 2.5V
	1	0	external supply 1.8V
	1	1	external supply 1.5V



Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

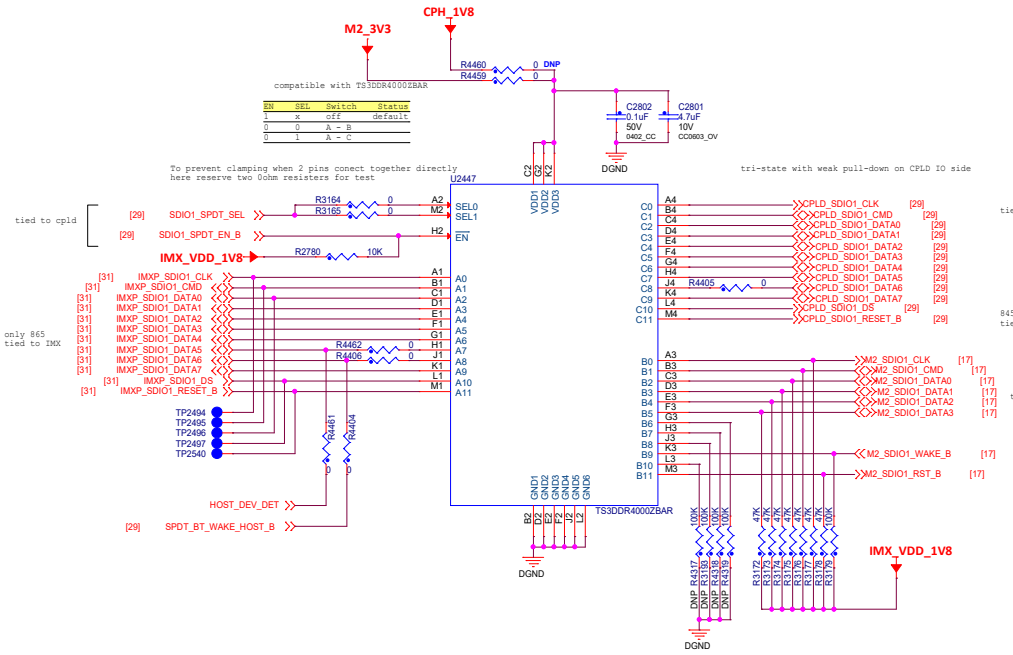
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

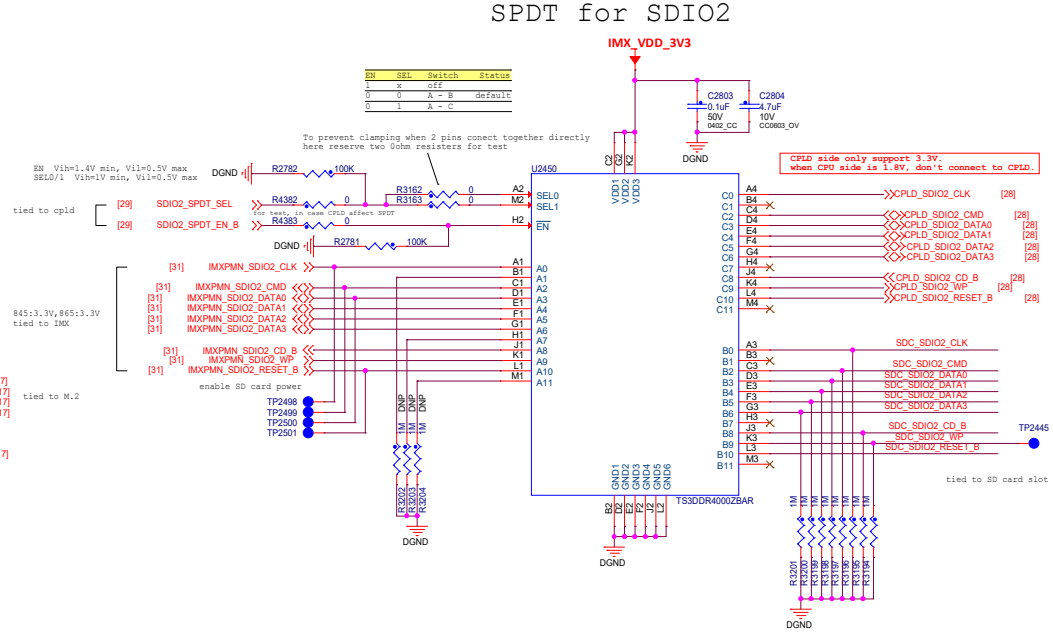
Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: Ethernet PHY		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 15 of 38	

SPDT SD Card MFI

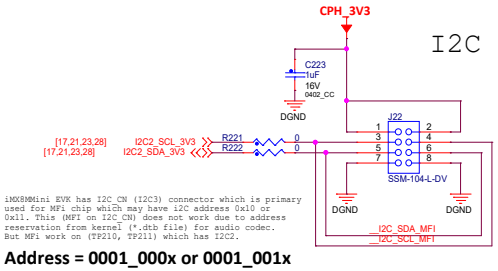
SPDT for SDIO1



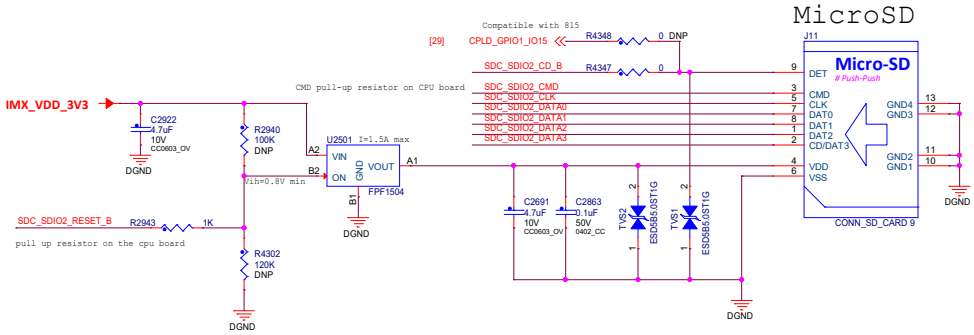
SPDT for SDIO2



I2C CN

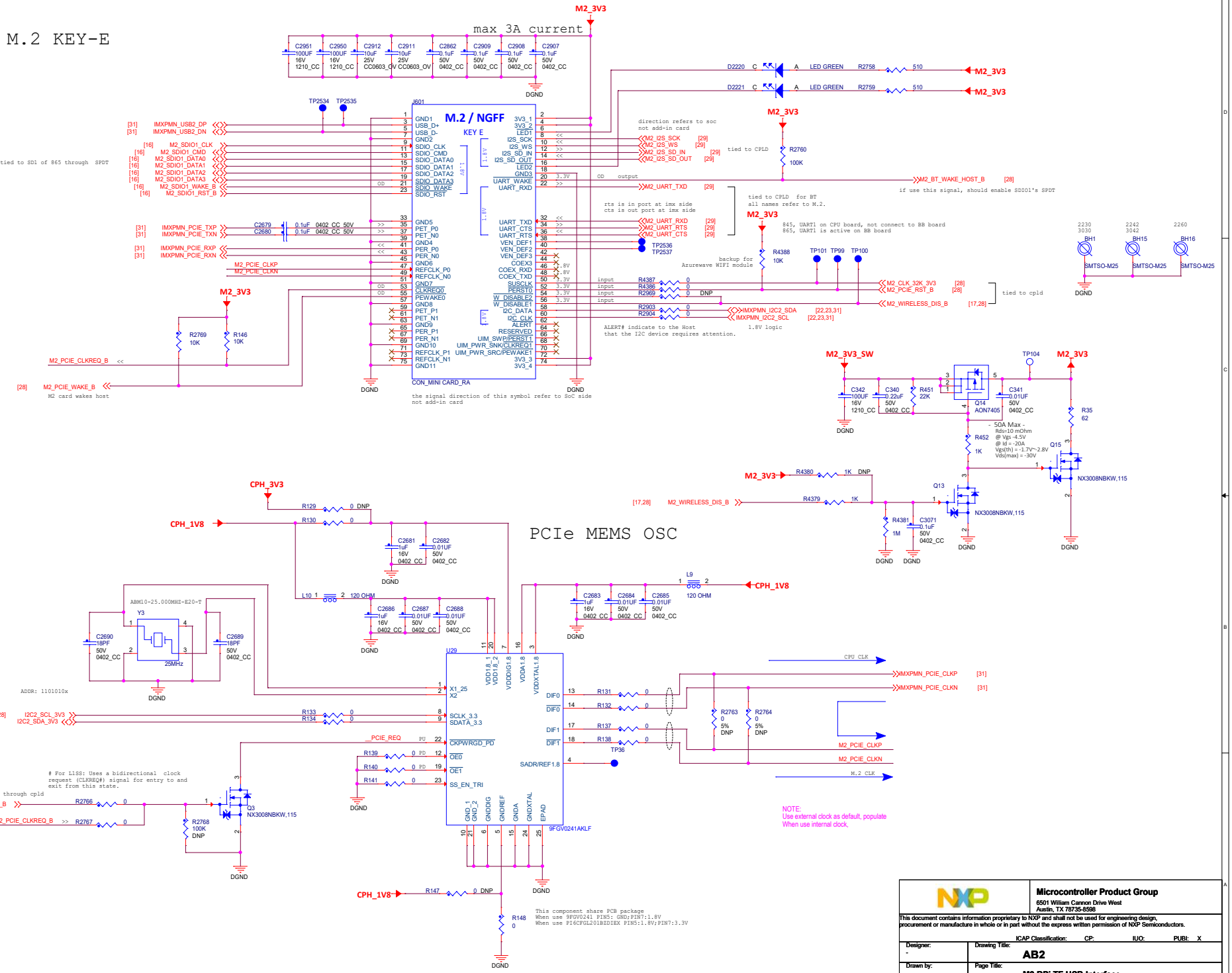


MicroSD



NXP	Microcontroller Product Group 6501 William Cannon Drive West Austin, TX 78735-8598		
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.			
ICAP Classification:	CP:	IUO:	PUBI: X
Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: SPDT SD Card MFI		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 16 of 38	

M.2 KEY-E



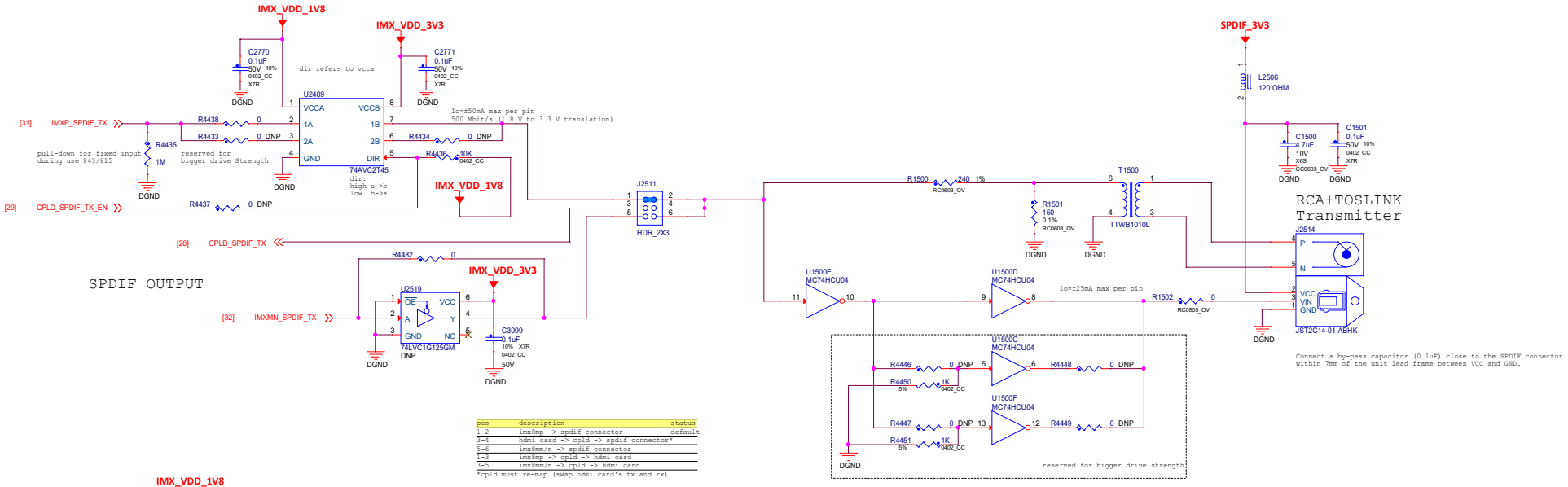
NXP	**Microcontroller Product Group** 6501 William Cannon Drive West Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

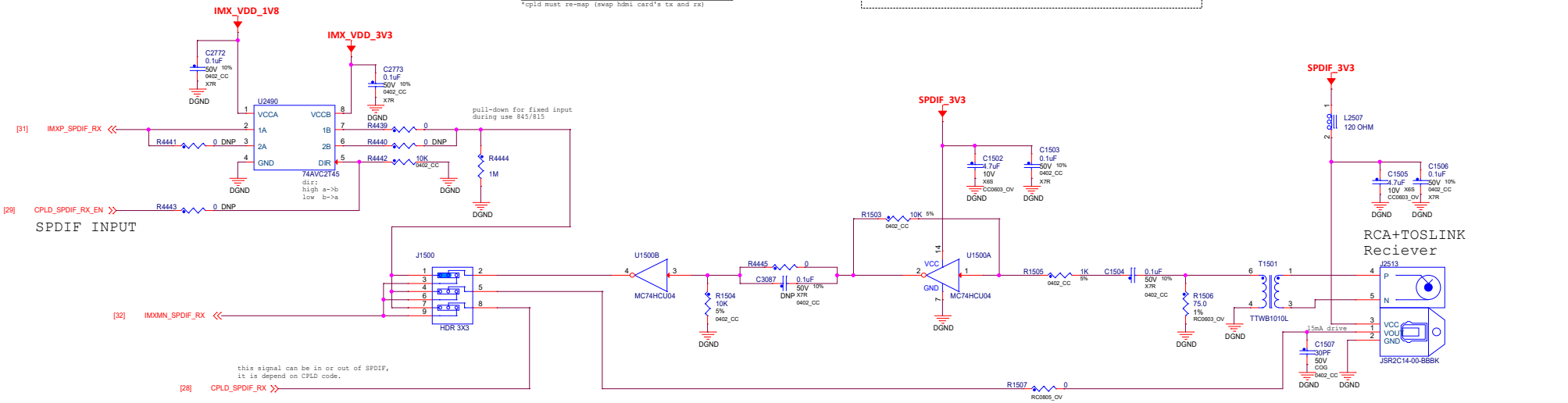
Designer: -	Drawing Title: **AB2**		
Drawn by: -	Page Title: **M2 RPi TF USB Interface**		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 17 of 38	

SPDIF IN/OUT



pos	description	status
1-2	imx8mp -> spdif connector	default
3-4	hdmi card -> cpld -> spdif connector*	
5-6	imx8mm/n -> spdif connector	
1-3	imx8mp -> cpld -> hdmi card	
3-5	imx8mm/n -> cpld -> hdmi card	

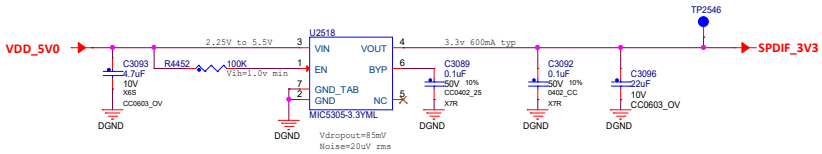
*cpld must re-map (swap hdmi card's tx and rx)



pos	description	status
1-2	coaxial connector -> imx8mp	default
4-5	optical connector -> imx8mp	
7-8	hdmi card -> cpld -> imx8mp	
2-3	coaxial connector -> imx8mm/n	
5-6	optical connector -> imx8mm/n	
8-9	hdmi card -> cpld -> imx8mm/n	
5-8	optical connector -> cpld -> hdmi card*	
2-8	coaxial connector -> cpld -> hdmi card*	

*cpld must re-map (swap hdmi card's tx and rx)

1. Connect a by-pass capacitor (0.1uF) close to the SPDIF connector within 7mm of the unit lead frame.
2. Connect a by-pass capacitor (30pF) between GND and Vout avoid loading effect.



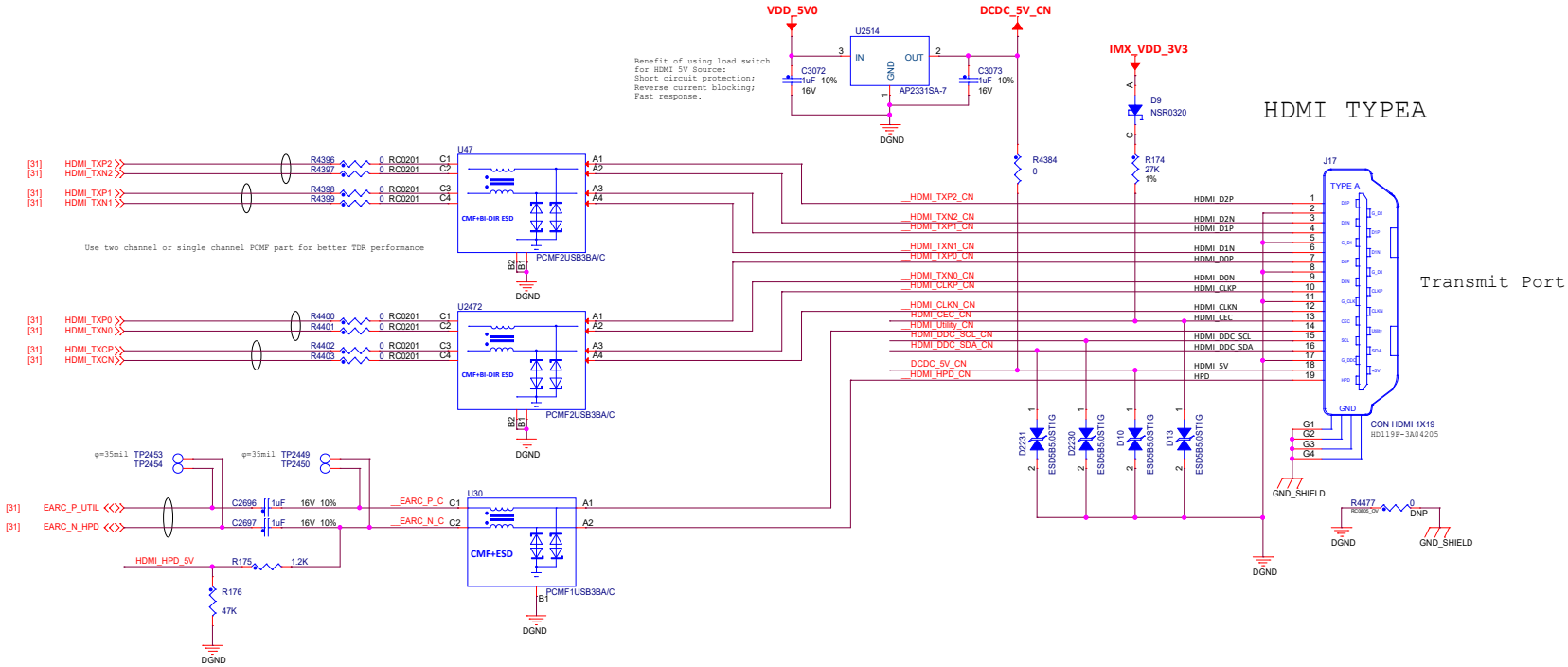
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

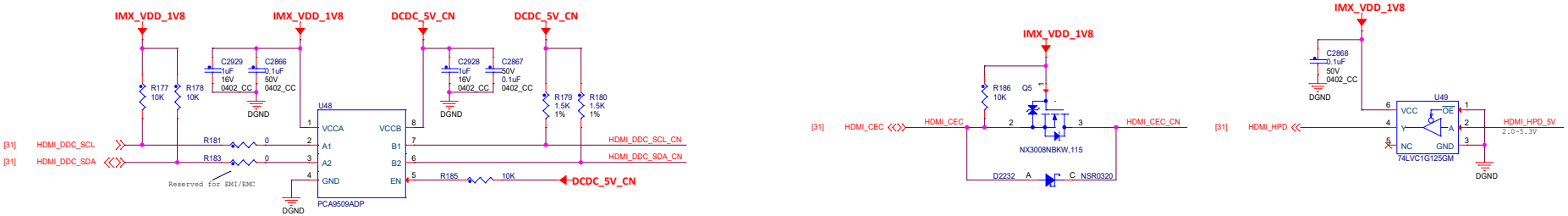
ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: SPDIF		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 18 of 38	

HDMI Display with eARC

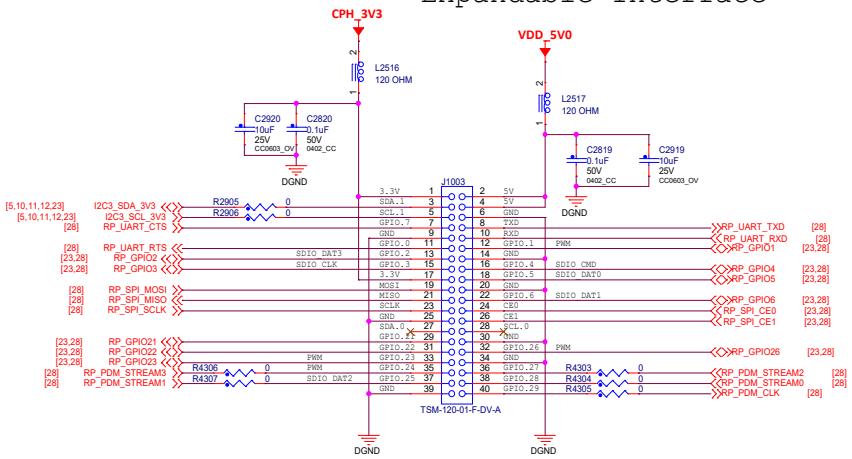


Level shifter



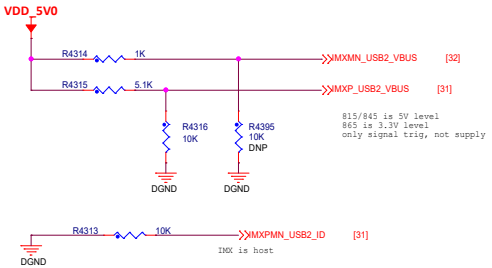
NXP	Microcontroller Product Group 6501 William Cannon Drive West Austin, TX 78735-8598		
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.			
	ICAP Classification: CP: IUO: PUBI: X		
Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: IMX HDMI		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 19 of 38	

Expandable Interface

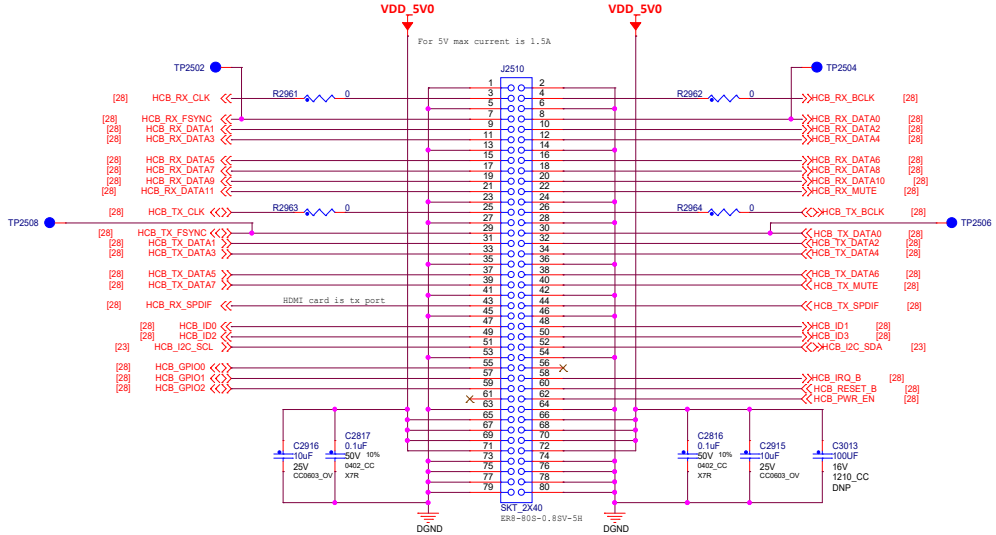


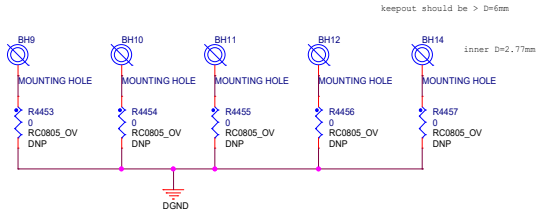
IMX USB2

only host mode



HDMI Card Interface

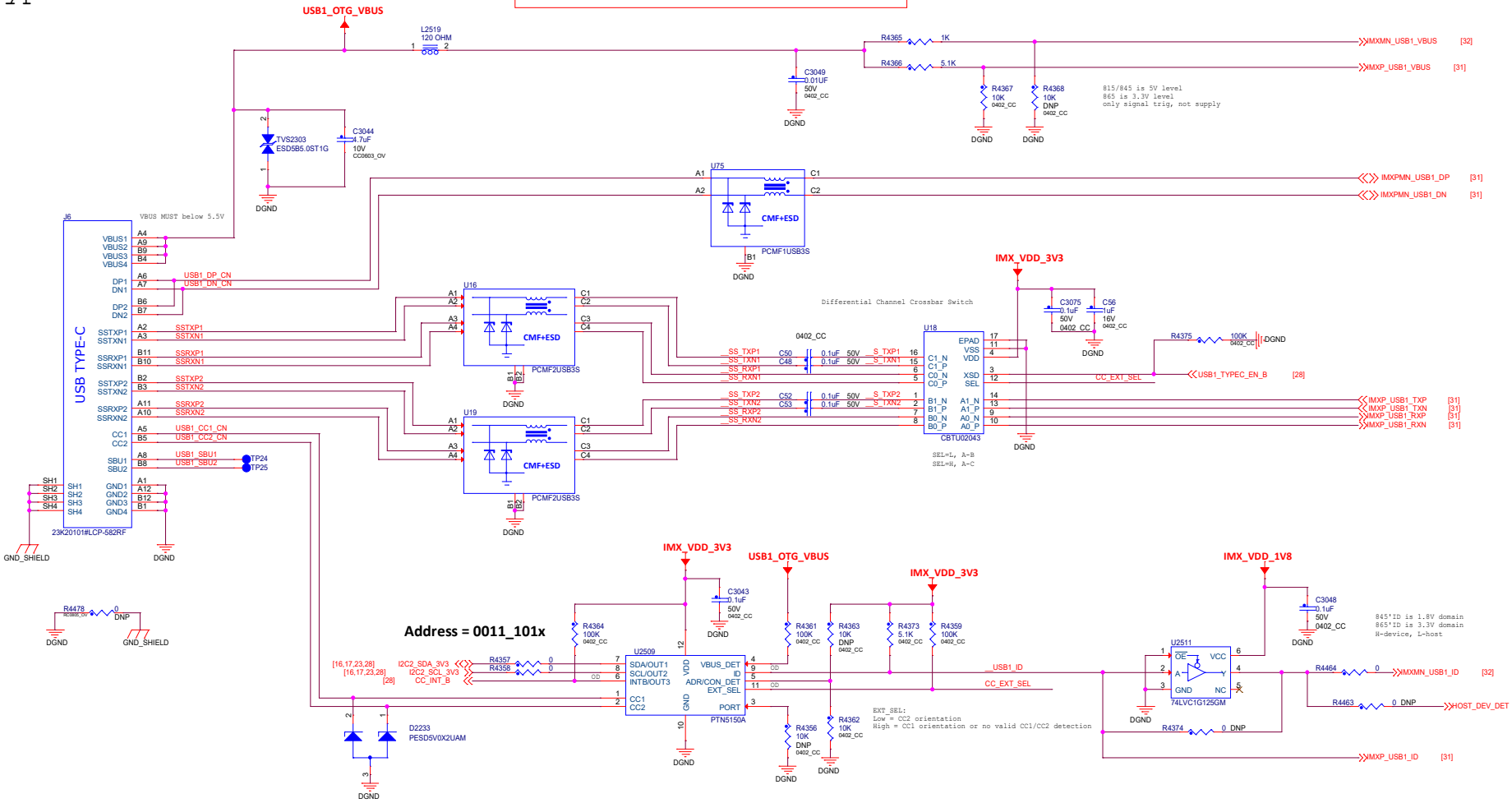




NXP	**Microcontroller Product Group** 6501 William Cannon Drive West Austin, TX 78735-8598		
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.			
	ICAP Classification: CP: IUO: PUBI: X		
Designer: -	Drawing Title: **AB2**		
Drawn by: -	Page Title: **HDMI Card Interface**		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 20 of 38	

USB Type C

Don't support Power Delivery feature



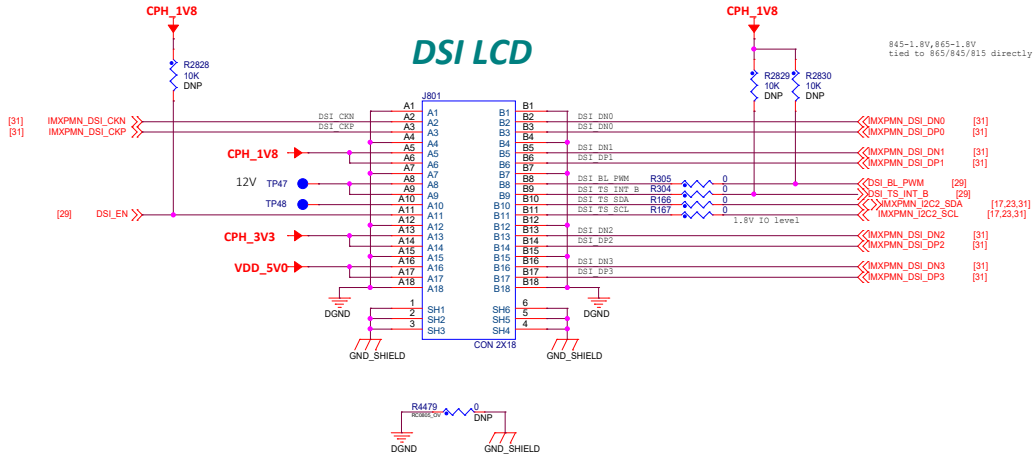
NXP	**Microcontroller Product Group** 6501 William Cannon Drive West Austin, TX 78735-8598

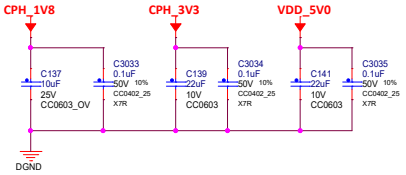
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

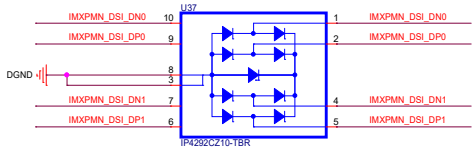
ICAP Classification: CP: IUO: X PUBI:

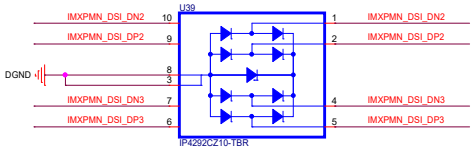
Designer: -	Drawing Title: **AB2**		
Drawn by: -	Page Title: **USB Type C**		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 21 of 38	

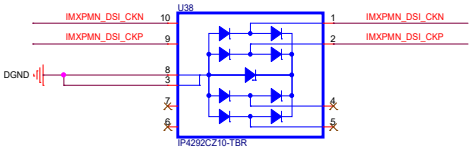
DSI LCD











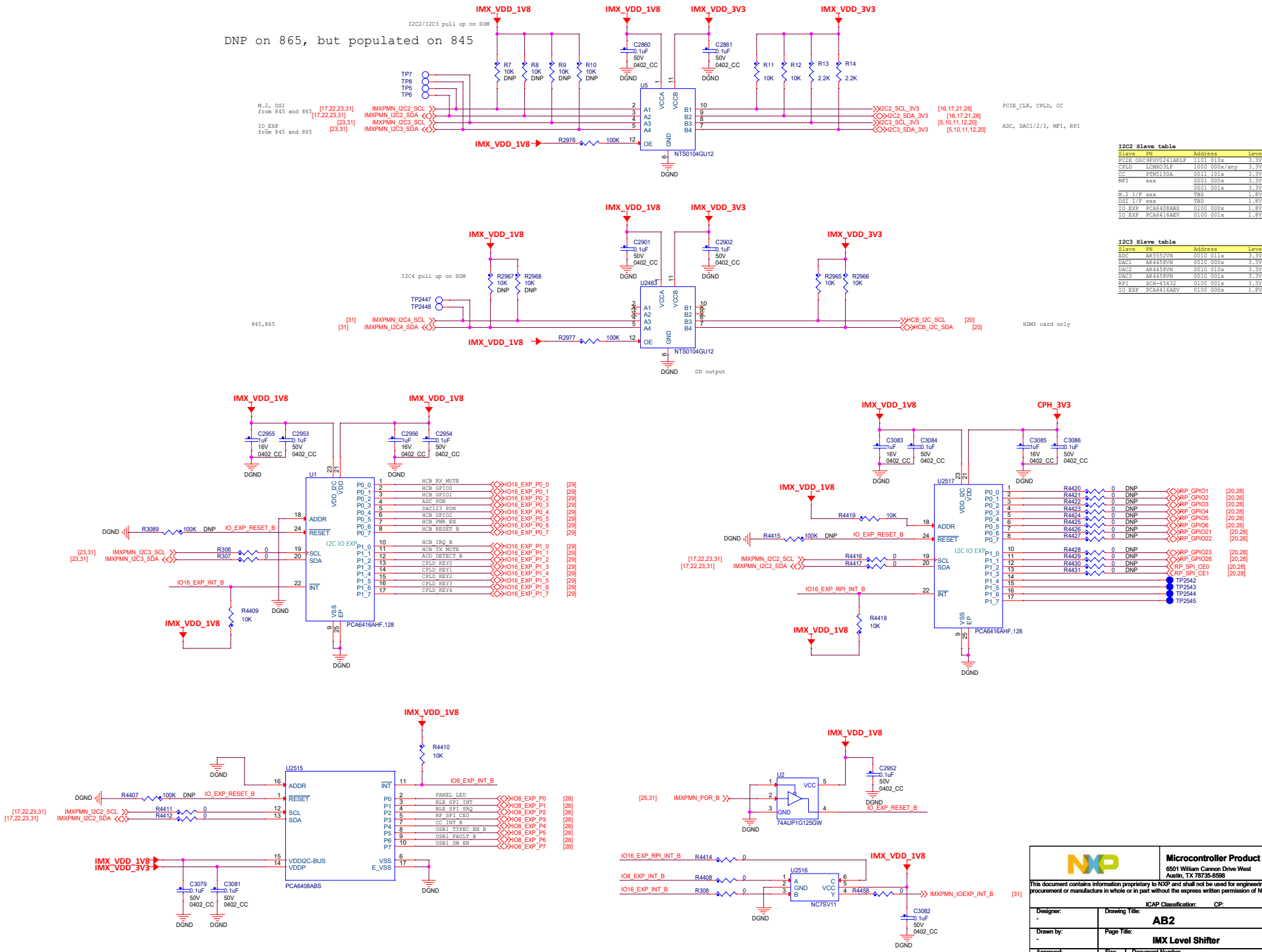
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: DSI LCD		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 22 of 38	

IMX Level Shifter



I2C2 Slave table

Slave	PN	Address	Level
PCIE	GSC9FGV0241AKLF	1101 010x	3.3V
CPLD	LCMXO3LF	1000 000x/any	3.3V
CC	PTN5150A	0011 101x	3.3V
MPI	xxx	0001 000x	3.3V
		0001 001x	3.3V
M.2 I/F	xxx	TBD	1.8V
DSI I/F	xxx	TBD	1.8V
IO EXP	PCA6408ABS	0100 000x	1.8V
IO EXP	PCA6416AEV	0100 001x	1.8V

I2C3 Slave table

Slave	PN	Address	Level
ADC	AK5552VN	0010 011x	3.3V
DAC1	AK4458VN	0010 000x	3.3V
DAC2	AK4458VN	0010 010x	3.3V
DAC3	AK4458VN	0010 001x	3.3V
RPI	SCH-45632	0100 001x	3.3V
IO EXP	PCA6416AEV	0100 000x	1.8V

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

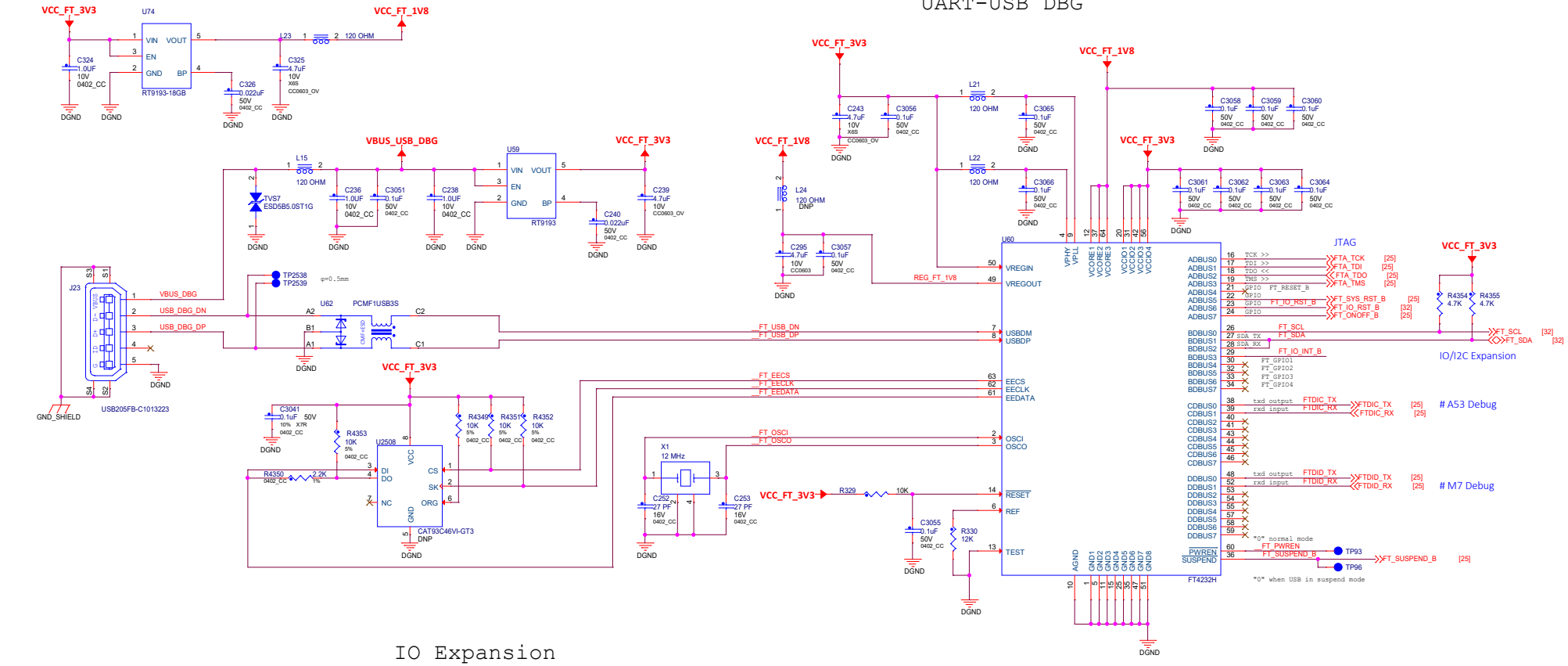
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

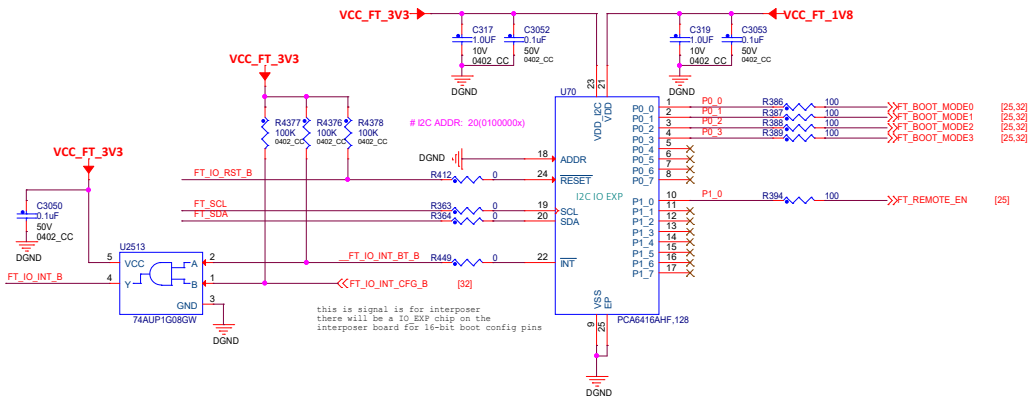
Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: IMX Level Shifter		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 23 of 38	

Remote Debug Tool SHOULD support Local Debug as default, and enable Remote Debug when user clicks the button on PC.

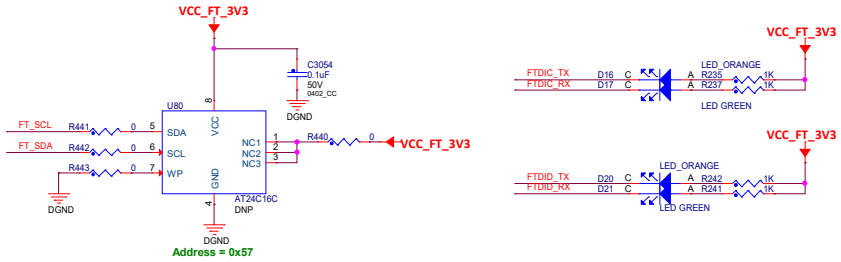
UART-USB DBG



IO Expansion

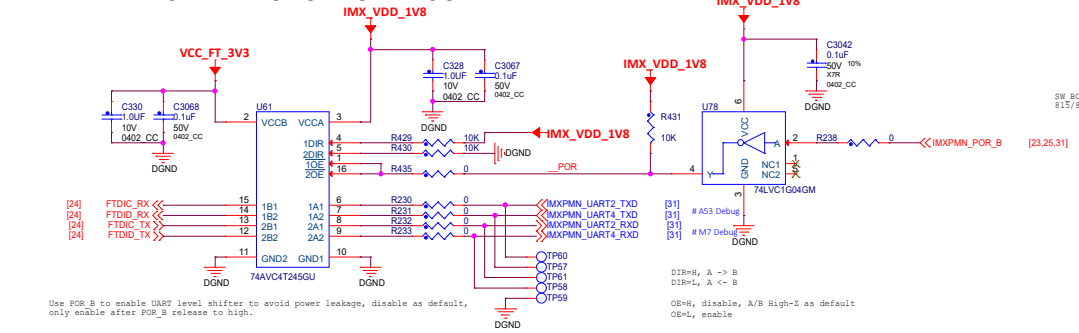


System ID

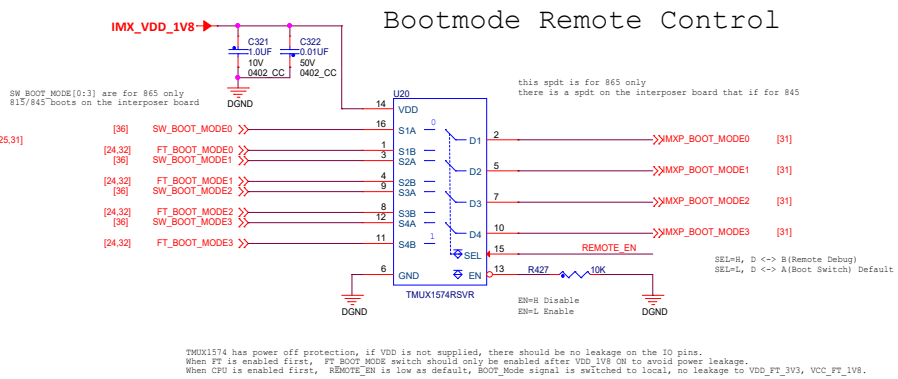


NXP	**Microcontroller Product Group** 6501 William Cannon Drive West Austin, TX 78735-8598		
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.			
	ICAP Classification: CP: IUO: X PUBI:		
Designer: -	Drawing Title: **AB2**		
Drawn by: -	Page Title: **Remote Debug**		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 24 of 38	

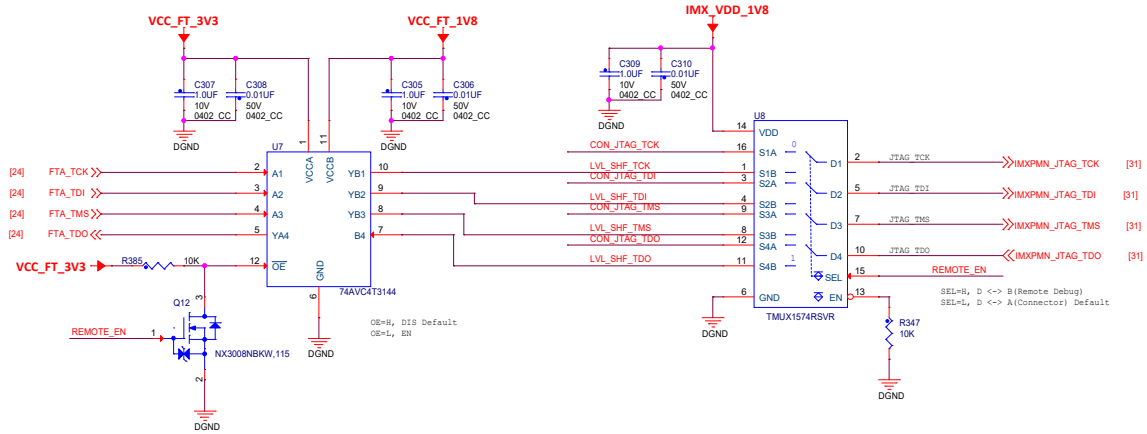
UART Level Shifter

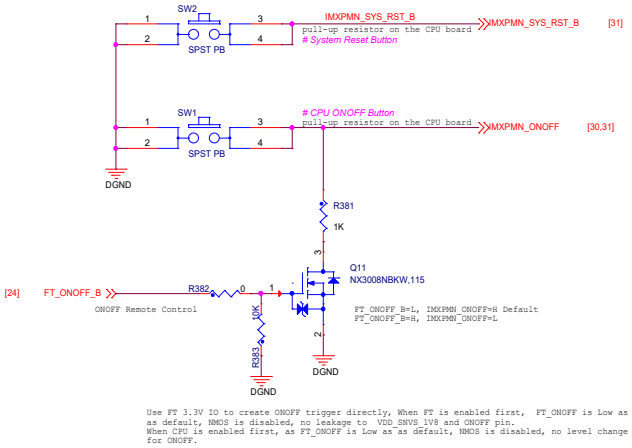


Bootmode Remote Control

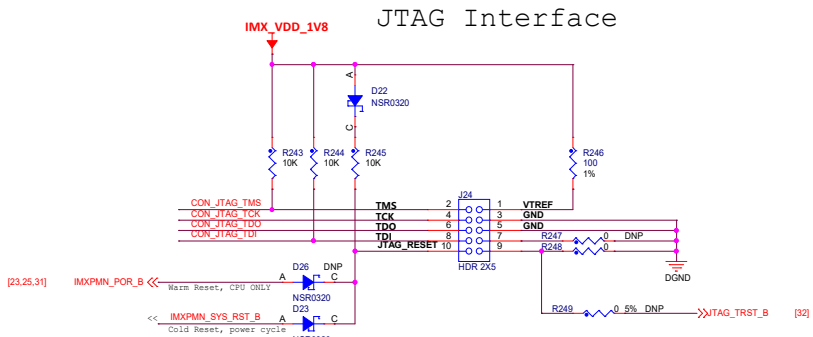


JTAG Remote Control

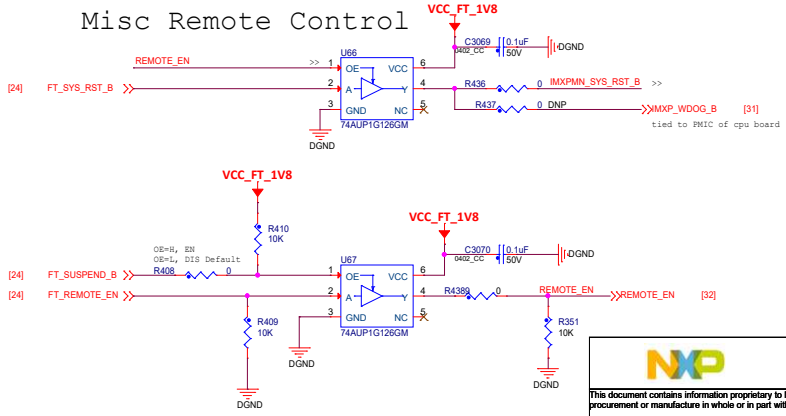




JTAG Interface



Misc Remote Control



Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

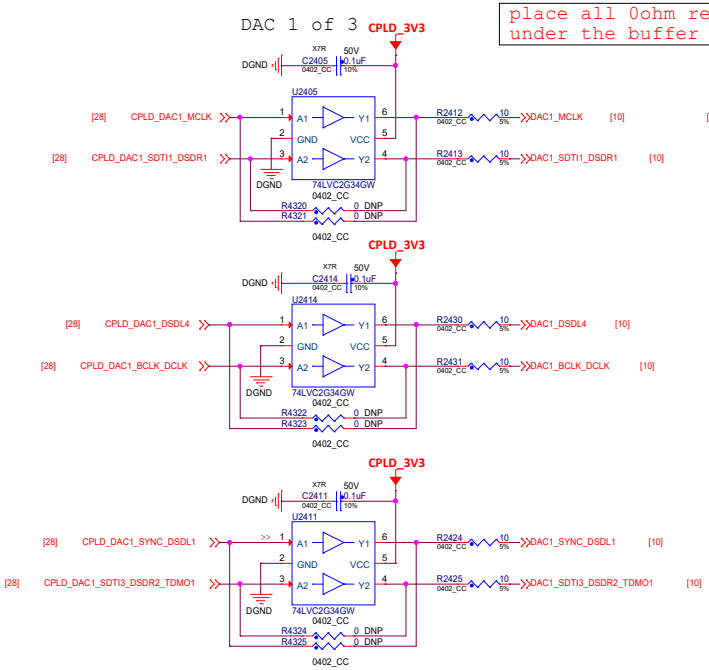
ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: **AB2**		
Drawn by: -	Page Title: **Remote Debug Isolation**		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 25 of 38	

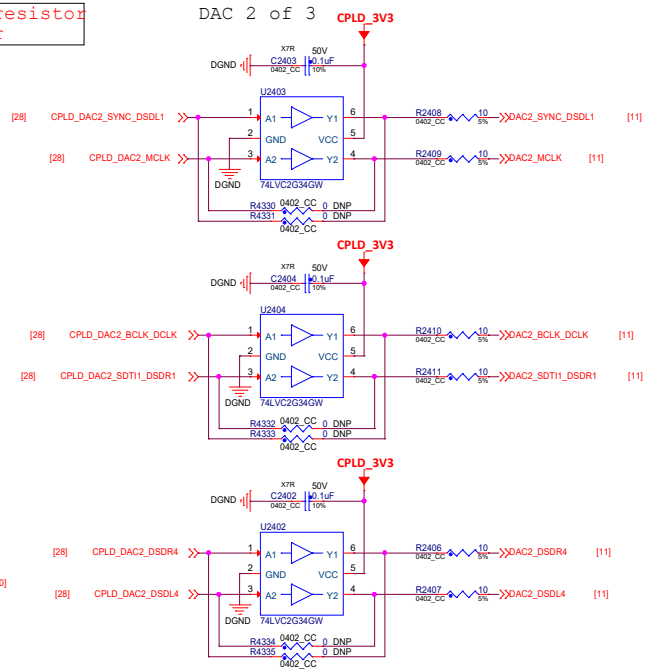
DAC and ADC Buffers

place all 0ohm resistor
under the buffer

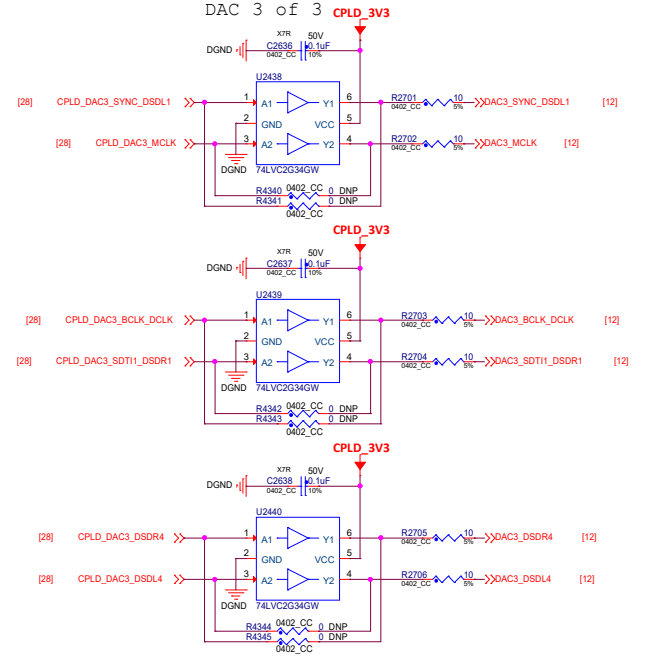
DAC 1 of 3



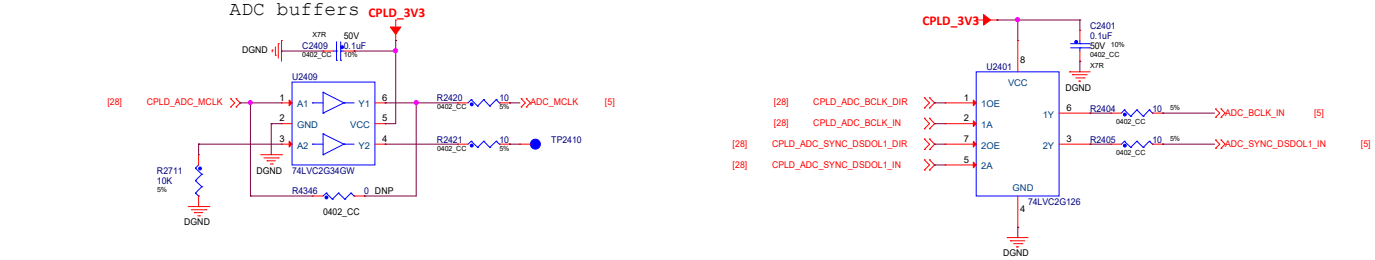
DAC 2 of 3



DAC 3 of 3



ADC buffers



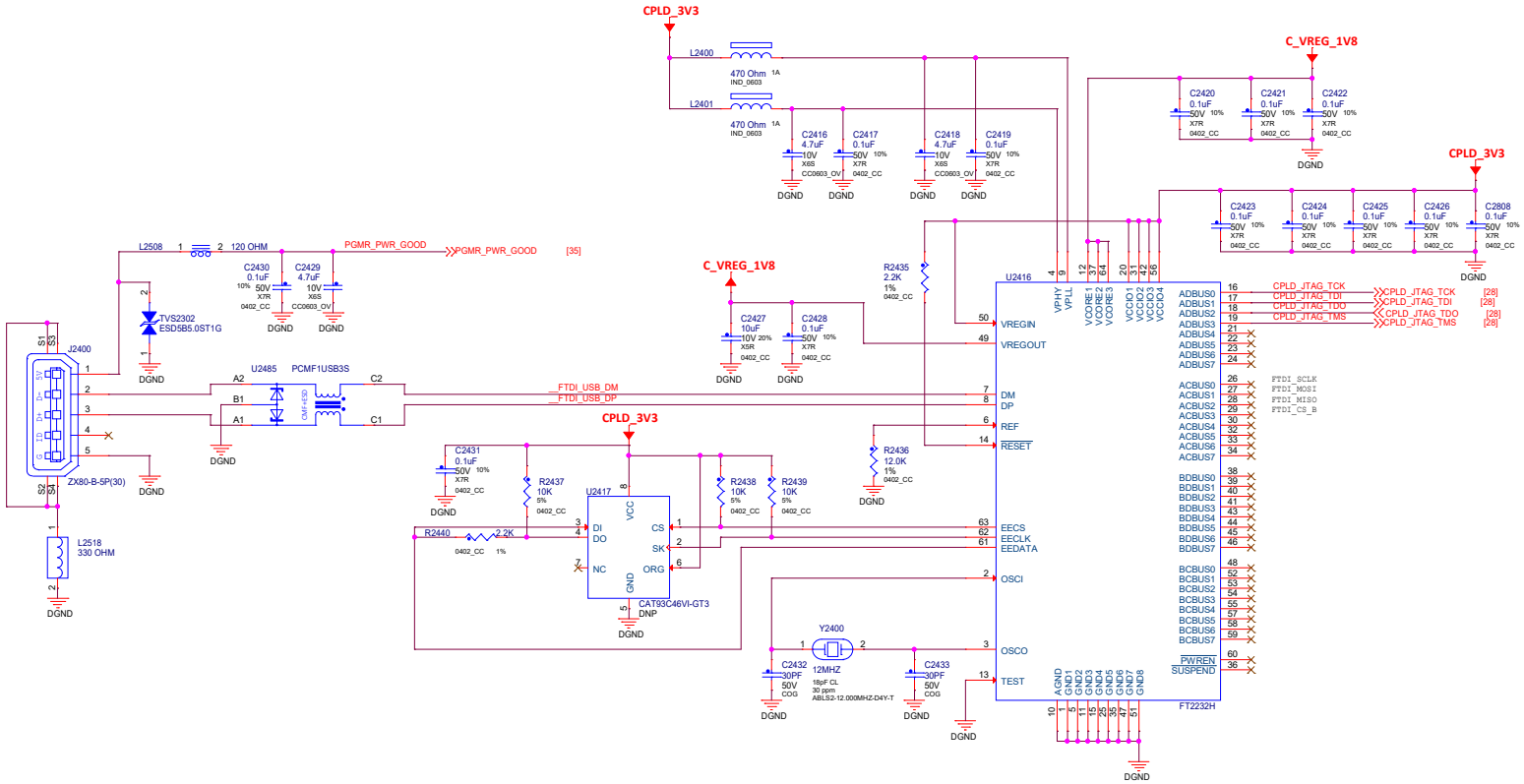
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

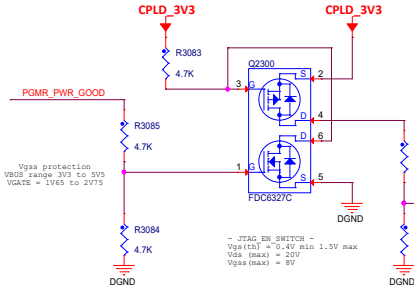
ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: DAC Buffer		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 26 of 38	

CPLD JTAG Programming Interface



CPLD JTAG ENABLE



The JTAGENB pin is only available when the JTAG_PORT is in the DISABLE state

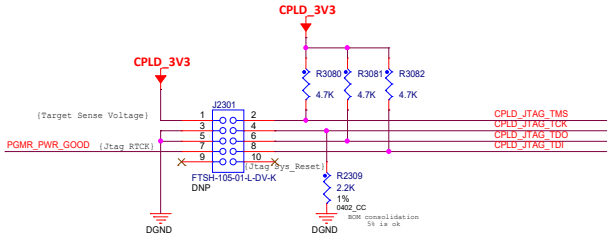
Programming Cable (VBUS) will enable JTAG on the CPLD
CPLD_JTAGEN must rise with VDD_3V3 at Power-On be enabled.

H:jtag mode, L:gpio mode

When JTAG_PORT = ENABLE in spreadsheet (default)
the JTAGEN is a GPIO.

When JTAG_PORT = DISABLE in spreadsheet
the JTAGEN = 1, is JTAG port. the JTAGEN = 0, is GPIO.

CPLD JTAG



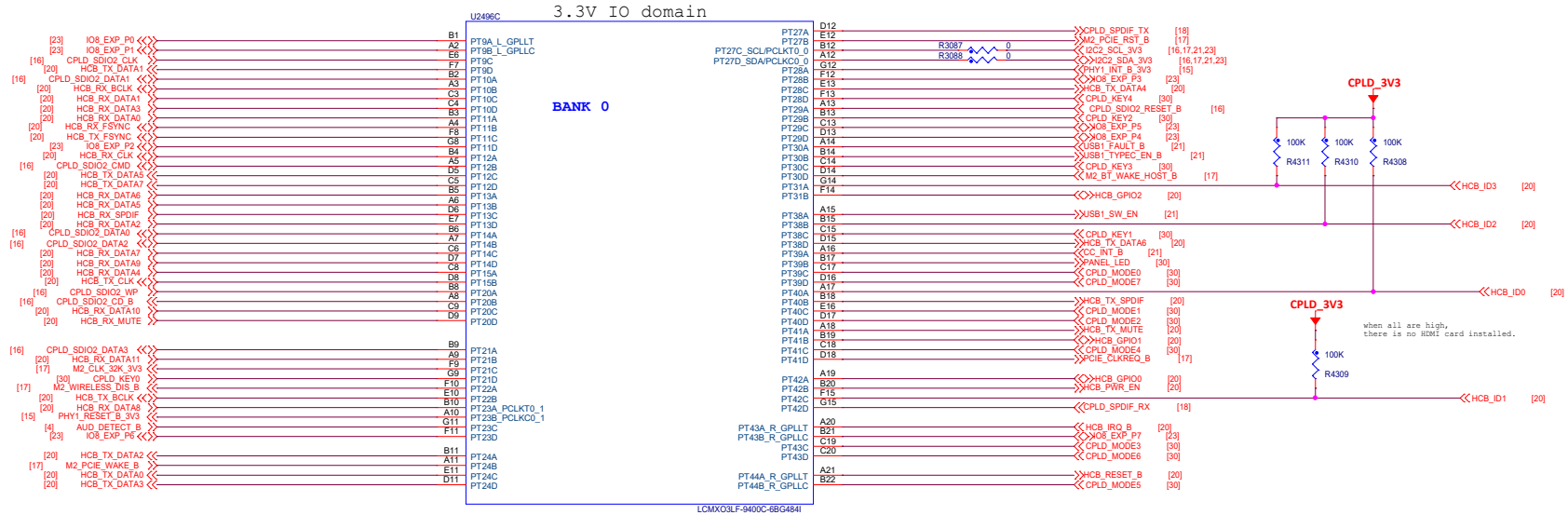
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

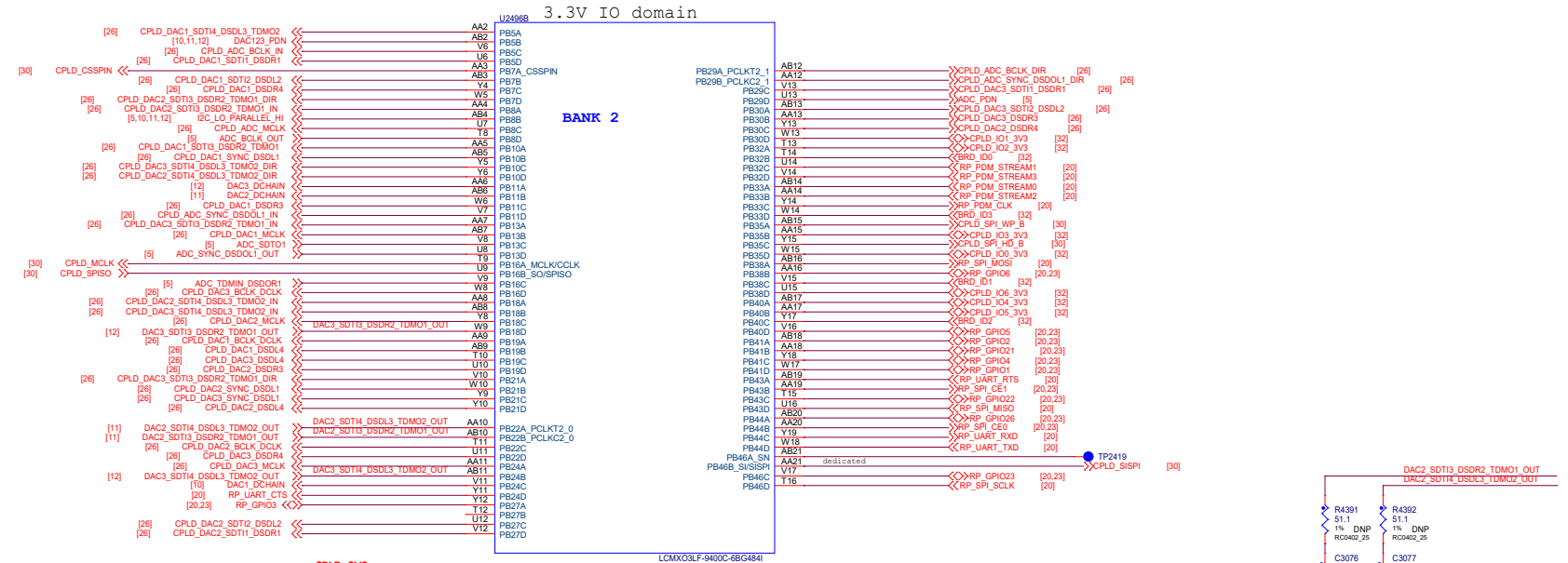
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

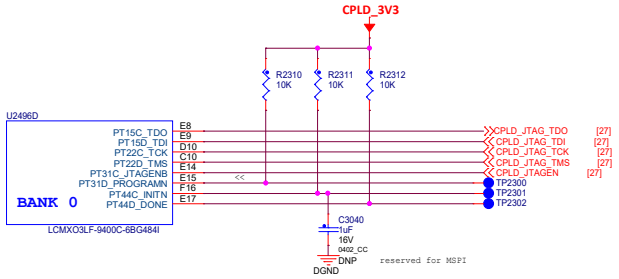
ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: CPLD JTAG Interface		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 27 of 38	

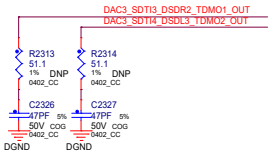
CPLD IO







Optional Termination for DAC3



Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

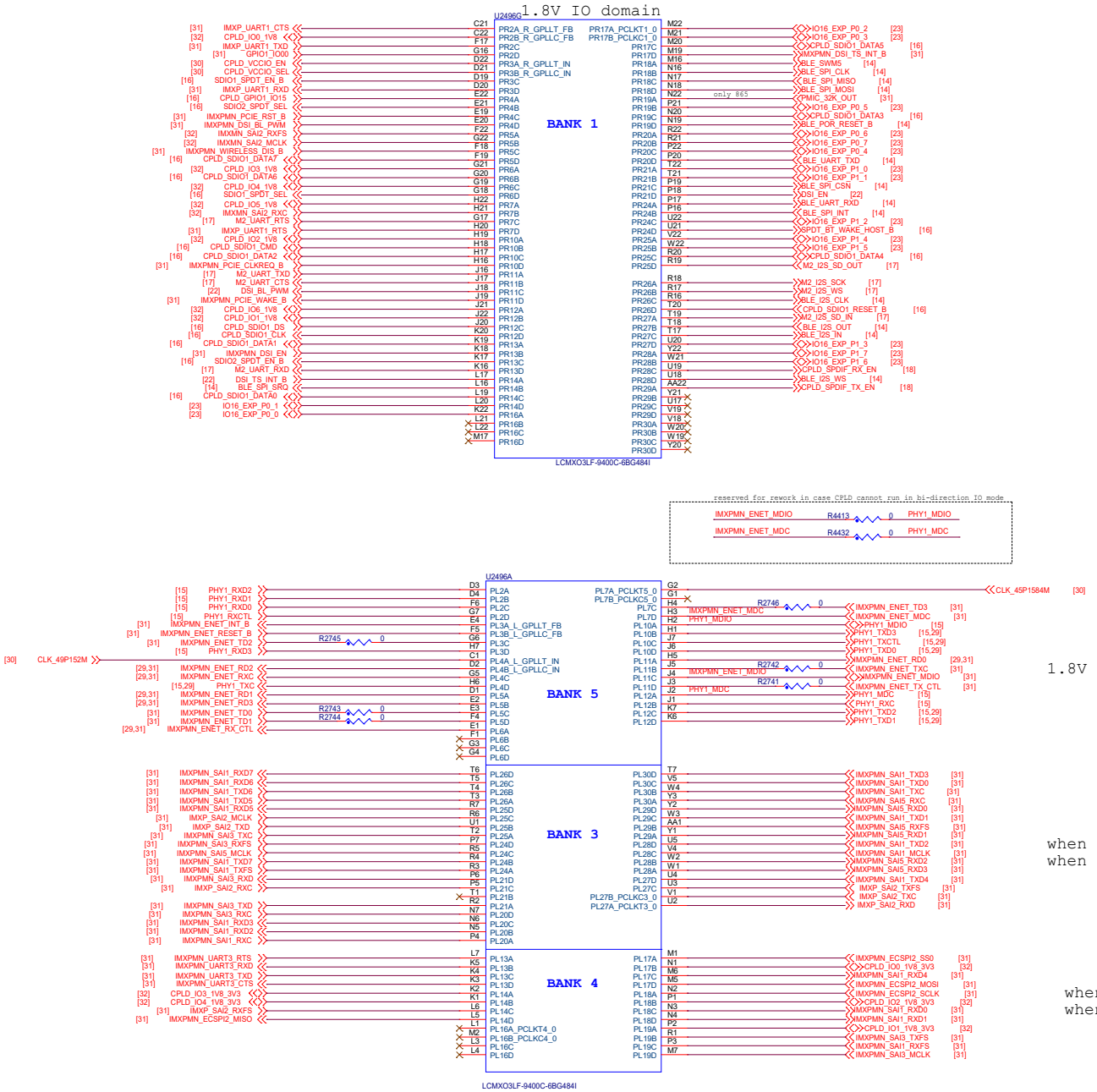
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: CPLD 1		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 28 of 38	

CPLD IO

B and L tied to IMX



1.8V IO domain

when install 845/815, this domain must be 3.3V
when install 865, this domain must be 1.8V

when install 845/815, this domain must be 3.3V
when install 865, this domain must be 1.8V

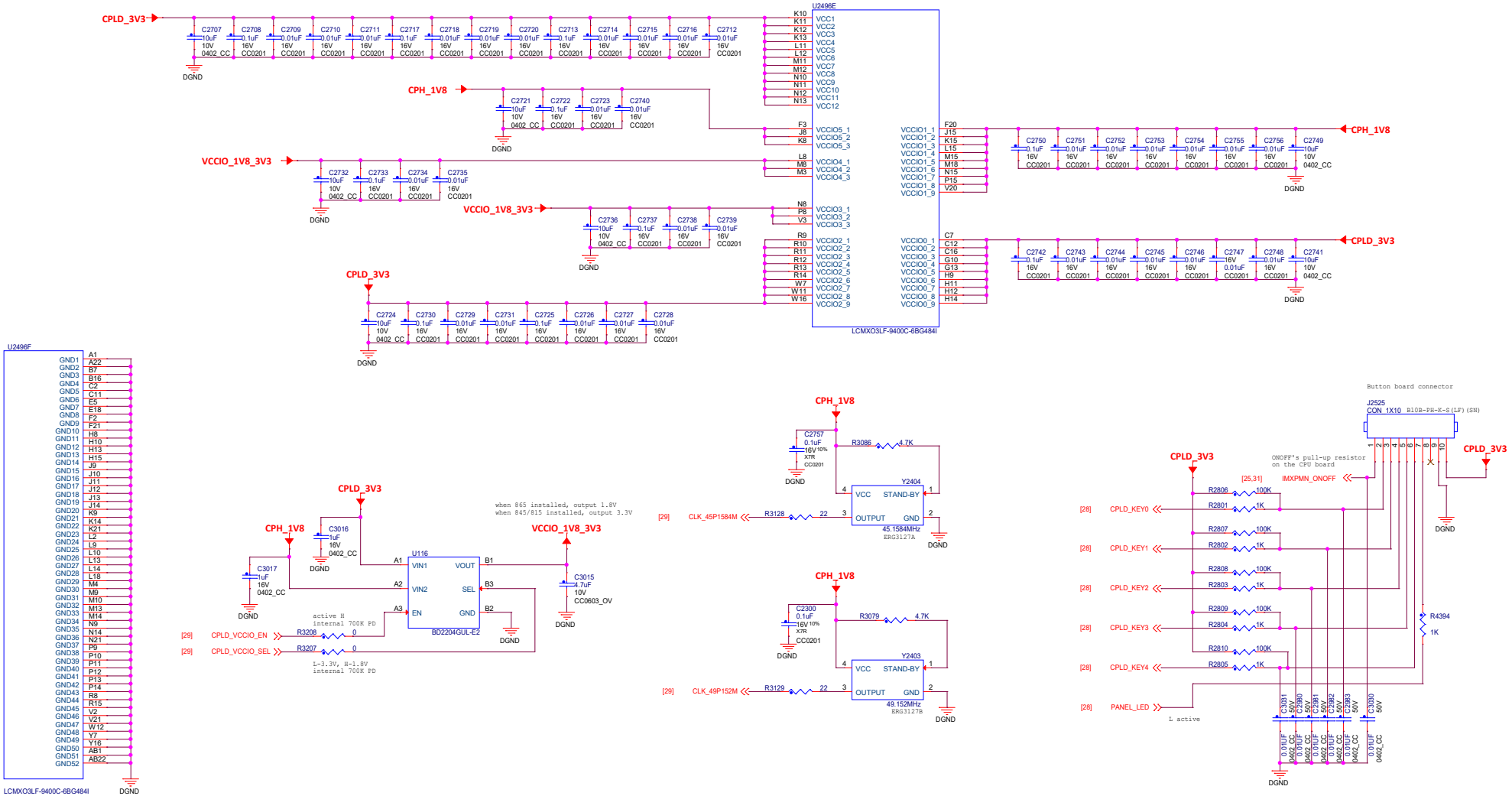
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

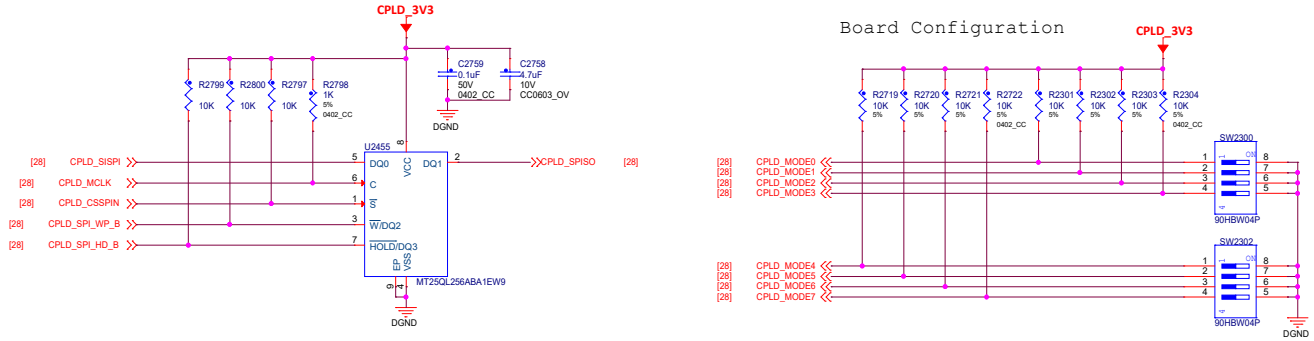
ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: CPLD 2		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 29 of 38	

CPLD Power



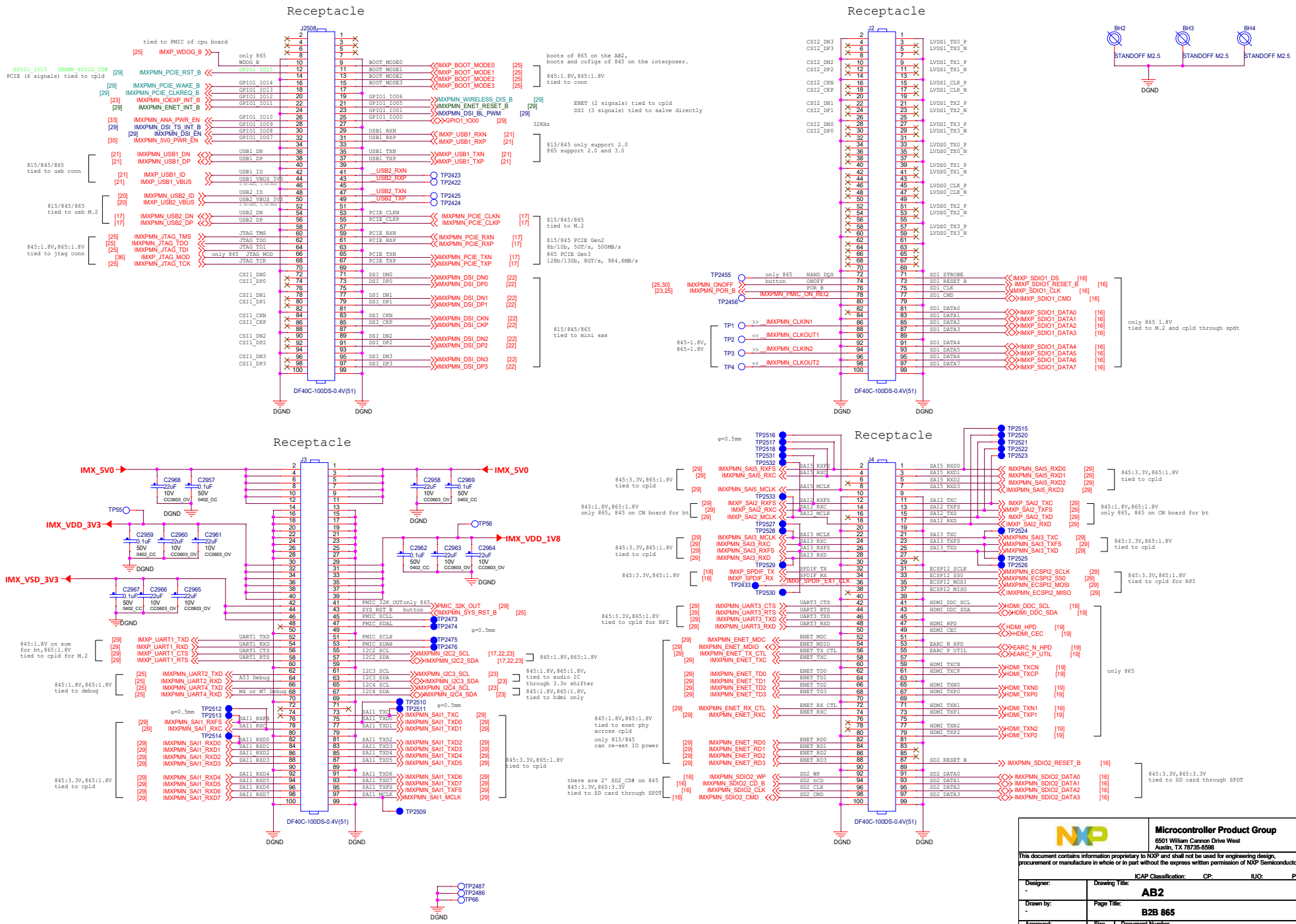
Board Configuration



NXP	**Microcontroller Product Group** 6501 William Cannon Drive West Austin, TX 78735-8598		
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.			
ICAP Classification:	CP:	IUO:	PUBI: X
Designer: -	Drawing Title: **AB2**		
Drawn by: -	Page Title: **CPLD 3**		
Approved:	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 30 of 38	

B2B Connector of 815/845/865

PIN NAME	865	845	815
BOOT_MODE0	BOOT_MODE0	BOOT_MODE0	BOOT_MODE0
BOOT_MODE1	BOOT_MODE1	BOOT_MODE1	BOOT_MODE1
BOOT_MODE2	BOOT_MODE2	JTAG TRST B	BOOT_MODE2
BOOT_MODE3	BOOT_MODE3	TEST_MODE	BOOT_MODE3



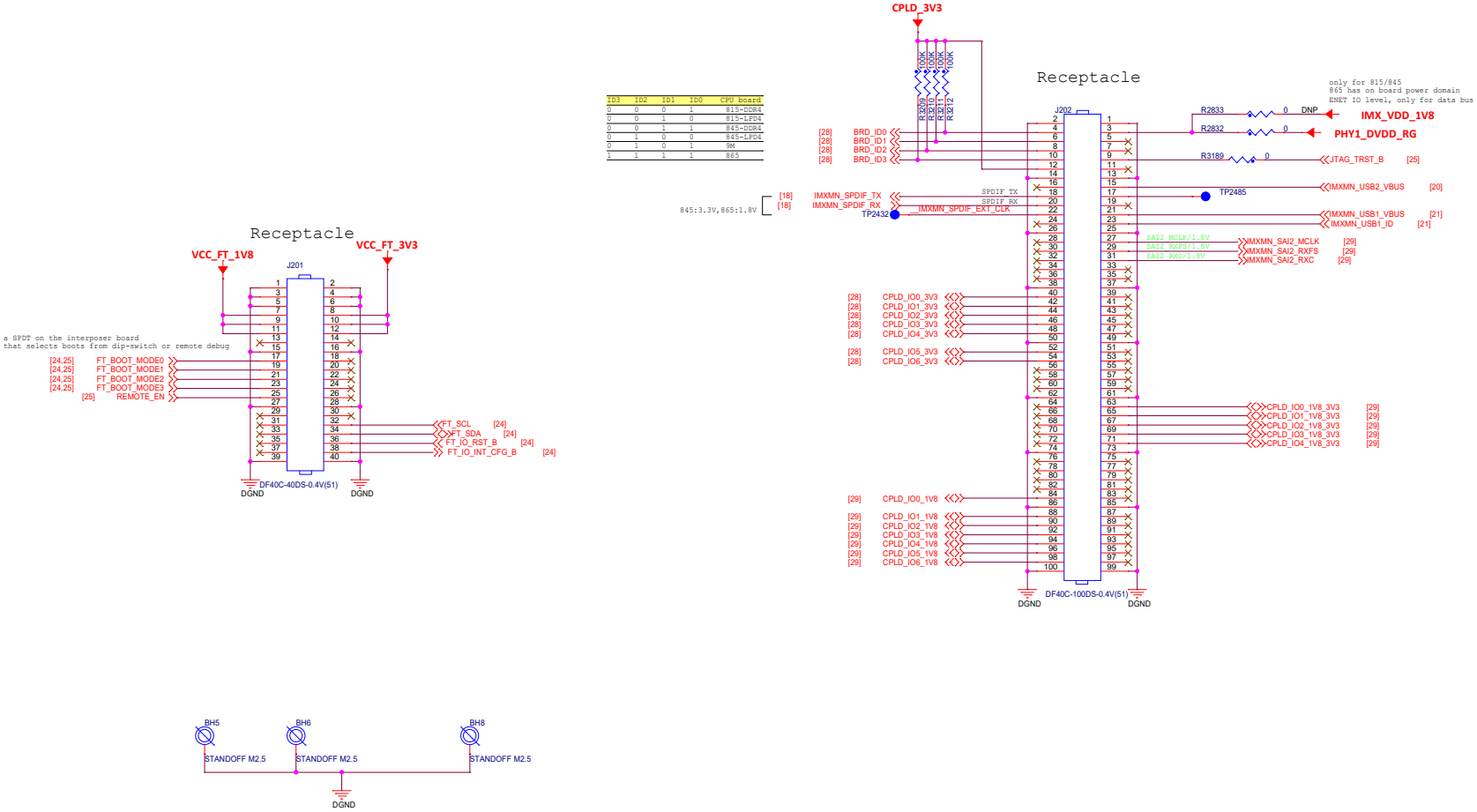
NXP	**Microcontroller Product Group** 6501 William Cannon Drive West Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: **AB2**		
Drawn by: -	Page Title: **B2B 865**		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 31 of 38	

B2B Connector of 845/815



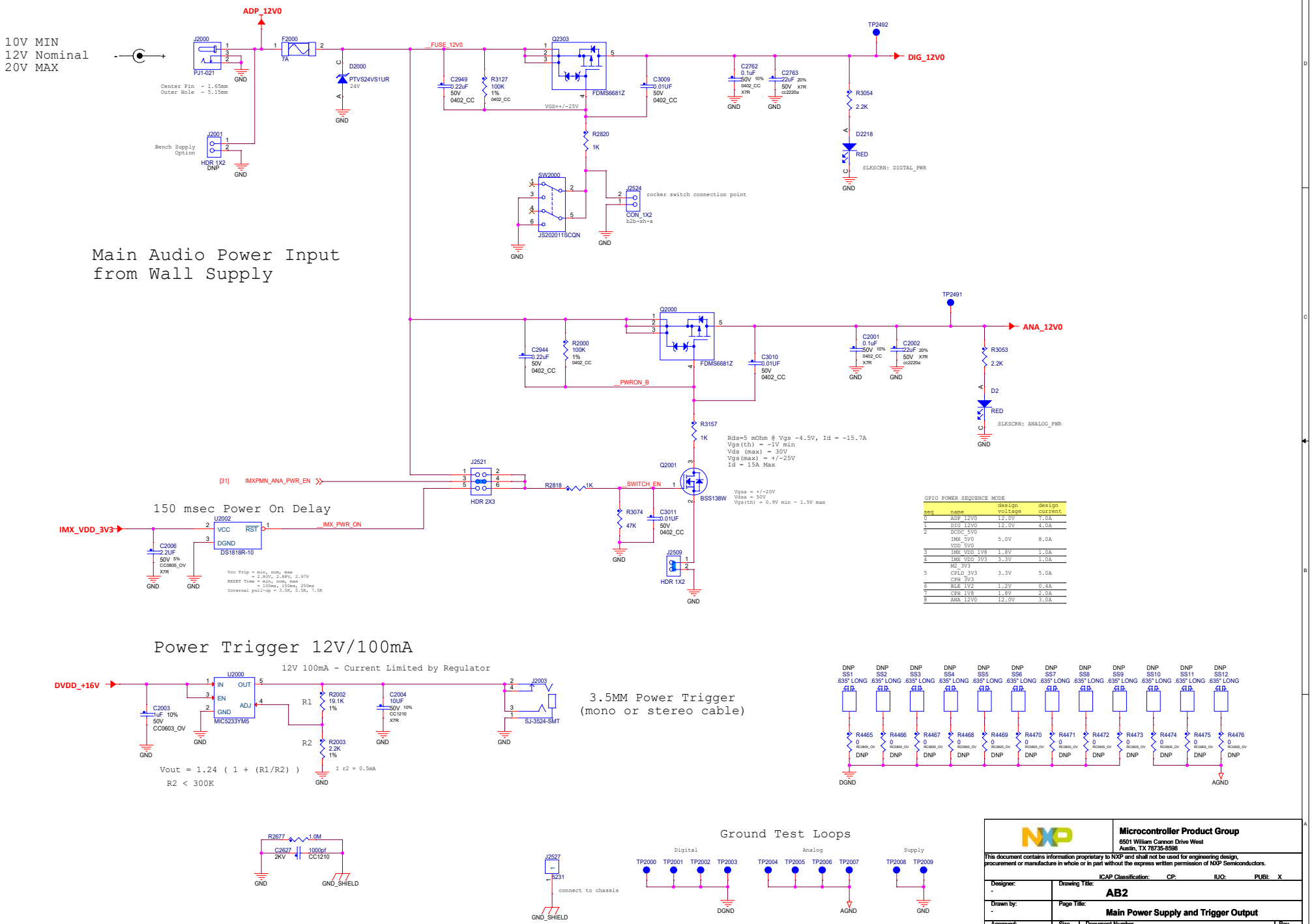
ID3	ID2	ID1	ID0	CPU board
0	0	0	1	815-DDR4
0	0	1	0	815-LPD4
0	0	1	1	845-DDR4
0	1	0	0	845-LPD4
0	1	0	1	9M
1	1	1	1	865

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

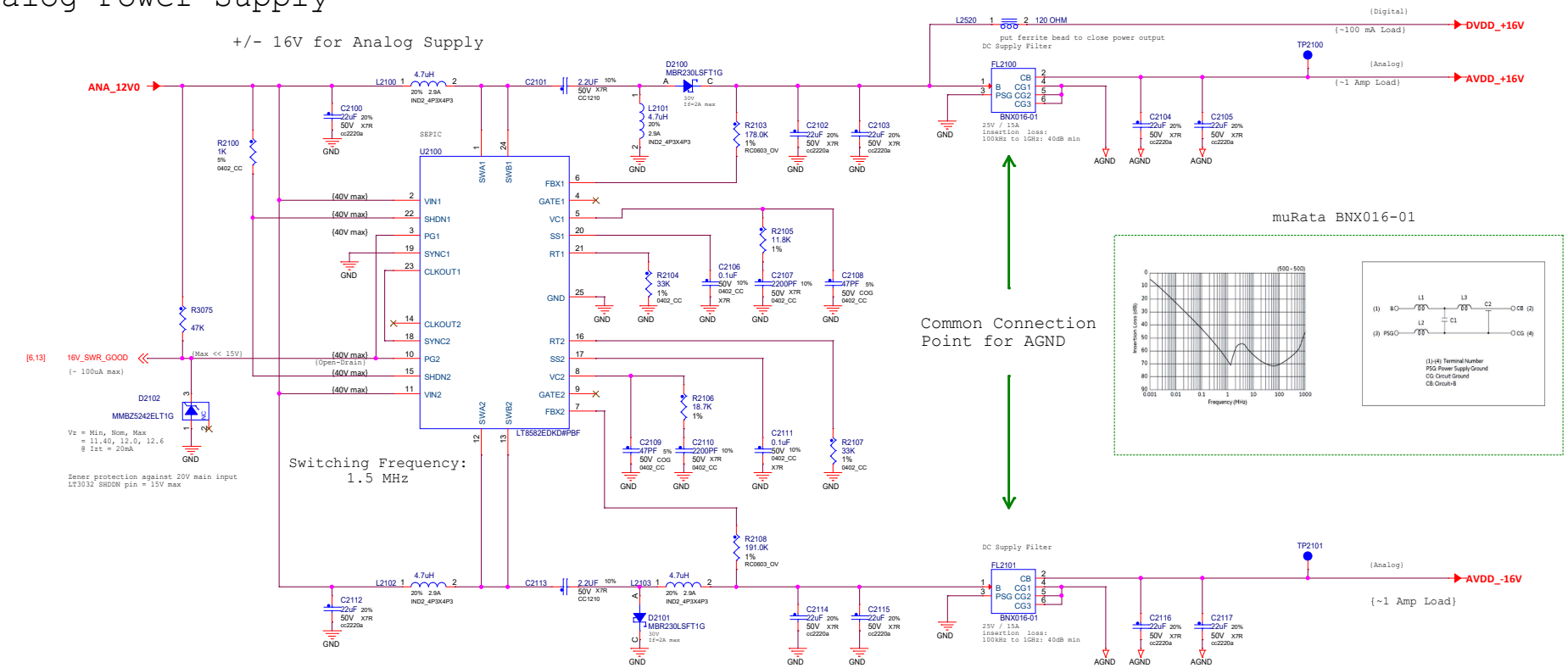
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

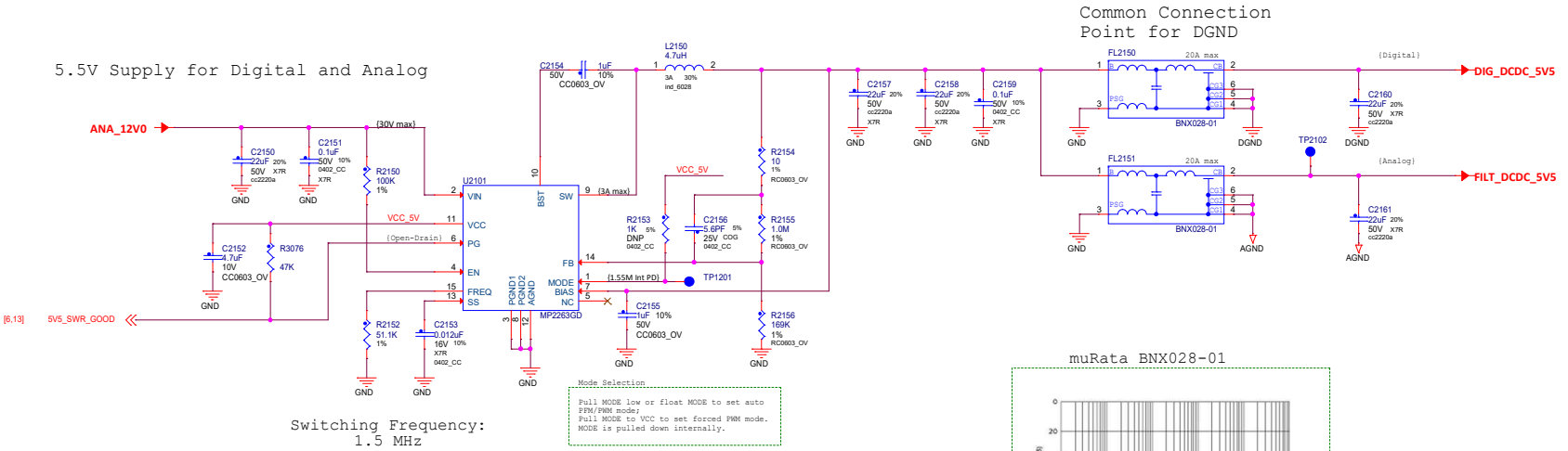
ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: B2B 845/815		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 32 of 38	


10V MIN
12V Nominal
20V MAX
ADP_12V0
J2000
PJ1-021
Center Pin - 1.65mm
Outer Hole - 5.15mm
F2000
7A
D2000
PTVS24VS1UR
24V
__FUSE_12V0
C2949
0.22uF
50V
0402_CC
R3127
100K
1%
0402_CC
Q2303
FDMS6681Z
VGS=+/-25V
C3009
0.01UF
50V
0402_CC
C2762
0.1uF
50V
0402_CC
X7R
C2763
22uF
50V
cc2220a
X7R
TP2492
DIG_12V0
R3054
2.2K
D2218
RED
SLKSCRN: DIGTAL_PWR
J2001
Bench Supply Option
HDR 1X2
DNP
R2820
1K
SW2000
JS202011SCQN
J2524
rocker switch connection point
CON_1X2
b2b-xh-a
Main Audio Power Input from Wall Supply
Q2000
FDMS6681Z
C2944
0.22uF
50V
0402_CC
R2000
100K
1%
0402_CC
__PWRON_B
C3010
0.01UF
50V
0402_CC
C2001
0.1uF
50V
0402_CC
X7R
C2002
22uF
50V
cc2220a
X7R
TP2491
ANA_12V0
R3053
2.2K
D2
RED
SLKSCRN: ANALOG_PWR
R3157
1K
Rds=5 mOhm @ Vgs -4.5V, Id = -15.7A
Vgs(th) = -1V min
Vds (max) = 30V
Vgs(max) = +/-25V
Id = 15A Max
Q2001
BSS138W
Vgss = +/-20V
Vdss = 50V
Vgs(th) = 0.9V min - 1.5V max
J2521
HDR 2X3
[31] IMXPMN_ANA_PWR_EN
R2818
1K
SWITCH_EN
R3074
47K
C3011
0.01UF
50V
0402_CC
J2509
HDR 1X2
150 msec Power On Delay
IMX_VDD_3V3
U2002
DS1818R-10
VCC
RST
DGND
__IMX_PWR_ON
C2006
2.2UF
50V
CC0805_OV
X7R
Vcc Trip = min, nom, max
= 2.80V, 2.88V, 2.97V
RESET Time = min, nom, max
= 100ms, 150ms, 250ms
Internal pull-up = 3.5K, 5.5K, 7.5K
Power Trigger 12V/100mA
12V 100mA - Current Limited by Regulator
DVDD_+16V
U2000
MIC5233YM5
IN
OUT
EN
ADJ
GND
C2003
1uF
50V
CC0603_OV
R1
R2
R2002
19.1K
1%
R2003
2.2K
1%
C2004
10UF
50V
CC1210
X7R
J2003
SJ-3524-SMT
Vout = 1.24 (1 + (R1/R2))
R2 < 300K
I r2 = 0.5mA
3.5MM Power Trigger
(mono or stereo cable)
DNP SS1 .635" LONG
DNP SS2 .635" LONG
DNP SS3 .635" LONG
DNP SS4 .635" LONG
DNP SS5 .635" LONG
DNP SS6 .635" LONG
DNP SS7 .635" LONG
DNP SS8 .635" LONG
DNP SS9 .635" LONG
DNP SS10 .635" LONG
DNP SS11 .635" LONG
DNP SS12 .635" LONG
R4465
R4466
R4467
R4468
R4469
R4470
R4471
R4472
R4473
R4474
R4475
R4476
DNP
DGND
AGND
R2677
1.0M
C2627
2KV
1000pf
CC1210
GND_SHIELD
Ground Test Loops
J2527
connect to chassis
Digital
TP2000
TP2001
TP2002
TP2003
Analog
TP2004
TP2005
TP2006
TP2007
Supply
TP2008
TP2009
GPIO POWER SEQUENCE MODE
seq | name | design voltage | design current
0 | ADP_12V0 | 12.0V | 7.0A
1 | DIG_12V0 | 12.0V | 4.0A
2 | DCDC_5V0 | | |
INX_5V0 | 5.0V | 8.0A
VDD_5V0
3 | INX_VDD_1V8 | 1.8V | 1.0A
4 | INX_VDD_3V3 | 3.3V | 1.0A
M2_3V3
5 | CPLD_3V3 | 3.3V | 5.0A
CPH_3V3
6 | BLE_1V2 | 1.2V | 0.4A
7 | CPH_1V8 | 1.8V | 2.0A
8 | ANA_12V0 | 12.0V | 3.0A
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.
ICAP Classification: CP: IUO: PUBI: X
Designer: -
Drawing Title: AB2
Drawn by: -
Page Title: Main Power Supply and Trigger Output
Approved: -
Size C
Document Number SCH-29616 PDF: SPF-29616
Rev D
Date: Wednesday, September 09, 2020
Sheet 33 of 38

Analog Power Supply





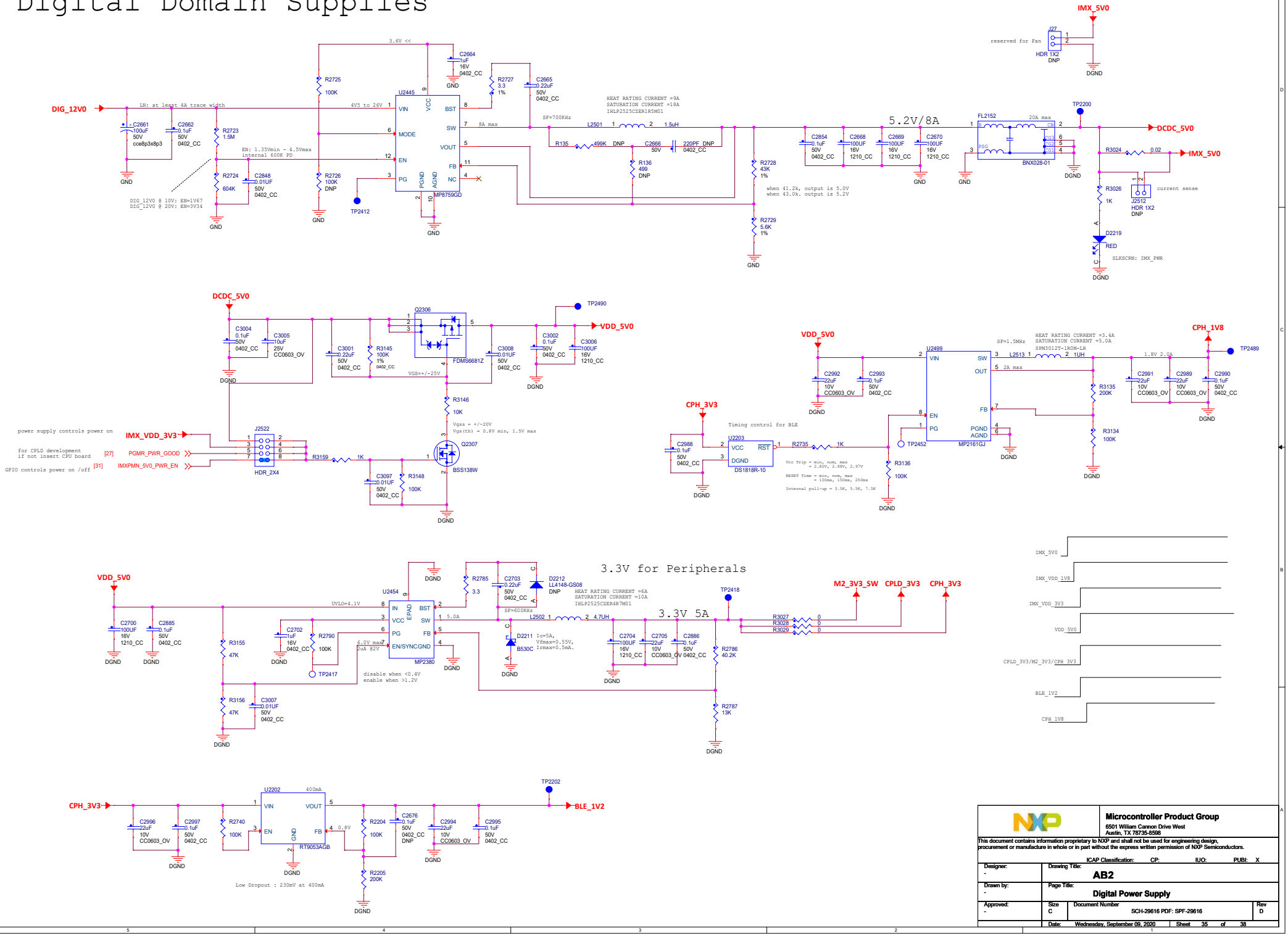
NXP	**Microcontroller Product Group** 6501 William Cannon Drive West Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: **AB2**		
Drawn by: -	Page Title: **Analog Power Supply**		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 34 of 38	

Digital Domain Supplies



NXP	Microcontroller Product Group 6501 William Cannon Drive West Austin, TX 78735-8598		
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.			
	ICAP Classification:	CP:	IUO: PUBI: X
Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: Digital Power Supply		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 35 of 38	

Boot Mode and CFG Switch

i.MX8M Plus ROM Fuse

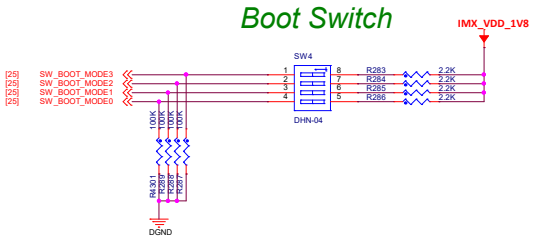
Full Line Address	Physical Address	7	6	5	4	3	2	1	0
0x470[15:0]	0x470[7:0]	OVERRIDE_NAND_PG_PER_BLK_VAL 00 - 32 pages 01 - 64 pages 10 - 128 pages 11 - 32 pages		OVERRIDE_FLEXSPI_BT_SEL 0 - Do not overriude 1 - Override	OVERRIDE_FLEXSPI_BT_SEL_VAL 00 - FlexSPI (Hyperflash 1.8V) 01 - FlexSPI (Flash with 48 READ(1x13 default supported) 10 - Default Octal mode (Micron, supported on 8QXP B0 already) 11 - Default Octal mode (Mxic, Nice to have)	FLEXSPI_AUTO_PROBE_EN 0 - Disable 1 - Enable	FLEXSPI_AUTO_PROBE_TYPE 00 - QuadSPI NOR 01 - MxicOctal 10 - MicronOctal 11 - AdestoOctal	
0x480[15:0]	0x480[7:0]	Reserved	FLEXSPI_DUMMY_CYCLE_SEL				FLEXSPI_FEQ_SEL 000 - 100 MHz 001 - 133 MHz 010 - 166 MHz 011 - 200 MHz 100 - 80 MHz 101 - 20 MHz		
0x480[31:16]	0x480[23:16]	NOC_ID_REMAP_BYPASS	ROM_NO_LOG if blown, ROM will not log event to log buffer	SDP_DISABLE Disable USB serial download	FORCE_BT_FROM_FUSE Boot from programmed fuses, not Boot Mode Pins	FLEXSPI_HOLD_TIME_SEL 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		WDOG_TIMEOUT_SELECT 00 - 2.0s 01 - 1.5s 10 - 1.0s 11 - 0.5s	
0x490[15:0]	0x490[7:0]	USDHC_PWR_EN 0 - No power cycle 1 - Enabled via	EMMC_FAST_BT 0 - Regular 1 - Fast Boot	SDMMC_BUS_WIDTH 00 - 8-bit 01 - 4-bit 10 - 8-bit DDR (MMC 4.4) 11 - 4-bit DDR (MMC 4.4)		SD_SPEED: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104	EMMC_SPEED: 00 - Normal 01 - High	USDHC_VOL_SEL For Normal Boot Mode IO Voltage 0 - 3.3V 1 - 1.8V	USDHC_MFG_VOL_SEL For Mfg Mode IO Voltage 0 - 3.3V 1 - 1.8V
0x490[31:16]	0x490[23:16]	RECOVERY_SDMMC_BOOT_DIS 0 - Enable 1 - Disable	IMG_CNTN_SET1_OFFSET				USDHC_PAD_SION_EN 0 - Disable 1 - Enable	Reserved	USDHC_DLL_EN 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eMMC
0x4A0[15:0]	0x4A0[7:0]	SD_CALI_STEP '00' - 1 TBD	USDHC_PWR_INTERVAL 00 - 20ms 01 - 10ms 10 - 5ms 11 - 2.5			USDHC_PWR_DELAY 0 - 5ms 1 - 2.5ms	USDHC_PWR_POLARITY 0 - Low 1 - High	USDHC_OVRD_PAD_SETTING_UP1	EMMC_FAST_BT_ACK 0 - Boot Ack Disabled 1 - Boot Ack Enabled
0x4A0[31:16]	0x4A0[23:16]	Reserved							
0x4B0[15:0]	0x4B0[7:0]	Reserved	NAND_GPMI_DDR_DLL_VAL (GPMI Read DDR DLL Target Value) 0000 - 7 0001 - 1 0111 - 0 1111 - 15					Reserved	NAND_CS_NUM (Nand Number Of Devices) 00 - 1 01 - 2 10 - 4 11 - Reserved
0x4B0[31:16]	0x4B0[23:16]	Reserved	FlexSPI NAND Busy Bit Offset Override			FlexSPI NAND CS Interval 00-100ns 01-200ns 10-400ns 11-50ns		FlexSPI NAND Column Address Width 00-12 01-13 10-14 11-15	

Full Line Address	Physical Address	7	6	5	4	3	2	1	0
0x470[15:0]	0x470[15:8]	BOOT_MODE_FUSES BootRom will retrieve boot mode from these fuses instead of BOOT_MODE pins if * BOOT_MODE_PINS=0x0 or * BT_FUSE_SEL blown				OVERRIDE_USDHC_BT_SEL 0 - Do not override 1 - Override	OVERRIDE_USDHC_BT_SEL_VAL 00 - uSDHC1 SD 01 - uSDHC1 eMMC 10 - uSDHC2 eMMC 11 - uSDHC3 SD		OVERRIDE_NAND_PG_PER_BLK 0 - Do not override 1 - Override
0x480[15:0]	0x480[15:8]	BT_LPB (Core/DDR/Bus) '00'/'01' - LPB Disable '10' - Div by2 '11' - Div by 4		BT_LPB_POLARITY (GPIO polarity)	ICACHE_DIS L1 I-Cache DISABLE	TZASC_EN	WDOG_EN '0' - Disabled '1' - Enabled	BT_FREQ_SEL (ARM/DDR) 0 - 800 / 800 MHz 1 - 400 / 400 MHz	DCACHE_DIS Disable L1 and L2 D-Cache
0x480[31:16]	0x480[31:24]	ECSPI_PORT_SEL 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3		ECSPI_ADDR_SEL 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)	ECSPI_CS_SEL(SPI only) 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		RECOVER_ECSPI_BOOT_EN '0' - Disabled '1' - Enabled		DCACHE_BYPASS_DIS
0x490[15:0]	0x490[15:8]	USDHC_DLL_SEL 0 - DLL Slave Mode for 1 - DLL Override Mode	SDMMC_DLL_DLY[6:0] Delay target for USDHC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						
0x490[31:16]	0x490[31:24]	USDHC_OVRD_PAD_SETTING_LOW8[7:0]							
0x4A0[15:0]	0x4A0[15:8]	BT_TOGGLE_MODE	NAND_FCB_SERCH_COUNT 00 - 2 01 - 2 10 - 4 11 - 8		NAND_TG_PREAMBLE_RD_LATENCY (Toggle Mode 33MHz Preamble Delay, Read Latency) '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111'- 15 GPMICLK cycles.				NAND_RST_TIME
0x4A0[31:16]	0x4A0[31:24]	NAND_OVERRIDE_PAD_SETTING[7:0]							
0x4B0[15:0]	0x4B0[15:8]	NAND_READ_RETRY_SEQ_ID[3:0] 0000 - don't use read retry(RR) sequence embedded in ROM 0001 - Micron 20nm RR sequence 0010 - Toshiba A19nm RR sequence 0011 - Toshiba 19nm RR sequence 0100 - SanDisk 19nm RR sequence 0101 - SanDisk 1ynmRR sequence 0110 - Hynix 20nm A Die RR sequence 0111 - Hynix 26nm RR sequence 1000 - Hynix 20nm B Die RR sequence 1001 - Hynix 20nm C Die RR sequence Others - Reserved				NAND_ROW_ADDR_BYTES 00 - 3 01 - 2 10 - 4 11 - 5		Reserved	Reserved
0x4B0[31:16]	0x4B0[31:24]	RNG_TRIM[7:0]							

i.MX8M Plus Boot Mode

BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	Boot Modes
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	***0***	***1***	***0***	***USDHC3 (eMMC boot only, SD3 8-bit) Default***
0	0	1	1	USDHC2 (SD boot only, SD2)
0	1	0	0	NAND 8-bit single device 256 page
0	1	0	1	NAND 8-bit single device 512 page
0	1	1	0	QSPI 3B Read
0	1	1	1	QSPI Hyperflash 3.3V
1	0	0	0	ecSPI Boot
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Boot Switch



BSDL Mode Switch

Caution:
BOOT_MODE0, BOOT_MODE1, BOOT_MODE2, BOOT_MODE3, JTAG_MOD and POR_B must be pulled to "111111" for i.MX8M Plus to enter Boundary Scan mode.

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: X PUBL

Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: BOOT CFG		
Approved: <Approver>	Size A2	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 38 of 38	

i.MX 8M MINI IOMUX

NAME	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
TEST_MODE	tcu.TEST_MODE	tcu.TEST_MODE							
BOOT_MODE0	ccmsrcgpcmix.BOOT_MODE[0]	ccmsrcgpcmix.BOOT_MODE[0]							
BOOT_MODE1	ccmsrcgpcmix.BOOT_MODE[1]	ccmsrcgpcmix.BOOT_MODE[1]							
JTAG_MOD	cjtag_wrapper.MOD	cjtag_wrapper.MOD							
JTAG_TRST_B	cjtag_wrapper.TRST_B	cjtag_wrapper.TRST_B							
JTAG_TDI	cjtag_wrapper.TDI	cjtag_wrapper.TDI							
JTAG_TMS	cjtag_wrapper.TMS	cjtag_wrapper.TMS							
JTAG_TCK	cjtag_wrapper.TCK	cjtag_wrapper.TCK							
JTAG_TDO	cjtag_wrapper.TDO	cjtag_wrapper.TDO							
RTC_XTALI	snvsmix.RTC	snvsmix.RTC							
RTC_XTALO									
PMIC_STBY_REQ	ccmsrcgpcmix.PMIC_STBY_REQ	ccmsrcgpcmix.PMIC_STBY_REQ							
PMIC_ON_REQ	snvsmix.PMIC_ON_REQ	snvsmix.PMIC_ON_REQ							
ONOFF	snvsmix.ONOFF	snvsmix.ONOFF							
POR_B	snvsmix.POR_B	snvsmix.POR_B							
RTC_RESET_B	snvsmix.RTC_POR_B	snvsmix.RTC_RESET_B							
GPIO1_IO00	gpio1.IO[0]	gpio1.IO[0]	ccmsrcgpcmix.ENET_PHY_REF_CLK_ROOT				anamix.REF_CLK_32K	reserved	reserved
GPIO1_IO01	gpio1.IO[1]	gpio1.IO[1]	pwm1.OUT				anamix.REF_CLK_24M	reserved	reserved
GPIO1_IO02	gpio1.IO[2]	gpio1.IO[2]	wdog1.WDOG_B				wdog1.WDOG_ANY		reserved
GPIO1_IO03	gpio1.IO[3]	gpio1.IO[3]	usdhc1.VSELECT				sdma1.EXT_EVENT[0]	reserved	reserved
GPIO1_IO04	gpio1.IO[4]	gpio1.IO[4]	usdhc2.VSELECT				sdma1.EXT_EVENT[1]	reserved	reserved
GPIO1_IO05	gpio1.IO[5]	gpio1.IO[5]	m4.NMI				ccmsrcgpcmix.PMIC_READY	reserved	reserved
GPIO1_IO06	gpio1.IO[6]	gpio1.IO[6]	enet1.MDC				usdhc1.CD_B	reserved	reserved
GPIO1_IO07	gpio1.IO[7]	gpio1.IO[7]	enet1.MDIO				usdhc1.WP	reserved	reserved
GPIO1_IO08	gpio1.IO[8]	gpio1.IO[8]	enet1.1588_EVENT0_IN				usdhc2.RESET_B	reserved	reserved
GPIO1_IO09	gpio1.IO[9]	gpio1.IO[9]	enet1.1588_EVENT0_OUT			usdhc3.RESET_B	sdma2.EXT_EVENT[0]	reserved	reserved
GPIO1_IO10	gpio1.IO[10]	gpio1.IO[10]	usb1.OTG_ID						reserved
GPIO1_IO11	gpio1.IO[11]	gpio1.IO[11]	usb2.OTG_ID			usdhc3.VSELECT	ccmsrcgpcmix.PMIC_READY	reserved	reserved
GPIO1_IO12	gpio1.IO[12]	gpio1.IO[12]	usb1.OTG_PWR				sdma2.EXT_EVENT[1]	reserved	reserved
GPIO1_IO13	gpio1.IO[13]	gpio1.IO[13]	usb1.OTG_OC				pwm2.OUT	reserved	reserved
GPIO1_IO14	gpio1.IO[14]	gpio1.IO[14]	usb2.OTG_PWR			usdhc3.CD_B	pwm3.OUT	reserved	reserved
GPIO1_IO15	gpio1.IO[15]	gpio1.IO[15]	usb2.OTG_OC			usdhc3.WP	pwm4.OUT	reserved	reserved
ENET_MDC	gpio1.IO[16]	enet1.MDC					gpio1.IO[16]		
ENET_MDIO	gpio1.IO[17]	enet1.MDIO					gpio1.IO[17]		
ENET_TD3	gpio1.IO[18]	enet1.RGMII_TD3					gpio1.IO[18]		
ENET_TD2	gpio1.IO[19]	enet1.RGMII_TD2	"INPUT=enet1.TX_CLK OUTPUT=ccmsrcgpcmix.ENET_REF_CLK_ROOT"				gpio1.IO[19]		
ENET_TD1	gpio1.IO[20]	enet1.RGMII_TD1					gpio1.IO[20]		
ENET_TD0	gpio1.IO[21]	enet1.RGMII_TD0					gpio1.IO[21]		
ENET_TX_CTL	gpio1.IO[22]	enet1.RGMII_TX_CTL					gpio1.IO[22]		
ENET_TXC	gpio1.IO[23]	enet1.RGMII_TXC	enet1.TX_ER				gpio1.IO[23]		
ENET_RX_CTL	gpio1.IO[24]	enet1.RGMII_RX_CTL					gpio1.IO[24]		
ENET_RXC	gpio1.IO[25]	enet1.RGMII_RXC	enet1.RX_ER				gpio1.IO[25]		
ENET_RD0	gpio1.IO[26]	enet1.RGMII_RD0					gpio1.IO[26]		
ENET_RD1	gpio1.IO[27]	enet1.RGMII_RD1					gpio1.IO[27]		
ENET_RD2	gpio1.IO[28]	enet1.RGMII_RD2					gpio1.IO[28]		
ENET_RD3	gpio1.IO[29]	enet1.RGMII_RD3					gpio1.IO[29]		
SD1_CLK	gpio2.IO[0]	usdhc1.CLK					gpio2.IO[0]		
SD1_CMD	gpio2.IO[1]	usdhc1.CMD					gpio2.IO[1]		
SD1_DATA0	gpio2.IO[2]	usdhc1.DATA0					gpio2.IO[2]		
SD1_DATA1	gpio2.IO[3]	usdhc1.DATA1					gpio2.IO[3]		
SD1_DATA2	gpio2.IO[4]	usdhc1.DATA2					gpio2.IO[4]		
SD1_DATA3	gpio2.IO[5]	usdhc1.DATA3					gpio2.IO[5]		
SD1_DATA4	gpio2.IO[6]	usdhc1.DATA4					gpio2.IO[6]		
SD1_DATA5	gpio2.IO[7]	usdhc1.DATA5					gpio2.IO[7]		
SD1_DATA6	gpio2.IO[8]	usdhc1.DATA6					gpio2.IO[8]		
SD1_DATA7	gpio2.IO[9]	usdhc1.DATA7					gpio2.IO[9]		
SD1_RESET_B	gpio2.IO[10]	usdhc1.RESET_B					gpio2.IO[10]		
SD1_STROBE	gpio2.IO[11]	usdhc1.STROBE					gpio2.IO[11]		
SD2_CD_B	gpio2.IO[12]	usdhc2.CD_B					gpio2.IO[12]		
SD2_CLK	gpio2.IO[13]	usdhc2.CLK					gpio2.IO[13]	reserved	reserved
SD2_CMD	gpio2.IO[14]	usdhc2.CMD					gpio2.IO[14]	reserved	reserved
SD2_DATA0	gpio2.IO[15]	usdhc2.DATA0					gpio2.IO[15]	reserved	reserved
SD2_DATA1	gpio2.IO[16]	usdhc2.DATA1					gpio2.IO[16]	reserved	reserved
SD2_DATA2	gpio2.IO[17]	usdhc2.DATA2					gpio2.IO[17]	reserved	reserved
SD2_DATA3	gpio2.IO[18]	usdhc2.DATA3					gpio2.IO[18]	reserved	
SD2_RESET_B	gpio2.IO[19]	usdhc2.RESET_B					gpio2.IO[19]	reserved	
SD2_WP	gpio2.IO[20]	usdhc2.WP					gpio2.IO[20]		reserved
NAND_ALE	gpio3.IO[0]	rawnand.ALE	qspi.A_SCLK				gpio3.IO[0]		reserved
NAND_CE0_B	gpio3.IO[1]	rawnand.CE0_B	qspi.A_SS0_B				gpio3.IO[1]		reserved
NAND_CE1_B	gpio3.IO[2]	rawnand.CE1_B	qspi.A_SS1_B	usdhc3.STROBE			gpio3.IO[2]		reserved
NAND_CE2_B	gpio3.IO[3]	rawnand.CE2_B	qspi.B_SS0_B	usdhc3.DATA5			gpio3.IO[3]		reserved
NAND_CE3_B	gpio3.IO[4]	rawnand.CE3_B	qspi.B_SS1_B	usdhc3.DATA6			gpio3.IO[4]		reserved
NAND_CLE	gpio3.IO[5]	rawnand.CLE	qspi.B_SCLK	usdhc3.DATA7			gpio3.IO[5]		reserved
NAND_DATA00	gpio3.IO[6]	rawnand.DATA00	qspi.A_DATA[0]				gpio3.IO[6]		reserved
NAND_DATA01	gpio3.IO[7]	rawnand.DATA01	qspi.A_DATA[1]				gpio3.IO[7]		reserved
NAND_DATA02	gpio3.IO[8]	rawnand.DATA02	qspi.A_DATA[2]	usdhc3.CD_B			gpio3.IO[8]		reserved
NAND_DATA03	gpio3.IO[9]	rawnand.DATA03	qspi.A_DATA[3]	usdhc3.WP			gpio3.IO[9]		reserved
NAND_DATA04	gpio3.IO[10]	rawnand.DATA04	qspi.B_DATA[0]	usdhc3.DATA0			gpio3.IO[10]		reserved
NAND_DATA05	gpio3.IO[11]	rawnand.DATA05	qspi.B_DATA[1]	usdhc3.DATA1			gpio3.IO[11]		reserved
NAND_DATA06	gpio3.IO[12]	rawnand.DATA06	qspi.B_DATA[2]	usdhc3.DATA2			gpio3.IO[12]		reserved
NAND_DATA07	gpio3.IO[13]	rawnand.DATA07	qspi.B_DATA[3]	usdhc3.DATA3			gpio3.IO[13]		reserved
NAND_DQS	gpio3.IO[14]	rawnand.DQS	qspi.A_DQS				gpio3.IO[14]		reserved
NAND_RE_B	gpio3.IO[15]	rawnand.RE_B	qspi.B_DQS	usdhc3.DATA4			gpio3.IO[15]		reserved
NAND_READY_B	gpio3.IO[16]	rawnand.READY_B		usdhc3.RESET_B			gpio3.IO[16]		reserved
NAND_WE_B	gpio3.IO[17]	rawnand.WE_B		usdhc3.CLK			gpio3.IO[17]		reserved
NAND_WP_B	gpio3.IO[18]	rawnand.WP_B		usdhc3.CMD			gpio3.IO[18]		reserved
SAI5_RXFS	gpio3.IO[19]	sai5.RX_SYNC	sai1.TX_DATA[0]				gpio3.IO[19]		reserved
SAI5_RXC	gpio3.IO[20]	sai5.RX_BCLK	sai1.TX_DATA[1]			pdm.CLK	gpio3.IO[20]		reserved
SAI5_RXD0	gpio3.IO[21]	sai5.RX_DATA[0]	sai1.TX_DATA[2]			pdm.BIT_STREAM[0]	gpio3.IO[21]		
SAI5_RXD1	gpio3.IO[22]	sai5.RX_DATA[1]	sai1.TX_DATA[3]	sai1.TX_SYNC	sai5.TX_SYNC	pdm.BIT_STREAM[1]	gpio3.IO[22]		
SAI5_RXD2	gpio3.IO[23]	sai5.RX_DATA[2]	sai1.TX_DATA[4]	sai1.TX_SYNC	sai5.TX_BCLK	pdm.BIT_STREAM[2]	gpio3.IO[23]		
SAI5_RXD3	gpio3.IO[24]	sai5.RX_DATA[3]	sai1.TX_DATA[5]	sai1.TX_SYNC	sai5.TX_DATA[0]	pdm.BIT_STREAM[3]	gpio3.IO[24]		
SAI5_MCLK	gpio3.IO[25]	sai5.MCLK	sai1.TX_BCLK				gpio3.IO[25]	reserved	
SAI1_RXFS	gpio4.IO[0]	sai1.RX_SYNC	sai5.RX_SYNC			coresight.TRACE_CLK	gpio4.IO[0]		reserved
SAI1_RXC	gpio4.IO[1]	sai1.RX_BCLK	sai5.RX_BCLK			coresight.TRACE_CTL	gpio4.IO[1]		reserved
SAI1_RXD0	gpio4.IO[2]	sai1.RX_DATA[0]	sai5.RX_DATA[0]	sai1.TX_DATA[1]	pdm.BIT_STREAM[0]	coresight.TRACE[0]	gpio4.IO[2]	ccmsrcgpcmix.BOOT_CFG[0]	reserved
SAI1_RXD1	gpio4.IO[3]	sai1.RX_DATA[1]	sai5.RX_DATA[1]		pdm.BIT_STREAM[1]	coresight.TRACE[1]	gpio4.IO[3]	ccmsrcgpcmix.BOOT_CFG[1]	reserved
SAI1_RXD2	gpio4.IO[4]	sai1.RX_DATA[2]	sai5.RX_DATA[2]		pdm.BIT_STREAM[2]	coresight.TRACE[2]	gpio4.IO[4]	ccmsrcgpcmix.BOOT_CFG[2]	reserved
SAI1_RXD3	gpio4.IO[5]	sai1.RX_DATA[3]	sai5.RX_DATA[3]		pdm.BIT_STREAM[3]	coresight.TRACE[3]	gpio4.IO[5]	ccmsrcgpcmix.BOOT_CFG[3]	reserved
SAI1_RXD4	gpio4.IO[6]	sai1.RX_DATA[4]	sai6.TX_BCLK	sai6.RX_BCLK		coresight.TRACE[4]	gpio4.IO[6]	ccmsrcgpcmix.BOOT_CFG[4]	reserved
SAI1_RXD5	gpio4.IO[7]	sai1.RX_DATA[5]	sai6.TX_DATA[0]	sai6.RX_DATA[0]	sai1.RX_SYNC	coresight.TRACE[5]	gpio4.IO[7]	ccmsrcgpcmix.BOOT_CFG[5]	reserved
SAI1_RXD6	gpio4.IO[8]	sai1.RX_DATA[6]	sai6.TX_SYNC	sai6.RX_SYNC		coresight.TRACE[6]	gpio4.IO[8]	ccmsrcgpcmix.BOOT_CFG[6]	reserved
SAI1_RXD7	gpio4.IO[9]	sai1.RX_DATA[7]	sai6.MCLK	sai1.TX_SYNC	sai1.TX_DATA[4]	coresight.TRACE[7]	gpio4.IO[9]	ccmsrcgpcmix.BOOT_CFG[7]	reserved
SAI1_TXFS	gpio4.IO[10]	sai1.TX_SYNC	sai5.TX_SYNC			coresight.EVENTO	gpio4.IO[10]		reserved
SAI1_TXC	gpio4.IO[11]	sai1.TX_BCLK	sai5.TX_BCLK			coresight.EVENT1	gpio4.IO[11]		reserved
SAI1_TXD0	gpio4.IO[12]	sai1.TX_DATA[0]	sai5.TX_DATA[0]			coresight.TRACE[8]	gpio4.IO[12]	ccmsrcgpcmix.BOOT_CFG[8]	reserved
SAI1_TXD1	gpio4.IO[13]	sai1.TX_DATA[1]	sai5.TX_DATA[1]			coresight.TRACE[9]	gpio4.IO[13]	ccmsrcgpcmix.BOOT_CFG[9]	reserved
SAI1_TXD2	gpio4.IO[14]	sai1.TX_DATA[2]	sai5.TX_DATA[2]			coresight.TRACE[10]	gpio4.IO[14]	ccmsrcgpcmix.BOOT_CFG[10]	reserved
SAI1_TXD3	gpio4.IO[15]	sai1.TX_DATA[3]	sai5.TX_DATA[3]			coresight.TRACE[11]	gpio4.IO[15]	ccmsrcgpcmix.BOOT_CFG[11]	reserved
SAI1_TXD4	gpio4.IO[16]	sai1.TX_DATA[4]	sai6.RX_BCLK	sai6.TX_BCLK		coresight.TRACE[12]	gpio4.IO[16]	ccmsrcgpcmix.BOOT_CFG[12]	reserved
SAI1_TXD5	gpio4.IO[17]	sai1.TX_DATA[5]	sai6.RX_DATA[0]	sai6.TX_DATA[0]		coresight.TRACE[13]	gpio4.IO[17]	ccmsrcgpcmix.BOOT_CFG[13]	reserved
SAI1_TXD6	gpio4.IO[18]	sai1.TX_DATA[6]	sai6.RX_SYNC	sai6.TX_SYNC		coresight.TRACE[14]	gpio4.IO[18]	ccmsrcgpcmix.BOOT_CFG[14]	reserved
SAI1_TXD7	gpio4.IO[19]	sai1.TX_DATA[7]	sai6.MCLK		pdm.CLK	coresight.TRACE[15]	gpio4.IO[19]	ccmsrcgpcmix.BOOT_CFG[15]	reserved
SAI1_MCLK	gpio4.IO[20]	sai1.MCLK	sai5.MCLK	sai1.TX_BCLK	pdm.CLK		gpio4.IO[20]		reserved
SAI2_RXFS	gpio4.IO[21]	sai2.RX_SYNC	sai5.TX_SYNC	sai5.TX_DATA[1]	sai2.RX_DATA[1]	uart1.TX	gpio4.IO[21]		reserved
SAI2_RXC	gpio4.IO[22]	sai2.RX_BCLK	sai5.TX_BCLK			uart1.RX	gpio4.IO[22]		reserved
SAI2_RXD0	gpio4.IO[23]	sai2.RX_DATA[0]	sai5.TX_DATA[0]			uart1.RTS_B	gpio4.IO[23]		reserved
SAI2_TXFS	gpio4.IO[24]	sai2.TX_SYNC	sai5.TX_DATA[1]		sai2.TX_DATA[1]	uart1.CTS_B	gpio4.IO[24]		reserved
SAI2_TXC	gpio4.IO[25]	sai2.TX_BCLK	sai5.TX_DATA[2]				gpio4.IO[25]		reserved
SAI2_TXD0	gpio4.IO[26]	sai2.TX_DATA[0]	sai5.TX_DATA[3]				gpio4.IO[26]		reserved
SAI2_MCLK	gpio4.IO[27]	sai2.MCLK	sai5.MCLK				gpio4.IO[27]		reserved
SAI3_RXFS	gpio4.IO[28]	sai3.RX_SYNC	gpt1.CAPTURE1	sai5.RX_SYNC	sai3.RX_DATA[1]		gpio4.IO[28]		reserved
SAI3_RXC	gpio4.IO[29]	sai3.RX_BCLK	gpt1.CLK	sai5.RX_BCLK		uart2.CTS_B	gpio4.IO[29]		reserved
SAI3_RXD	gpio4.IO[30]	sai3.RX_DATA[0]	gpt1.COMPARE1	sai5.RX_DATA[0]		uart2.RTS_B	gpio4.IO[30]		reserved
SAI3_TXFS	gpio4.IO[31]	sai3.TX_SYNC	gpt1.CAPTURE2	sai5.RX_DATA[1]	sai3.TX_DATA[1]	uart2.RX	gpio4.IO[31]		reserved
SAI3_TXC	gpio5.IO[0]	sai3.TX_BCLK	gpt1.COMPARE2	sai5.RX_DATA[2]		uart2.TX	gpio5.IO[0]		reserved
SAI3_TXD	gpio5.IO[1]	sai3.TX_DATA[0]	gpt1.COMPARE3	sai5.RX_DATA[3]			gpio5.IO[1]		reserved
SAI3_MCLK	gpio5.IO[2]	sai3.MCLK	pwm4.OUT	sai5.MCLK			gpio5.IO[2]		reserved
SPDIF_TX	gpio5.IO[3]	spdif1.OUT	pwm3.OUT				gpio5.IO[3]		reserved
SPDIF_RX	gpio5.IO[4]	spdif1.IN	pwm2.OUT				gpio5.IO[4]		reserved
SPDIF_EXT_CLK	gpio5.IO[5]	spdif1.EXT_CLK	pwm1.OUT				gpio5.IO[5]		reserved
ECSPI1_SCLK	gpio5.IO[6]	ecspi1.SCLK	uart3.RX				gpio5.IO[6]		reserved
ECSPI1_MOSI	gpio5.IO[7]	ecspi1.MOSI	uart3.TX				gpio5.IO[7]		reserved
ECSPI1_MISO	gpio5.IO[8]	ecspi1.MISO	uart3.CTS_B				gpio5.IO[8]		reserved
ECSPI1_SS0	gpio5.IO[9]	ecspi1.SS0	uart3.RTS_B				gpio5.IO[9]		reserved
ECSPI2_SCLK	gpio5.IO[10]	ecspi2.SCLK	uart4.RX				gpio5.IO[10]		reserved
ECSPI2_MOSI	gpio5.IO[11]	ecspi2.MOSI	uart4.TX				gpio5.IO[11]		reserved
ECSPI2_MISO	gpio5.IO[12]	ecspi2.MISO	uart4.CTS_B				gpio5.IO[12]		reserved
ECSPI2_SS0	gpio5.IO[13]	ecspi2.SS0	uart4.RTS_B				gpio5.IO[13]		reserved
I2C1_SCL	gpio5.IO[14]	i2c1.SCL	enet1.MDC				gpio5.IO[14]		reserved
I2C1_SDA	gpio5.IO[15]	i2c1.SDA	enet1.MDIO				gpio5.IO[15]		reserved
I2C2_SCL	gpio5.IO[16]	i2c2.SCL	enet1.1588_EVENT1_IN	usdhc3.CD_B			gpio5.IO[16]		reserved
I2C2_SDA	gpio5.IO[17]	i2c2.SDA	enet1.1588_EVENT1_OUT	usdhc3.WP			gpio5.IO[17]		reserved
I2C3_SCL	gpio5.IO[18]	i2c3.SCL	pwm4.OUT	gpt2.CLK			gpio5.IO[18]		reserved
I2C3_SDA	gpio5.IO[19]	i2c3.SDA	pwm3.OUT	gpt3.CLK			gpio5.IO[19]		reserved
I2C4_SCL	gpio5.IO[20]	i2c4.SCL	pwm2.OUT	pcie1.CLKREQ_B			gpio5.IO[20]		reserved
I2C4_SDA	gpio5.IO[21]	i2c4.SDA	pwm1.OUT				gpio5.IO[21]		reserved
UART1_RXD	gpio5.IO[22]	uart1.RX	ecspi3.SCLK				gpio5.IO[22]		reserved
UART1_TXD	gpio5.IO[23]	uart1.TX	ecspi3.MOSI				gpio5.IO[23]		reserved
UART2_RXD	gpio5.IO[24]	uart2.RX	ecspi3.MISO				gpio5.IO[24]		reserved
UART2_TXD	gpio5.IO[25]	uart2.TX	ecspi3.SS0				gpio5.IO[25]		reserved
UART3_RXD	gpio5.IO[26]	uart3.RX	uart1.CTS_B	usdhc3.RESET_B			gpio5.IO[26]		reserved
UART3_TXD	gpio5.IO[27]	uart3.TX	uart1.RTS_B	usdhc3.VSELECT			gpio5.IO[27]		reserved
UART4_RXD	gpio5.IO[28]	uart4.RX	uart2.CTS_B	pcie1.CLKREQ_B			gpio5.IO[28]		reserved
UART4_TXD	gpio5.IO[29]	uart4.TX	uart2.RTS_B				gpio5.IO[29]		reserved
CLKIN1		anamix.CLKIN1							
CLKIN2		anamix.CLKIN2							
CLKOUT1		anamix.CLKOUT1							
CLKOUT2		anamix.CLKOUT2							
XTALI_24M		anamix.xtal_24M							
XTALO_24M									

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: i.MX 8M MINI IOMUX		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 37 of 38	

i.MX 8M QUAD IOMUX

NAME	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
TEST_MODE	tcu.TEST_MODE	tcu.TEST_MODE							
BOOT_MODE0	ccmsrcgpcmix.BOOT_MODE[0]	ccmsrcgpcmix.BOOT_MODE[0]							
BOOT_MODE1	ccmsrcgpcmix.BOOT_MODE[1]	ccmsrcgpcmix.BOOT_MODE[1]							
JTAG_MOD	cjtag_wrapper.MOD	cjtag_wrapper.MOD							
JTAG_TRST_B	cjtag_wrapper.TRST_B	cjtag_wrapper.TRST_B							
JTAG_TDI	cjtag_wrapper.TDI	cjtag_wrapper.TDI							
JTAG_TMS	cjtag_wrapper.TMS	cjtag_wrapper.TMS							
JTAG_TCK	cjtag_wrapper.TCK	cjtag_wrapper.TCK							
JTAG_TDO	cjtag_wrapper.TDO	cjtag_wrapper.TDO							
RTC	snvsmix.RTC	snvsmix.RTC							
PMIC_STBY_REQ	ccmsrcgpcmix.PMIC_STBY_REQ	ccmsrcgpcmix.PMIC_STBY_REQ							
PMIC_ON_REQ	snvsmix.PMIC_ON_REQ	snvsmix.PMIC_ON_REQ							
ONOFF	snvsmix.ONOFF	snvsmix.ONOFF							
POR_B	snvsmix.POR_B	snvsmix.POR_B							
RTC_RESET_B	snvsmix.RTC_POR_B	snvsmix.RTC_RESET_B							
GPIO1_IO00	gpio1.IO[0]	gpio1.IO[0]	ccmsrcgpcmix.ENET_PHY_REF_CLK_ROOT				anamix.REF_CLK_32K	ccmsrcgpcmix.EXT_CLK1	reserved
GPIO1_IO01	gpio1.IO[1]	gpio1.IO[1]	pwm1.OUT				anamix.REF_CLK_24M	ccmsrcgpcmix.EXT_CLK2	reserved
GPIO1_IO02	gpio1.IO[2]	gpio1.IO[2]	wdog1.WDOG_B				wdog1.WDOG_ANY		reserved
GPIO1_IO03	gpio1.IO[3]	gpio1.IO[3]	usdhc1.VSELECT				sdma1.EXT_EVENT[0]	reserved	reserved
GPIO1_IO04	gpio1.IO[4]	gpio1.IO[4]	usdhc2.VSELECT				sdma1.EXT_EVENT[1]	reserved	reserved
GPIO1_IO05	gpio1.IO[5]	gpio1.IO[5]	m4.NMI				ccmsrcgpcmix.PMIC_READY	reserved	reserved
GPIO1_IO06	gpio1.IO[6]	gpio1.IO[6]	enet1.MDC				usdhc1.CD_B	ccmsrcgpcmix.EXT_CLK3	reserved
GPIO1_IO07	gpio1.IO[7]	gpio1.IO[7]	enet1.MDIO				usdhc1.WP	ccmsrcgpcmix.EXT_CLK4	reserved
GPIO1_IO08	gpio1.IO[8]	gpio1.IO[8]	enet1.1588_EVENT0_IN				usdhc2.RESET_B	reserved	reserved
GPIO1_IO09	gpio1.IO[9]	gpio1.IO[9]	enet1.1588_EVENT0_OUT				sdma2.EXT_EVENT[0]	reserved	reserved
GPIO1_IO10	gpio1.IO[10]	gpio1.IO[10]	usb1.OTG_ID						reserved
GPIO1_IO11	gpio1.IO[11]	gpio1.IO[11]	usb2.OTG_ID				ccmsrcgpcmix.PMIC_READY	reserved	reserved
GPIO1_IO12	gpio1.IO[12]	gpio1.IO[12]	usb1.OTG_PWR				sdma2.EXT_EVENT[1]	reserved	reserved
GPIO1_IO13	gpio1.IO[13]	gpio1.IO[13]	usb1.OTG_OC				pwm2.OUT	reserved	reserved
GPIO1_IO14	gpio1.IO[14]	gpio1.IO[14]	usb2.OTG_PWR				pwm3.OUT	ccmsrcgpcmix.CLKO1	reserved
GPIO1_IO15	gpio1.IO[15]	gpio1.IO[15]	usb2.OTG_OC				pwm4.OUT	ccmsrcgpcmix.CLKO2	reserved
ENET_MDC	gpio1.IO[16]	enet1.MDC					gpio1.IO[16]		
ENET_MDIO	gpio1.IO[17]	enet1.MDIO					gpio1.IO[17]		
ENET_TD3	gpio1.IO[18]	enet1.RGMII_TD3					gpio1.IO[18]		
ENET_TD2	gpio1.IO[19]	enet1.RGMII_TD2	"INPUT=enet1.TX_CLK OUTPUT=ccmsrcgpcmix.ENET_REF_CLK_ROOT"				gpio1.IO[19]		
ENET_TD1	gpio1.IO[20]	enet1.RGMII_TD1					gpio1.IO[20]		
ENET_TD0	gpio1.IO[21]	enet1.RGMII_TD0					gpio1.IO[21]		
ENET_TX_CTL	gpio1.IO[22]	enet1.RGMII_TX_CTL					gpio1.IO[22]		
ENET_TXC	gpio1.IO[23]	enet1.RGMII_TXC	enet1.TX_ER				gpio1.IO[23]		
ENET_RX_CTL	gpio1.IO[24]	enet1.RGMII_RX_CTL					gpio1.IO[24]		
ENET_RXC	gpio1.IO[25]	enet1.RGMII_RXC	enet1.RX_ER				gpio1.IO[25]		
ENET_RD0	gpio1.IO[26]	enet1.RGMII_RD0					gpio1.IO[26]		
ENET_RD1	gpio1.IO[27]	enet1.RGMII_RD1					gpio1.IO[27]		
ENET_RD2	gpio1.IO[28]	enet1.RGMII_RD2					gpio1.IO[28]		
ENET_RD3	gpio1.IO[29]	enet1.RGMII_RD3					gpio1.IO[29]		
SD1_CLK	gpio2.IO[0]	usdhc1.CLK					gpio2.IO[0]		
SD1_CMD	gpio2.IO[1]	usdhc1.CMD					gpio2.IO[1]		
SD1_DATA0	gpio2.IO[2]	usdhc1.DATA0					gpio2.IO[2]		
SD1_DATA1	gpio2.IO[3]	usdhc1.DATA1					gpio2.IO[3]		
SD1_DATA2	gpio2.IO[4]	usdhc1.DATA2					gpio2.IO[4]		
SD1_DATA3	gpio2.IO[5]	usdhc1.DATA3					gpio2.IO[5]		
SD1_DATA4	gpio2.IO[6]	usdhc1.DATA4					gpio2.IO[6]		
SD1_DATA5	gpio2.IO[7]	usdhc1.DATA5					gpio2.IO[7]		
SD1_DATA6	gpio2.IO[8]	usdhc1.DATA6					gpio2.IO[8]		
SD1_DATA7	gpio2.IO[9]	usdhc1.DATA7					gpio2.IO[9]		
SD1_RESET_B	gpio2.IO[10]	usdhc1.RESET_B					gpio2.IO[10]		
SD1_STROBE	gpio2.IO[11]	usdhc1.STROBE					gpio2.IO[11]		
SD2_CD_B	gpio2.IO[12]	usdhc2.CD_B					gpio2.IO[12]		
SD2_CLK	gpio2.IO[13]	usdhc2.CLK					gpio2.IO[13]	reserved	reserved
SD2_CMD	gpio2.IO[14]	usdhc2.CMD					gpio2.IO[14]	reserved	reserved
SD2_DATA0	gpio2.IO[15]	usdhc2.DATA0					gpio2.IO[15]	reserved	reserved
SD2_DATA1	gpio2.IO[16]	usdhc2.DATA1					gpio2.IO[16]	reserved	reserved
SD2_DATA2	gpio2.IO[17]	usdhc2.DATA2					gpio2.IO[17]	reserved	reserved
SD2_DATA3	gpio2.IO[18]	usdhc2.DATA3					gpio2.IO[18]	reserved	
SD2_RESET_B	gpio2.IO[19]	usdhc2.RESET_B					gpio2.IO[19]	reserved	
SD2_WP	gpio2.IO[20]	usdhc2.WP					gpio2.IO[20]		reserved
NAND_ALE	gpio3.IO[0]	rawnand.ALE	qspi1.A_SCLK				gpio3.IO[0]		reserved
NAND_CE0_B	gpio3.IO[1]	rawnand.CE0_B	qspi1.A_SS0_B				gpio3.IO[1]		reserved
NAND_CE1_B	gpio3.IO[2]	rawnand.CE1_B	qspi1.A_SS1_B				gpio3.IO[2]		reserved
NAND_CE2_B	gpio3.IO[3]	rawnand.CE2_B	qspi1.B_SS0_B				gpio3.IO[3]		reserved
NAND_CE3_B	gpio3.IO[4]	rawnand.CE3_B	qspi1.B_SS1_B				gpio3.IO[4]		reserved
NAND_CLE	gpio3.IO[5]	rawnand.CLE	qspi1.B_SCLK				gpio3.IO[5]		reserved
NAND_DATA00	gpio3.IO[6]	rawnand.DATA00	qspi1.A_DATA[0]				gpio3.IO[6]		reserved
NAND_DATA01	gpio3.IO[7]	rawnand.DATA01	qspi1.A_DATA[1]				gpio3.IO[7]		reserved
NAND_DATA02	gpio3.IO[8]	rawnand.DATA02	qspi1.A_DATA[2]				gpio3.IO[8]		reserved
NAND_DATA03	gpio3.IO[9]	rawnand.DATA03	qspi1.A_DATA[3]				gpio3.IO[9]		reserved
NAND_DATA04	gpio3.IO[10]	rawnand.DATA04	qspi1.B_DATA[0]				gpio3.IO[10]		reserved
NAND_DATA05	gpio3.IO[11]	rawnand.DATA05	qspi1.B_DATA[1]				gpio3.IO[11]		reserved
NAND_DATA06	gpio3.IO[12]	rawnand.DATA06	qspi1.B_DATA[2]				gpio3.IO[12]		reserved
NAND_DATA07	gpio3.IO[13]	rawnand.DATA07	qspi1.B_DATA[3]				gpio3.IO[13]		reserved
NAND_DQS	gpio3.IO[14]	rawnand.DQS	qspi1.A_DQS				gpio3.IO[14]		reserved
NAND_RE_B	gpio3.IO[15]	rawnand.RE_B	qspi1.B_DQS				gpio3.IO[15]		reserved
NAND_READY_B	gpio3.IO[16]	rawnand.READY_B					gpio3.IO[16]		reserved
NAND_WE_B	gpio3.IO[17]	rawnand.WE_B					gpio3.IO[17]		reserved
NAND_WP_B	gpio3.IO[18]	rawnand.WP_B					gpio3.IO[18]		reserved
SAI5_RXFS	gpio3.IO[19]	sai5.RX_SYNC	sai1.TX_DATA[0]				gpio3.IO[19]		
SAI5_RXC	gpio3.IO[20]	sai5.RX_BCLK	sai1.TX_DATA[1]				gpio3.IO[20]		
SAI5_RXD0	gpio3.IO[21]	sai5.RX_DATA[0]	sai1.TX_DATA[2]				gpio3.IO[21]		
SAI5_RXD1	gpio3.IO[22]	sai5.RX_DATA[1]	sai1.TX_DATA[3]	sai1.TX_SYNC	sai5.TX_SYNC		gpio3.IO[22]		
SAI5_RXD2	gpio3.IO[23]	sai5.RX_DATA[2]	sai1.TX_DATA[4]	sai1.TX_SYNC	sai5.TX_BCLK		gpio3.IO[23]		
SAI5_RXD3	gpio3.IO[24]	sai5.RX_DATA[3]	sai1.TX_DATA[5]	sai1.TX_SYNC	sai5.TX_DATA[0]		gpio3.IO[24]		
SAI5_MCLK	gpio3.IO[25]	sai5.MCLK	sai1.TX_BCLK	sai4.MCLK			gpio3.IO[25]	reserved	
SAI1_RXFS	gpio4.IO[0]	sai1.RX_SYNC	sai5.RX_SYNC			coresight.TRACE_CLK	gpio4.IO[0]		reserved
SAI1_RXC	gpio4.IO[1]	sai1.RX_BCLK	sai5.RX_BCLK			coresight.TRACE_CTL	gpio4.IO[1]		reserved
SAI1_RXD0	gpio4.IO[2]	sai1.RX_DATA[0]	sai5.RX_DATA[0]			coresight.TRACE[0]	gpio4.IO[2]	ccmsrcgpcmix.BOOT_CFG[0]	reserved
SAI1_RXD1	gpio4.IO[3]	sai1.RX_DATA[1]	sai5.RX_DATA[1]			coresight.TRACE[1]	gpio4.IO[3]	ccmsrcgpcmix.BOOT_CFG[1]	reserved
SAI1_RXD2	gpio4.IO[4]	sai1.RX_DATA[2]	sai5.RX_DATA[2]			coresight.TRACE[2]	gpio4.IO[4]	ccmsrcgpcmix.BOOT_CFG[2]	reserved
SAI1_RXD3	gpio4.IO[5]	sai1.RX_DATA[3]	sai5.RX_DATA[3]			coresight.TRACE[3]	gpio4.IO[5]	ccmsrcgpcmix.BOOT_CFG[3]	reserved
SAI1_RXD4	gpio4.IO[6]	sai1.RX_DATA[4]	sai6.TX_BCLK	sai6.RX_BCLK		coresight.TRACE[4]	gpio4.IO[6]	ccmsrcgpcmix.BOOT_CFG[4]	reserved
SAI1_RXD5	gpio4.IO[7]	sai1.RX_DATA[5]	sai6.TX_DATA[0]	sai6.RX_DATA[0]	sai1.RX_SYNC	coresight.TRACE[5]	gpio4.IO[7]	ccmsrcgpcmix.BOOT_CFG[5]	reserved
SAI1_RXD6	gpio4.IO[8]	sai1.RX_DATA[6]	sai6.TX_SYNC	sai6.RX_SYNC		coresight.TRACE[6]	gpio4.IO[8]	ccmsrcgpcmix.BOOT_CFG[6]	reserved
SAI1_RXD7	gpio4.IO[9]	sai1.RX_DATA[7]	sai6.MCLK	sai1.TX_SYNC	sai1.TX_DATA[4]	coresight.TRACE[7]	gpio4.IO[9]	ccmsrcgpcmix.BOOT_CFG[7]	reserved
SAI1_TXFS	gpio4.IO[10]	sai1.TX_SYNC	sai5.TX_SYNC			coresight.EVENTO	gpio4.IO[10]		reserved
SAI1_TXC	gpio4.IO[11]	sai1.TX_BCLK	sai5.TX_BCLK			coresight.EVENTI	gpio4.IO[11]		reserved
SAI1_TXD0	gpio4.IO[12]	sai1.TX_DATA[0]	sai5.TX_DATA[0]			coresight.TRACE[8]	gpio4.IO[12]	ccmsrcgpcmix.BOOT_CFG[8]	reserved
SAI1_TXD1	gpio4.IO[13]	sai1.TX_DATA[1]	sai5.TX_DATA[1]			coresight.TRACE[9]	gpio4.IO[13]	ccmsrcgpcmix.BOOT_CFG[9]	reserved
SAI1_TXD2	gpio4.IO[14]	sai1.TX_DATA[2]	sai5.TX_DATA[2]			coresight.TRACE[10]	gpio4.IO[14]	ccmsrcgpcmix.BOOT_CFG[10]	reserved
SAI1_TXD3	gpio4.IO[15]	sai1.TX_DATA[3]	sai5.TX_DATA[3]			coresight.TRACE[11]	gpio4.IO[15]	ccmsrcgpcmix.BOOT_CFG[11]	reserved
SAI1_TXD4	gpio4.IO[16]	sai1.TX_DATA[4]	sai6.RX_BCLK	sai6.TX_BCLK		coresight.TRACE[12]	gpio4.IO[16]	ccmsrcgpcmix.BOOT_CFG[12]	reserved
SAI1_TXD5	gpio4.IO[17]	sai1.TX_DATA[5]	sai6.RX_DATA[0]	sai6.TX_DATA[0]		coresight.TRACE[13]	gpio4.IO[17]	ccmsrcgpcmix.BOOT_CFG[13]	reserved
SAI1_TXD6	gpio4.IO[18]	sai1.TX_DATA[6]	sai6.RX_SYNC	sai6.TX_SYNC		coresight.TRACE[14]	gpio4.IO[18]	ccmsrcgpcmix.BOOT_CFG[14]	reserved
SAI1_TXD7	gpio4.IO[19]	sai1.TX_DATA[7]	sai6.MCLK			coresight.TRACE[15]	gpio4.IO[19]	ccmsrcgpcmix.BOOT_CFG[15]	reserved
SAI1_MCLK	gpio4.IO[20]	sai1.MCLK	sai5.MCLK	sai1.TX_BCLK			gpio4.IO[20]		reserved
SAI2_RXFS	gpio4.IO[21]	sai2.RX_SYNC	sai5.TX_SYNC				gpio4.IO[21]		reserved
SAI2_RXC	gpio4.IO[22]	sai2.RX_BCLK	sai5.TX_BCLK				gpio4.IO[22]		reserved
SAI2_RXD0	gpio4.IO[23]	sai2.RX_DATA[0]	sai5.TX_DATA[0]				gpio4.IO[23]		reserved
SAI2_RXD1	gpio4.IO[24]	sai2.RX_DATA[1]	sai5.TX_DATA[1]				gpio4.IO[24]		reserved
SAI2_TXC	gpio4.IO[25]	sai2.TX_BCLK	sai5.TX_DATA[2]				gpio4.IO[25]		reserved
SAI2_TXD0	gpio4.IO[26]	sai2.TX_DATA[0]	sai5.TX_DATA[3]				gpio4.IO[26]		reserved
SAI2_MCLK	gpio4.IO[27]	sai2.MCLK	sai5.MCLK				gpio4.IO[27]		reserved
SAI3_RXFS	gpio4.IO[28]	sai3.RX_SYNC	gpt1.CAPTURE1	sai5.RX_SYNC			gpio4.IO[28]		reserved
SAI3_RXC	gpio4.IO[29]	sai3.RX_BCLK	gpt1.CAPTURE2	sai5.RX_BCLK			gpio4.IO[29]		reserved
SAI3_RXD	gpio4.IO[30]	sai3.RX_DATA[0]	gpt1.COMPARE1	sai5.RX_DATA[0]			gpio4.IO[30]		reserved
SAI3_TXFS	gpio4.IO[31]	sai3.TX_SYNC	gpt1.CLK	sai5.RX_DATA[1]			gpio4.IO[31]		reserved
SAI3_TXC	gpio5.IO[0]	sai3.TX_BCLK	gpt1.COMPARE2	sai5.RX_DATA[2]			gpio5.IO[0]		reserved
SAI3_TXD	gpio5.IO[1]	sai3.TX_DATA[0]	gpt1.COMPARE3	sai5.RX_DATA[3]			gpio5.IO[1]		reserved
SAI3_MCLK	gpio5.IO[2]	sai3.MCLK	pwm4.OUT	sai5.MCLK			gpio5.IO[2]		reserved
SPDIF_TX	gpio5.IO[3]	spdif1.OUT	pwm3.OUT				gpio5.IO[3]		reserved
SPDIF_RX	gpio5.IO[4]	spdif1.IN	pwm2.OUT				gpio5.IO[4]		reserved
SPDIF_EXT_CLK	gpio5.IO[5]	spdif1.EXT_CLK	pwm1.OUT				gpio5.IO[5]		reserved
ECSPI1_SCLK	gpio5.IO[6]	ecspi1.SCLK	uart3.RX				gpio5.IO[6]		reserved
ECSPI1_MOSI	gpio5.IO[7]	ecspi1.MOSI	uart3.TX				gpio5.IO[7]		reserved
ECSPI1_MISO	gpio5.IO[8]	ecspi1.MISO	uart3.CTS_B				gpio5.IO[8]		reserved
ECSPI1_SS0	gpio5.IO[9]	ecspi1.SS0	uart3.RTS_B				gpio5.IO[9]		reserved
ECSPI2_SCLK	gpio5.IO[10]	ecspi2.SCLK	uart4.RX				gpio5.IO[10]		reserved
ECSPI2_MOSI	gpio5.IO[11]	ecspi2.MOSI	uart4.TX				gpio5.IO[11]		reserved
ECSPI2_MISO	gpio5.IO[12]	ecspi2.MISO	uart4.CTS_B				gpio5.IO[12]		reserved
ECSPI2_SS0	gpio5.IO[13]	ecspi2.SS0	uart4.RTS_B				gpio5.IO[13]		reserved
I2C1_SCL	gpio5.IO[14]	i2c1.SCL	enet1.MDC				gpio5.IO[14]		reserved
I2C1_SDA	gpio5.IO[15]	i2c1.SDA	enet1.MDIO				gpio5.IO[15]		reserved
I2C2_SCL	gpio5.IO[16]	i2c2.SCL	enet1.1588_EVENT1_IN				gpio5.IO[16]		reserved
I2C2_SDA	gpio5.IO[17]	i2c2.SDA	enet1.1588_EVENT1_OUT				gpio5.IO[17]		reserved
I2C3_SCL	gpio5.IO[18]	i2c3.SCL	pwm4.OUT	gpt2.CLK			gpio5.IO[18]		reserved
I2C3_SDA	gpio5.IO[19]	i2c3.SDA	pwm3.OUT	gpt3.CLK			gpio5.IO[19]		reserved
I2C4_SCL	gpio5.IO[20]	i2c4.SCL	pwm2.OUT	pcie1.CLKREQ_B			gpio5.IO[20]		reserved
I2C4_SDA	gpio5.IO[21]	i2c4.SDA	pwm1.OUT	pcie2.CLKREQ_B			gpio5.IO[21]		reserved
UART1_RXD	gpio5.IO[22]	uart1.RX	ecspi3.SCLK				gpio5.IO[22]		reserved
UART1_TXD	gpio5.IO[23]	uart1.TX	ecspi3.MOSI				gpio5.IO[23]		reserved
UART2_RXD	gpio5.IO[24]	uart2.RX	ecspi3.MISO				gpio5.IO[24]		reserved
UART2_TXD	gpio5.IO[25]	uart2.TX	ecspi3.SS0				gpio5.IO[25]		reserved
UART3_RXD	gpio5.IO[26]	uart3.RX	uart1.CTS_B				gpio5.IO[26]		reserved
UART3_TXD	gpio5.IO[27]	uart3.TX	uart1.RTS_B				gpio5.IO[27]		reserved
UART4_RXD	gpio5.IO[28]	uart4.RX	uart2.CTS_B	pcie1.CLKREQ_B			gpio5.IO[28]		reserved
UART4_TXD	gpio5.IO[29]	uart4.TX	uart2.RTS_B	pcie2.CLKREQ_B			gpio5.IO[29]		reserved
CLK1_P									
CLK1_N									
CLK2_P									
CLK2_N									
XTALI_25M									
XTALO_25M									
XTALI_27M									
XTALO_27M									

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: PUBI: X

Designer: -	Drawing Title: AB2		
Drawn by: -	Page Title: i.MX 8M QUAD IOMUX		
Approved: -	Size C	Document Number SCH-29616 PDF: SPF-29616	Rev D
	Date: Wednesday, September 09, 2020	Sheet 38 of 38	