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## Change list

| | |
|---|---|
| A1 | 1. Add 2x10 male JTAG header J12 for zigbe module |
| | 2. Separate CT pins of magnetic U1/U2 to save several mA current |
| | 3. Change MPC8308 pin Y23 from NC to VDD (net VCORE) per latest MPC8308EC Rev 2 |
| | 4. Remove DNP pull up resistors R42/R43 on net MDIO |
| | 5. EMI consideration<br>1) Change R140 from DNP to populate<br>2) Change C75/C78/C80/C93 from DNP to populate<br>3) Change C121/C122 decoupling capacitors for PHY VDDH from 0.1uF to 100pF<br>4) Add 18pF capacitors C359/C360 to GND on net TSEC1_GTX_CLK25 & TSEC2_GTX_CLK25<br>5) Change terminated series resistors R36/R37 on net G1_RX_CLK & G2_RX_CLK from 0ohm to 22ohm, add series bead L32/L31 and 18pF capacitors C363/C362 to GND<br>6) Add series bead L30/L31 and 18pF capacitors C361/C362 to GND on net G1_GTX_CLK & G2_GTX_CLK<br>7) Add bead L34/L35 on U6/U7 pin3 VDD33<br>8) Swap MDI interface on magnetic U1/U2 |
| | 6. Remove test point TP1~TP2, TP6~TP8, TP10~TP16, TP21, TP22, TP18 for layout space limitation |

## Revisions

| Rev | Description | Date | Approved |
|---|---|---|---|
| A | Release Rev. A | April 6,11 | |
| A1 | Add 2X10 JTAG Header for Zigbee Module<br>Changes for EMI consideration. Details refer to A1 change list. | June 24,11 | |
| B | Release Rev. B | June 30,11 | |

# MPC8308 - NSG


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Networking & Multimedia Group
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Austin, TX 78735-8598



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| | | |
|---|---|---|
| Designer: James Zhang | Drawing Title: MPC8308 - NSG | |
| Drawn by: James Zhang | Page Title: TITLE PAGE | |
| Approved: Tanis Qiu | Size: C | Document Number: SCH-27072 PDF: SPF-27072 — Rev: B |
| | Date: Thursday, June 30, 2011 | Sheet 1 of 11 |

ecified:
ohms

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   # Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

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Drawing Title: **MPC8308 - NSG**

Page Title: **NOTES**

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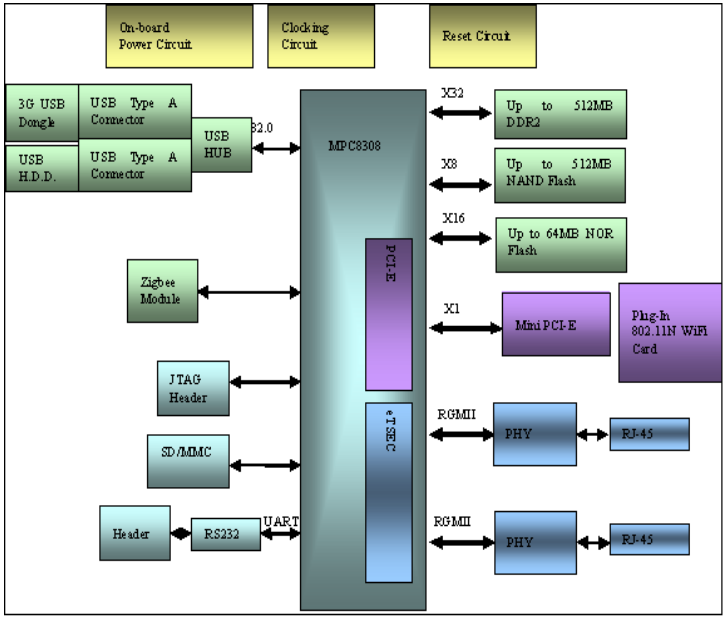


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Drawing Title:
**MPC8308 - NSG**

Page Title:
**BLOCK**

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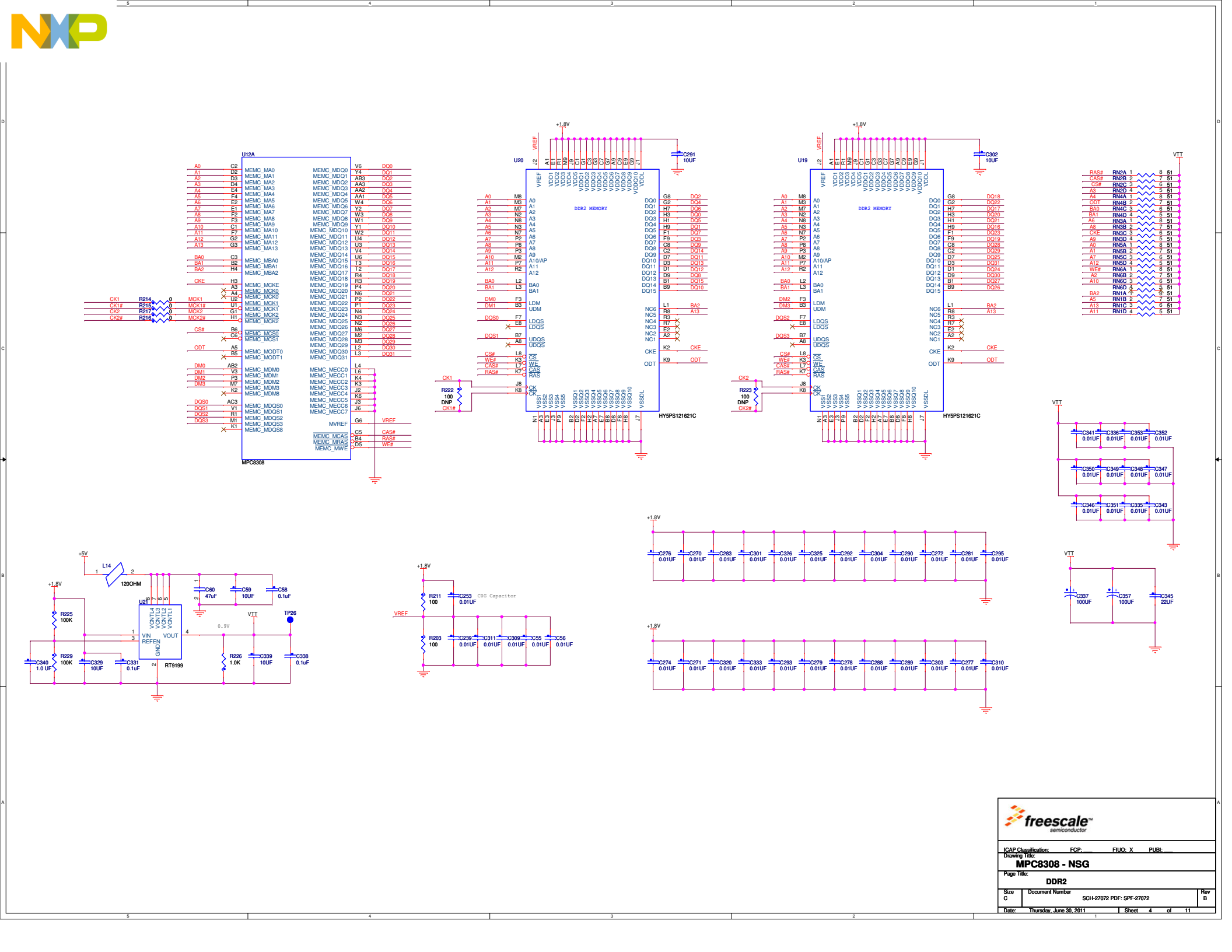


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| Size: C | Document Number: SCH-27072 PDF: SPF-27072 | | Rev: B |
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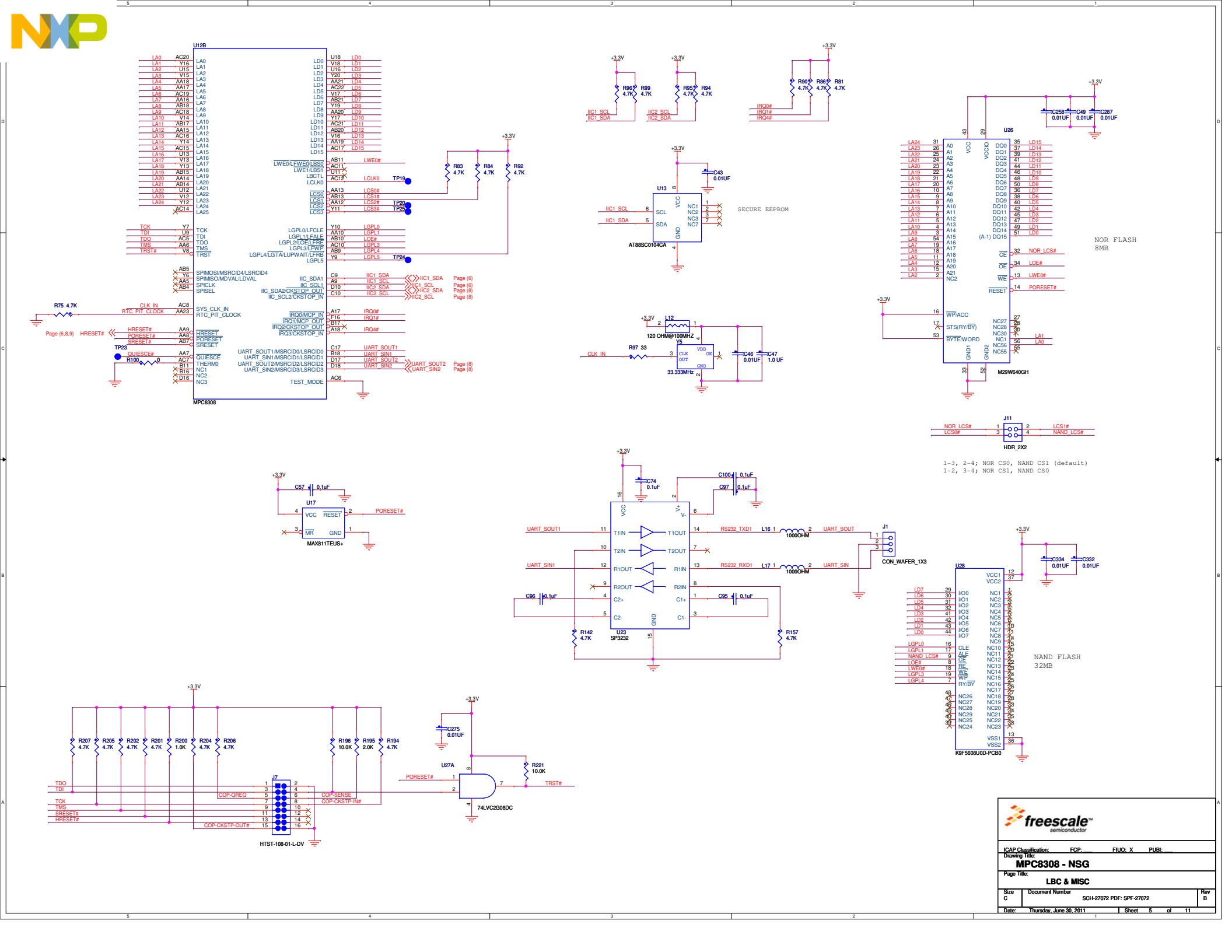
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MPC8308
U13
AT88SC0104CA
SECURE EEPROM
U26
M29W640GH
NOR FLASH
8MB
U28
K9F5608U0D-PCB0
NAND FLASH
32MB
J11
HDR_2X2
1-3, 2-4; NOR CS0, NAND CS1 (default)
1-2, 3-4; NOR CS1, NAND CS0
U17
MAX811TEUS+
U23
SP3232
J1
CON_WAFER_1X3
J7
HTST-108-01-L-DV
U27A
74LVC2G08DC
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ICAP Classification: FCP: ___ FIUO: X PUBI: ___
Drawing Title:
MPC8308 - NSG
Page Title:
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Size C
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Rev B
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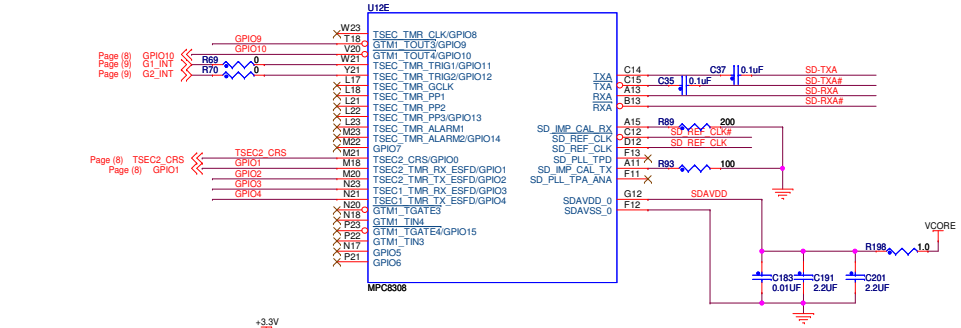
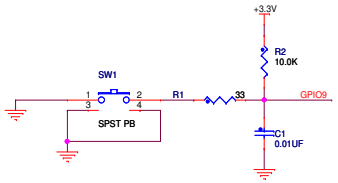
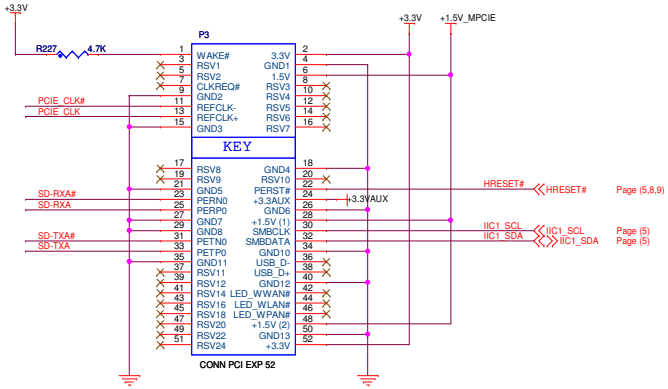
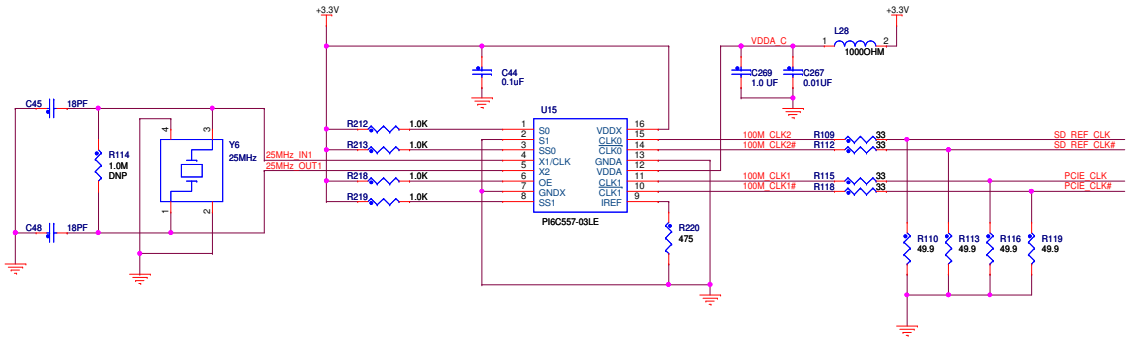
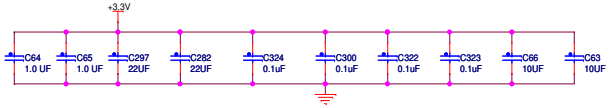


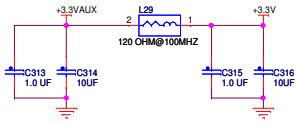



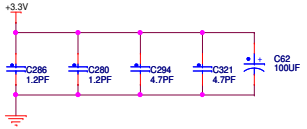

Manual Reset Buttom

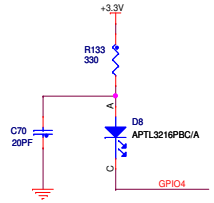


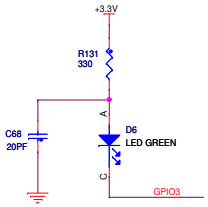



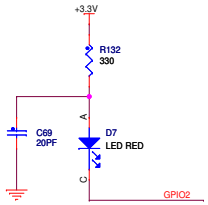



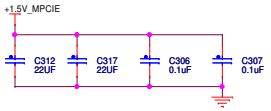

WiFi LED




Run LED




Error LED

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**MPC8308 - NSG**

Page Title:

**PCIE**

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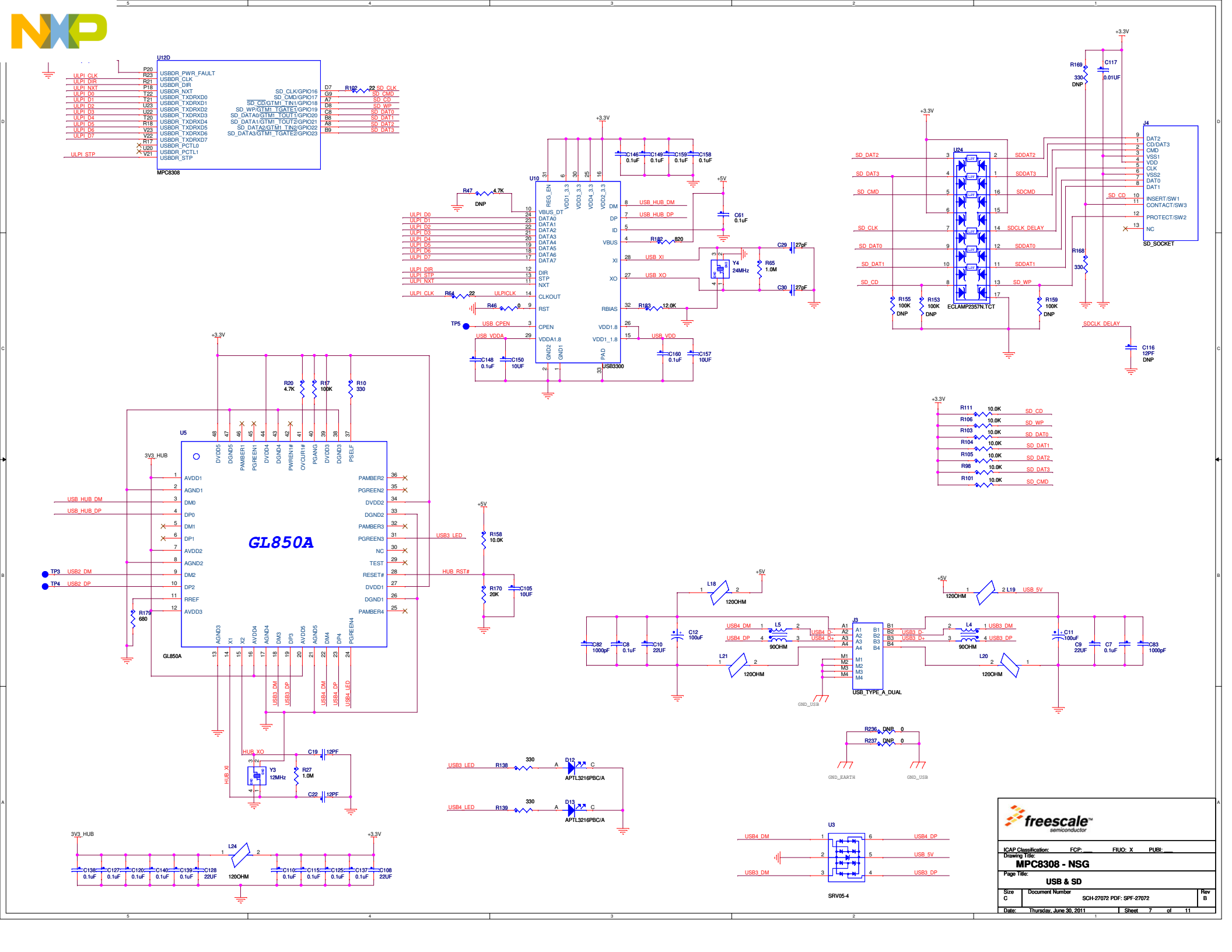


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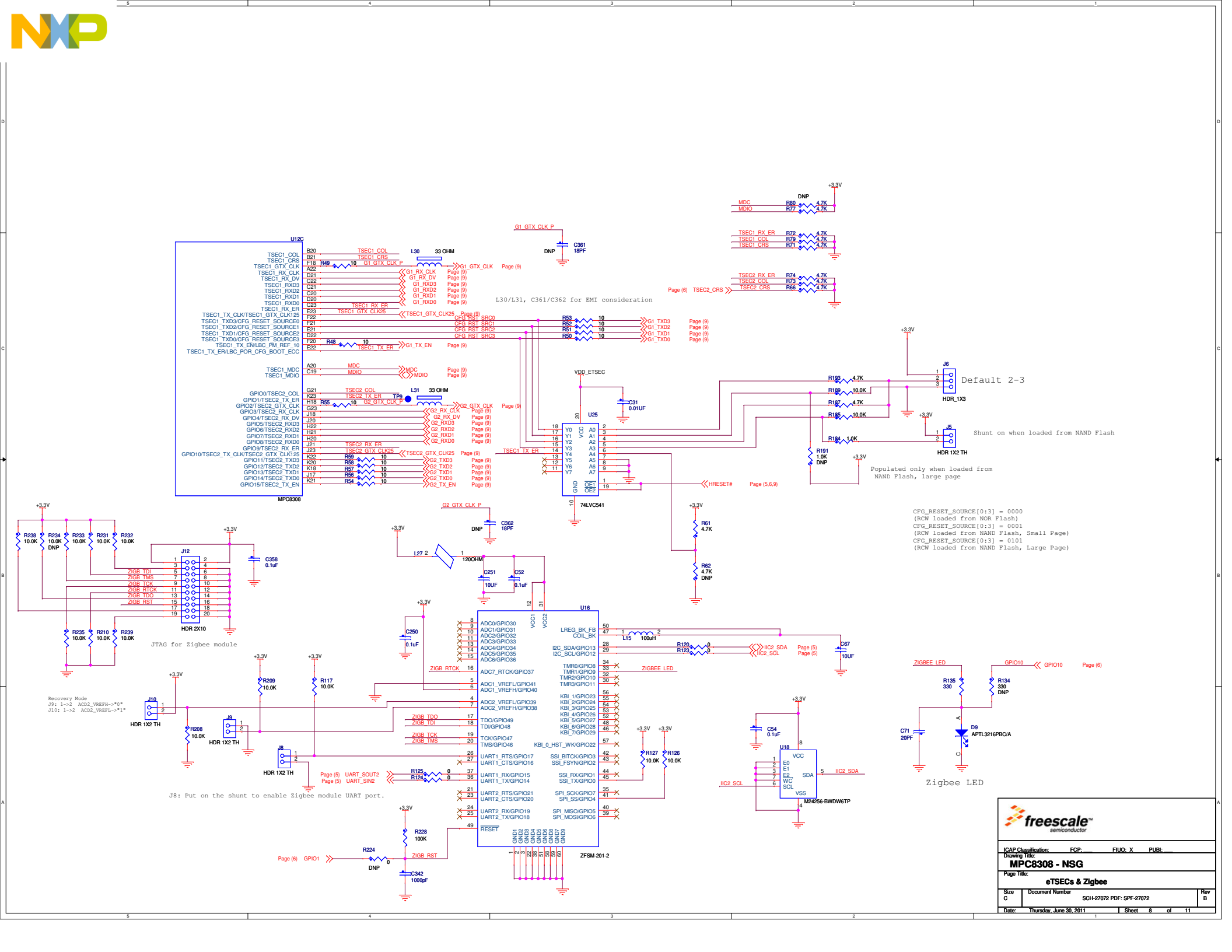
U12C
MPC8308
TSEC1_COL
TSEC1_CRS
TSEC1_GTX_CLK
TSEC1_RX_CLK
TSEC1_RX_DV
TSEC1_RXD3
TSEC1_RXD2
TSEC1_RXD1
TSEC1_RXD0
TSEC1_RX_ER
TSEC1_TX_CLK/TSEC1_GTX_CLK125
TSEC1_TXD3/CFG_RESET_SOURCE0
TSEC1_TXD2/CFG_RESET_SOURCE1
TSEC1_TXD1/CFG_RESET_SOURCE2
TSEC1_TXD0/CFG_RESET_SOURCE3
TSEC1_TX_EN/LBC_PM_REF_10
TSEC1_TX_ER/LBC_POR_CFG_BOOT_ECC
TSEC1_MDC
TSEC1_MDIO
GPIO0/TSEC2_COL
GPIO1/TSEC2_TX_ER
GPIO2/TSEC2_GTX_CLK
GPIO3/TSEC2_RX_CLK
GPIO4/TSEC2_RX_DV
GPIO5/TSEC2_RXD3
GPIO6/TSEC2_RXD2
GPIO7/TSEC2_RXD1
GPIO8/TSEC2_RXD0
GPIO9/TSEC2_RX_ER
GPIO10/TSEC2_TX_CLK/TSEC2_GTX_CLK125
GPIO11/TSEC2_TXD3
GPIO12/TSEC2_TXD2
GPIO13/TSEC2_TXD1
GPIO14/TSEC2_TXD0
GPIO15/TSEC2_TX_EN
L30 33 OHM
L31 33 OHM
G1_GTX_CLK P
G2_GTX_CLK P
C361 18PF DNP
C362 18PF DNP
L30/L31, C361/C362 for EMI consideration
U25
74LVC541
VDD_ETSEC
C31 0.01UF
HRESET#
U16
ZFSM-201-2
ADC0/GPIO30
ADC1/GPIO31
ADC2/GPIO32
ADC3/GPIO33
ADC4/GPIO34
ADC5/GPIO35
ADC6/GPIO36
ADC7_RTCK/GPIO37
ADC1_VREFL/GPIO41
ADC1_VREFH/GPIO40
ADC2_VREFL/GPIO39
ADC2_VREFH/GPIO38
TDO/GPIO49
TDI/GPIO48
TCK/GPIO47
TMS/GPIO46
UART1_RTS/GPIO17
UART1_CTS/GPIO16
UART1_RX/GPIO15
UART1_TX/GPIO14
UART2_RTS/GPIO21
UART2_CTS/GPIO20
UART2_RX/GPIO19
UART2_TX/GPIO18
RESET
LREG_BK_FB
COIL_BK
I2C_SDA/GPIO13
I2C_SCL/GPIO12
TMR0/GPIO8
TMR1/GPIO9
TMR2/GPIO10
TMR3/GPIO11
KBI_1/GPIO23
KBI_2/GPIO24
KBI_3/GPIO25
KBI_4/GPIO26
KBI_5/GPIO27
KBI_6/GPIO28
KBI_7/GPIO29
KBI_0_HST_WK/GPIO22
SSI_BITCK/GPIO3
SSI_FSYN/GPIO2
SSI_RX/GPIO1
SSI_TX/GPIO0
SPI_SCK/GPIO7
SPI_SS/GPIO4
SPI_MISO/GPIO5
SPI_MOSI/GPIO6
L15 100uH
C67 10UF
IIC2_SDA
IIC2_SCL
ZIGBEE_LED
ZIGB_RTCK
ZIGB_TDO
ZIGB_TDI
ZIGB_TCK
ZIGB_TMS
ZIGB_RST
U18
M24256-BWDW6TP
J6
HDR_1X3
Default 2-3
J5
HDR 1X2 TH
Shunt on when loaded from NAND Flash
Populated only when loaded from NAND Flash, large page
J12
HDR 2X10
JTAG for Zigbee module
J10
HDR 1X2 TH
Recovery Mode
J9: 1->2 ACD2_VREFH->"0"
J10: 1->2 ACD2_VREFL->"1"
J9
HDR 1X2 TH
J8
HDR 1X2 TH
J8: Put on the shunt to enable Zigbee module UART port.
D9 APTL3216PBC/A
Zigbee LED
CFG_RESET_SOURCE[0:3] = 0000
(RCW loaded from NOR Flash)
CFG_RESET_SOURCE[0:3] = 0001
(RCW loaded from NAND Flash, Small Page)
CFG_RESET_SOURCE[0:3] = 0101
(RCW loaded from NAND Flash, Large Page)
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ICAP Classification: FCP: FIUO: X PUBI:
Drawing Title: MPC8308 - NSG
Page Title: eTSECs & Zigbee
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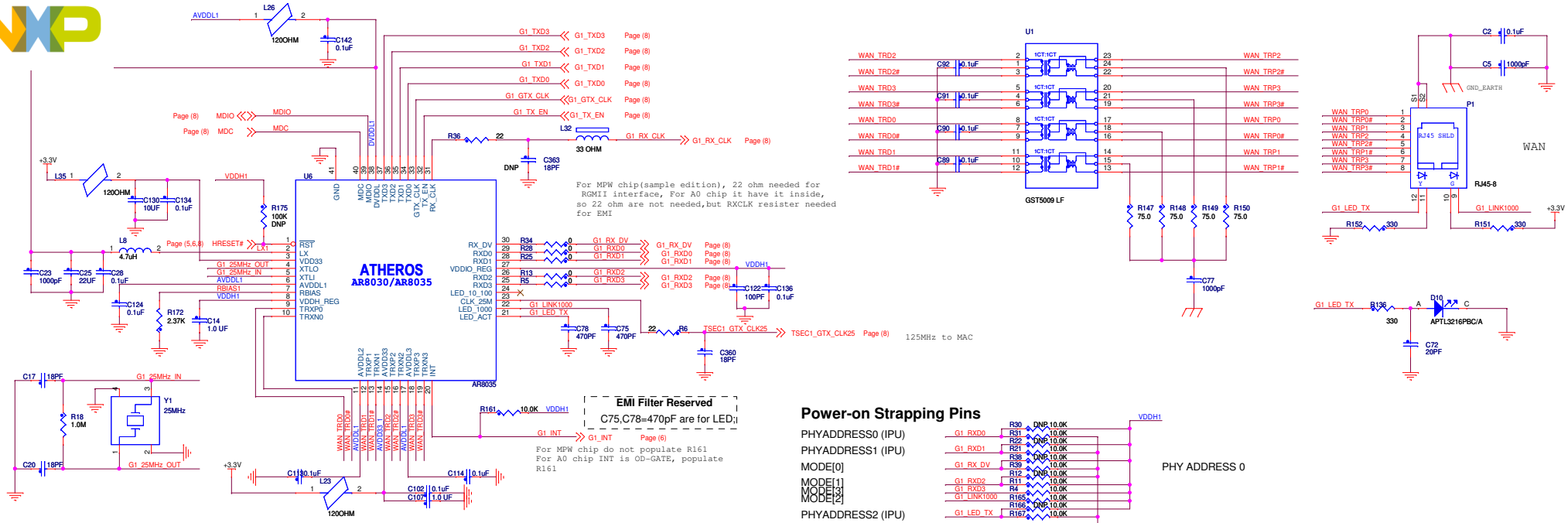


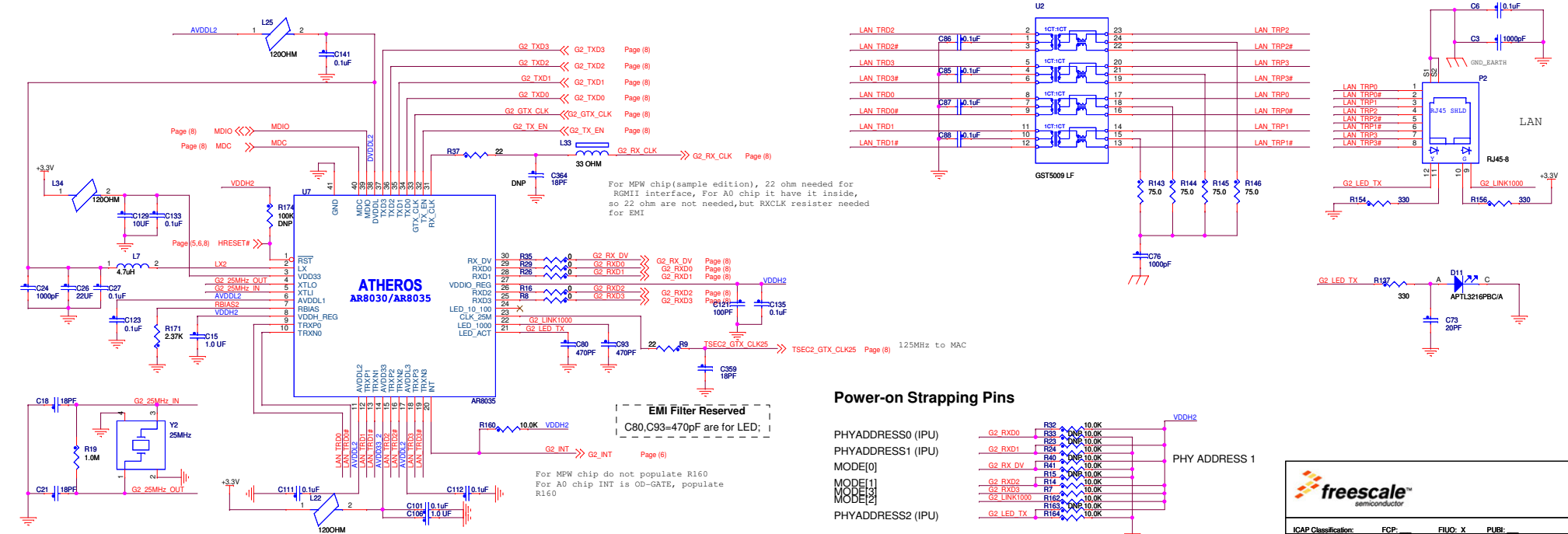


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Drawing Title: **MPC8308 - NSG**

Page Title: **GBE PHY**

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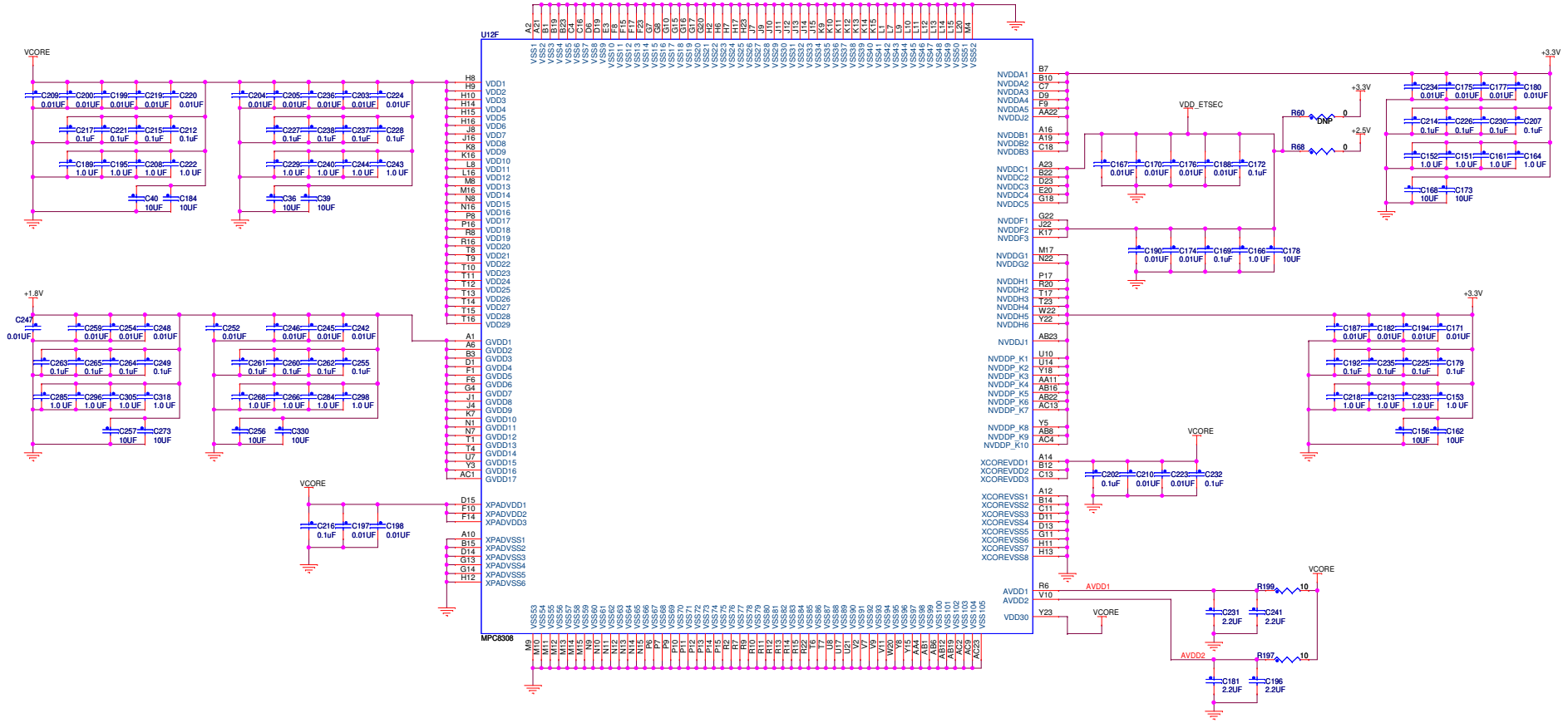


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Drawing Title: **MPC8308 - NSG**

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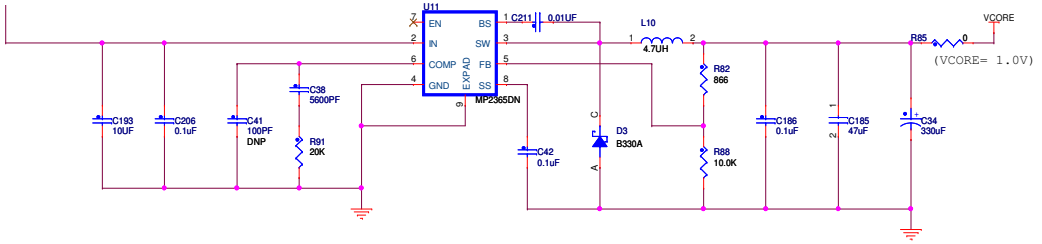


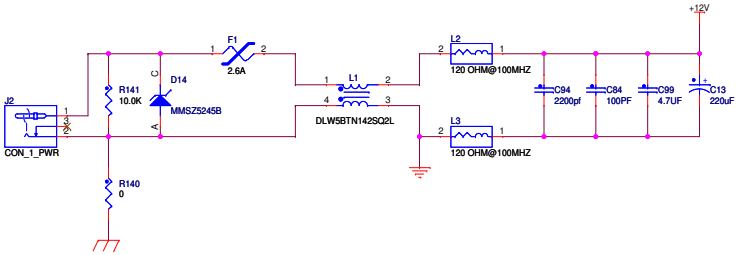


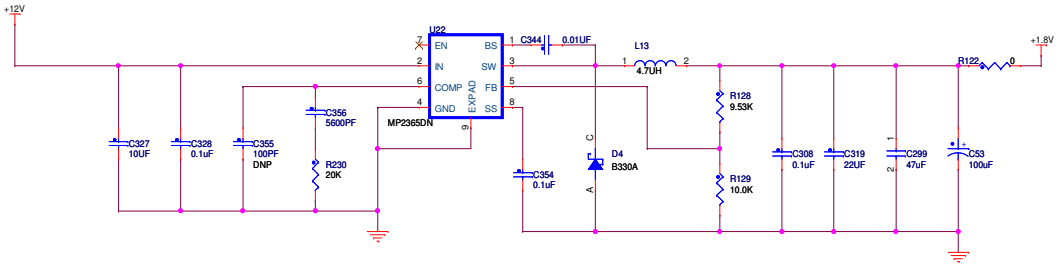


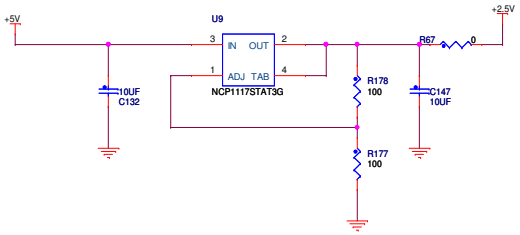


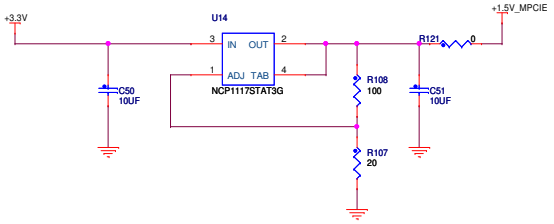


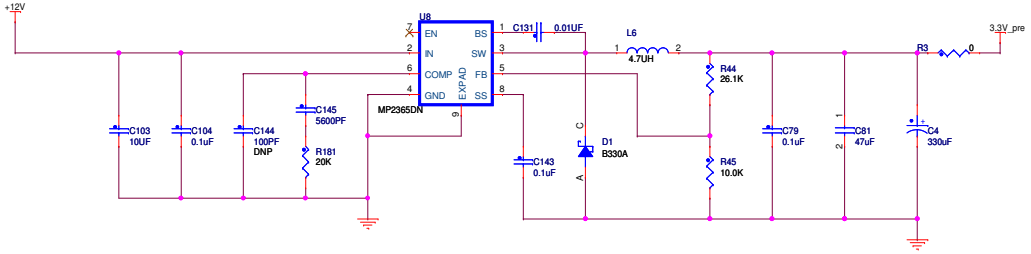


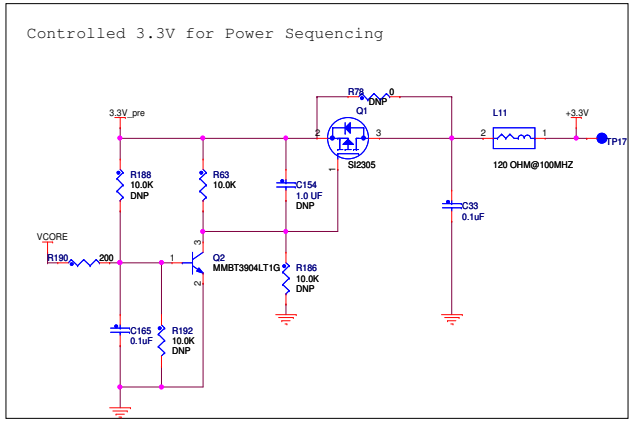


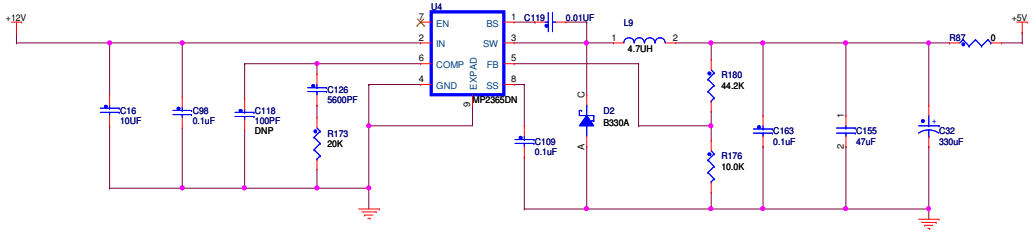


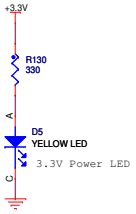


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