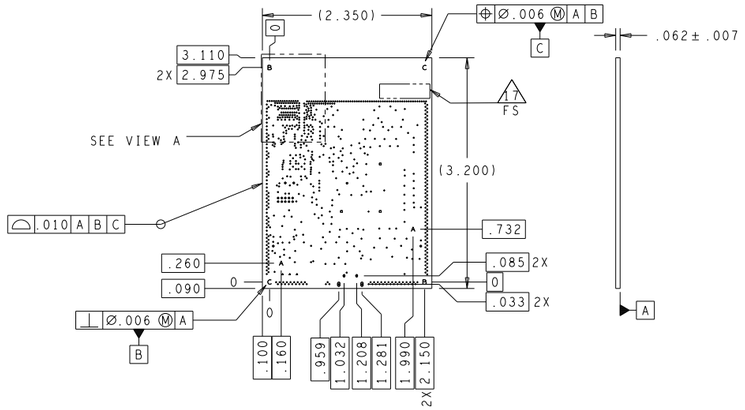
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	XX-XX-XX	X.X.

NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).
2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
4. COPPER FOIL WEIGHT - SEE STACKUP SECTION 'B'
5. CHARACTERISTIC IMPEDANCE - SEE TABLEL 'C'
6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .007"/.005"
7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
   .05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER
   2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL.
8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.
9. SOLDERMASK - GREEN COLOR (TAIYO OR EQUIVALENT), BOTH SIDES.
   MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.
10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.
11. ELECTRICAL TEST - 100% IPCD356.
12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS.
    UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.
14. TEARDROPS MAYBE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
15. TWO SOLDER SAMPLES TO BE PROVIDED.
16. BASIC GRID INCREMENT AT 1:1 IS .0001.
17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
    - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (pf)
19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)
20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP.
21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS.
    THE ADDITION OF RAILS AND .125"NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF
    CONTRACT MANUFACTURER.PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.
22. THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS,
    KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES.
23. INTENTIONAL SHORTS AT:

SH1	P2V8	AND	V_MCU
SH2	P2V8	AND	V_RF
SH3	V5_BUS	AND	P5V_USB
SH4	BAT	AND	V_BATT
SH5	DIO4	AND	PTA19
SH6	DIO0	AND	PTC3
SH7	DIO1	AND	PTC2
SH8	DIO5/CLKOUT	AND	PTA18
SH9	V_IN	AND	V_BRD



HOLE CHART				
ALL UNITS ARE IN INCHES				
FIGURE	SIZE	TOLERANCE	PLATING	QUANTITY
+	.010	+.000/-.010	PLATED	713
□	.015	+.002/-.002	PLATED	3
◇	.028	+.002/-.002	PLATED	10
△	.035	+.002/-.002	PLATED	3
○	.040	+.003/-.003	PLATED	5
A	.104	+.002/-.002	NON-PLATED	2
B	.125	+.002/-.002	NON-PLATED	2
C	.125	+.002/-.002	NON-PLATED	2
⓪	.034x.026	+.002/-.002	PLATED	2
⓪	.060x.033	+.002/-.002	PLATED	2

Ø.015 M A B C
Ø.015 M A B C

FINISHED Cu WEIGHT

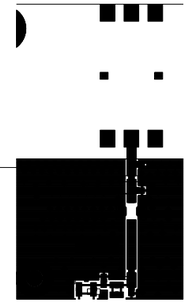
LAYER 1 COMPONENT SIDE 1 oz.
LAYER 2 SOLDER SIDE 1 oz.

SECTION B
LAYER STACKUP
SCALE: NONE

TABLE C
IMPEDANCE REQUIREMENTS
(Dk 4.3 USED FOR CALCULATIONS)

Layers	GROUNDED COPLANAR WAVEGUIDE		
	Trace Width (Mils)	Trace Airgap (Mils)	Impedance (Ohms)
L1_PS	32	6	50+/-10%

SEE TABLE C



VIEW A
TOP ETCH
SCALE: NONE

--- COMPANY PUBLIC
X COMPANY INTERNAL
--- COMPANY CONFIDENTIAL

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX .01 .0-30'
.XXX .005
√ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS.
REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

PART NO. 170-29210

APPROVALS	DATE
DRAWN J.SCHWARTZ	16-03-11
CHECKED A. QUIROZ	16-03-11
DESIGN ENGINEER J.A.QUIROZ	16-03-11

NXP SEMICONDUCTORS
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD
X-KW01-RCD-RD

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-29210	FAB-29210	A

SCALE 1/1 DO NOT SCALE DRAWING SHEET 1 OF 1