Multiple Independent Gate Field Effect Transistors – Device, Process, Applications.

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ABSTRACT

Double gate SOI devices have been widely researched to replace the current planar SOI devices. These double gate device structures have multiple gate surfaces but a single gate electrode. Recently double gate structures with independent gate structures have been studied. Independent gate devices offer additional advantages and challenges. This paper will review some of the challenges and advantages of such structures covering process integration, device architecture, compact models and circuit design. Experimental results of device, circuit and performance will be presented.

INTRODUCTION

The semiconductor industry has scaled the MOSFET over the last decade using electrostatic scaling rules[1]. Manufacturing capabilities have made it feasible to scale the device structures to be shorter by advancing lithography, thinner dielectrics using more precise process controls of diffusion and shallower junctions by better Ion Implant and diffusion technologies[1]. The move to SOI has been a significant change in the structure such as reducing junction capacitances. Copper interconnects and Low-K dielectrics are significant changes in materials to reduce interconnect delay. This path to scaling is becoming more difficult and new device structures and materials are proposed to replace the planar CMOS structures[1]. Thinning down the channel (FD-SOI) and using an additional gate to control the channel (Double Gate) are the most promising novel structures proposed to continue scaling these device structures. The improvements due to Double gate devices do not have to be limited to better short channel control and better performance of existing circuits. If the gates that control the thin channel region can be split and independently controlled a slew of new applications is feasible. It is challenging to make such devices but new process techniques have made such devices feasible and new applications are being explored.
In order to be effective devices with more than one gate need to meet various requirements outlined below and represented in Figure 1.

- Integration with single gate electrode and multiple gate electrode structures
- Alignment of the Multiple gates
- Minimal overlap of the Multiple gates
- Good gate dielectric quality of the Multiple gates

These requirements are typical for both single gate electrode and Independent gate electrodes versions of multiple gate devices. The Vertical Multiple Independent Gate FET (MIGFET) [2] has come closest to meeting all the requirements of such device structures and its performance characteristics and applications will be discussed in detail.

![Figure 1. Optimal Multiple gate Devices require perfectly aligned gates and good quality dielectrics on both sides of the channel.](image)

**PLANAR Vs VERTICAL**

Various device architectures have been proposed to make multi-gate devices, the predominant difference is a planar channel structure or a vertical channel structure. The planar structures have used various process techniques such as undercut below the channel or wafer bonding techniques[3]. The planar structures typically have one of the following problems mis-alignment, overlap of one gate, gate oxide integrity. The Vertical structures demonstrated are similar using a single gate electrode surrounding a silicon channel region but named differently such as DeltaFET[4], FinFET[5-6], OmegaFET[7], TriGate[8] or simply Mesa Isolated SOI. These devices have single gate electrode and hence are self aligned on both sides of the channel. They have good dielectric integrity since the dielectric is typically grown simultaneously on all sides of the channel. Since the same gate bias is applied to all sides of the channel these multi-
gate single gate electrode devices have excellent sub-threshold characteristics and short channel control.

**MIGFET and finFET PROCESS TECHNOLOGY.**

The vertical double gate device with single gate electrode has become commonly known as the finFET[5][6]. The finFET offers excellent short channel control and device characteristics for digital applications. It is desirable that independent multiple gate devices be integrated with these finFET devices. The MIGFET devices make such integration feasible [2]. The silicon gate region above the silicon fins are removed in MIGFET devices as shown in Figure 2. This is a mask-less process and the finFET devices are protected during this process. Thus applications where the MIGFET has advantages can use these devices and in digital CMOS applications where the finFET is useful they can be used and do not have an area penalty due to additional contact regions.

![Figure 2. The MIGFET (a) has Independent gates on both sides of thin Silicon channels. b) The MIGFET is easily integrated with finFET](image)

![Figure 3. Overhanging spacer on the silicon fins prevent silicides shorting the channel to the gates in CMP less process of making MIGFET devices.](image)
The devices shown in Figure 2-3 have channel dimensions as small as 30nm and gates of 80nm. The channel is left undoped and hence the devices end up being fully depleted when both gates are biased. The process uses 90nm SOI process techniques and is completed with a cobalt silicide and copper backend process.

**MIGFET Device Characteristics**

Figures 4(a-b) shows the electrical characteristics of the NMOS MIGFET. When both gates are under the same bias, the device shows double-gated depletion mode characteristics. In this mode the device has all the advantages of a normal finFET like structure it has extremely low leakage, DIBL and close to 65mV.dec SS. Independently biasing the gates of the device the threshold voltage, gain and sub-threshold swing are modulated (Figure 2 b,c). The devices show good drive and short channel characteristics for the case when the gates are tied together. The gain (Gm) sensitivity (Figure 5) to second gate bias demonstrate that this device is extremely useful for certain applications where the gain sensitivity to second gate bias can be used advantageously.

![Figure 4. The Id-Vg characteristics of NMOS MIGFET with the second gate Bias used to dynamically modulate the Vt and Subthreshold Swing](image)

![Figure 5. The Gain of the MIGFET is highest when both gains are tied. The gain is sensitive to the second gate bias](image)
Simulation of a 2-D cross section (Figure 6 a,b) for an NMOS MIGFET under strong negative gate 1 potential shows a parasitic hole inversion forming which screens the influence of gate 1 on the channel. Under strong positive gate 1 bias, an electron channel forms under the gate 1 (gate-1 channel). Since gate 2 is screened from the gate-1 channel, sub-threshold slope of this “buried” channel with respect to gate 2 decreases dramatically. The gate-1 influence on the conduction also diminishes for large bias once strong inversion at the gate 1 channel is attained due to inversion charge screening. This explains the convergence of Id-Vg curves for successive increase in VG2 bias. In linear device operation (Vds = 0.1V), the transconductance (Gm) is strongly influenced by the gate 1 bias and sub-threshold slope decreases, as gate 1 is increased in the positive direction, Gm profile shifts and starts to broaden as a function of.

Figure 6. 2D Device simulation of MIGFET shows the carrier density profile change with second gate bias(a). The Second gate coupling depends on the silicon thickness and the dielectric thickness (b)

**MIGFET-ANALOG APPLICATIONS.**

While digital CMOS has scaled considerably it has been difficult to scale devices to meet the stringent requirements to get scaled analog and mixed signal applications [1]. One of the key applications in mobile communication circuits is the RF mixer. The RF mixer is typically used in at least two stages in a transceiver[]. It has been shown that the MIGFET can be used as a Mixer[9]. Mixer topologies based on RF and LO signals applied to the gates of a MIGFET can help push RF and LO to higher frequencies. Or in the same frequency range we can relax the device channel length requirement to adopt high voltage or high power applications. [9]
In order to experimentally demonstrate the mixer two signals of 40kHz and 50kHz were used to bias the gates of a single fin MIGFET. The output across the supply and a resistor was sampled and the mixed output was obtained. This mixing action is possible due to the fully depleted condition of the undoped channel in a MIGFET. While this demonstration proves the feasibility of the MIGFET-Mixer a practical mixer will need more current than a single-fin mixer and multi-fin mixers will provide the required current to get a signal output with required power and conversion gain. Other MIGFET applications can include summer, differential amplifiers and phase detectors.

**MIGFET-Options and application as Memory cell**

The various MIGFET versions can have number of Independent gates, the two independent gate devices have self aligned gates on both sides of the channel. The MIGFET-T has three independent gates with the third gate below the channel, the proposed MIGFET-F has four independent gates with the fourth gate patterned during the patterning of the Silicon channel regions and the overlying gates(Figure 9). The versions with the third and fourth gate as evident will need the channel to be wider to have effective modulation of the channel or to make contacts.
The MIGFET-T can be efficiently used as a memory cell[10]. In this case the substrate was used to modulate the channel in addition to the two independent gates. It has been demonstrated that the MIGFET can be effectively used as a single transistor RAM. In such applications a common substrate biasing scheme is needed to do certain functions such as erasing an entire array. The MIGFET T characterization shown proves the feasibility of such third gate modulating the channel. The SOI Substrate was used as the third gate in characterizing the MIGFET-T (Figure 10).

**Figure 10.** a) Id-Vg of MIGFET-T, gate bias VG1 and VG3 are on the horizontal axis and each surface shows modulation with VG2 b)MIGFET-T ZRAM

**MIGFET LOGIC**

The second gate of a MIGFET can be used to substantially change the threshold voltage of the device but this requires additional area to make contacts to the second gate. In addition using a fixed second gate bias to set the threshold leads to degradation in sub-threshold characteristics hence this application of the MIGFET can be useful only in very limited circumstances for such applications. However it may be feasible to reduce the device count and make up for the area lost due to the additional contacts in reduced transistor count using novel circuits that use the
MIGFET as shown in the Logic OR gate implemented with combination of MIGFET and finFET devices (Figure 11).

Figure 11. Mixed-Mode Simulation of OR gate using MIGFET-FinFET devices. For this application the channel should be large or doped.

The MIGFET process when combined with the Asymmetric Double gate process can yield an Asymmetric Double gate MIGFET[11]. It has been proposed to use such an asymmetric double gate device to implement a Schmitt trigger that can substantially reduce the power requirements of these applications[12]. The ability of the MIGFET to be integrated with regular double gate CMOS finFET makes it possible to implement such a Schmitt trigger circuit that uses both these devices.

Figure 12. An Asymmetric Double gate MOSFET-MIGFET may be used to implement a 4T Schmitt Trigger to reduce power and transistor count.
Circuit and Device Simulations of MIGFET devices.

The MIGFET device provides unique challenges and opportunities to model it especially as compact model for circuit simulations. Since the MIGFET has only a very thin body which is modulated by multiple gates a simple charge sheet approximation of the channel will not predict the effects of coupling of the various gates in the channel region. UFDG[13] is a physics based compact model that elegantly models this coupling in the MIGFET devices. This has enabled circuit simulation to validate the applications such as the MIGFET-Mixer.

![UFDG Simulation of MIGFET includes bulk inversion effects.](image)

**SUMMARY AND CONCLUSIONS**

We demonstrated the successful development of double gate devices that have single gate electrode on multiple sides that can be used to further scale CMOS digital technology and the MIGFET which has multiple independent gates. The MIGFET which has two independent gates self aligned on both sides of a thin silicon channel and its application in digital and analog mixed signal applications have been explored. The MIGFET-T with three independent gates that can be used in single transistor memory devices. All these devices use well understood materials and interfaces and can be integrated with each other using exiting process technologies. This allows these mixed signal devices to be scaled and integrated with the digital CMOS devices even as they are continuously scaled. New circuits using MIGFET have been demonstrated such as dynamic Vt modulation, RF Mixers and single transistor memory elements. These SOI based
device should substantially enable new products and applications when combined with the superior performance of ultra-thin body double gated devices.

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