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Top Three European Semiconductor Manufacturers Announce Initiative to Eliminate Lead from Semiconductor Products

Infineon Technologies, Philips Semiconductors and STMicroelectronics propose standard for defining and evaluating lead-free semiconductor devices

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Munich, Germany, Eindhoven, Netherlands and Geneva, Switzerland, July 12, 2001 - In a move aimed at accelerating the use of 'lead-free' packages and stimulating the further development of 'lead-free' technologies, Infineon Technologies (NYSE/FSE: IFX), Philips Semiconductors (NYSE: PHG, AEX:PHI), and STMicroelectronics (NYSE: STM) - Europe's three largest semiconductor manufacturers - today unveiled their proposal for the world's first standard for defining and evaluating 'lead-free' semiconductor devices.

The initiative shows the three companies' commitment to work towards the elimination of lead (Pb) in electronic systems to improve environmental protection, e.g. in recycling or disposal processes of electronic devices. Starting in February 2001, the three companies have developed the proposed standard, which provides a common definition of 'lead-free' and assesses factors such as solderability and reliability of alternative materials.

Lead in Semiconductor Products

Lead, along with tin, is a critical component of the solder traditionally used for printed circuit board assembly. It is also widely used in semiconductor packaging, for example, as a coating on the leads of packages, in power IC packages as the die attach and for the balls of Ball Grid Array (BGA) packages.

Lead is often found in nature in association with other metals, with the result that removing all traces of lead from the metals that are used in 'lead-free' solders is not economically viable or might even be harmful to the environment.

The Demand for International Standards

One of the major barriers against eliminating the use of lead in the industry has been a lack of internationally agreed standards and methodologies for evaluating the quality and reliability of 'lead-free' technologies. In contrast, single lead-tin alloy has been used for many decades and standard procedures are used worldwide to evaluate its quality and long-term reliability.

"Many different kinds of 'lead-free' solder alloys and soldering processes are being investigated or developed around the world, using multiple combinations of elements like tin, silver, copper, bismuth, indium and zinc, all of which require increased temperature profiles relative to the well known tin-lead alloys during the soldering process," said Carlo Cognetti, Vice President for New Package Development at STMicroelectronics. "To accelerate the transition to 'lead-free' technology, the electronics industry needs a common approach to quantifying solderability, heat resistance and other issues that affect reliability."

"At present, there is not even an internationally agreed definition of the maximum amount of lead that can be allowed in a 'lead-free' component or process," said Dr. Wolfgang Bloch, Head of Environment Protection and Safety Management at Infineon Technologies. "The market is confused because there are no rules or standards so far for evaluating alternative technologies. What we are doing is proposing some key ground rules that will help accelerate progress. Our initiative shows the inevitable transition to 'green' assembly on a global scale."

"Europe has taken the lead in proposing the world's first legislation to eliminate lead from electronic equipment and components," said Leo Klerks, Environmental Officer at Philips Semiconductors. "Our three companies' interest in using lead-free soldering technologies has partly been fuelled by legislative restrictions from the European Commission. Effective from 1 January 2006, materials such as lead, mercury, cadmium and others will be forbidden in electrical and electronic devices. By sharing our knowledge and enthusiasm, Europe's leading semiconductor manufacturers can make huge steps towards meeting this goal."

Implementation and Availability of 'Lead-free' Components The three companies will be able to introduce their 'lead-free' products far in advance to the legislative deadlines. Fully qualified 'lead-free' components will be available by the end of this year. The proposal of Infineon, Philips and STMicroelectronics contains an upper limit for 'lead-free' components of 0.1 percent related to the individual material, not to the whole package or component. The 'lead-free' products give at least their European clients a certainty to be 'green' in time.

Following detailed discussions of their individual aims and approaches, the three companies intend to continue their co-operation on standards and evaluation while pursuing their individual research programs to find the most economically and technologically effective ways to remove lead from the electronics industry.

About Infineon Technologies: Infineon Technologies AG, Munich, Germany, offers semiconductor and system solutions for applications in the wired and wireless communications markets, for security systems and smartcards, for the automotive and industrial sectors, as well as memory products. With a global presence, Infineon operates in the US from San Jose, CA, in the Asia-Pacific region from Singapore and in Japan from Tokyo. In the fiscal year 2000 (ending September), the company achieved sales of Euro 7.28 billion with about 29,000 employees worldwide. Infineon is listed on the DAX index of the Frankfurt Stock Exchange and on the New York Stock Exchange (ticker symbol: IFX). Further information is available at www.infineon.com.

About Philips Semiconductors: Philips Semiconductors, which had annual revenues of approximately US$6.3 billion in 2000, designs and manufactures semiconductors and silicon systems platforms. Philips Semiconductors is spearheading the emerging field of systems on silicon solutions with the innovative Nexperia™ platform and VLSI Velocity™ tool set. The company's Sea-of-IP™ design methodology allows plug and play intellectual property blocks for easily customizable products. The company is a leader in communications, consumer, PC peripherals and automotive semiconductors, which are key applications for convergence in end-user products. Philips Semiconductors is headquartered in Eindhoven, The Netherlands, and has operations throughout the world. For more information: www.semiconductors.philips.com

About STMicroelectronics: STMicroelectronics (formerly SGS-THOMSON Microelectronics) is a global independent semiconductor company, whose shares are traded on the New York Stock Exchange, on Euronext Paris and on the Milan Stock Exchange. The Company designs, develops, manufactures and markets a broad range of semiconductor integrated circuits (ICs) and discrete devices used in a wide variety of microelectronic applications, including telecommunications systems, computer systems, consumer products, automotive products and industrial automation and control systems. In 2000, the Company's net revenues were $7,813.2 million and net earnings were $1,452.1 million. According to Dataquest's annual ranking for 2000, STMicroelectronics is the sixth largest semiconductor company in the world. ST has won numerous international awards for its environmental initiatives and has publicly committed to achieving zero net emission of carbon dioxide by 2010. Further information on ST can be found at www.st.com

DEFINITION OF A GREEN PACKAGE FOR SEMICONDUCTOR DEVICES

July 16th, 2001-

The three Companies recognize the need of uniformity in the definition of a "green" package.
Following definition is agreed:
Semiconductor packages are considered GREEN when four elements: Pb, Br, Cl, Sb are not intentionally added during the manufacturing process. They can however be present in the finished units as impurities. The agreed maximum level for each element is given here below. It represents the concentration of the 4 elements in the packaging materials, like lead finish, molding compounds or substrates.
Note: Shipping materials such as blister-tape and paper-based boxes are not part of this consideration, since they are usually part of existing recycling processes.

Definition	**substance**	**upper limit (weight)**	**material e.g.**
Lead-free	Pb	< 1000 ppm	Lead finish Solder balls
Halogen-free	Cl + Br	$\Sigma < 900$ ppm	Mold compounds Laminates(*) Solder resist(*)
Antimony-free	Sb_2O_3	< 900 ppm	Mold compounds Laminates(*) Solder resist(*)
(*) = substrates of array packages			

Acceptable technical limits for different substances are aimed in respect to customer benefit, existing standards and technical cost implications.
Therefore the reasons for choosing above impurity levels in green package are:

Lead-free: Pb < 1000ppm:

- Anodes have 500ppm Pb, but Pb can fluctuate locally during plating: the level of 1000 ppm prevents the necessity for process control on Pb content in the terminations.
- ITRI, IPC and HDPUG recommend: 1000ppm. It is an achievable and sustainable level.
- Although legislation has not yet been consolidated, a maximum level of 1000ppm is mentioned in the law of some countries.
- Hazardous substances at levels below 1000 ppm do not need to be declared.
- Reduction of Pb-content below the current low level would mean a refining step that is costly and has a substantial impact on environment.

Halogen free: (Cl+Br) <900ppm

- Raw materials have some halogen concentration but material suppliers are making progress with conversion to industrially available green molding compounds. Based on progress the levels might be reduced further.
- Japanese industry is an important material supplier. The Japanese law indicates the 900 ppm as the upper limit for both Cl and Br.
- The definition is also based on the Japanese specification: JPCA-ES-01-1999.

Antimony-free: Sb_2O_3 <900ppm:

- For Sb2O3 inputs from material suppliers on their current capabilities have been used as a starting point for the maximum level of 900ppm.
- The definition is also based on the Japanese specification: JPCA-ES-01-1999.

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SOLDERABILITY TEST FOR Pb-FREE DEVICES

July 16th, 2001-

Existing board interconnection technology is using a limited number of Pb Sn alloys, basically the eutectic PbSn as solder paste and high tin (80-90%) alloy as coating of device terminations.
This has simplified the standardization of methodologies.
In the case of solderability test eutectic PbSn is widely used as wetting agent, with no other alternative: ref. method IEC60068-2-20.

On the contrary, in the present stage of development of Pb-free technology, a wide variety of solutions is under test for both solder pastes and coating of package termination; this opens a relatively large number of possible combinations of materials, which can affect the capability of producing data of general use.

As further element of complexity, it must be considered that for a long period the two technologies are espected to co-exist in the sense that in some board mounting the "new" Pb-free paste will be combined with the present Pb-based packages (this is already possible now, at the beginning of the conversion to Pb-free); in some other board mounting the "old" eutectic PbSn paste will be still used in combination with Pb-free devices (this is possible to happen in the second phase of the conversion).

Although progress in IEC will be taken into consideration, Infineon, Philips and STMicroelectronics have agreed on a common Pb-free solderability test, which will be used in parallel with the existing IEC60068-2-58 and -69, for the assessment of solderability of both Pb-based and Pb-free package terminations.

As solder alloy the choice is the ternary Ag(3.3-4.3%) Cu(0.4-1.1%) and Sn (balance).

Details about the test conditions and the flux used are given in the following table.

Solderability of Lead-free terminations

Dip & Look test

Solder bath	SnPb40		SnAgCu*
Dipping time	3 s	2 s	3 s
Solder bath Temperature	215 °C	235 °C	245 °C
Flux	25 % Colophony 75 % Isopropanol		25 % Colophony 75 % Isopropanol
Comment	according to IEC 60068-2-58		according to IEC 60068-2-58 using SnAgCu at 245 °C

*composition Ag: 3.3 % - 4.3 %, Cu: 0.4 % - 1.1 %, Sn: balance

Wetting balance test

- according to IEC 60068-2-69 using SnAgCu* at 245 °C
- both bath and globule test method can be used
- pass/fail criteria must be fixed for each package individually

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TEMPERATURE PROFILE FOR THE ASSESSMENT OF MOISTURE SENSITIVITY LEVEL(MSL) OF LEAD-FREE SEMICONDUCTOR DEVICES

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It is well known that in the soldering process of Surface Mount Technology (SMT), plastic encapsulated devices are exposed to the double effect of high temperature and the moisture absorbed in the moulding compound.

As a result, high internal water vapour pressure is developed, which cause delamination of a number of interfaces existing in the package and, in worst case, inner and outer cracks.

This is prevented by controlling the quantity of moisture existing in the product when board mounting takes place. Critical devices are dried during the assembly process and than sealed in damproof bags until they are opened by the end user. Robust devices are shipped without any special sealing.
When hermetic bag is open, shelf life can change from a few hours to many months, depending on a large number of factors, which involve package and silicon technology (ref.1).

Sensitivity of each product to absorbed moisture is defined in a three step assessment:

1] preconditioning of the units in moist ambient for a given time;
2] exposure to high temperature, following a thermal profile representative of the on board reflow soldering process;
3] physical analysis, by means of Scanning Acoustic Microscopy (SAM)or microesection with the detection of possible cracks and delaminations. The analysis is followed by reliability assessment when doubt exists about the results of physical observation.

As a result of the assessment, each device is given its own Moisture Sensitivity Level (MSL), indicating if drybag is needed and the shelf life once the bag is opened.

For Pb-based soldering, above process is specified by the procedure IPC/JEDEC J-STD-020A (apr 1999). It defines the 8 levels of moisture sensitiveness with their preconditioning, the reflow profile, the acceptance-failure criteria for delamination. Reflow profile has a peak of 225C for large packages and 235C for small packages, which must be compared with the melting point of eutectic PbSn at 183C.

As most common Pb-free solders have melting point of 215-225C it is anticipated that Pb-free soldering will require higher reflow temperature, above 235C. Also in this chase we will need to deal with differential peak temperatures for devices with large thermal inertia and devices with small thermal inertia. Two possible values are 245°C and 260°C respectively. It is clear that all devices for Pb-free electronics must be re-classified in Moisture Sensitivity Level (MSL) according to new standards which are not yet decided in this moment.

Infineon, Philips and STMicroelectronics have agreed on common specifications, with the following criteria:

1] preconditioning levels are the same as in the existing J-STD-020A, with the same MSL;

2] delamination criteria are more severe than the J-STD-020A: any crack detected by acoustic microscopy or microsection and any die-top delamination is enough to downgrade the MSL to the next level;

3] reflow profile is defined in a narrower range of values for relevant temperatures, times and ramp-up/ramp-down rate, with two possible peak temperatures: 245C and 260C (see table A and B or profile A and B). This is intended to limit the number of variables and to make the assessment of MSL more reproducible and consistent.

It must be highlighted that moving to higher reflow temperature can have a remarkable impact on device reliability. Preliminary data produced by the three Companies and published by international committees (ref. 2) have shown that while soldering in the range of 240-

245°C has limited impact on the package integrity, the range 255-260°C can cause severe delaminations and cracks in a large number of devices, with down stepping of their MSL of one or two levels.

Therefore, Infineon, Philips and STMicroelectronics recommend their customers to set the reflow temperature in the 240-245°C range, by suitable choice of furnace maximum temperature and belt speed.

They highlight also that in order to become compatible with the 255-260°C peak temperature, a number of devices must be re-designed by improving one or more
of the factors affecting MSL (ref. 1). This requires the development of new materials and processes.

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ref.1 - Factors affecting MSL:

- Package size, thickness
- Leadframe design, coatings
- Die attach materials, processes
- Mold compound materials, processes
- Die size
- Die coating, passivation
- Die pad size, shape, locking features

ref.2 - NEMI report - JAN 17, 2001

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Reflow profile parameters for MSL testing

Profile	**„260°C“**	**„245°C“**
Ramp rate	not specified	not specified
Preheat	125 °C to 220 °C 150 s to 210 s 0.4 K/s to 1.0 K/s	125 °C to 220 °C 150 s to 210 s 0.4 K/s to 1.0 K/s
Time at T>220 °C	60 s to 90 s	60 s to 90 s
Peak temperature	260 °C -5/+0 °C	245 °C -5/+0 °C
Peaktime	10 s to 30 s (≥ 250 °C)	10 s to 30 s (≥ 235 °C)
Cooling rate	≤ 6 K/s	≤ 6 K/s
Time from 25 °C to peak	240 s to 360 s	240 s to 360 s

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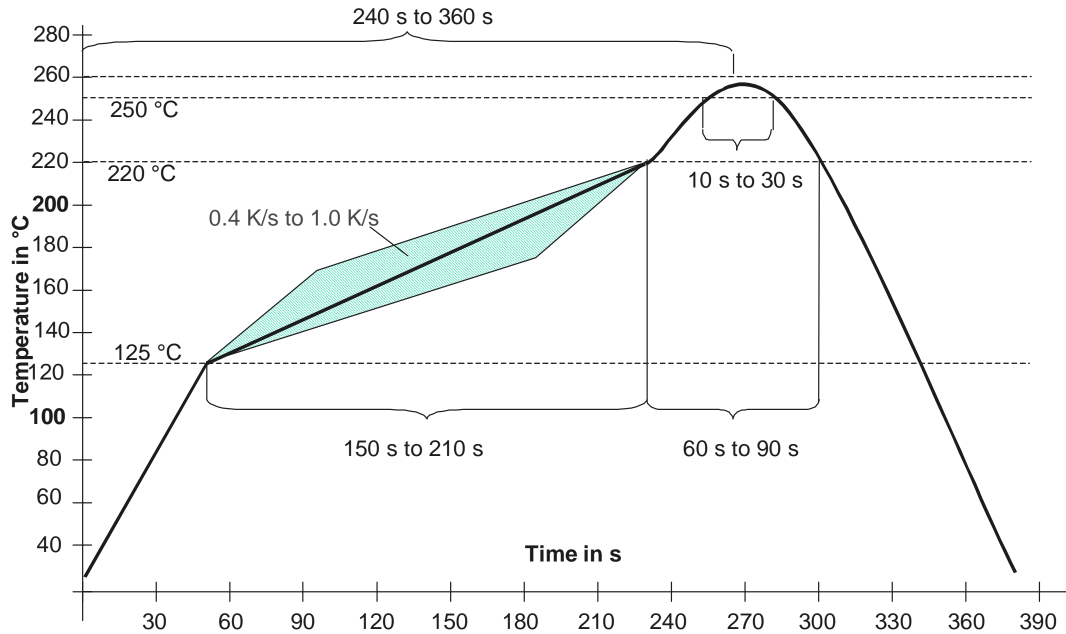
Reflow profile for MSL testing (260°C)



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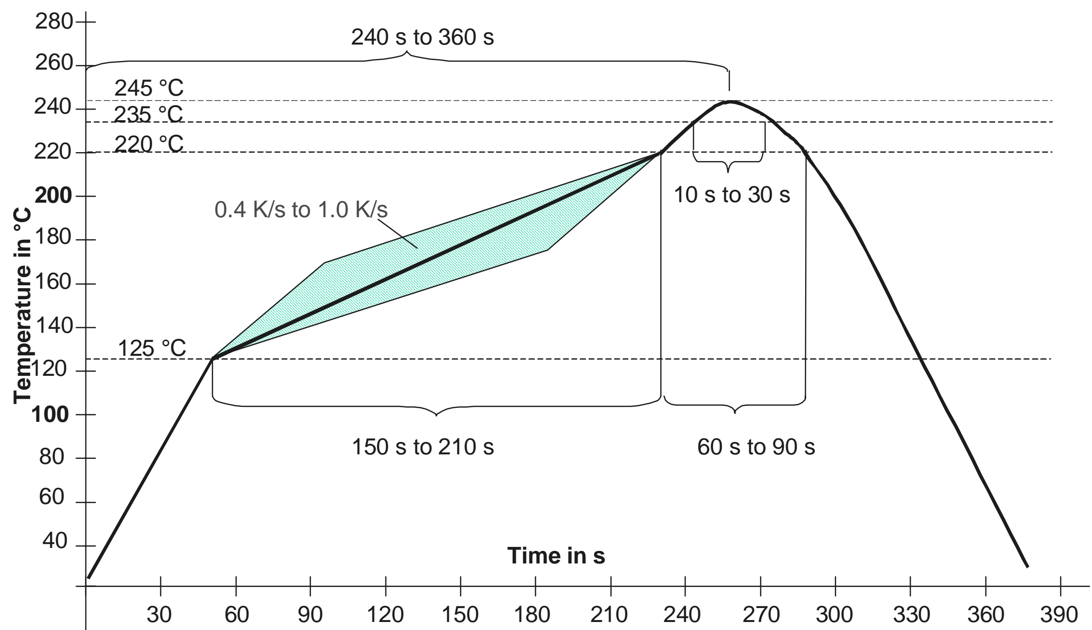
Reflow profile for MSL testing (245°C)



LEAD-FREE SOLDER COATING OF PACKAGE LEADS AND THE NEED OF ACCELERATED „WHISKER ASSESSMENT“ TEST

- *July 16th, 2001-*

The majority of devices are assembled in leadframe packages, whose external terminations are coated by Tin-Lead (SnPb)- deposited by electroplating. In Lead-free electronics, SnPb coating must be replaced by alloys, which are applied by a similar process using the same equipment. This limits the range of candidates to pure Sn and binary tin alloys like SnAg,SnBi and SnCu. Pure Sn is used since many years in Through Hole (TH) packages, like Dual In-Line (DIP) and TO-220. Pure tin and its alloys with small amount of additives are known to be prone to whisker formation and - as Surface Mount Devices (SMDs) have a much smaller pitch than TH packages - the potential growth of whiskers is a major concern.

Whiskers are needles of Sn - some microns in diameter and up to several hundred microns in length -, extruded from the plated layer under the effect of internal stress existing in the layer. They can cause short circuits and failures of electronic assemblies. Today SnPb-platings are regarded as whisker safe, whereas investigations performed by the three Companies have shown that under certain conditions Sn and its lead-free alloys can develop whiskers.

Several factors seem to influence the tendency to whisker formation. These are – among others - the substrate material, the composition of the plating itself
and its thickness, the grain structure of the plating, the chemicals, etc. All these factors contribute to the generation of internal stress in the solder layer. Depending on ambient conditions stress can increase and lead to such extrusions of tin crystals in form of filaments. Apart this rough model, the root cause for the formation of whiskers is still unknown, which makes the assessment of whiskers rather tough. It must be noticed that, once the solder layer is exposed to reflow, internal stresses are released and whiskers are not generated afterwards.

The maximum recommended storage time of devices before being mounted on PCB is two years, hence the three companies agree that components must be guaranteed „whisker-free" for at least two years in normal ambient conditions. The most obvious approach is to study whisker growth for these two years in ambient atmosphere. For this is very inconveniently, most efforts are dedicated to identify methods for the acceleration of whisker growth in order to have the risk assessment in a reasonably short time. Today several test methods are reported in literature, which can accelerate whisker formation (e.g. 55 °C / dry heat; 85 °C / 85 % r.H; HAST; temperature cycling ...). However, correlation of these conditions to normal storage is not yet available.

Another matter of study is the acceptable level of whiskers. The three Companies highlight that not every whisker is regarded to be dangerous. In their common understanding isolated whiskers with maximum length of 50 microns have no impact on reliability. Evaluations are ongoing in order to define the maximum allowable density, length and morphology. In order to speed up results and conclusions Infineon Technologies, Philips Semiconductors and STMicroelectronics have decided to share their know-how and experimental database. And they will also participate actively in international committees and working groups on the subject.