MOS Model 11

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Introduction : MOS Model 11

Goals for MOS Model 11:

- suitable for digital, analog and RF
- number of parameters comparable to MM9
- simulation time comparable to MM9
- physics based

Introduction : MOS Model 11 (II)

Model developed for accurate distortion analysis in circuit design:

- **surface-potential-based model**

  ⇒ accurate transition weak → strong inversion

- **symmetrical**
- **distortion**

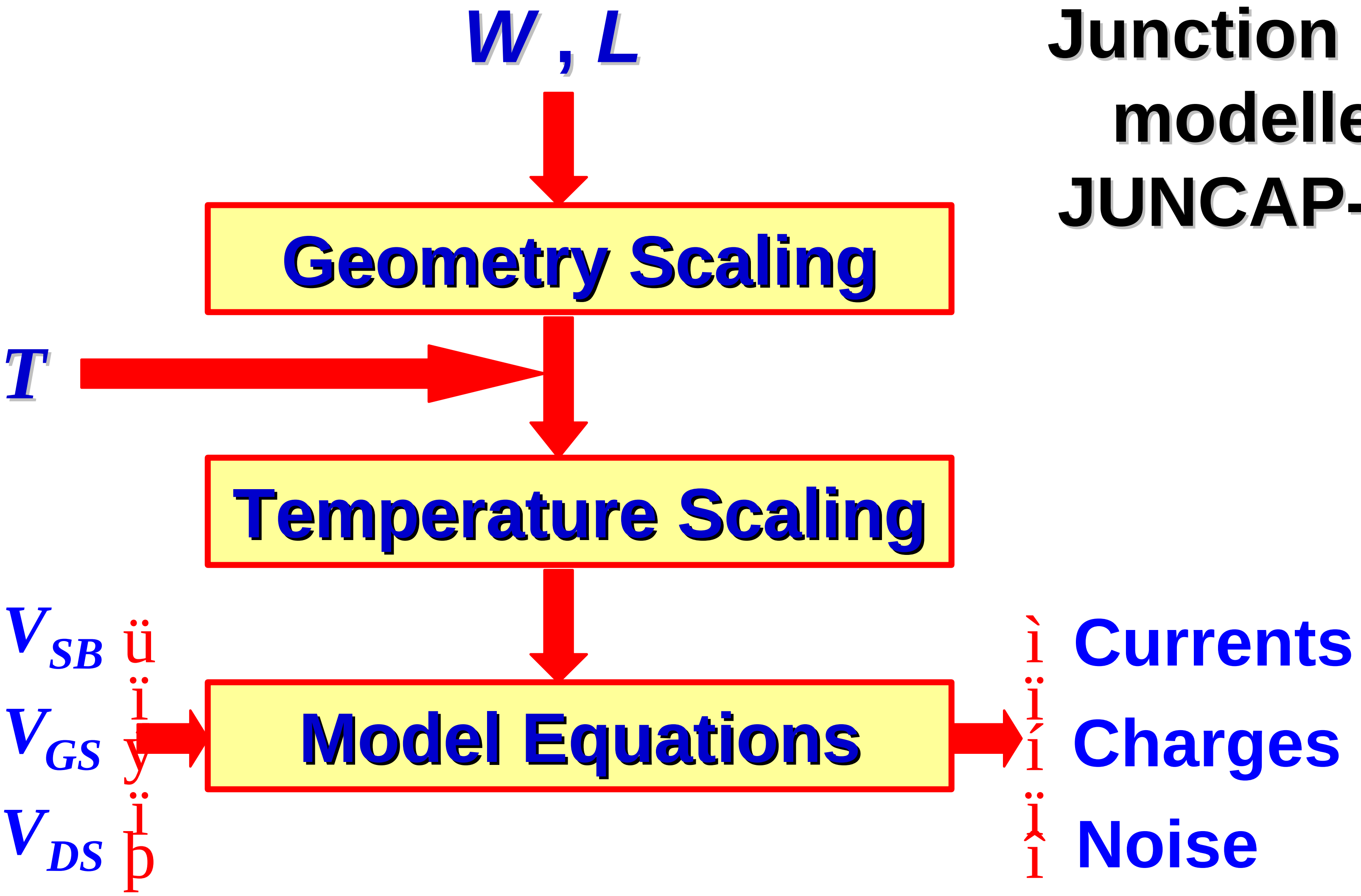
  ⇒ accurate description of third-order derivatives (i.e. $\partial^3 I/\partial V^3$)

Introduction : MOS Model 11 (III)

Implemented physical effects:

- mobility reduction
- bias-dependent series-resistance
- velocity saturation
- conductance effects (CLM, DIBL, etc.)
- gate leakage current
- gate depletion
- quantum-mechanical effects
- bias-dependent overlap capacitances

Introduction : Structure of MOS Model 11



W , *L*

Geometry Scaling

T

Temperature Scaling

V_{SB}
V_{GS}
V_{DS}

Model Equations

Currents
Charges
Noise

Junction diodes modelled by JUNCAP-model

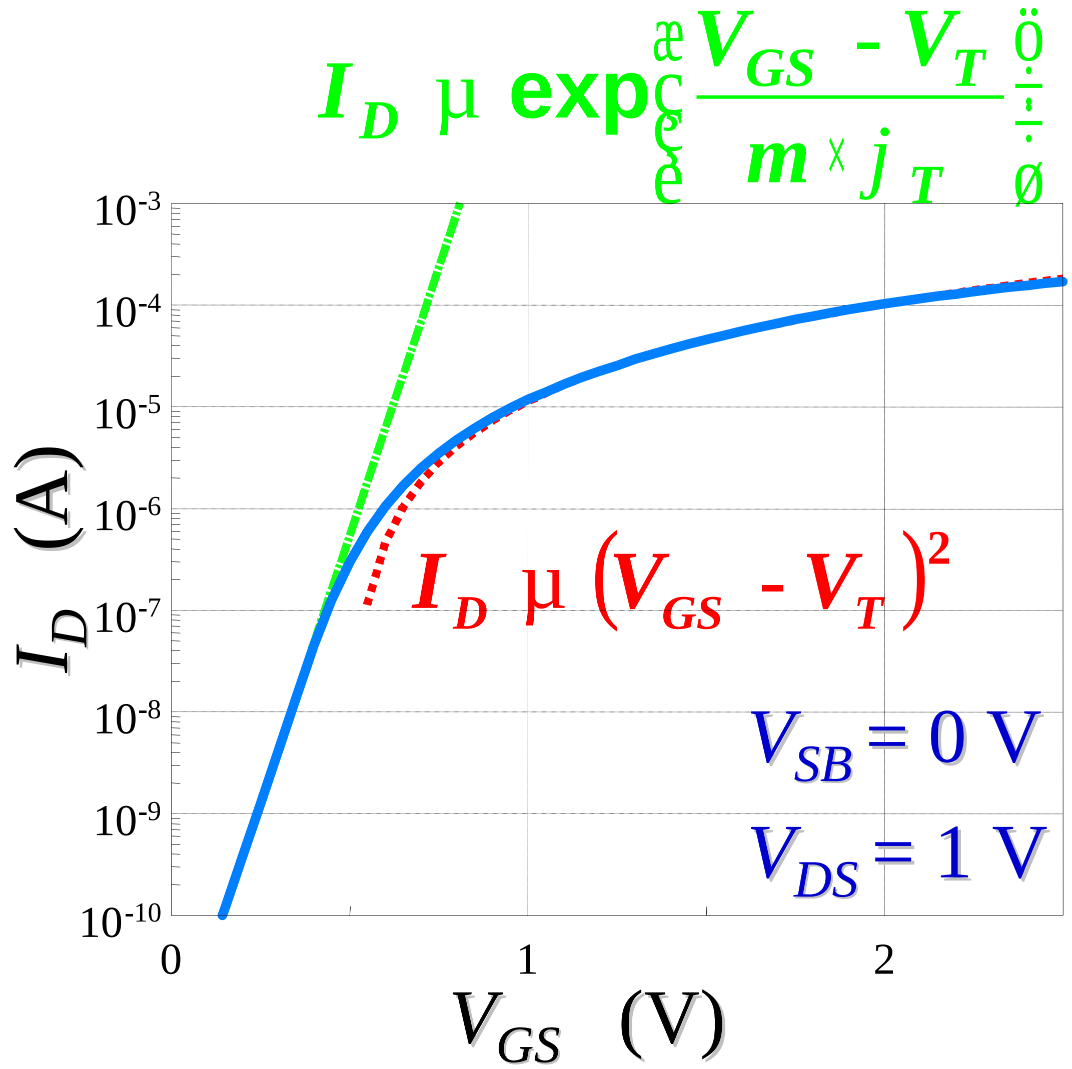
Outline

- Introduction
- DC-Model
- AC-Model
- Noise Model
- Model Parameters & Extraction
- Examples & Applications
- Conclusions

Outline : DC-Model

- V_T vs. ψ_s-based models
- Mobility reduction
- Bias-dependent series-resistance
- Velocity saturation
- Conductance effects
- Symmetry
- Gate leakage current
- Junction model

DC-Model : V_T-based model

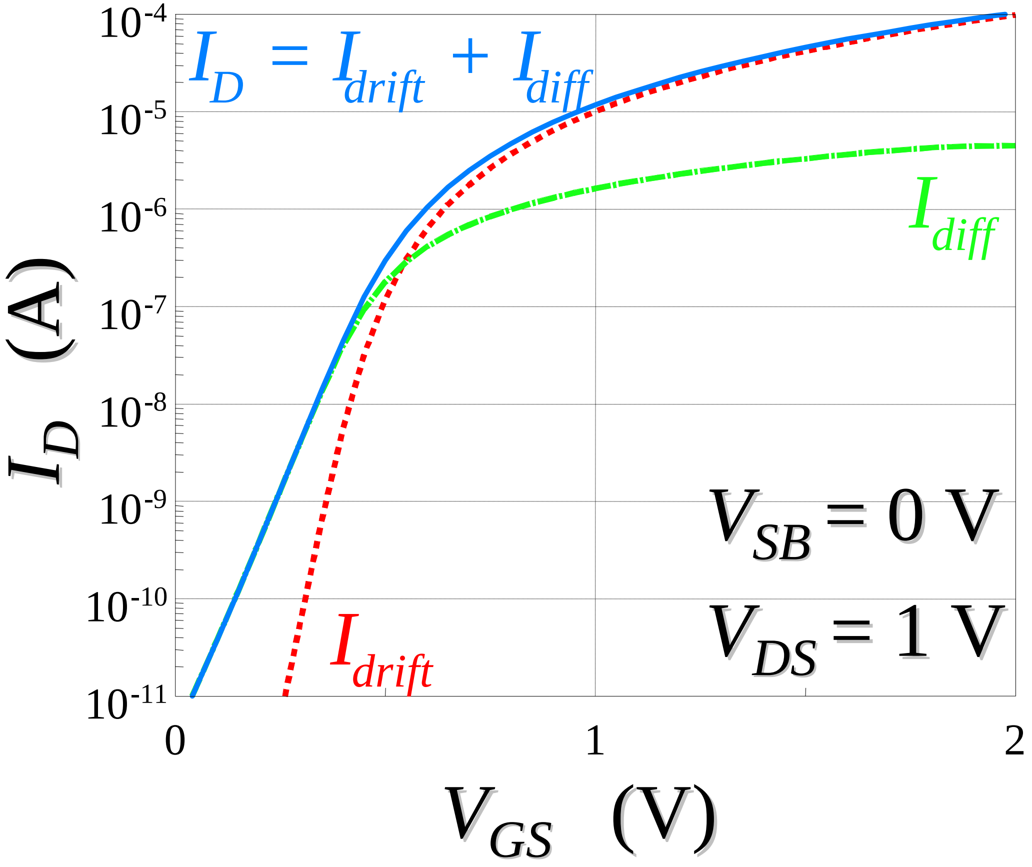


V_T-based model:

Interpolation needed between subthreshold and superthreshold (e.g. BSIM4 and MM9)

⇒ Smoothing function

DC-Model : Surface-Potential-Based Model



y_s-based model:

Single equation for whole operation range:

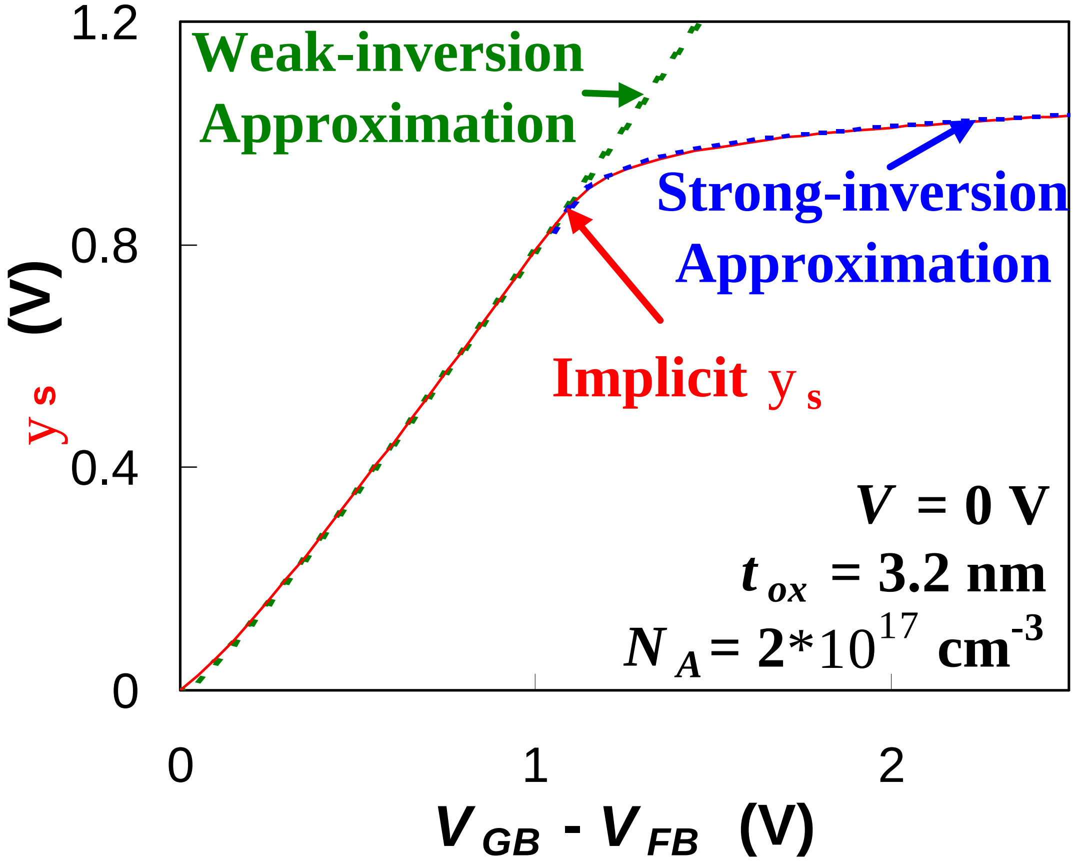
$$I_{drift} = f(V_{GB}, y_{s0}, y_{sL})$$

$$I_{diff} = g(V_{GB}, y_{s0}, y_{sL})$$

$$I_D = I_{drift} + I_{diff}$$

DC-Model : Surface Potential Approximation

$$\left(\frac{V_{GB}-V_{FB}-\psi_s}{k}\right)^2=\psi_s+\phi_T\cdot e^{\frac{-2\phi_F-V}{\phi_T}}\cdot\left(e^{\frac{\psi_s}{\phi_T}}-1\right)+\phi_T\cdot\left(e^{-\frac{\psi_s}{\phi_T}}-1\right)$$



⇒ **Iterative solution**

⇒ **Time consuming??**

⇒ **Approximation used:**

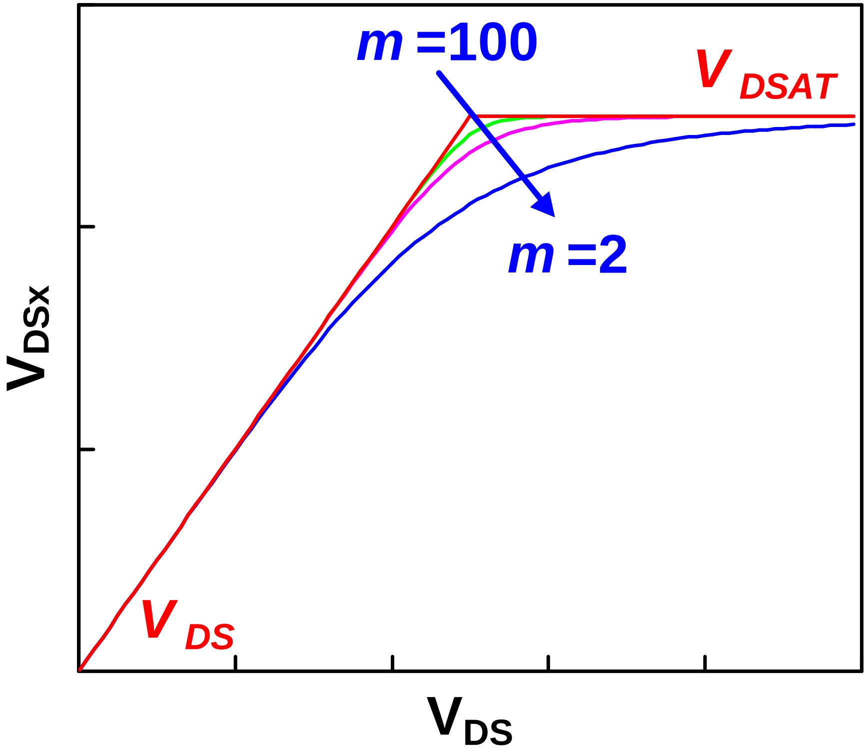
$$\psi_s=\psi_s(V_{GB},V)$$

(Solid-State Electron. 44, 2000)

DC-Model : Surface Potential Approximation (II)

Model incorporates linear/saturation region for long-channel case: $V_{DSAT} = V_{DSAT_{long}}$

⇒ Short-channel devices: $V_{DSAT} < V_{DSAT_{long}}$



Approximation used:

$$\psi_s = \psi_s(V_{GB}, V_{DSx} + V_{SB})$$

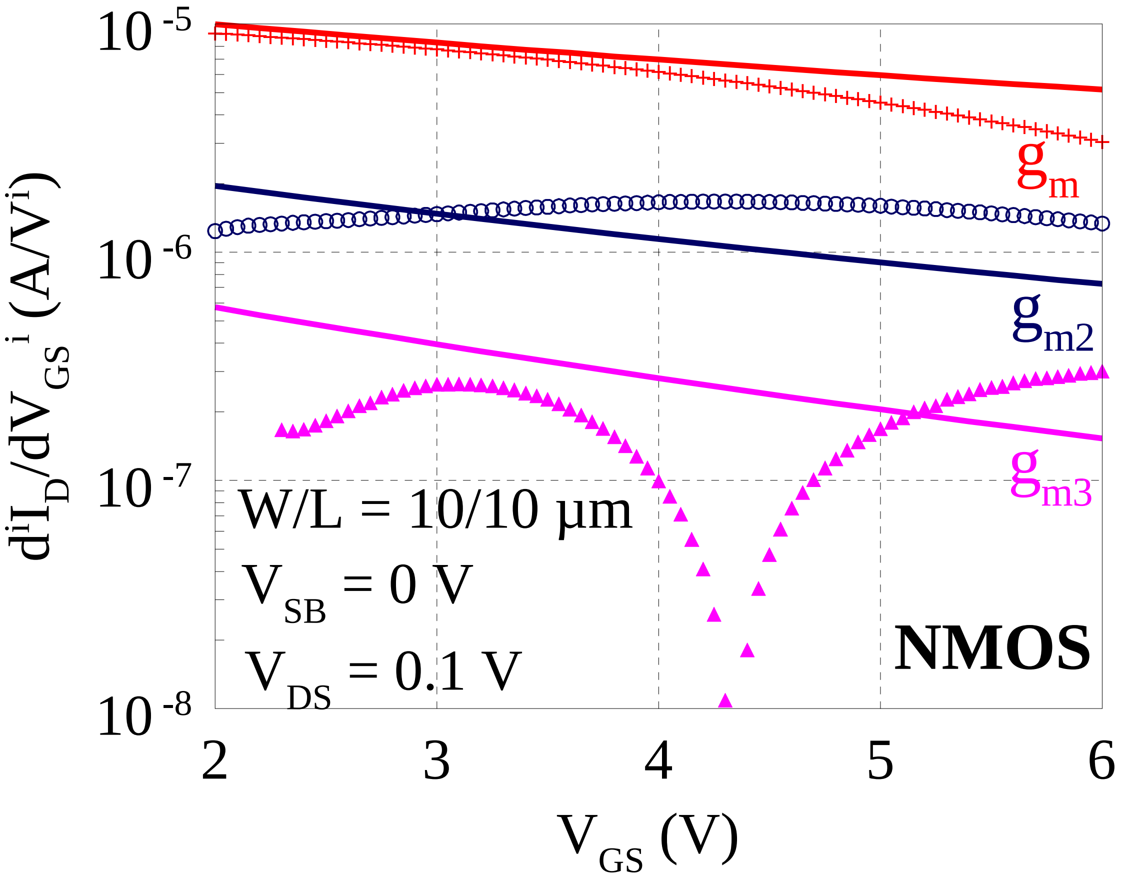
where:

$$V_{DSx} = \frac{V_{DS} \cdot V_{DSAT}}{\left(V_{DS}^{2m} + V_{DSAT}^{2m}\right)^{\frac{1}{2m}}}$$

(K. Joardar et al, IEEE TED-45, pp. 134-148, 1998)

DC-Model : Mobility Reduction

MOS Model 9: $m = \frac{m_0}{1 + q \times E_{eff}}$



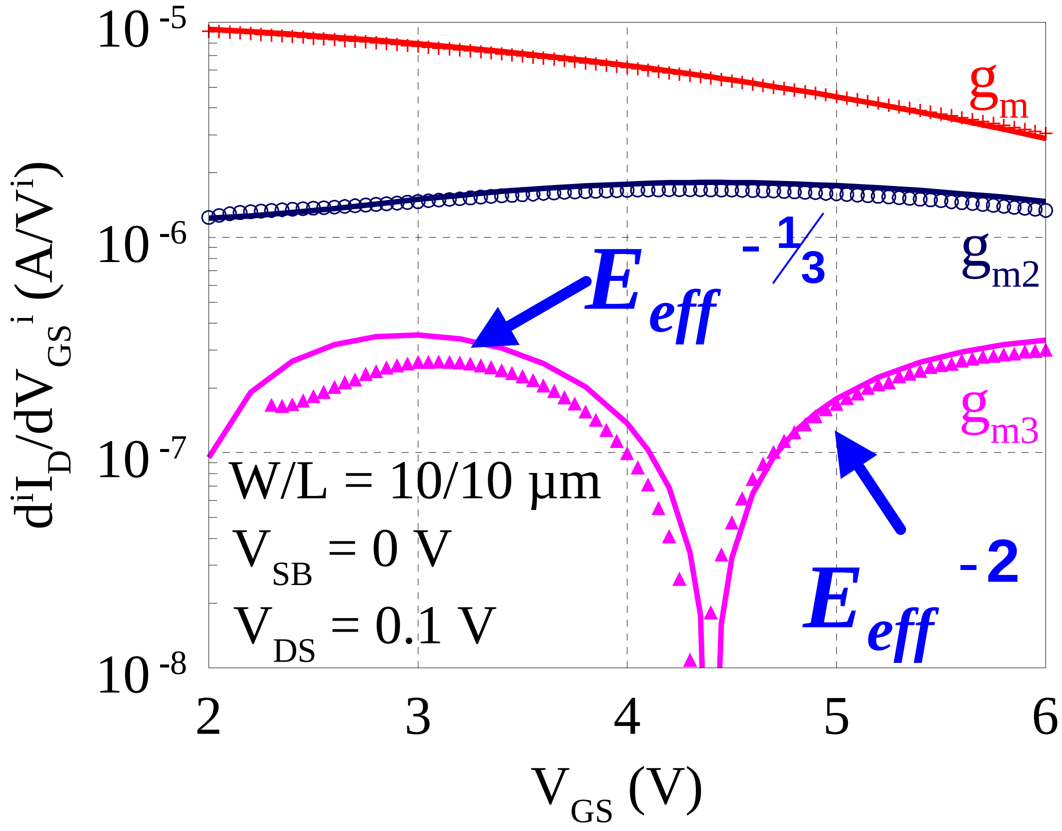
⇒ **higher-order derivatives:**

$$g_{mi} = \frac{\P^i I_D}{\P V_{GS}{}^i}$$

not well described

DC-Model : Mobility Reduction (II)

- **surface roughness scattering:** $\mu_{sr} \propto E_{eff}^{-2}$
- **phonon scattering:** $\mu_{ph} \propto E_{eff}^{-1/3}$



$$\mu = \frac{\mu_0}{1+\sqrt{\theta_{sr}\cdot E_{eff}^{4}+\theta_{ph}\cdot E_{eff}^{2/3}}}$$

(IEEE TED-44, No. 11, pp. 2044-2052, 1997)

$\Rightarrow$ **different for holes**

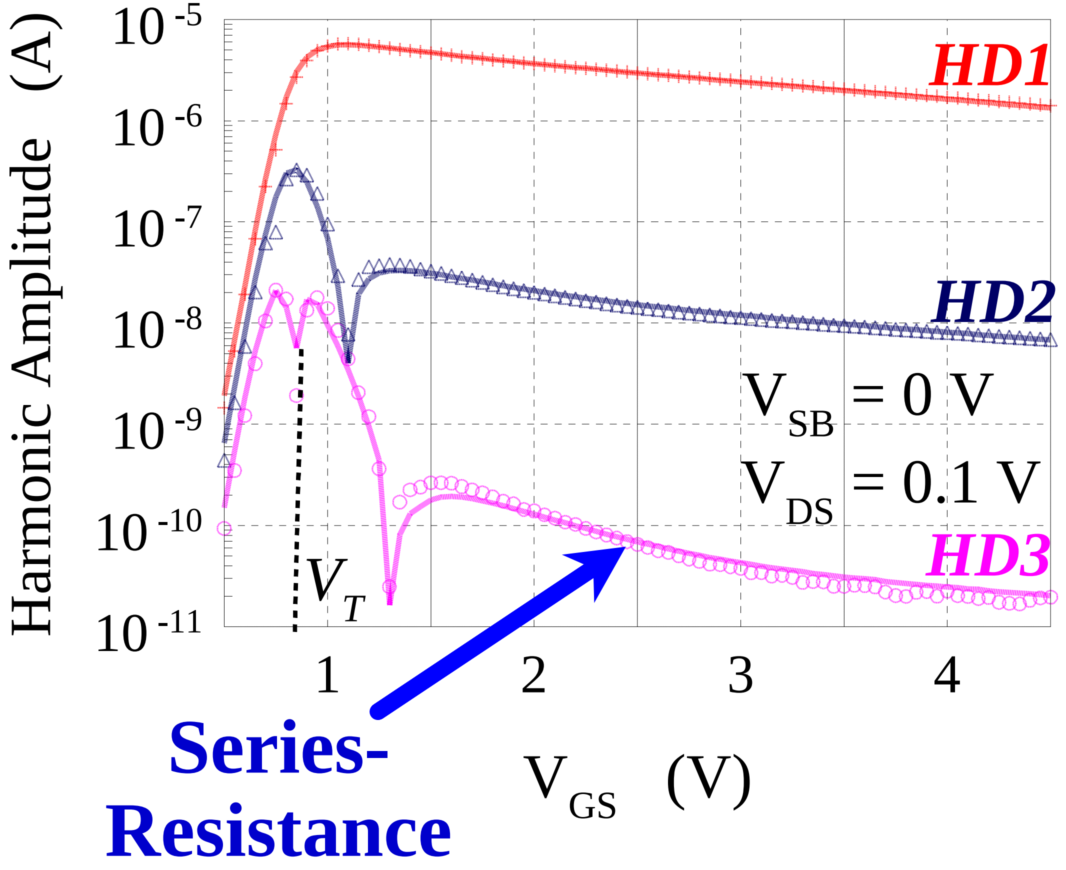
DC-Model : Bias-Dependent Series-Resistance

Internal series-resistance:

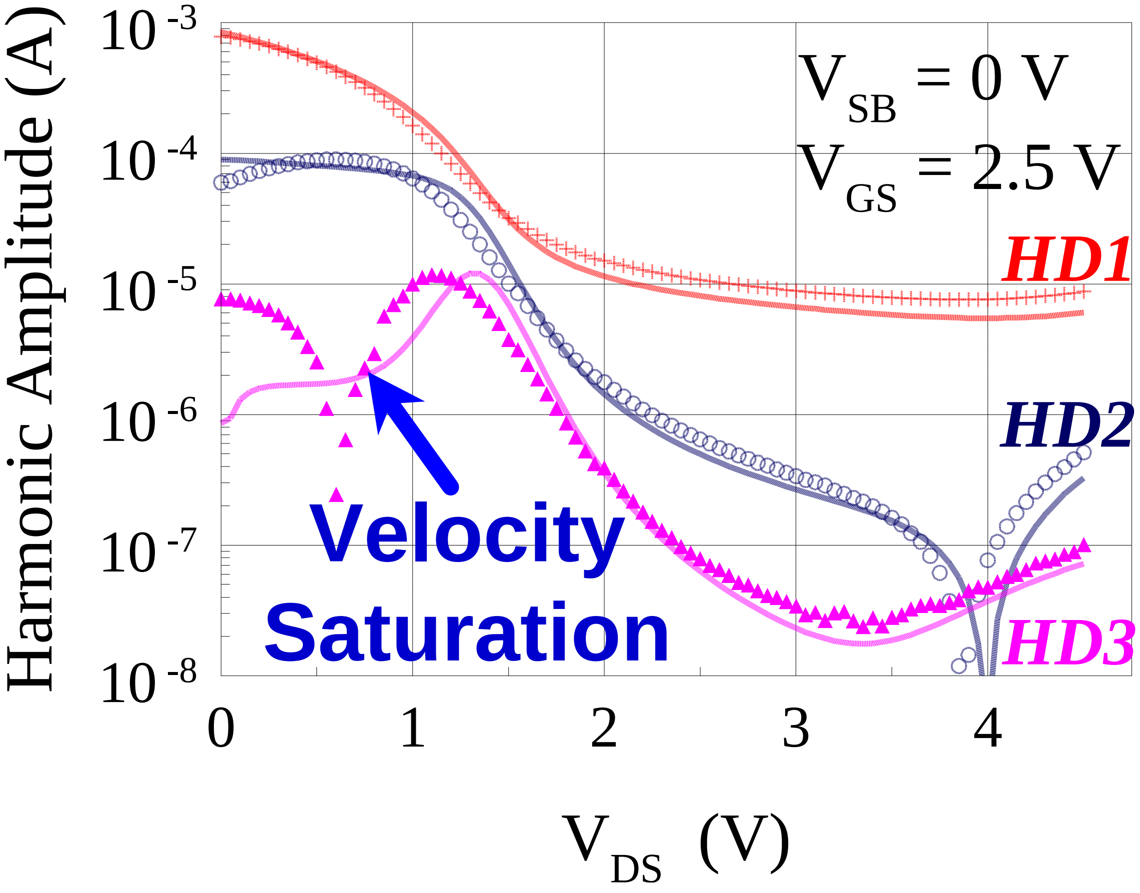
- **bias-dependent for LDD-MOSFETs**
- **independent parameters:**

$$q_R = 2 \cdot b \cdot R_{series}$$

Gate-bias induced distortion for NMOS W/L=10/1μm



DC-Model : Velocity Saturation



Velocity Saturation

Drain-bias induced distortion
NMOS, *W*/*L*=10 µm /1µm

Drain Current:

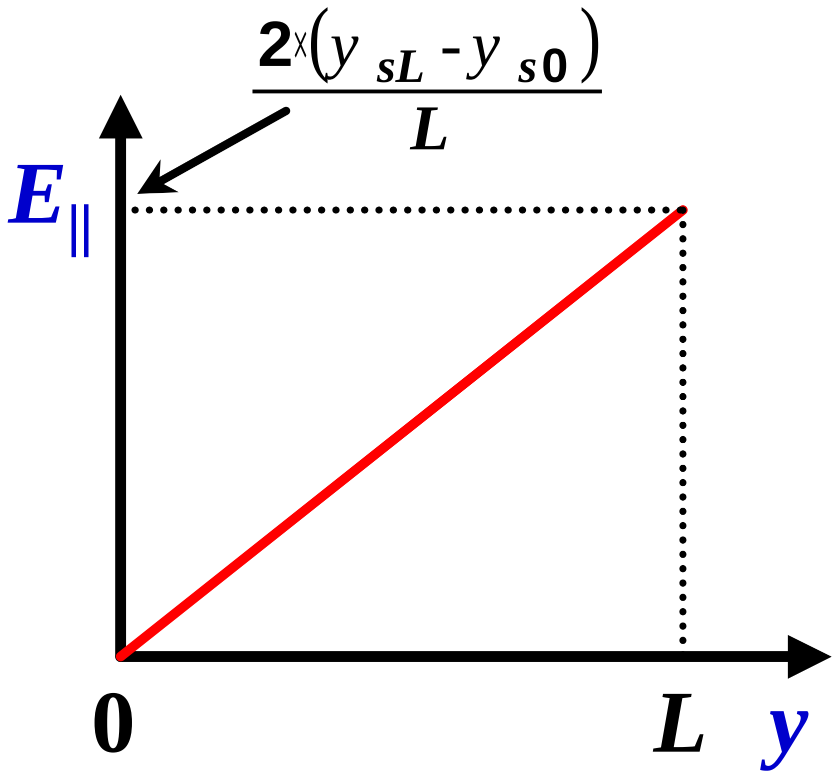
$$I_D = -W \times Q_{inv} \times v$$

Carrier Velocity (MM9, BSIM4):

$$v = \frac{\mu \times E_{\parallel}}{1 + \mu / v_{sat} \times E_{\parallel}}$$

DC-Model : Velocity Saturation (II)

Electron Velocity: $$v = \frac{\mu \cdot E_{\parallel}}{\sqrt{1 + \left(\mu / v_{sat} \cdot E_{\parallel} \right)^{2}}}$$

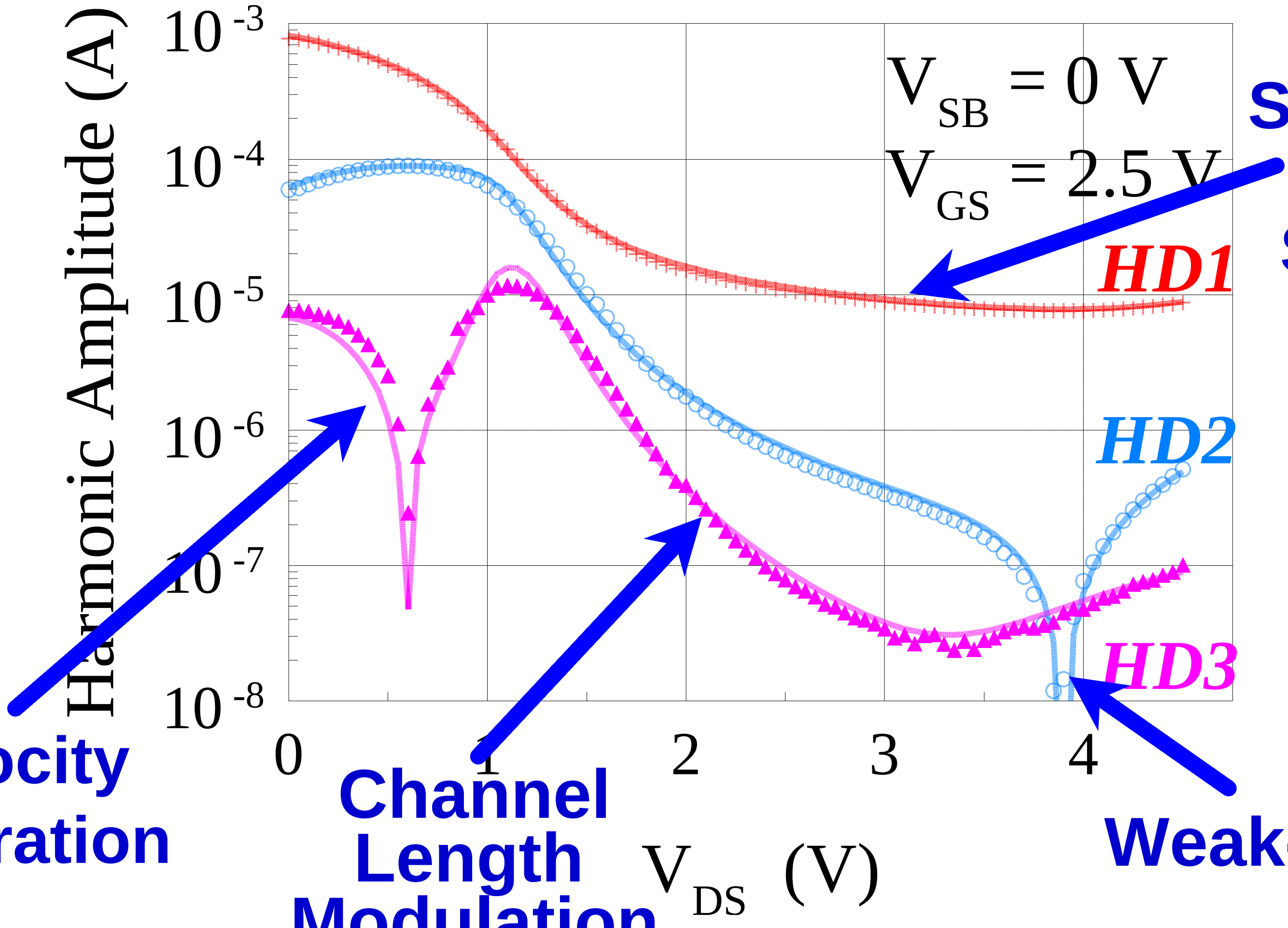


Approximation used in calculation of I_D:

Electric field $E_{\parallel}$ varies linearly along channel

DC-Model : Conductance Modelling

Drain-Bias Induced Distortion for NMOS W/L=10/1mm



Static Feedback and Self-Heating

Velocity Saturation

Channel Length Modulation

Weak-Avalanche

DC-Model : Symmetry

Symmetry of MOSFET : Drain ↔ Source

$$I_D(V_{GS} , V_{DS} , V_{SB}) = -I_D(V_{GD} , V_{SD} , V_{DB})$$

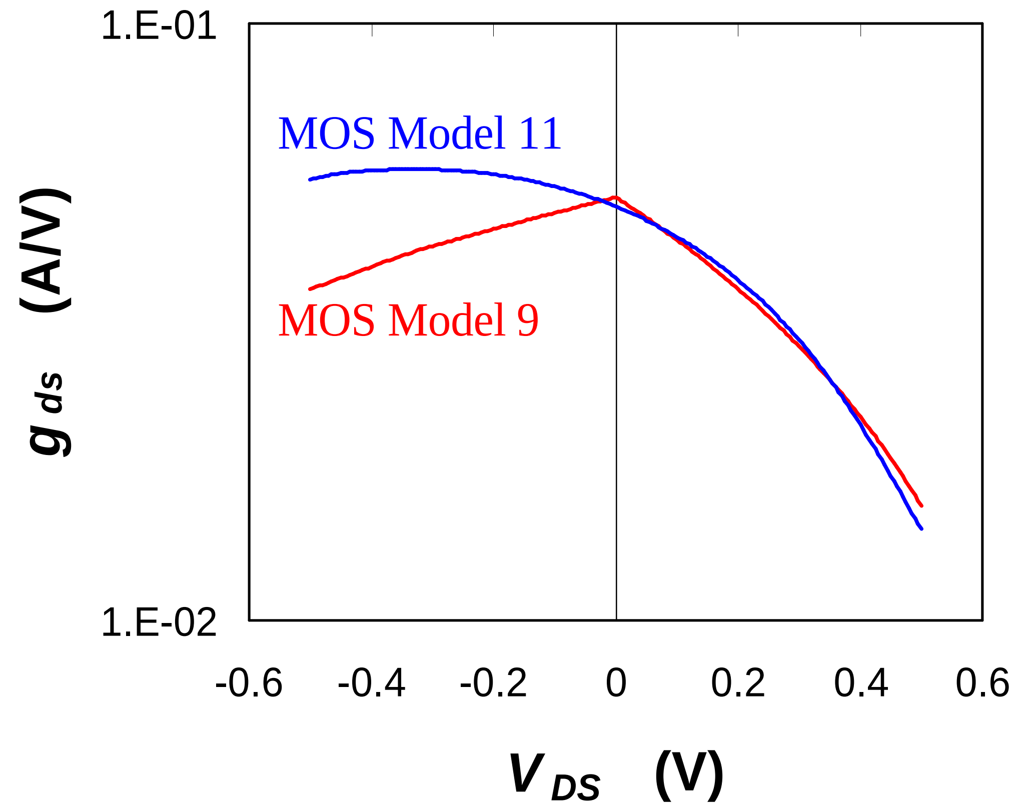
Care has to be taken with the implementation of:

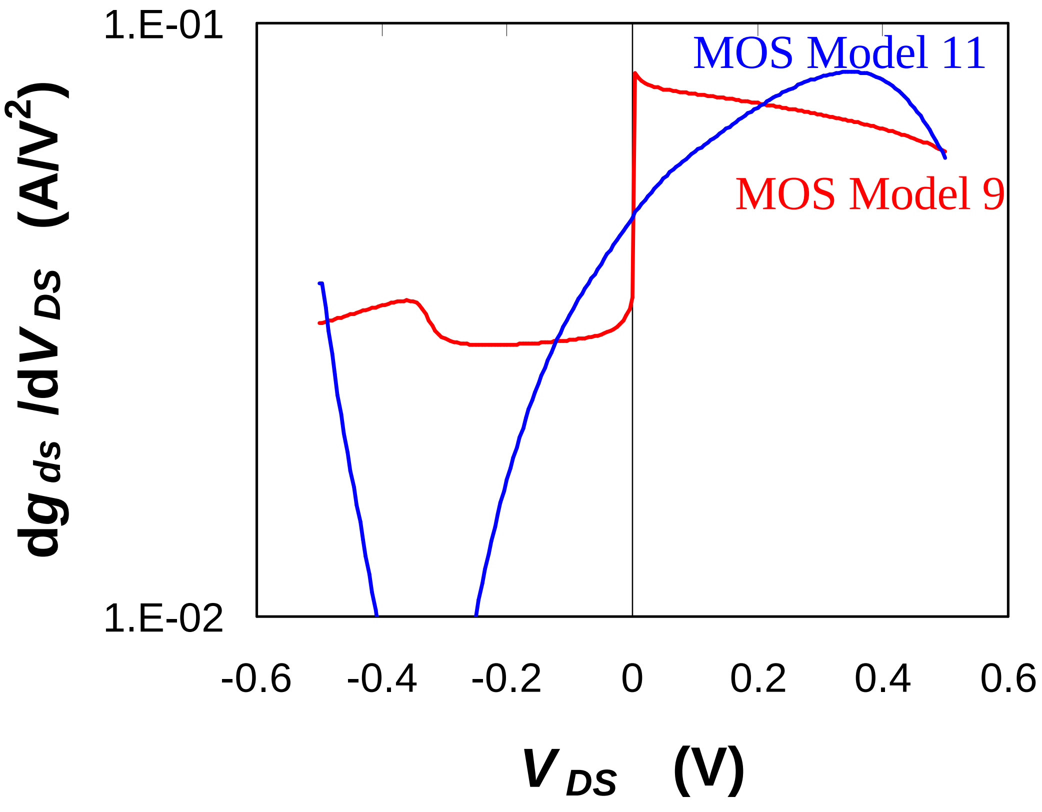
- ideal current equation
- velocity saturation
- DIBL/static feedback
- smoothing function (linear/saturation region)

DC-Model : Symmetry (II)

Symmetry of MOSFET : Drain ↔ Source

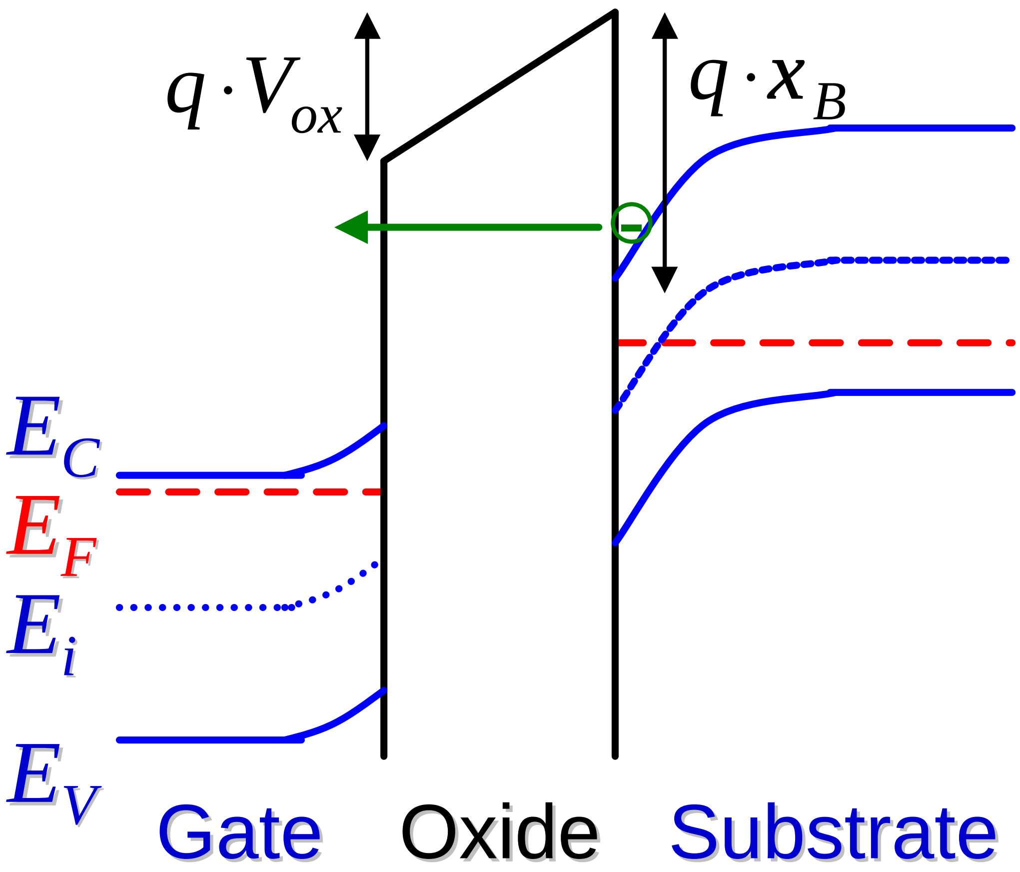
$$I_D(V_{GS}, V_{DS}, V_{SB}) = -I_D(V_{GD}, V_{SD}, V_{DB})$$





DC-Model : Gate Leakage Model

NMOS (in inversion):



Gate current density:

$$J_G \propto V_{ox} \cdot Q_{inv} \cdot P(V_{ox})$$

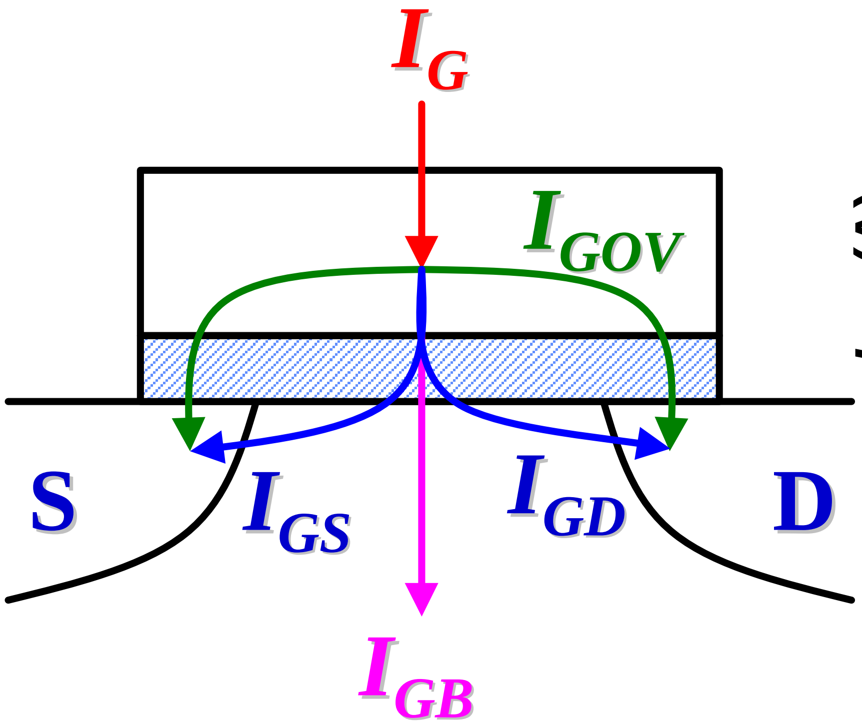
Direct-tunnelling probability:

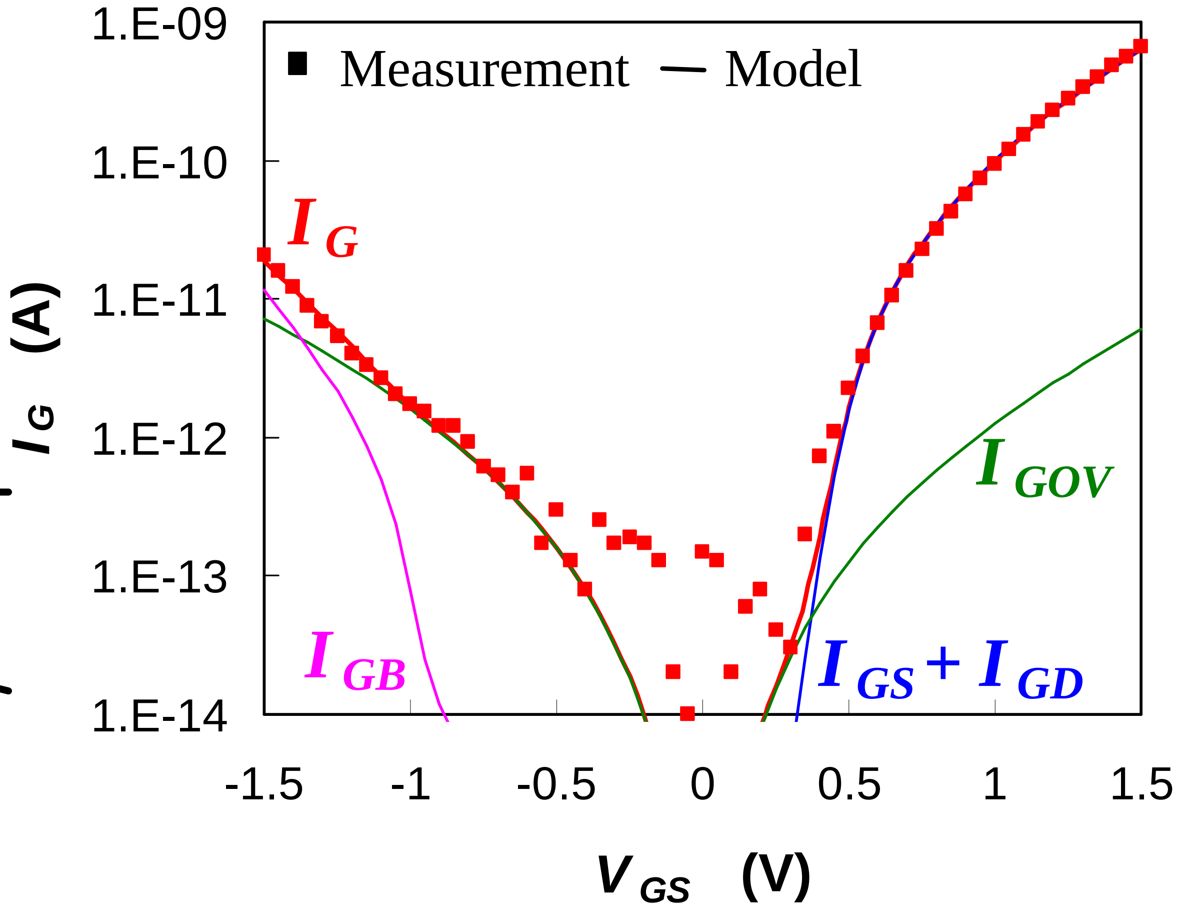
$$P(V_{ox}) = e^{B/V_{ox} \cdot \left[\left(1 - V_{ox}/x_B\right)^{3/2} - 1\right]}$$

Approximation (at V_{DS}=0 V):

$$I_G = \mathbf{I_O} \cdot V_{ox} \cdot Q_{inv} \cdot e^{\mathbf{B_O} \cdot V_{ox}}$$

DC-Model : Gate Leakage Model (II)

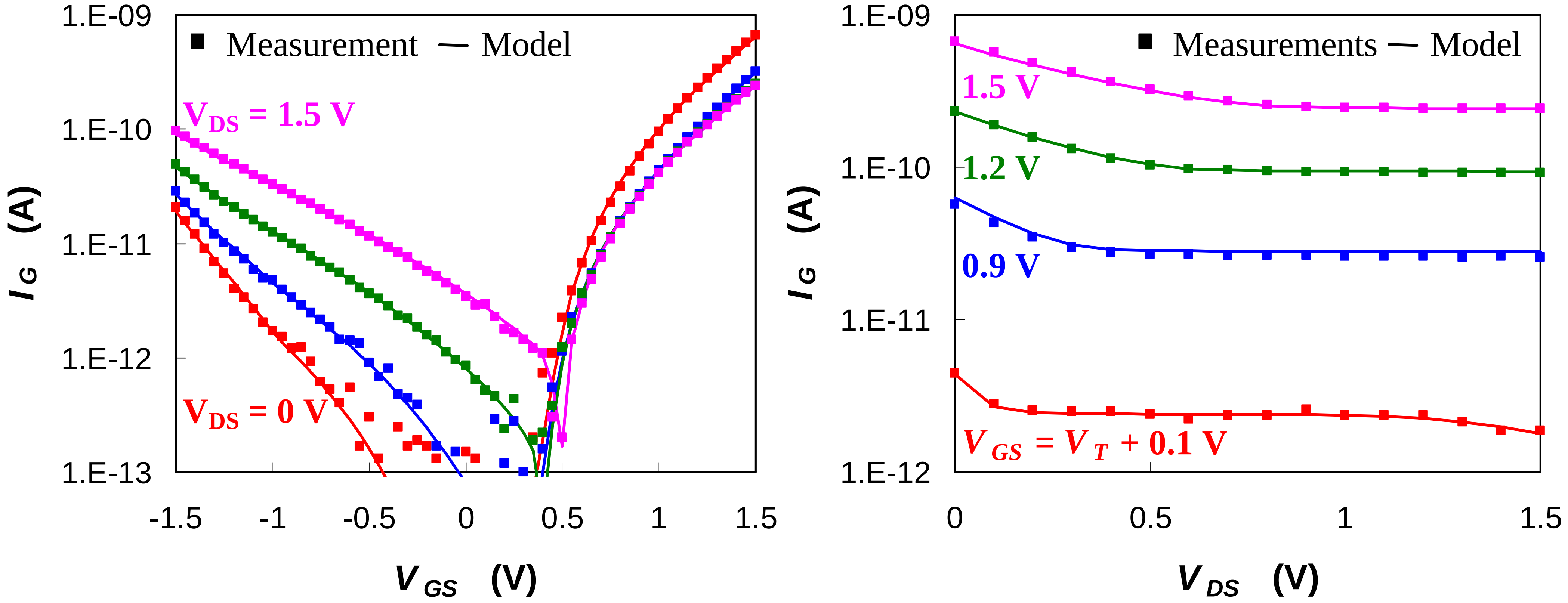




NMOS, V_{DS}=0 V, t_{ox}=2 nm, W/L=10/0.6μm

DC-Model : Gate Leakage Model (III)

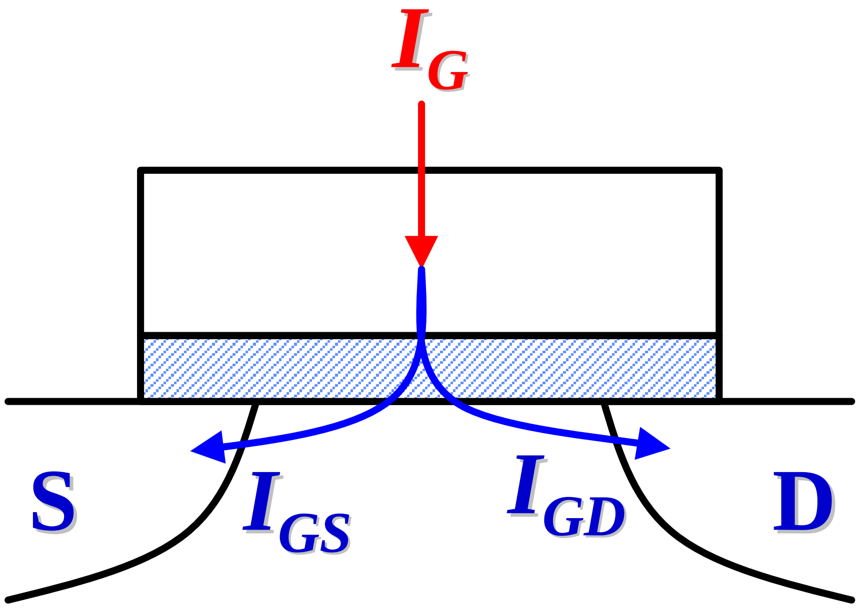
$$I_G = \mathbf{I_O} \cdot \int V_{ox} \cdot Q_{inv} \cdot e^{\mathbf{B_O} \cdot V_{ox}} \cdot {}^{dy}\!/_{L}$$

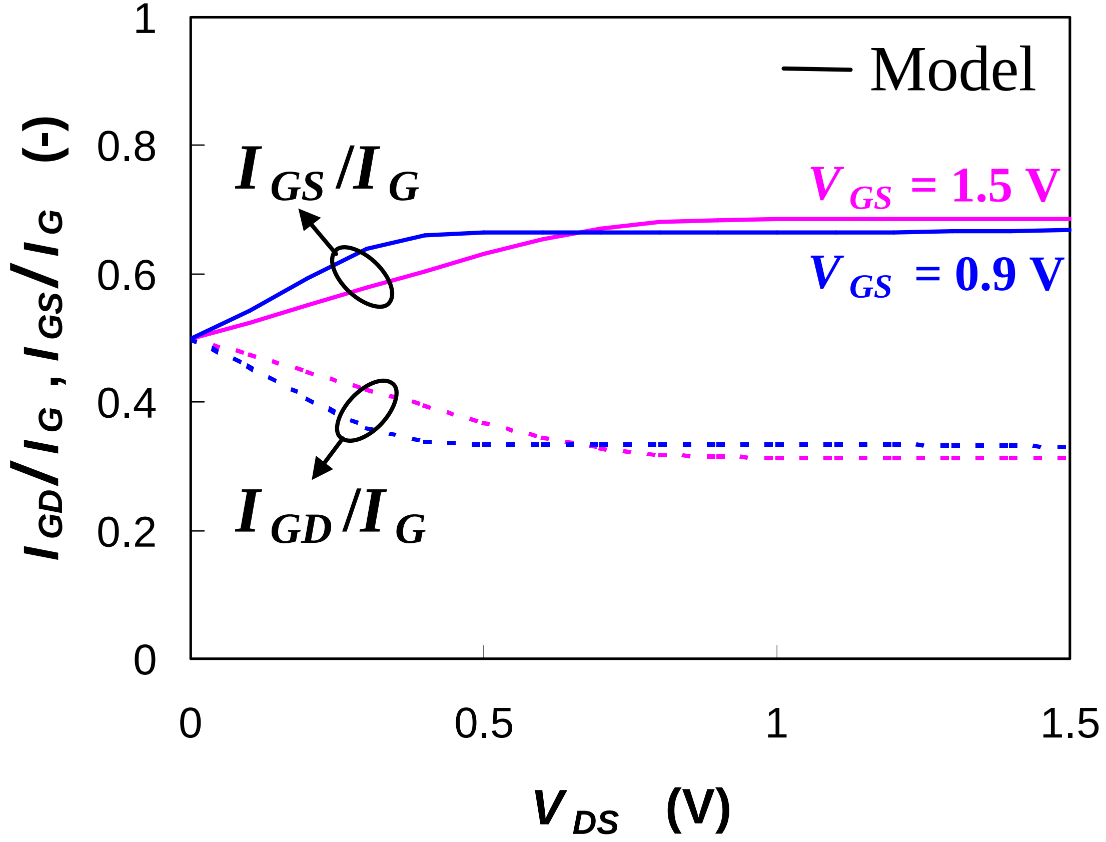


NMOS, V_{SB}=0 V, t_{ox}=2 nm, W/L=10/0.6μm

DC-Model : Gate Leakage Model (IV)

NMOS, t_{ox}=2 nm, W/L=10/0.6µm



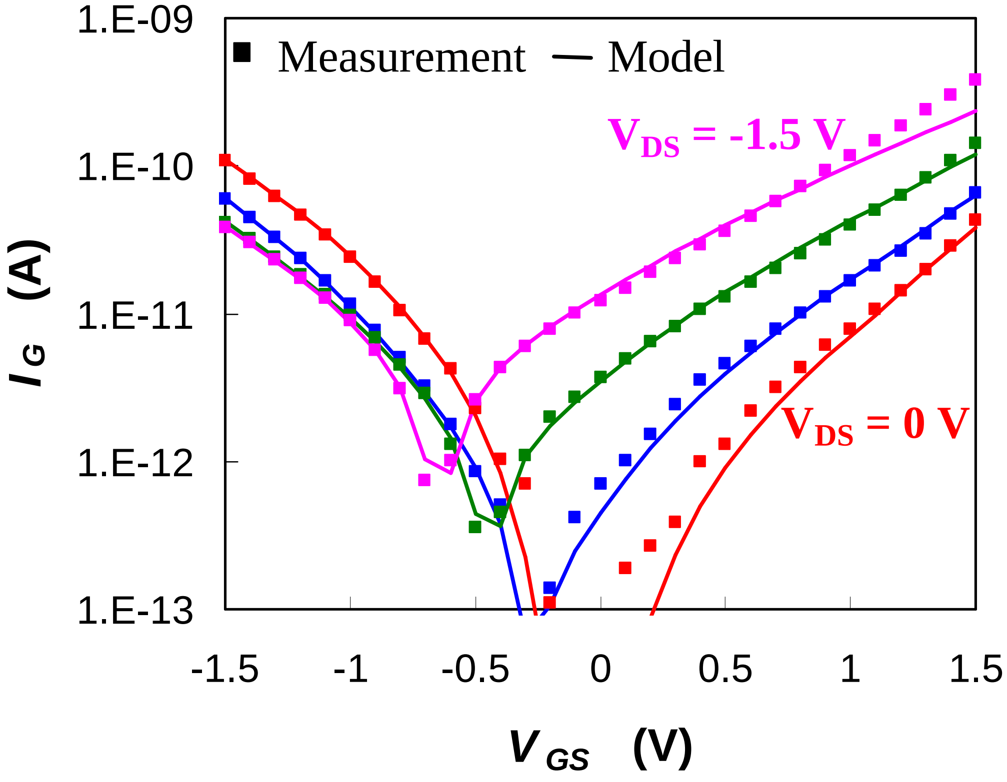


$$I_{GS} = I_G - I_{GD}$$

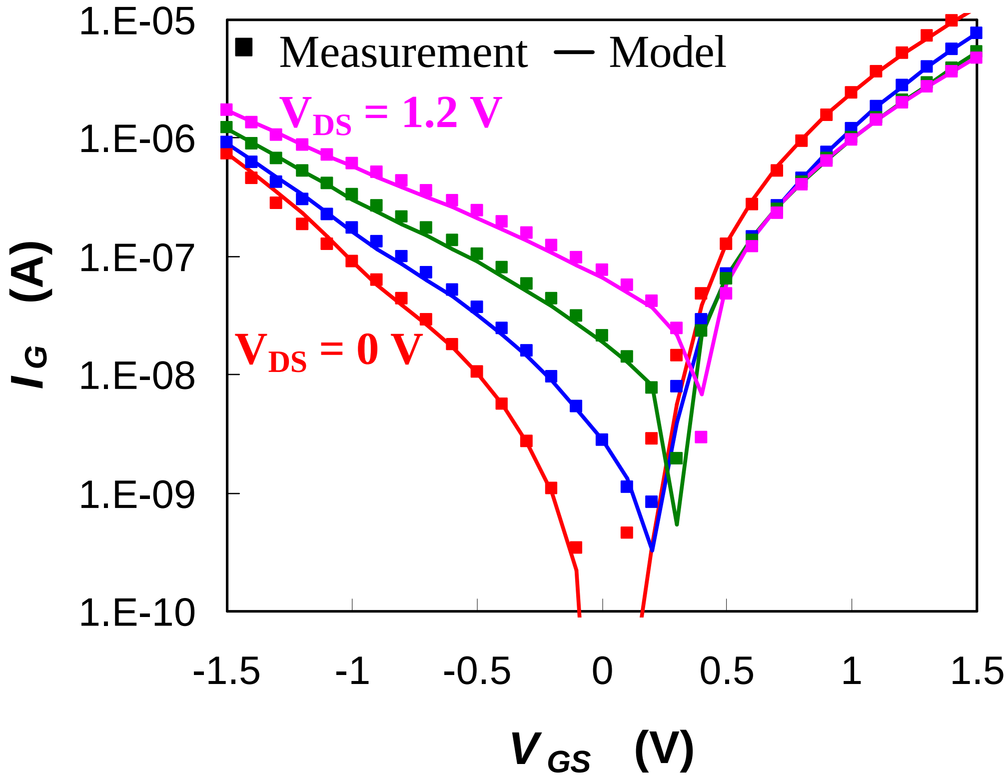
$$I_{GD} = \mathbf{I_O} \cdot \int {}^{y}\!/_{L} \cdot V_{ox} \cdot Q_{inv} \cdot e^{\mathbf{B_O} \cdot V_{ox}} \cdot {}^{dy}\!/_{L}$$

DC-Model : Gate Leakage Model (V)

W/L=10/0.6μm, V_{SB}=0 V

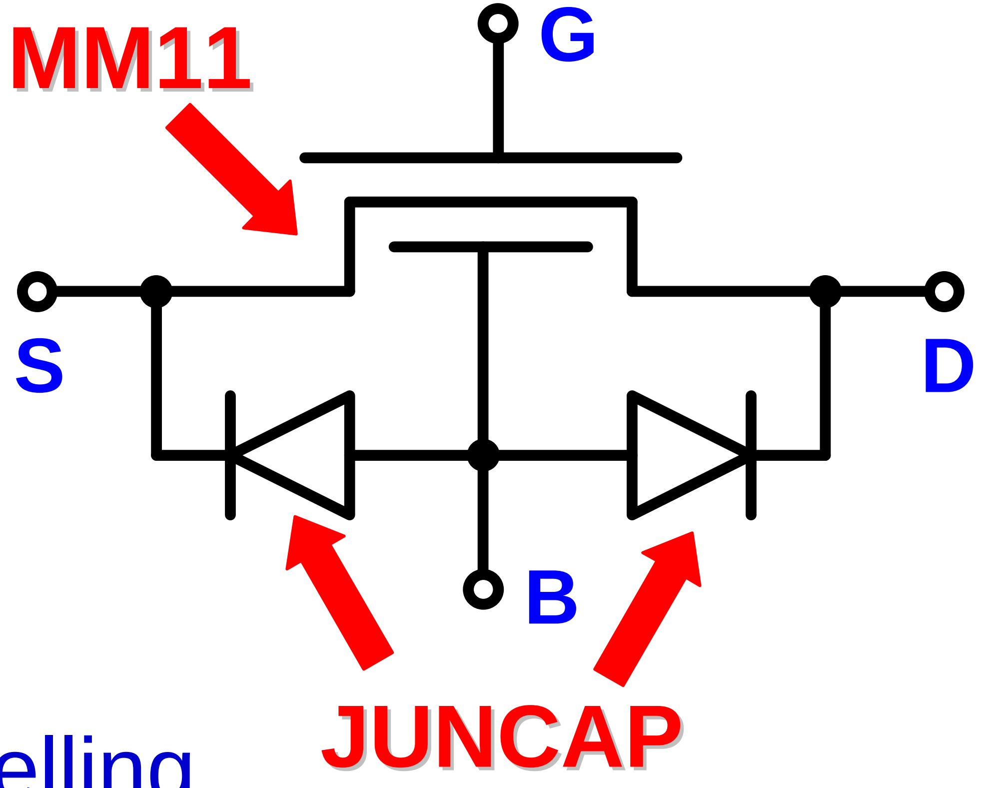


PMOS, t_{ox}=2 nm



NMOS, t_{ox}=1.55 nm

DC-Model : Junction Model



Junctions modelled by JUNCAP-model

⇒ based on Level=500 diode model:

- trap-assisted tunnelling
- band-to-band tunnelling

Outline : AC-Model

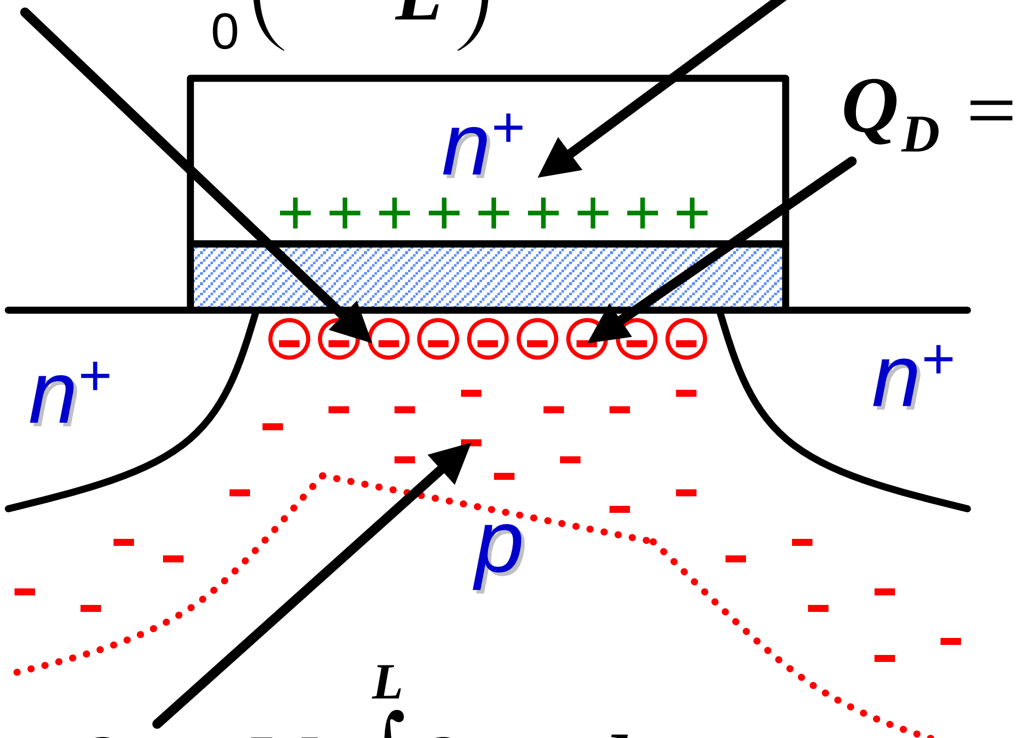
- Intrinsic charges
- Gate poly depletion
- Quantum-mechanical effects
- Bias-dependent overlap capacitance

AC-Model : Intrinsic Charges

$$Q_S = W \cdot \int_0^L \left(1 - \frac{y}{L}\right) \cdot Q_{inv} \cdot dy$$

$$Q_G = -Q_D - Q_S - Q_B$$

$$Q_D = W \cdot \int_0^L \frac{y}{L} \cdot Q_{inv} \cdot dy$$



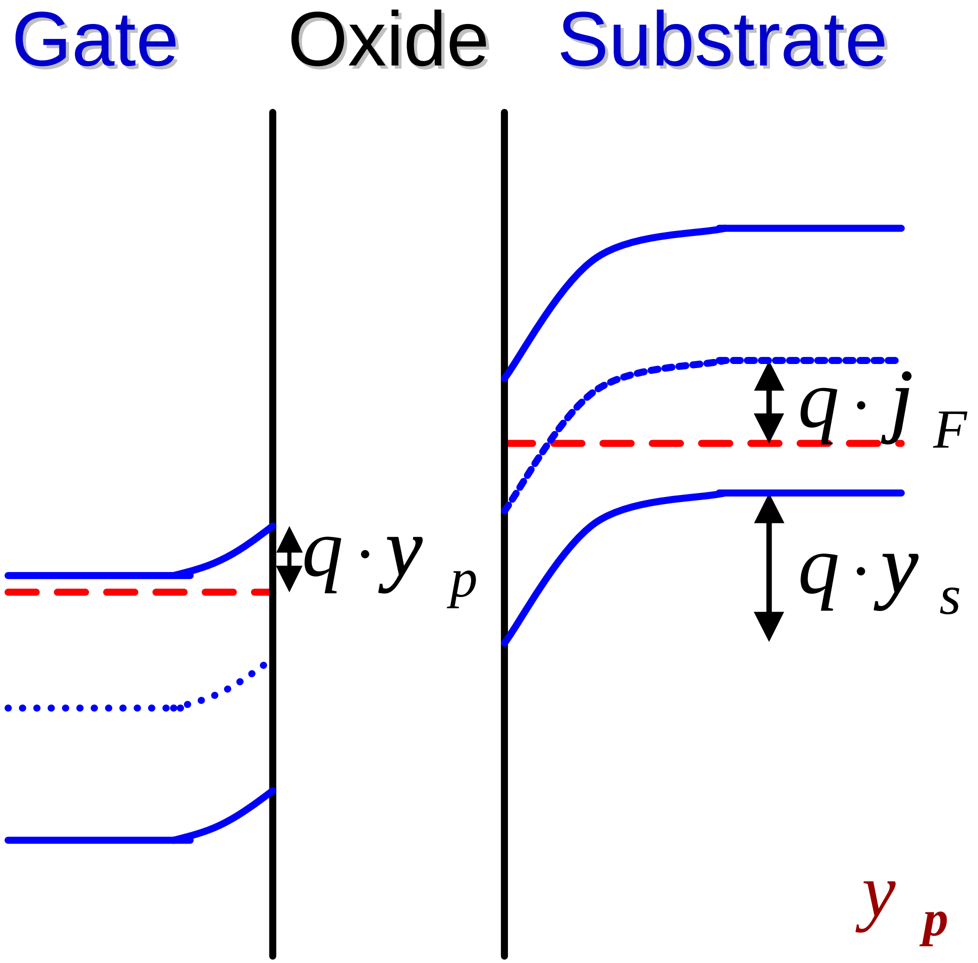
$$Q_B = W \cdot \int_0^L Q_{dep} \cdot dy$$

Intrinsic Capacitances:

$$C_{ij} = \begin{cases} \dfrac{\partial Q_i}{\partial V_j} & \text{for } i = j \\ -\dfrac{\partial Q_i}{\partial V_j} & \text{for } i \neq j \end{cases}$$

where *i*, *j* =G, S, D or B

AC-Model : Gate Depletion Effect



Body factor of poly-silicon:

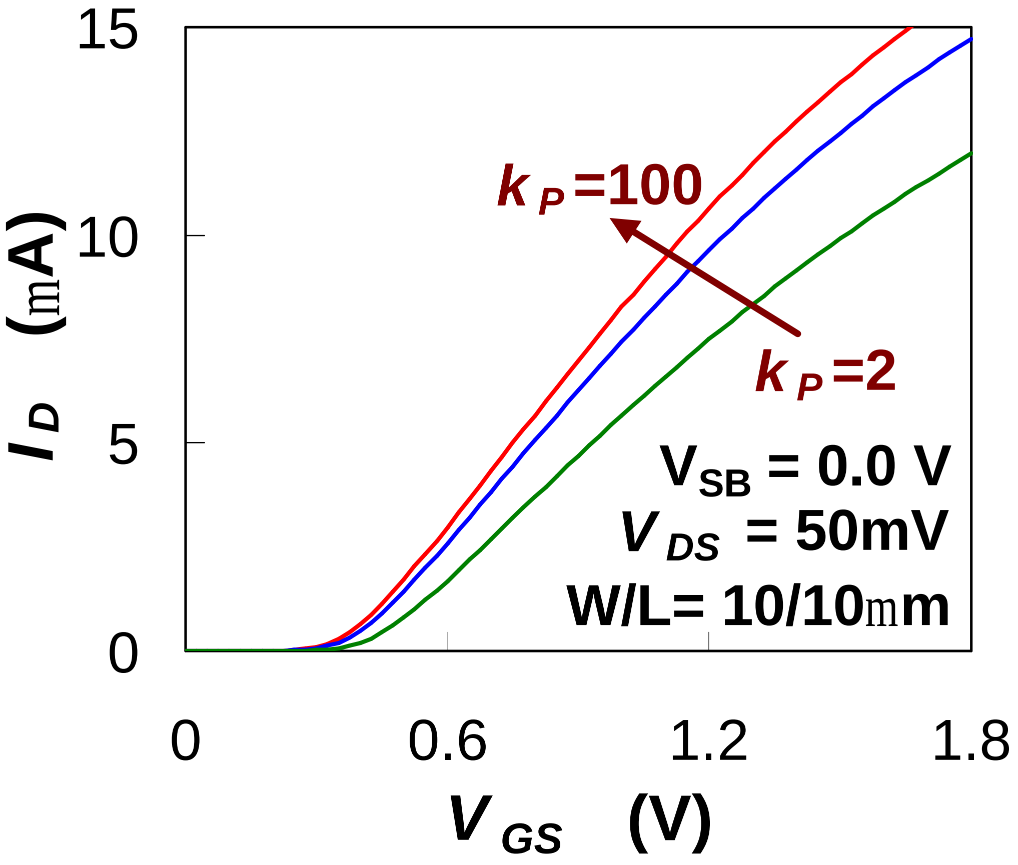
$$k_P = \frac{\sqrt{2 \cdot q \cdot \varepsilon_{Si} \cdot N_P}}{C_{ox}}$$

Gate surface potential:

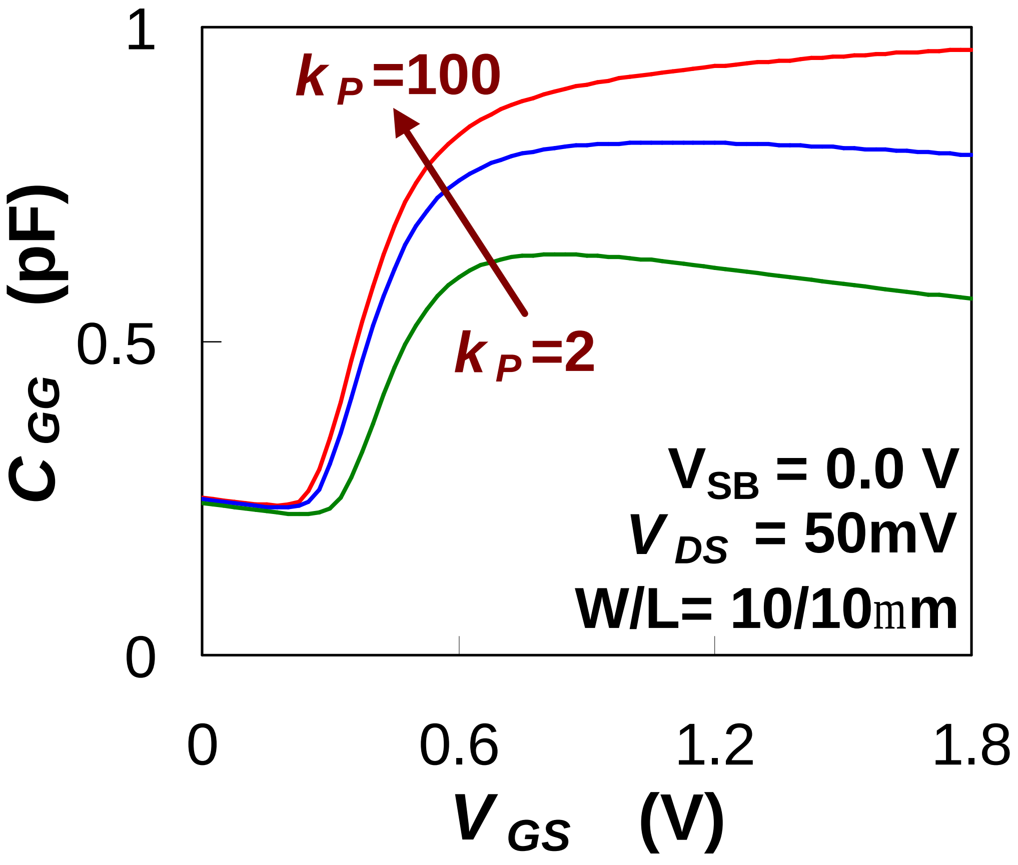
$$\psi_p = \left(\sqrt{\mathbf{V_{GB}} - \mathbf{V_{FB}} - \psi_s + \frac{\mathbf{k_p}^2}{4}} - \frac{\mathbf{k_p}}{2} \right)^2$$

AC-Model : Gate Depletion Effect (II)

Drain current

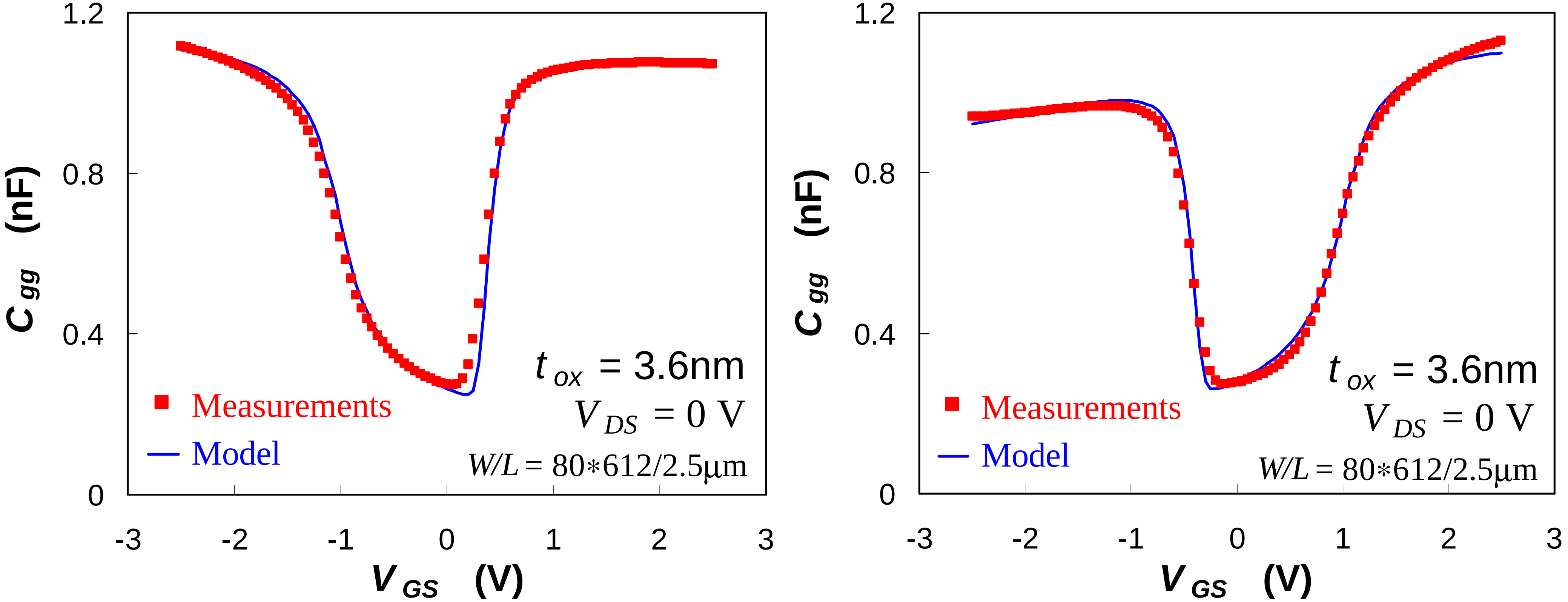


Gate capacitance



AC-Model : Gate Depletion Effect (III)

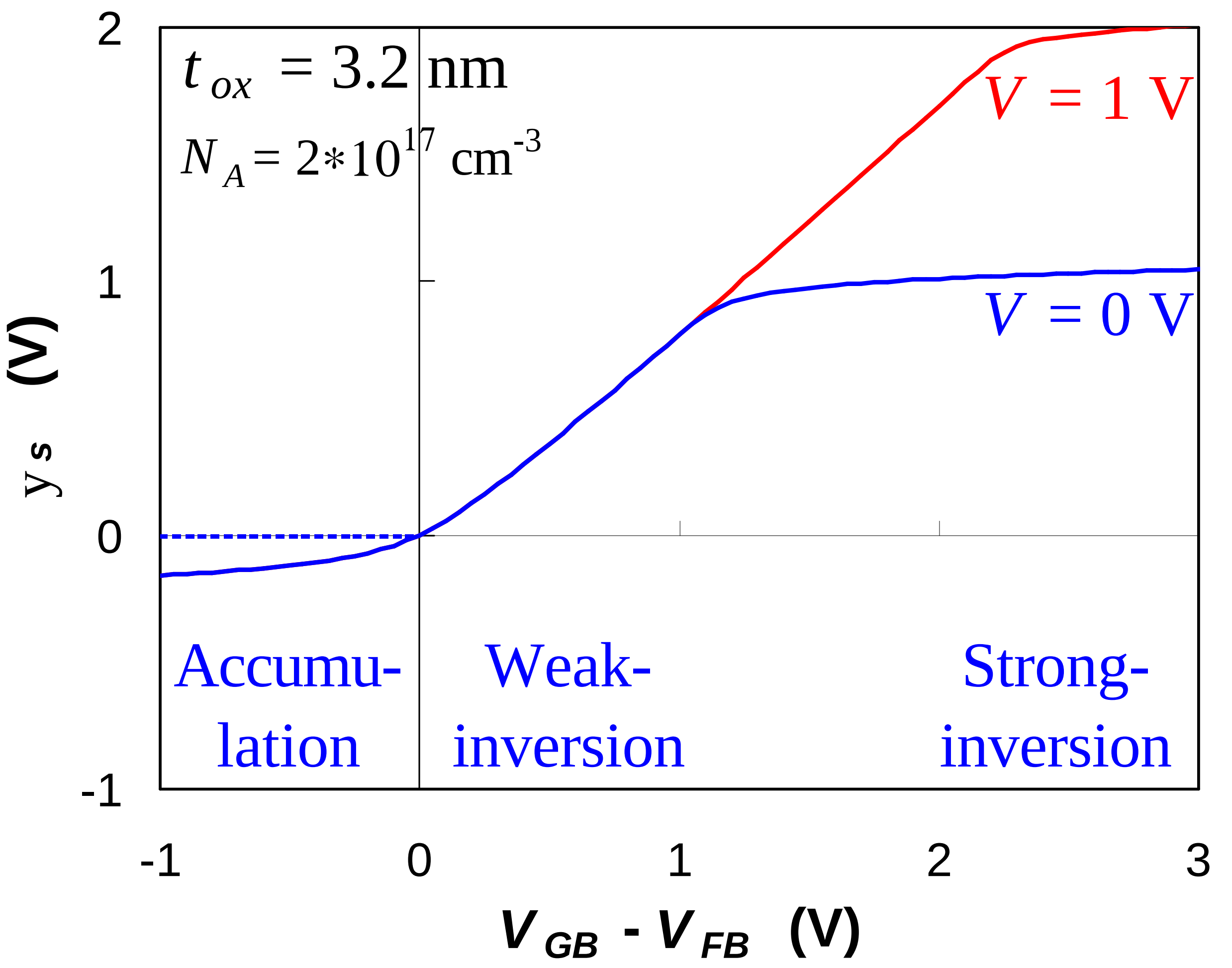
Including gate depletion effect ⇒ using electrical t_{ox}



NMOS 0.18µm CMOS PMOS

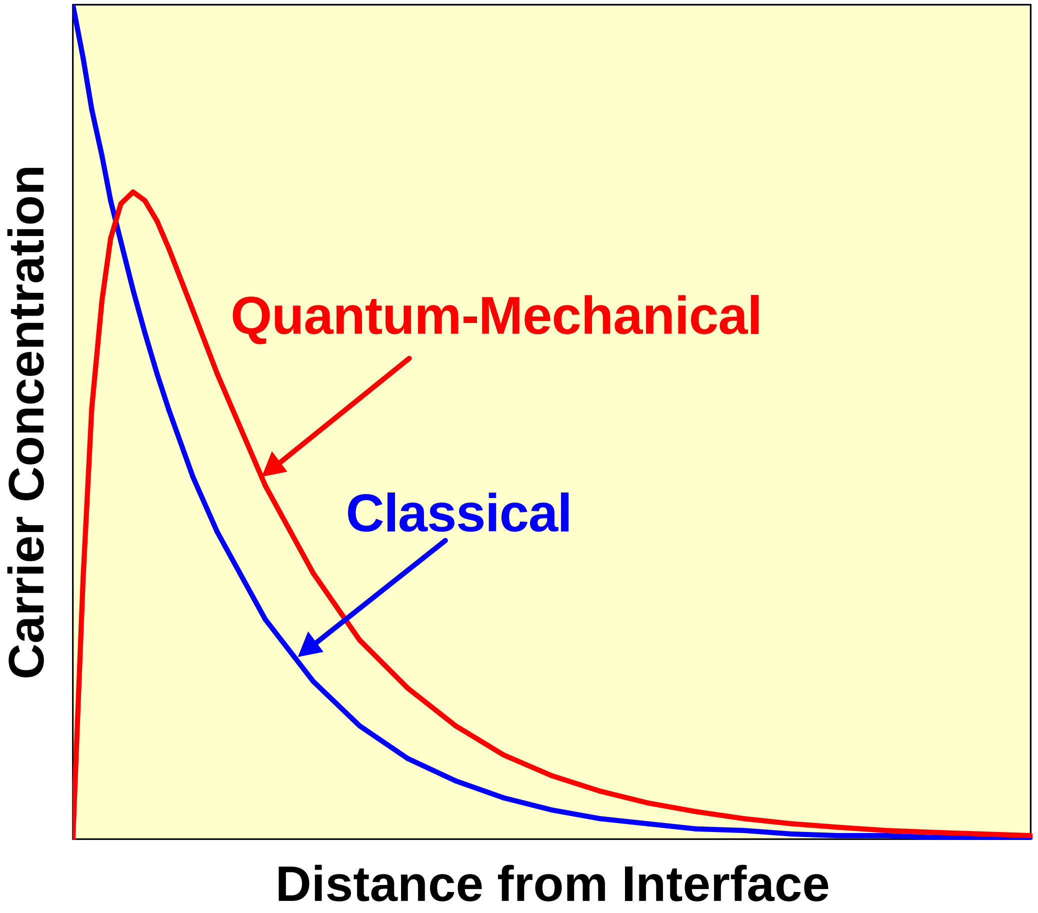
AC-Model : Accumulation

Approximation in accumulation (no parameters added)



AC-Model : Quantum-Mechanical Effects

Inversion-layer is formed at distance Δz from interface



$$\Delta z \propto E_{eff}^{-1/3}$$

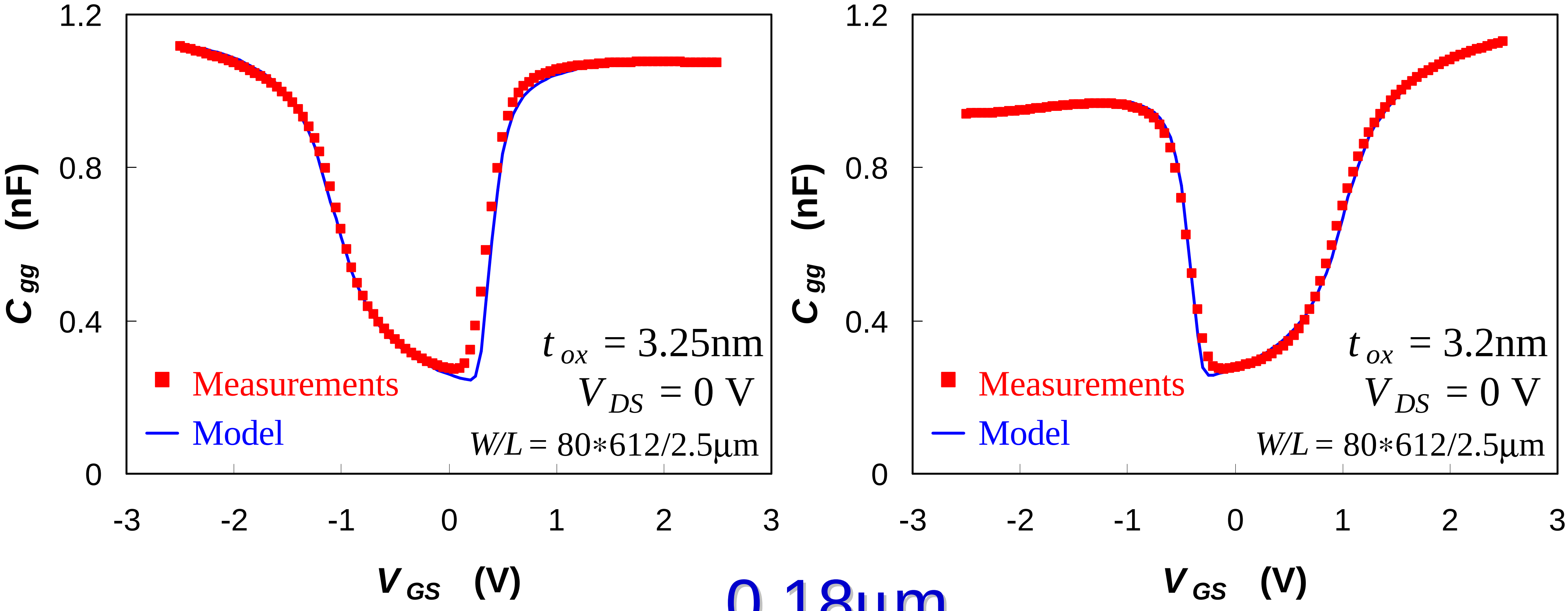
(F. Stern, CRC Crit. Rev. Solid State Sci., pp.499-514, 1974)

Effective oxide thickness:

$$t_{ox_{eff}} = t_{ox} + \frac{e_{ox}}{e_{Si}} \cdot \Delta z$$

AC-Model : QM-Effects (II)

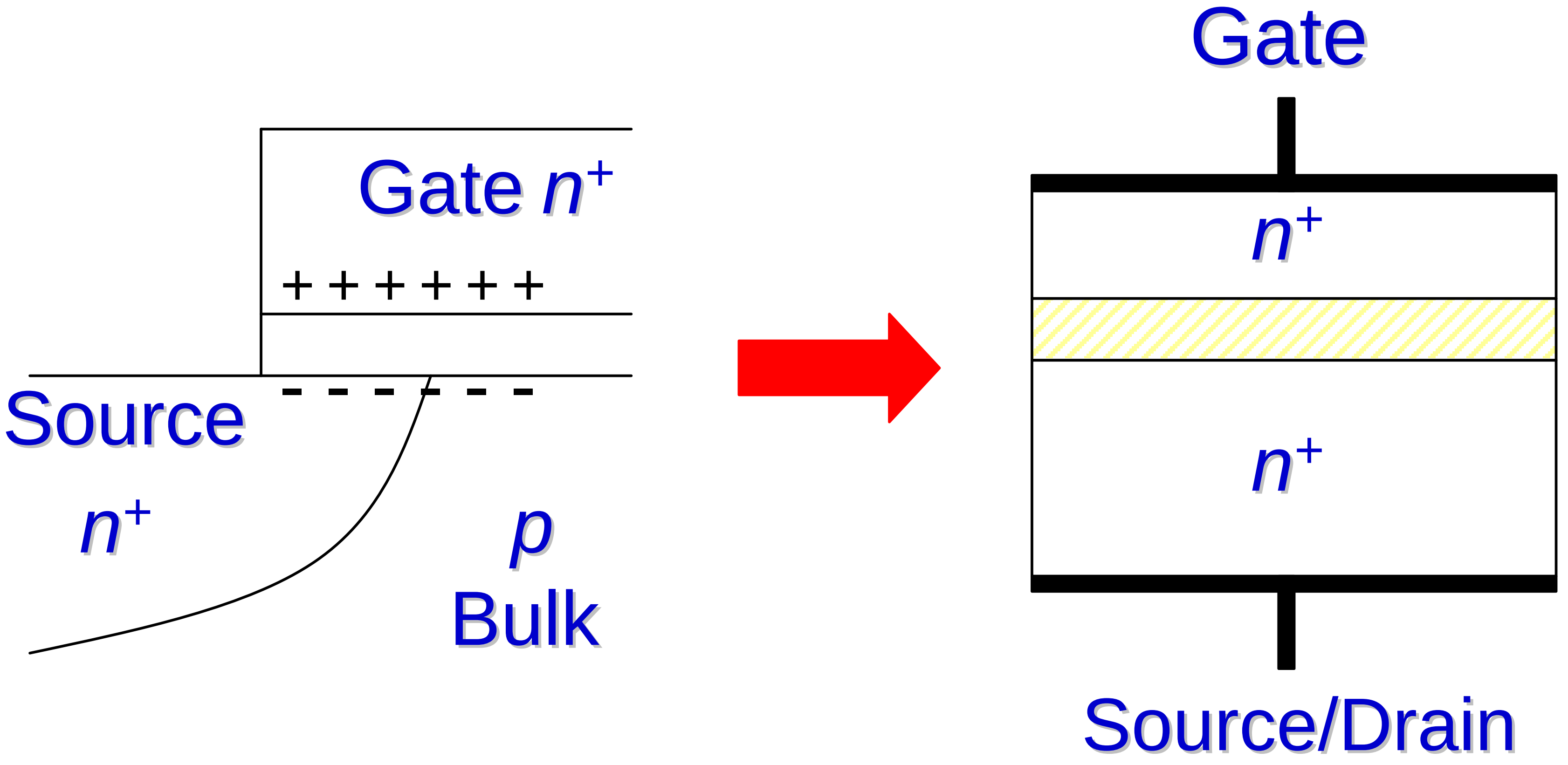
Including QM-effects ⇒ using physical t_{ox}



0.18µm

NMOS CMOS PMOS

AC-Model : Bias-Dependent Overlap Capacitance

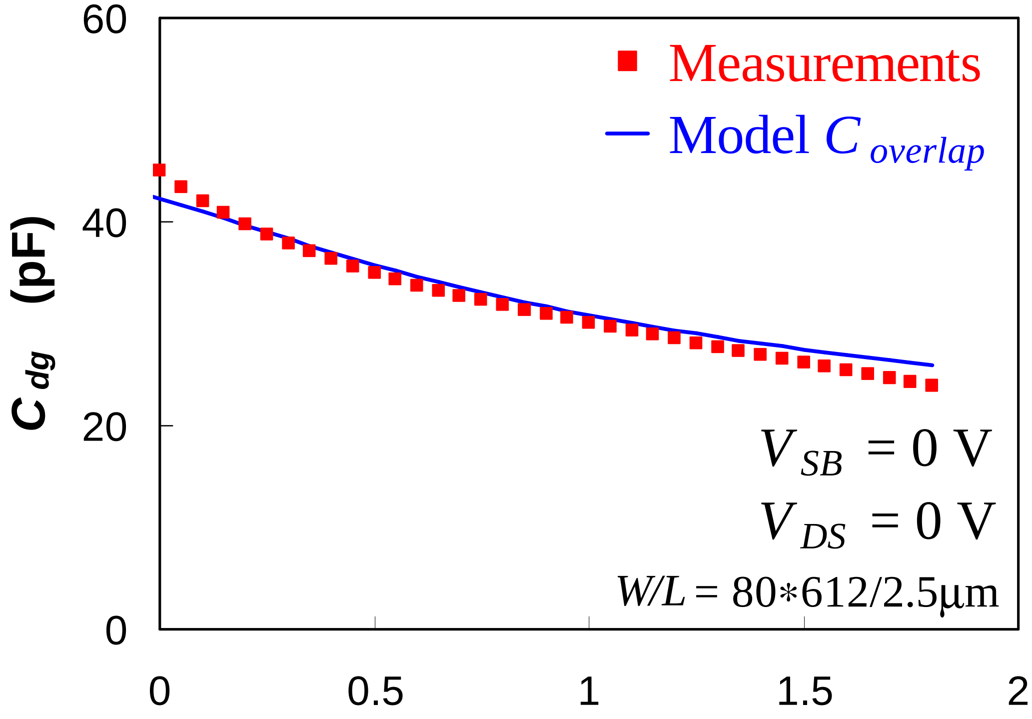


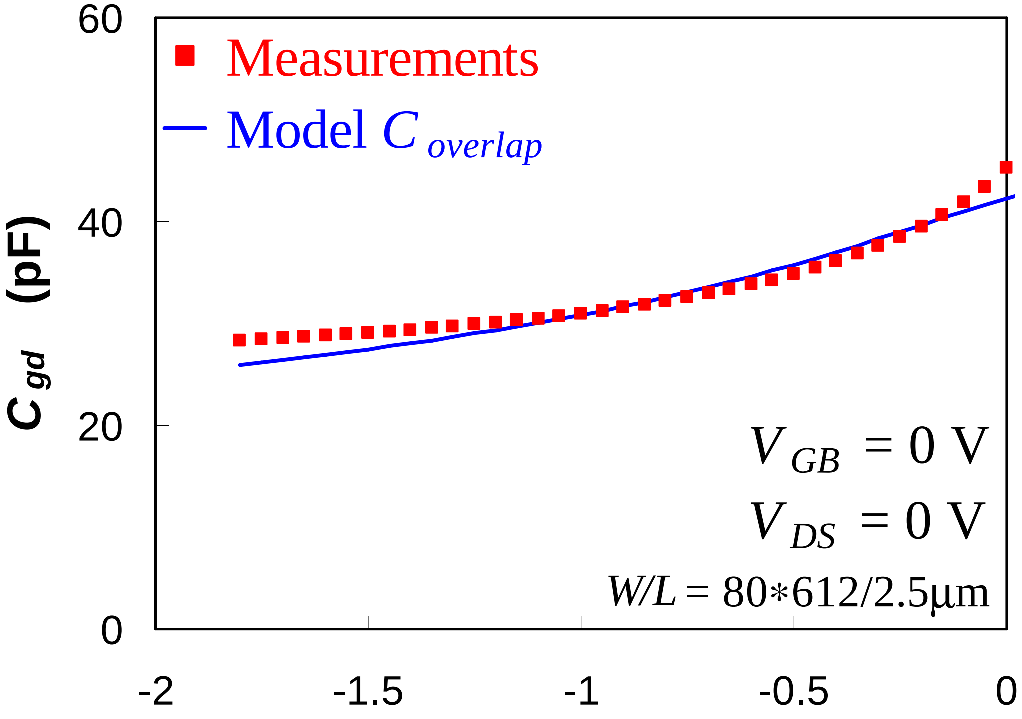
Two-terminal MOS-capacitance

Accumulation and depletion region included

AC-Model : Bias-Dependent Overlap Capacitance (II)

Two parameters (V_{FBov} and k_{ov})





C_{DG}

0.18µm CMOS

PMOS

C_{GD}

Outline

- Introduction
- DC-Model
- AC-Model
- **Noise Model**
- Model Parameters & Extraction
- Examples & Applications
- Conclusions

Noise Model

- **1/*f*-Noise: Unified Model (**BSIM4, MM9**)**

(Kwok K. Hung et al., IEEE TED-37 (3), p.654 , 1990;
ibid. (5), p.1323, 1990)

- **Thermal Noise:**

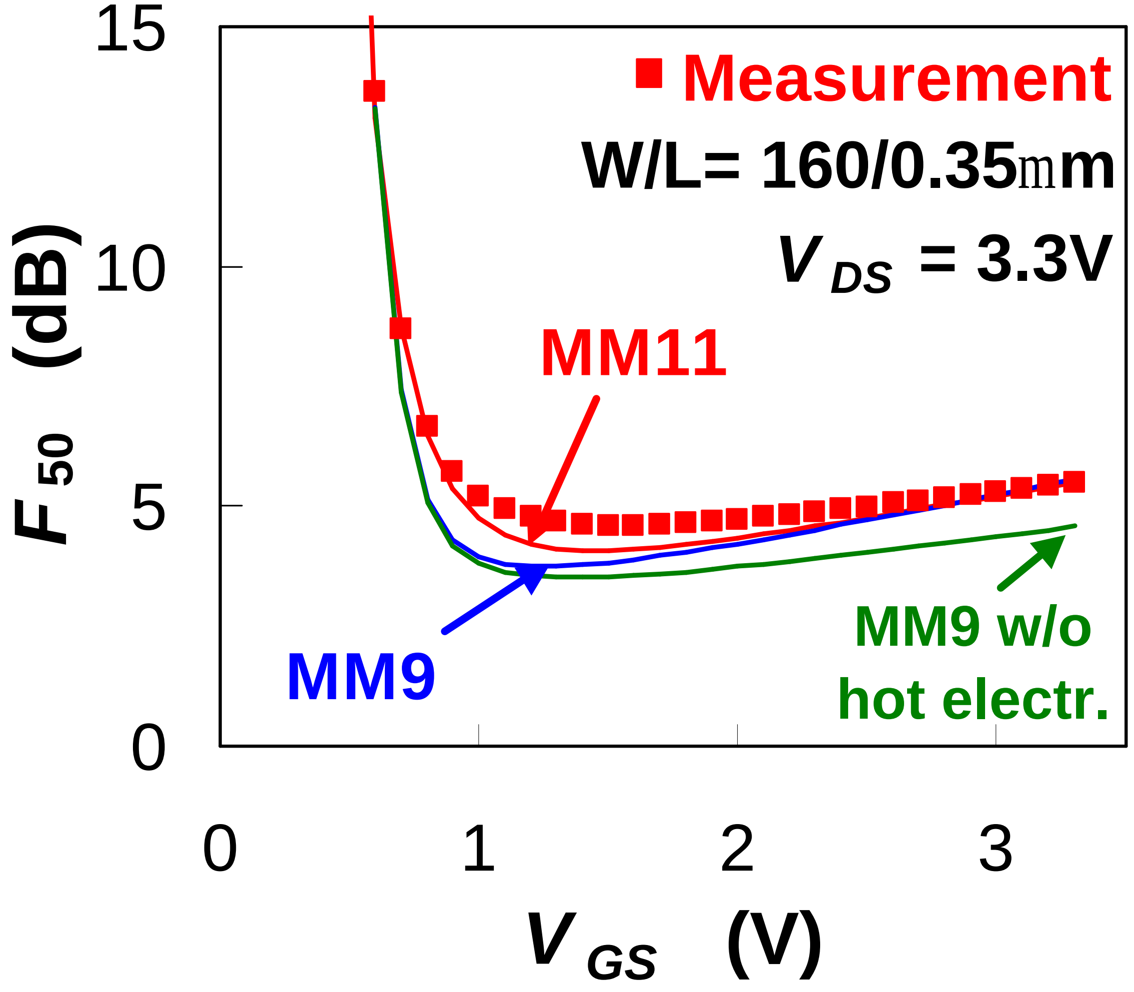
$$S_{ID} = \frac{4 \cdot k_B \cdot T}{I_D \cdot L^2} \cdot \int_0^{VD(SAT)} g^2(V) \cdot dV \quad \text{where:} \quad g(V) = -W \cdot \mu(V) \cdot Q_{inv}(V)$$

(F.M. Klaassen & J. Prins , Philips Res. Repts. 22, pp.504-514, 1967)

MOS Model 9	MOS Model 11
$\mu = \dfrac{\mu_{eff}}{1 + \mu_{eff}/v_{sat} \cdot E_{\parallel}}$	$\mu = \dfrac{\mu_{eff}}{\sqrt{1 + \left(\mu_{eff}/v_{sat} \cdot E_{\parallel} \right)^2}}$

Noise Model : Thermal Noise

50Ω Noise Figure

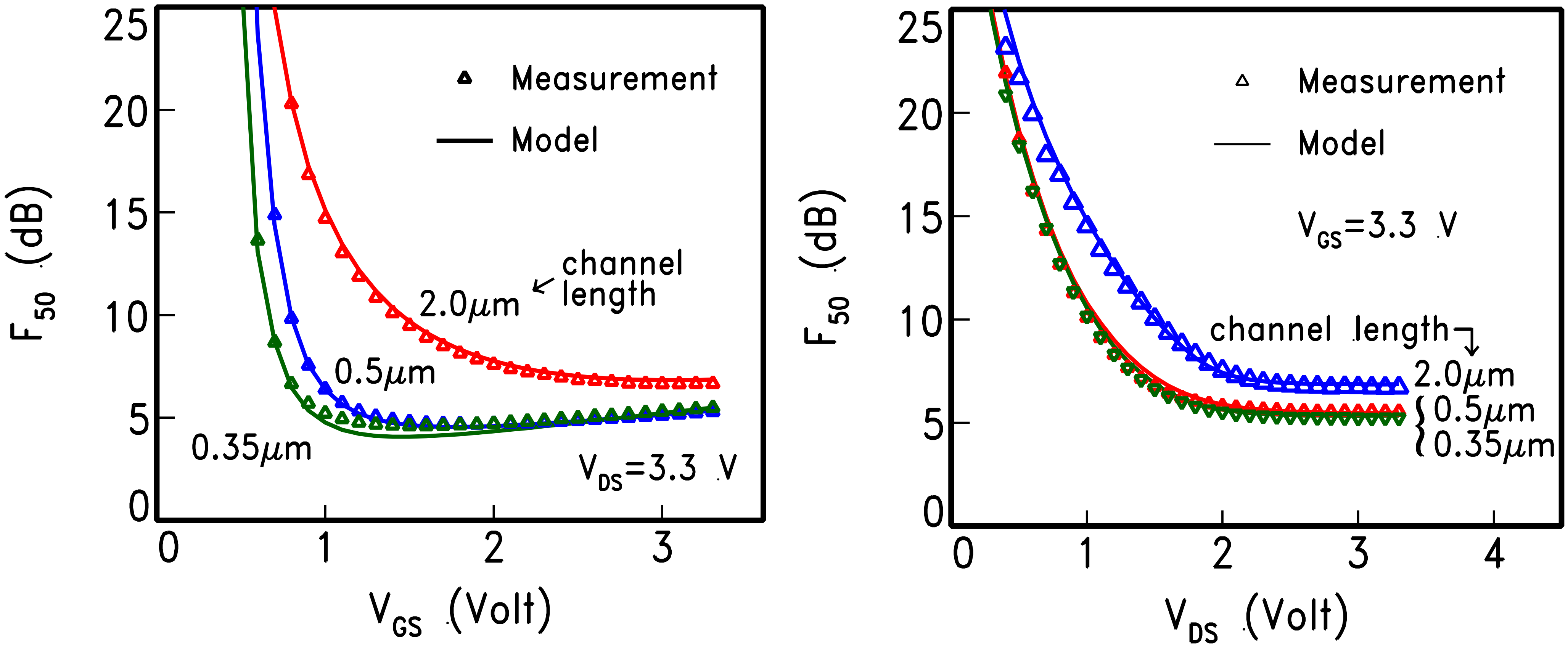


⇒ **no hot electron effect needed to describe noise behaviour**

(A.J. Scholten et al., IEDM Tech. Dig., pp.155-158, 1999)

Noise Model : Thermal Noise (II)

50W Noise Figure (no noise parameters needed)



Þ **Verified on 0.35mm, 0.25mm and 0.18mm CMOS**

(A.J. Scholten et al., IEDM Tech. Dig., pp.155-158, 1999)

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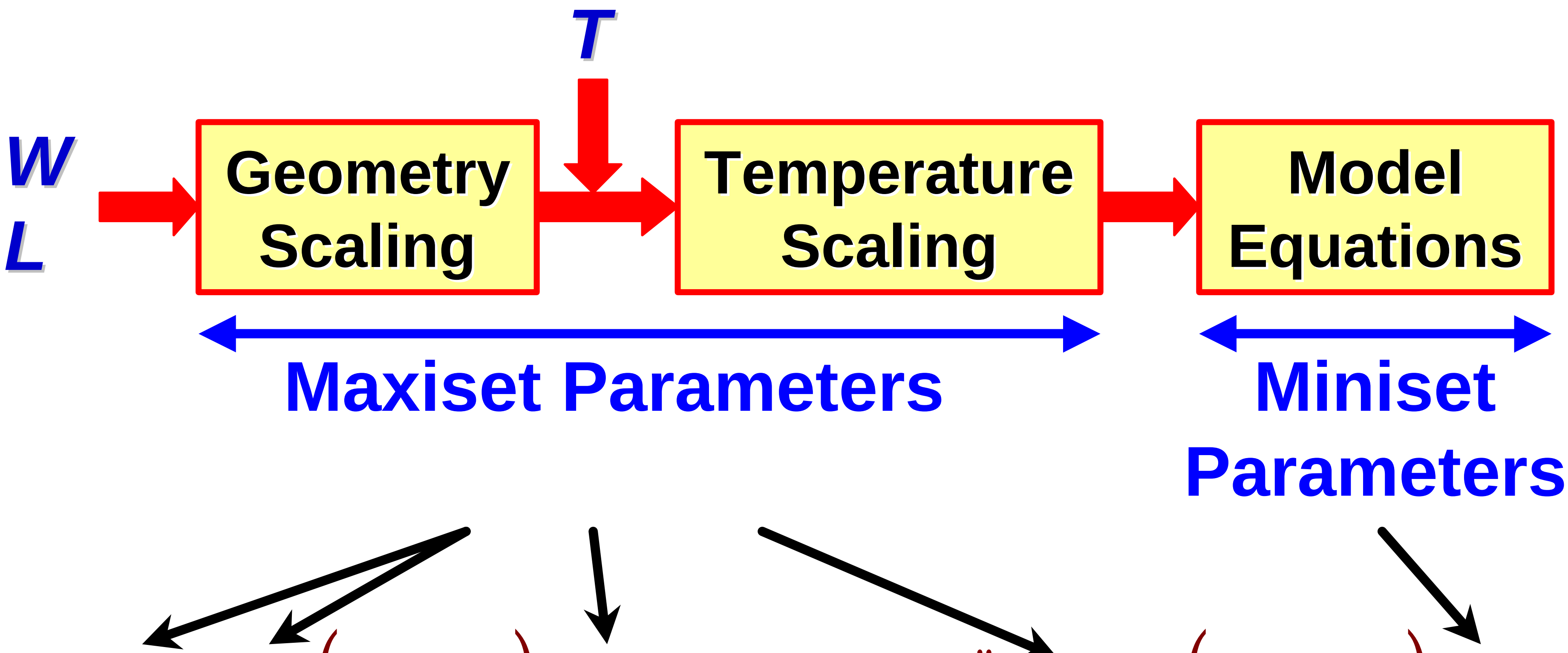
Model Parameters & Extraction



T

W

L

Geometry Scaling

Temperature Scaling

Model Equations

Maxiset Parameters

Miniset Parameters

$$k_R + s_L \cdot \left(\frac{1}{L} - \frac{1}{L_R}\right) + s_{L^2} \cdot \left(\frac{1}{L^2} - \frac{1}{{L_R}^2}\right) + s_W \cdot \left(\frac{1}{W} - \frac{1}{W_R}\right) = k$$

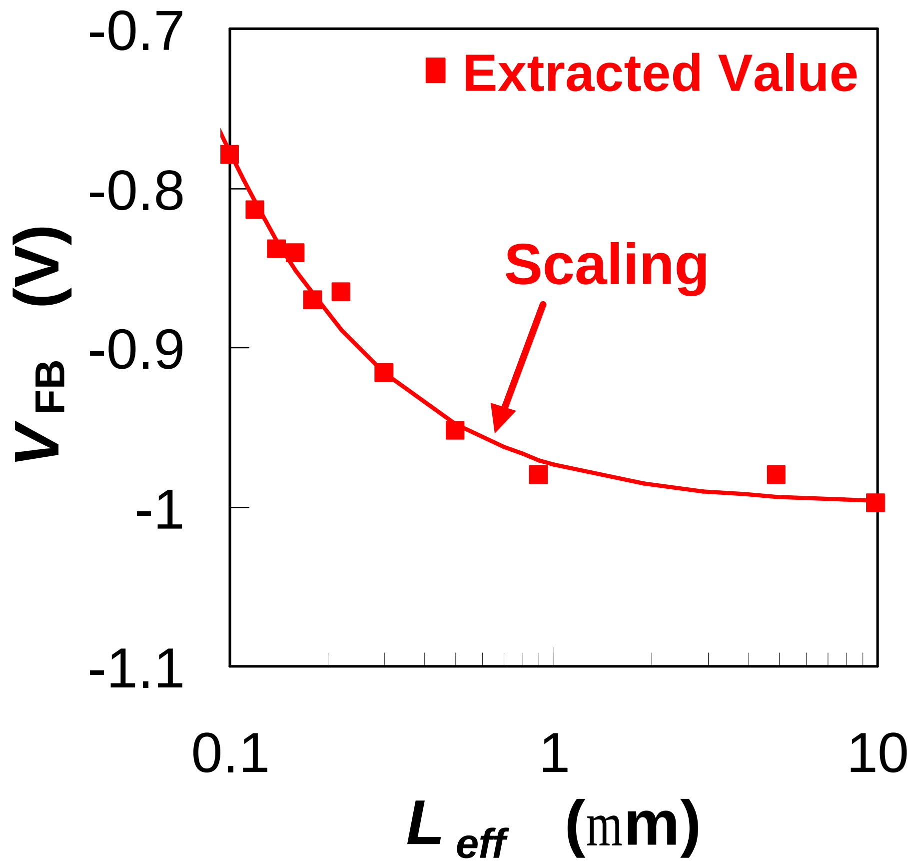
Model Parameters & Extraction (II)

Description of:	Parameters:
Single device	40
T-scaling	11
Geometry scaling	39
	+
Complete technology	90

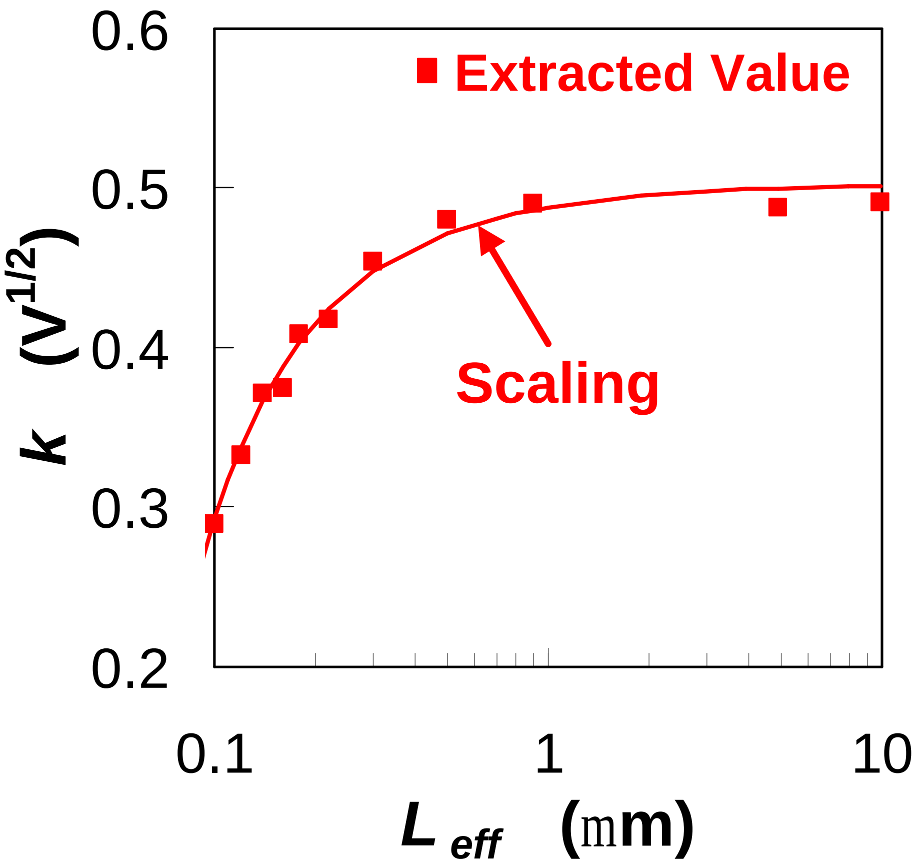
⇒ Binning will also be an option

Model Parameters : Parameter Scaling

Different parameters have different scaling relations



Flat-band voltage



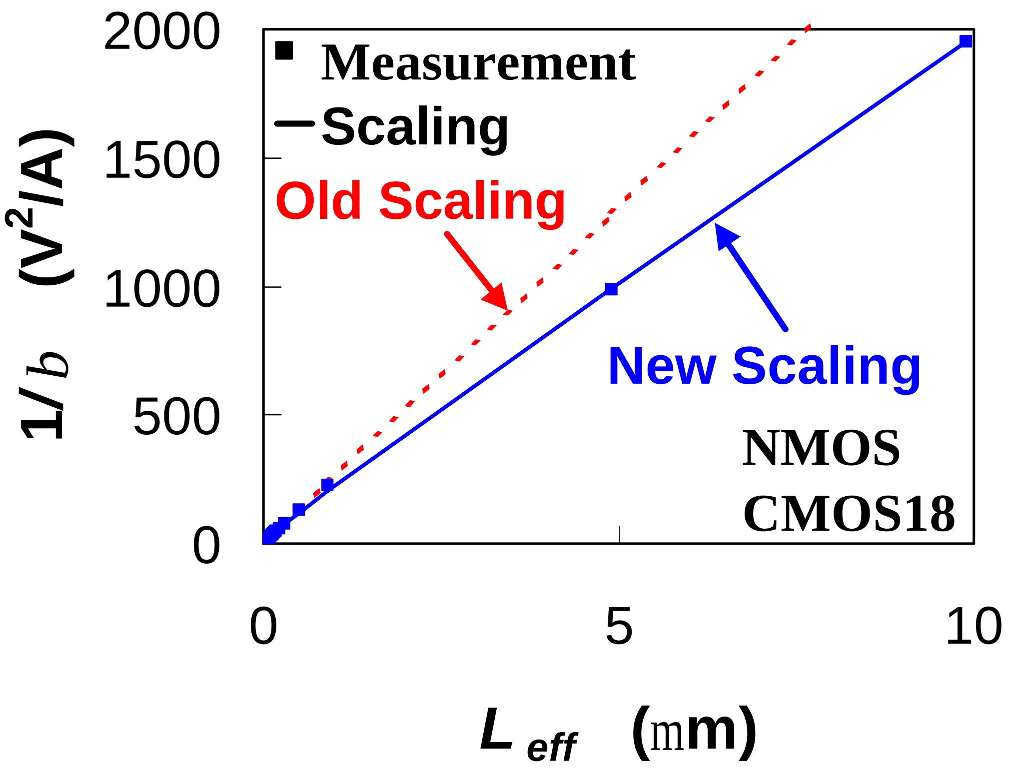
Body factor

Model Parameters : Parameter Scaling (II)

- Old β-scaling:

$$\beta = \beta_{sq} \cdot \frac{W_{eff}}{L_{eff}}$$

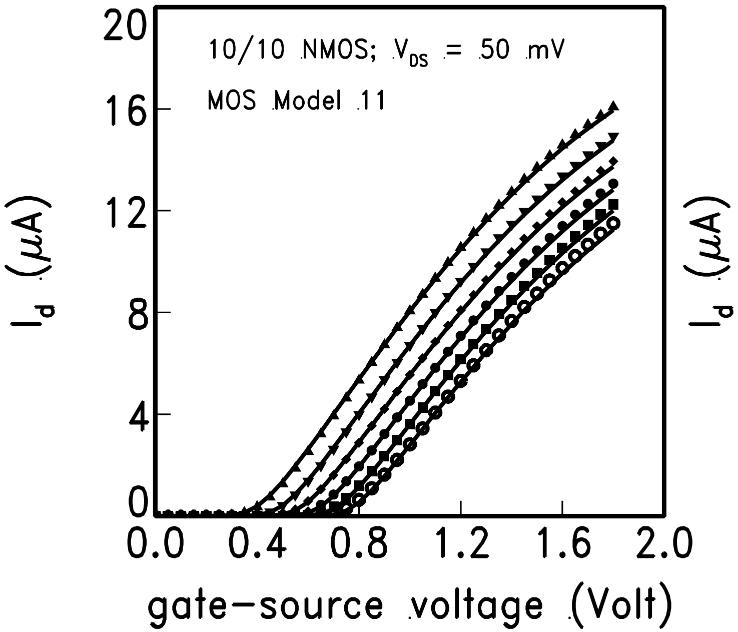
⇒ **influence of pockets**



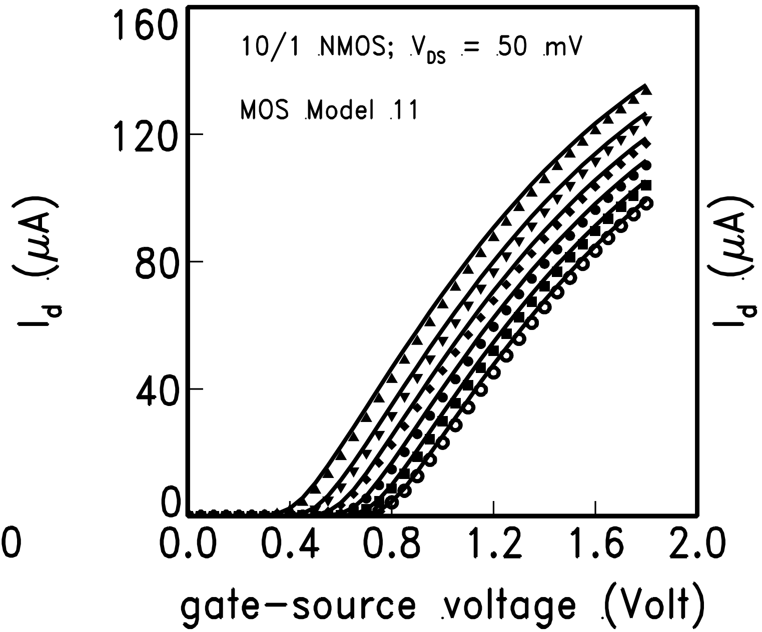
- New β-scaling: $$\beta = \frac{\beta_{sq}}{1 + \frac{\beta_{sq}}{\Delta\beta} \cdot \frac{L_P}{L_{eff}} \cdot \left(1 - \exp\left(-\frac{L_{eff}}{L_P}\right)\right)} \cdot \frac{W_{eff}}{L_{eff}}$$

Model Parameters : Scaling for 0.18mm CMOS

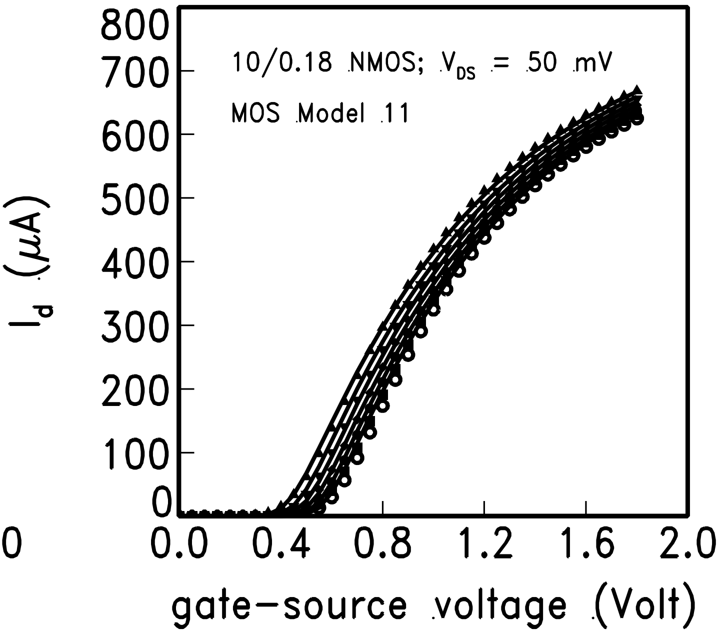
I_D - V_{GS}-characteristics



L=10μm



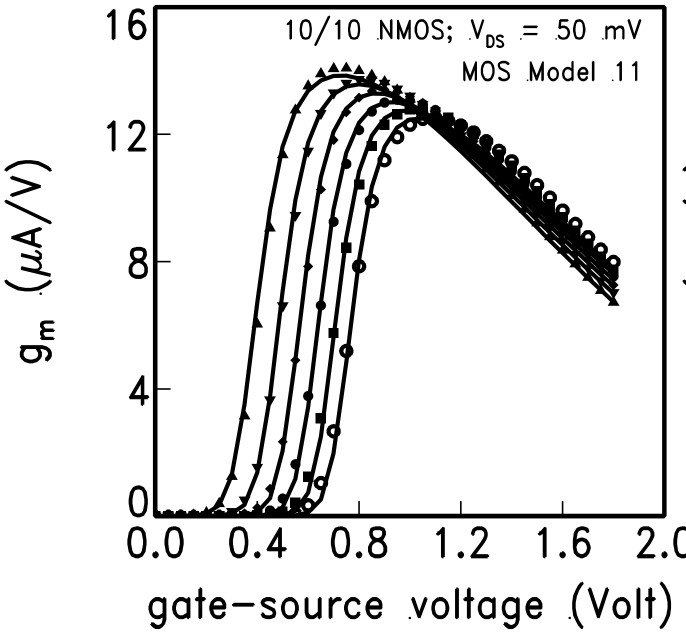
L=1μm



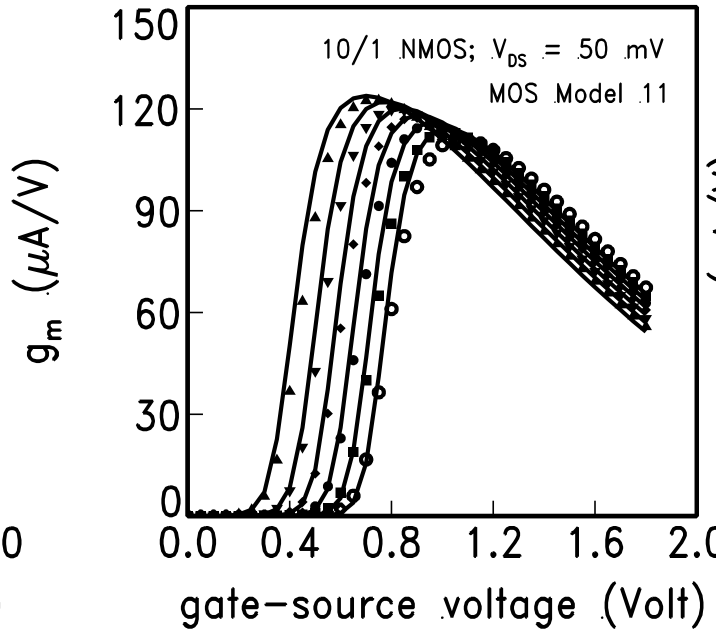
L=0.18μm

Model Parameters : Scaling for 0.18mm CMOS (II)

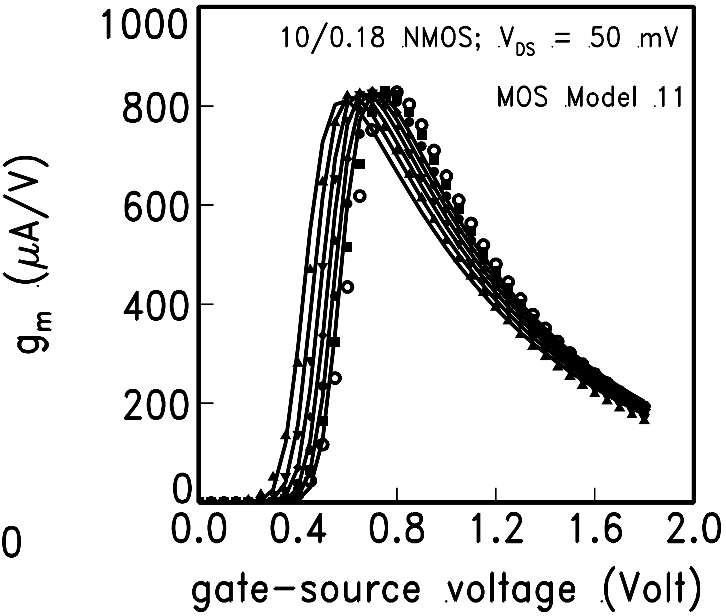
g_m - V_{GS}-characteristics



L=10µm



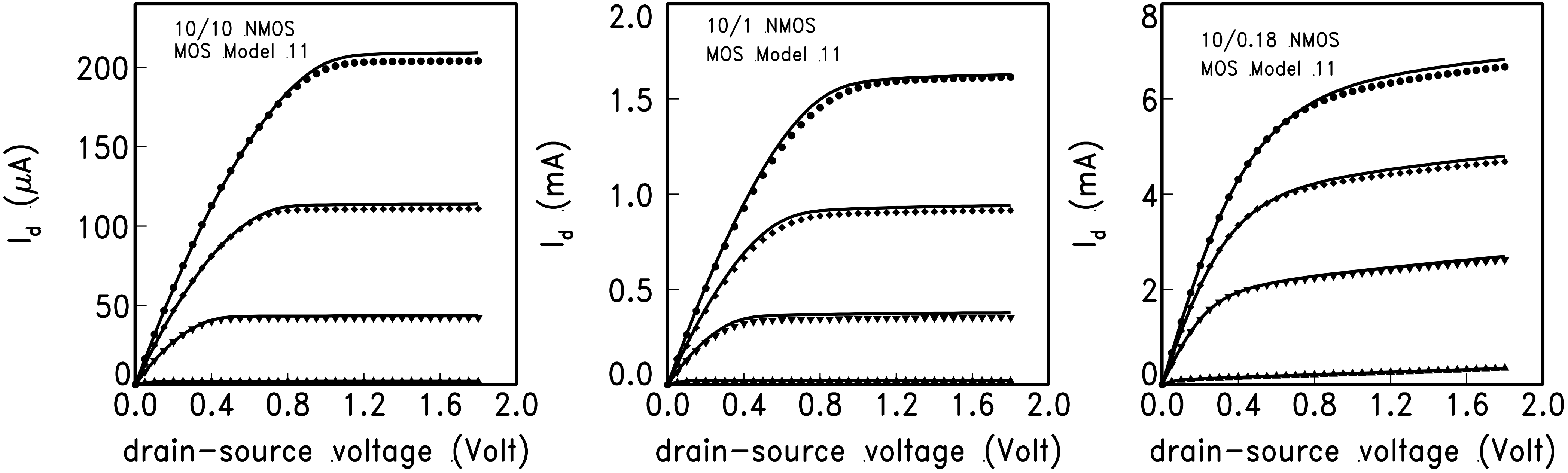
L=1µm



L=0.18µm

Model Parameters : Scaling for 0.18μm CMOS (III)

I_D - V_{DS} -characteristics



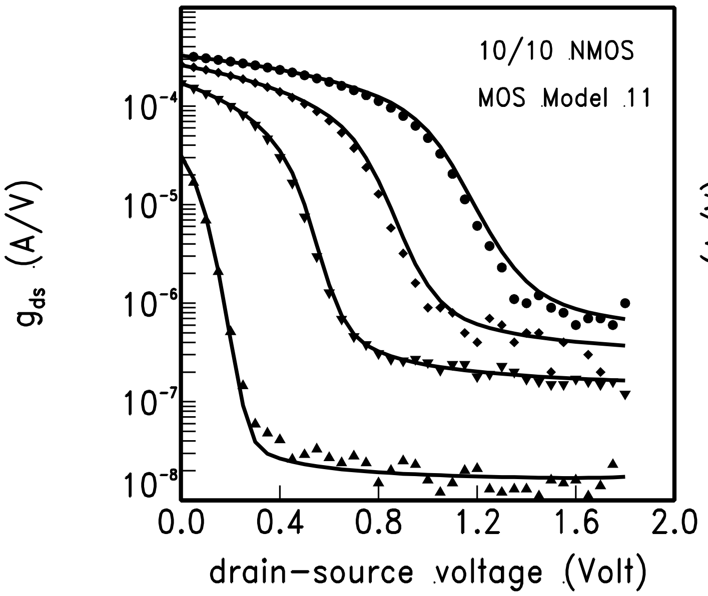
L=10μm

L=1μm

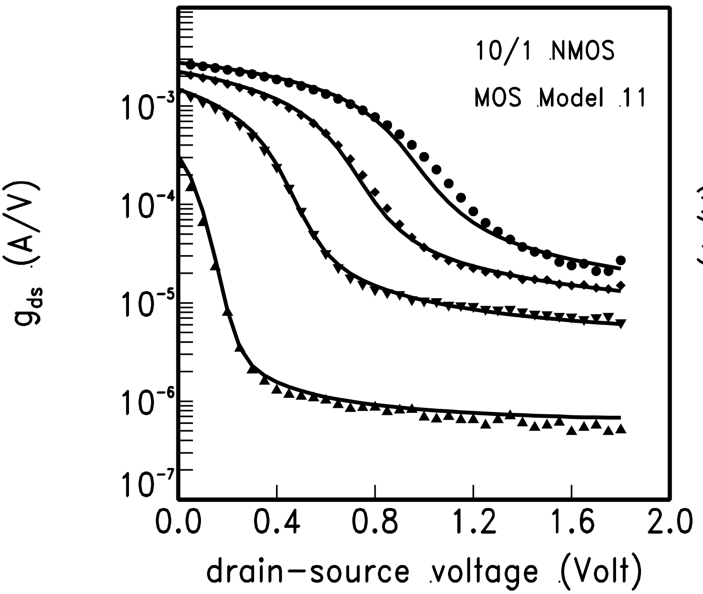
L=0.18μm

Model Parameters : Scaling for 0.18μm CMOS (IV)

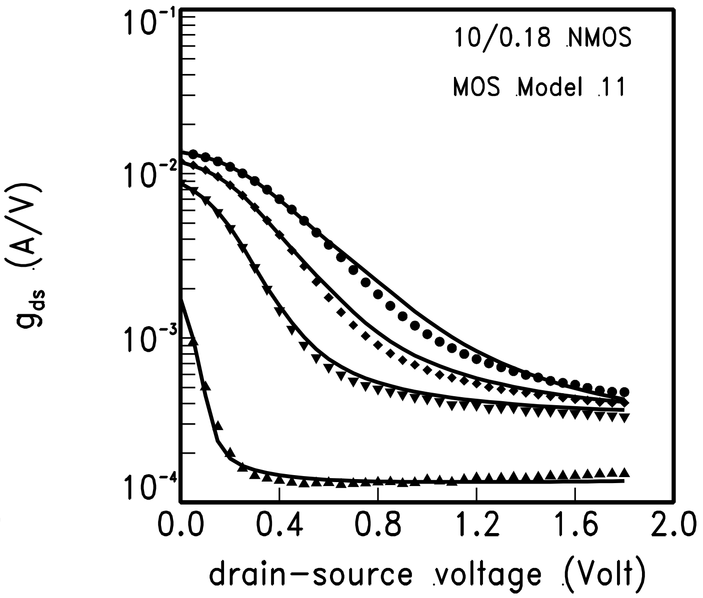
g_{ds} - V_{DS} -characteristics



L=10μm



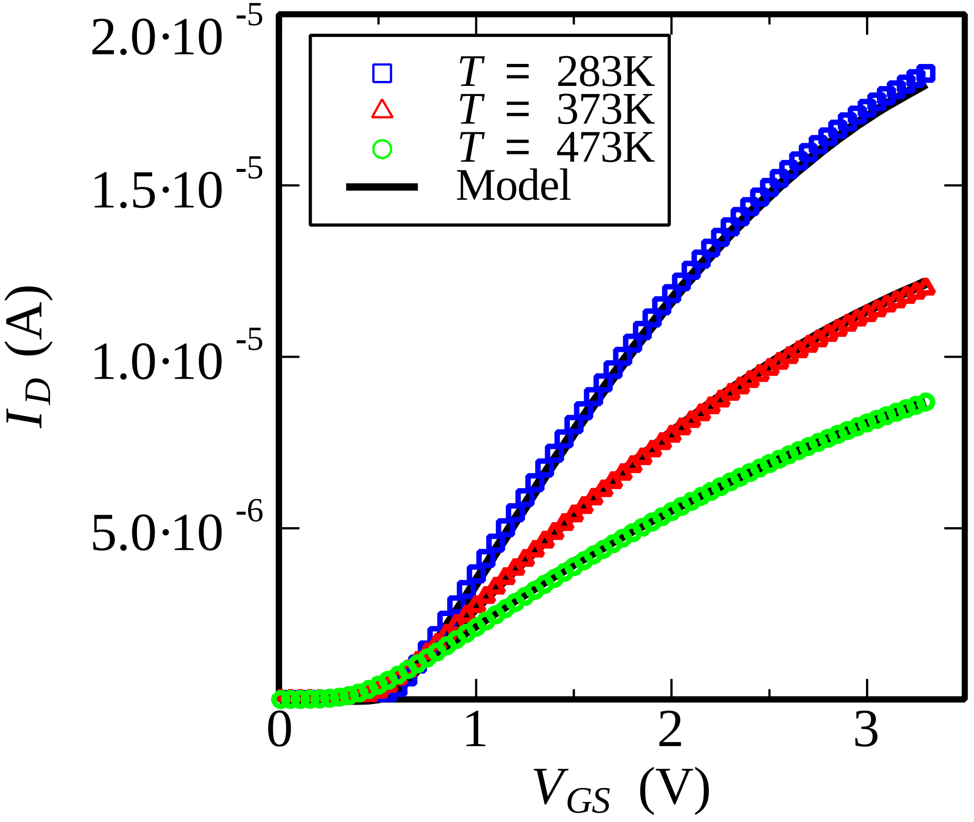
L=1μm



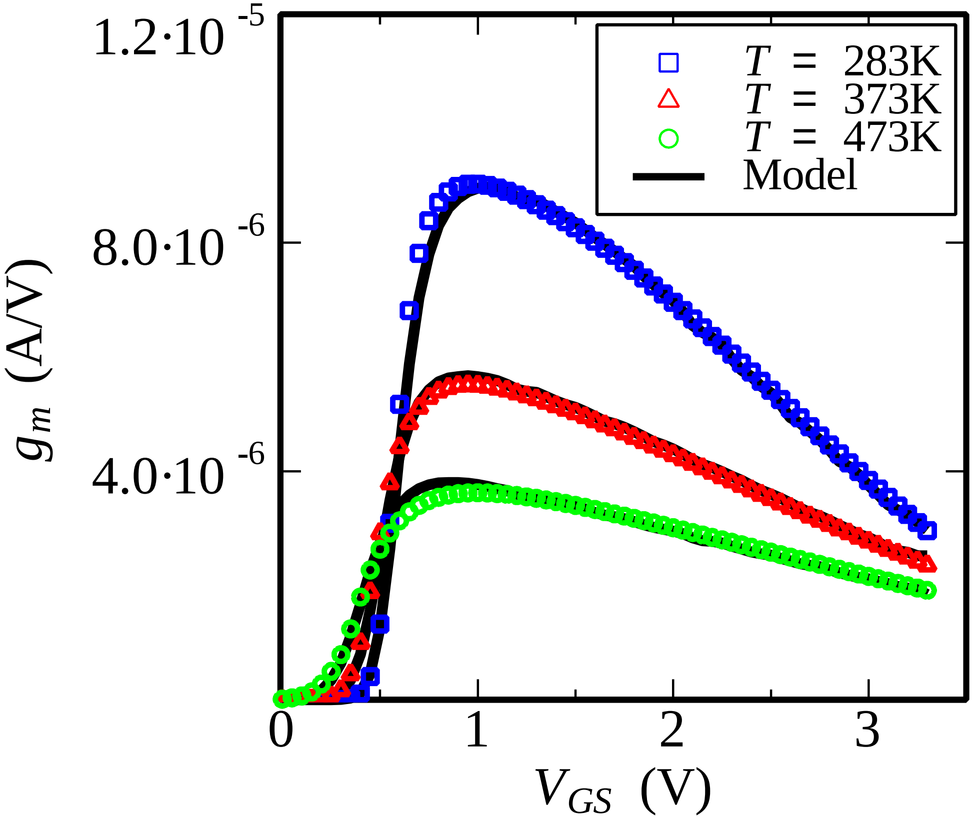
L=0.18μm

Model Parameters : Temperature Scaling

NMOS, W/L=10/10mm, V_{SB}=0 V



I_D - V_{GS}



g_m - V_{GS}

Model Parameters : Parameter Extraction

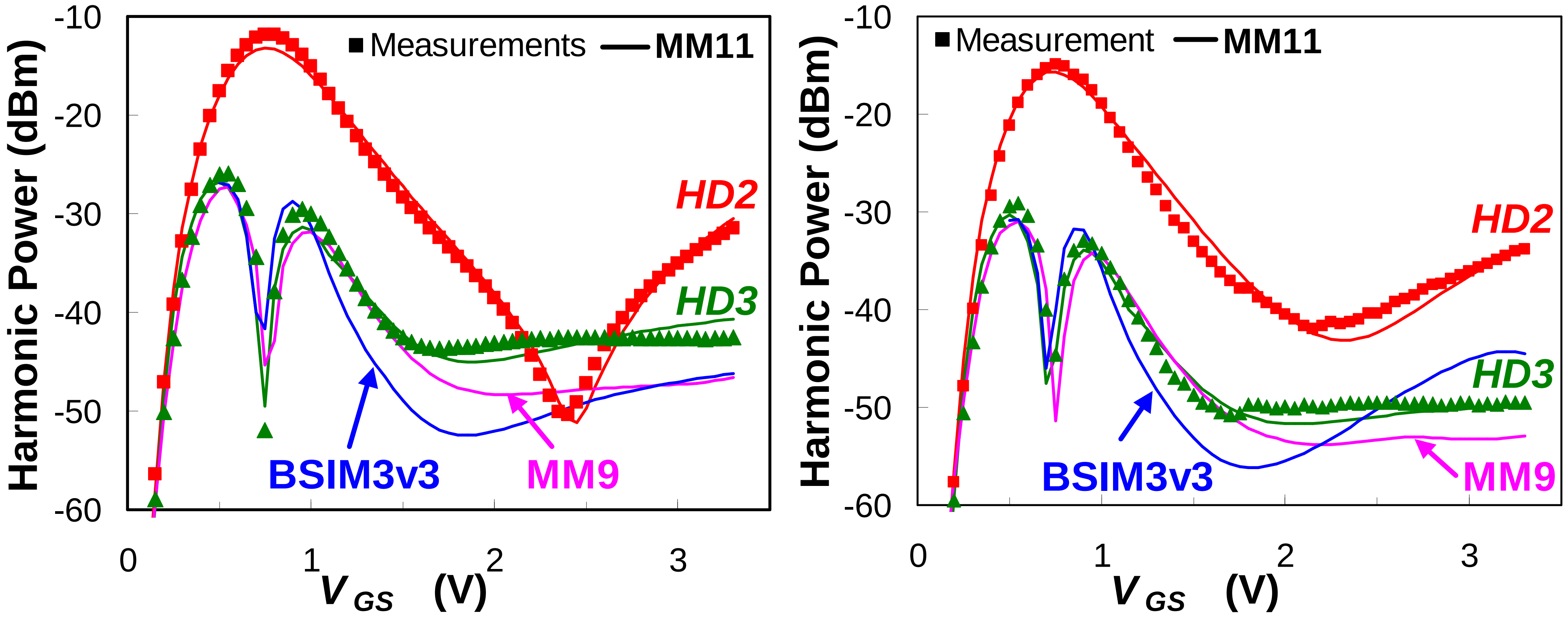
Characteristics:	**Parameters:**	**Fitted on:**
Subthreshold	Subthreshold	I_D
Gate Capacitance	Poly depletion	C_{gg}
Linear Region	Mobility, R_{series}	I_D & g_m
Output	Velocity saturation	I_D
	Conductance	g_d
Substrate Current	Weak-avalanche	I_B
Gate Current	Gate leakage	I_G

Outline

- Introduction
- DC-Model
- AC-Model
- Noise Model
- Model Parameters & Extraction
- Examples & Applications
- Conclusions

Examples & Applications : RF-Distortion

NMOS, W/L=160/0.35µm, V_{DS}=3.3 V, P_{IN}=-5dBm

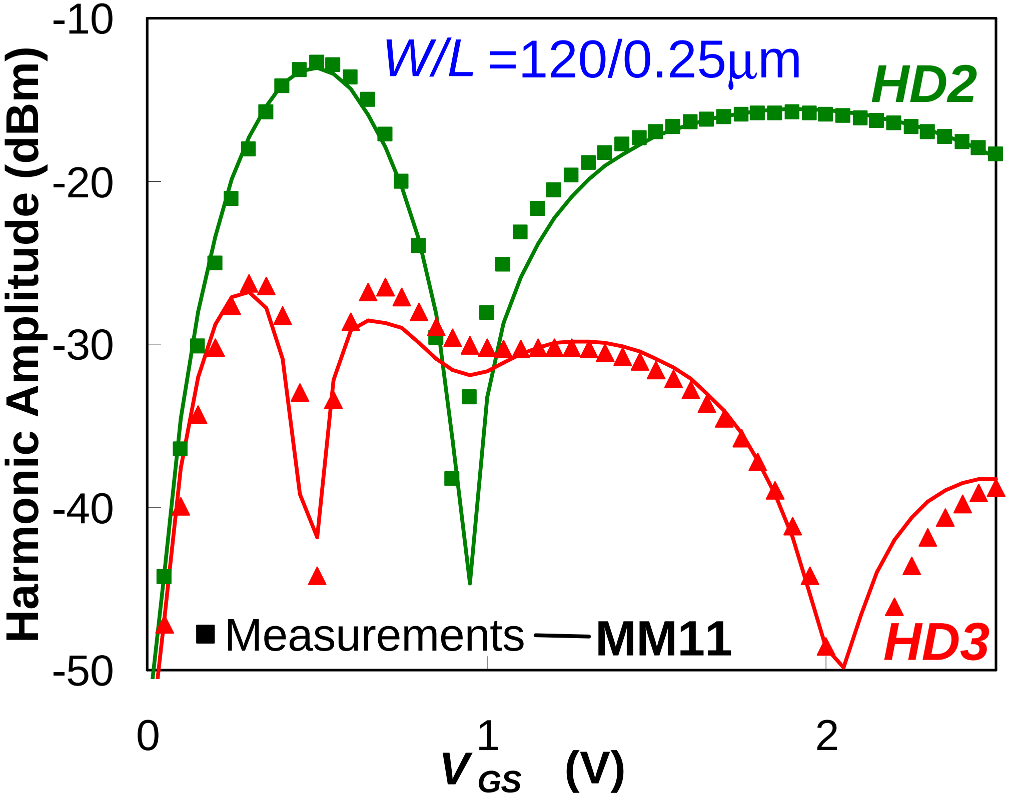


f=16 MHz

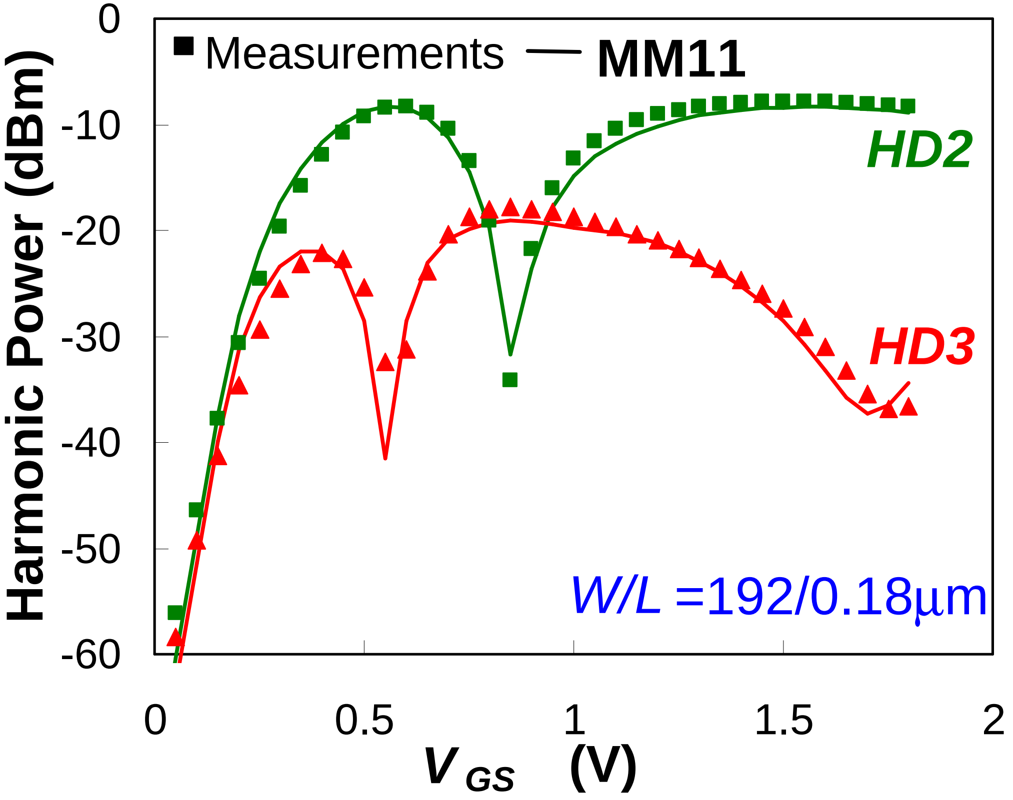
f=1 GHz

Examples & Applications : RF-Distortion (II)

NMOS, f=1GHz, V_{DS}=1.0 V, P_{IN}=-5dBm



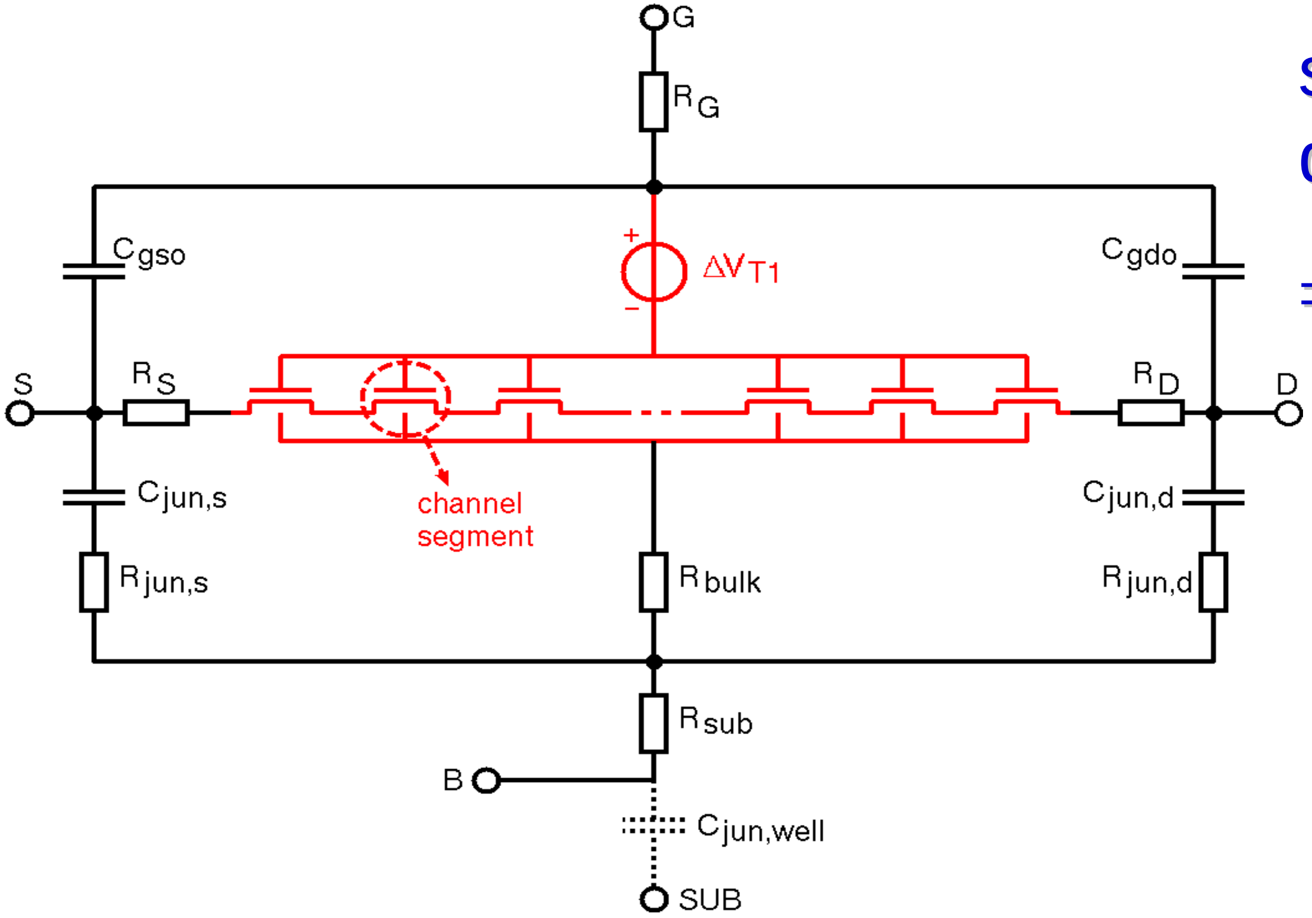
0.25µm CMOS



0.18µm CMOS

Examples & Applications : RF-CMOS Model

NQS-effects described by segmentation model:



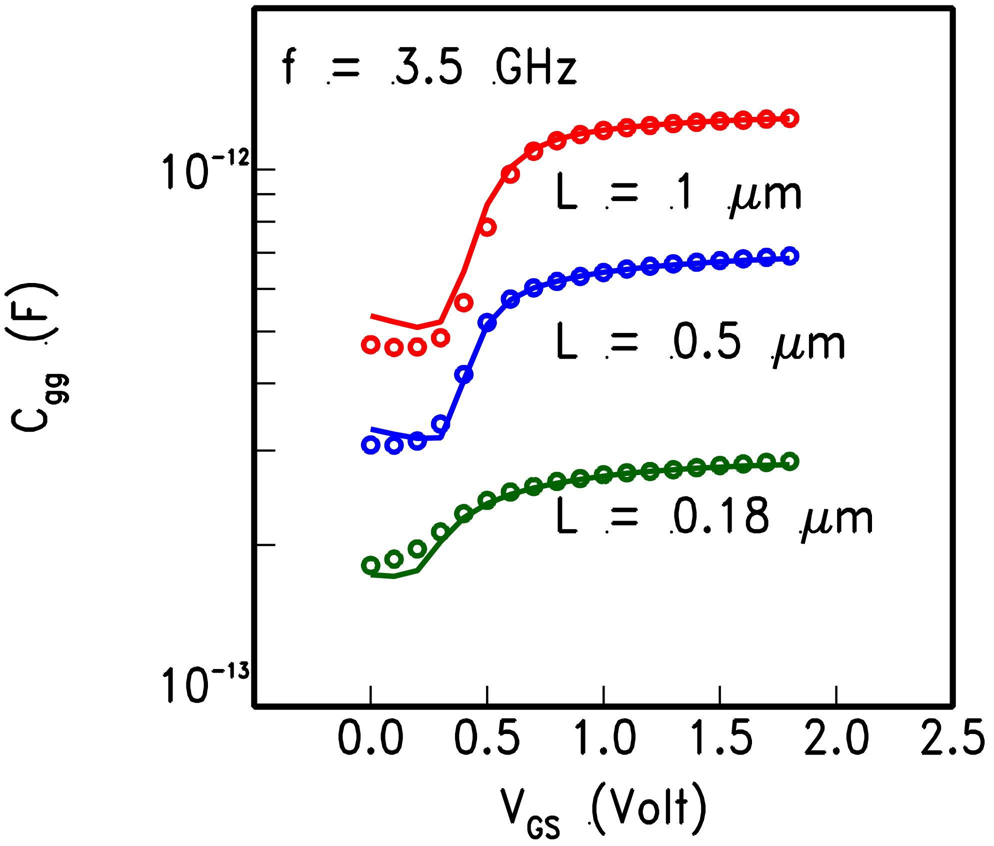
segments have only drain current noise

⇒ induced gate noise comes out naturally

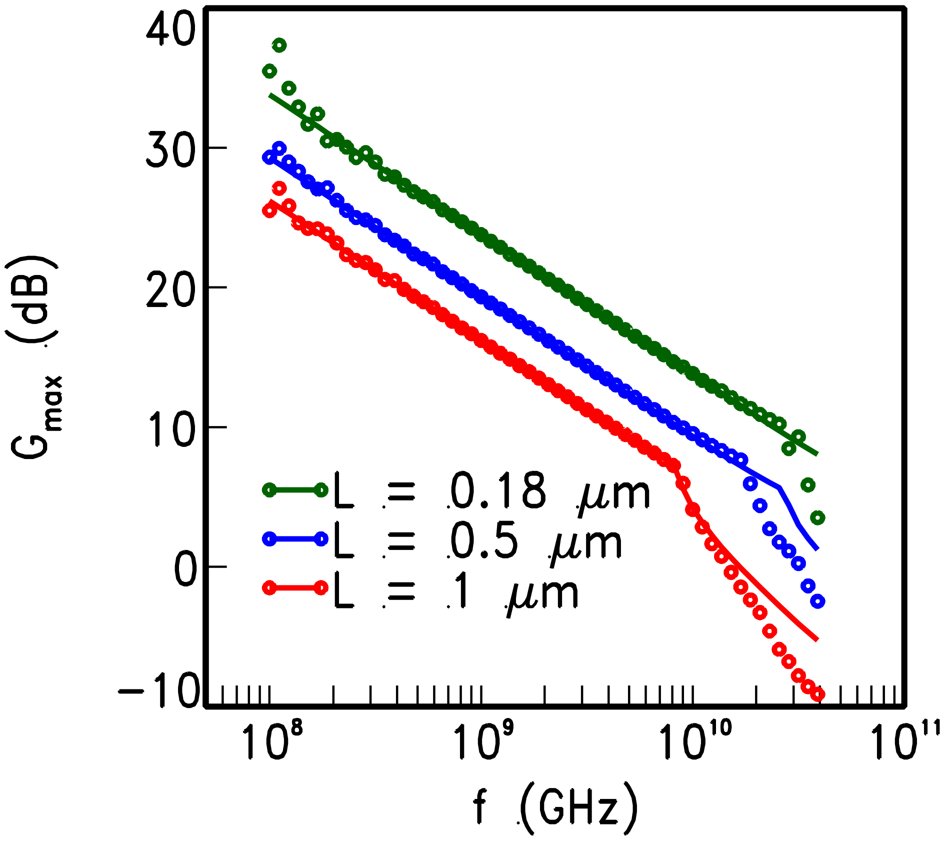
(A.J. Scholten et al., IEDM Tech. Dig., pp.163-166, 1999)

Examples & Applications : RF-CMOS Model (II)

0.18µm CMOS, NMOS, V_{DS}=1.8V NQS-Model, 5 segments



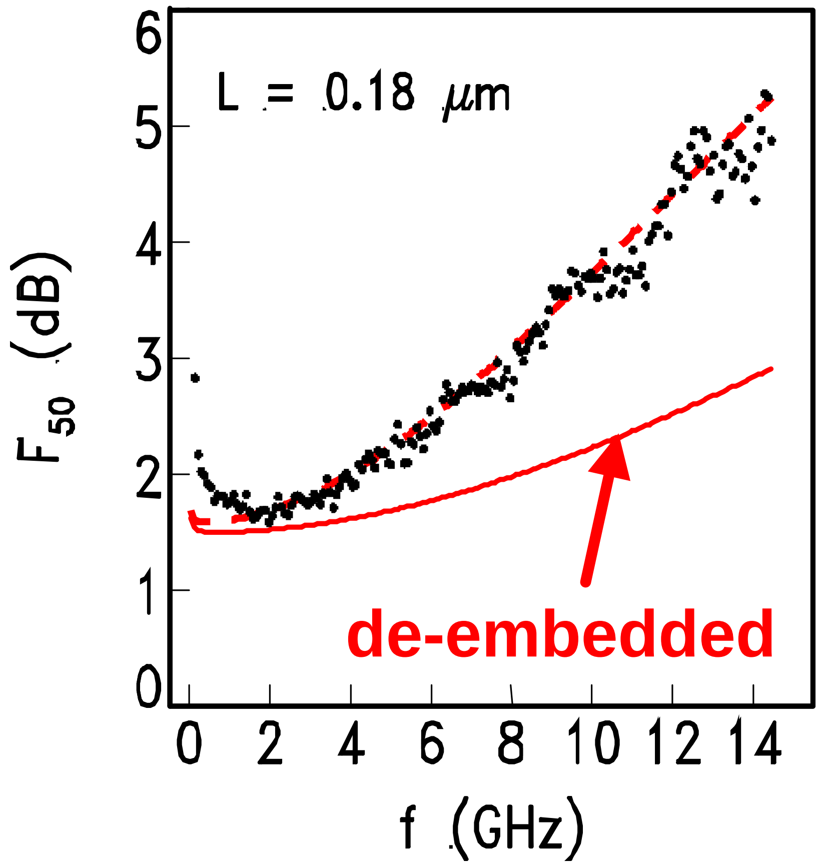
Input capacitance



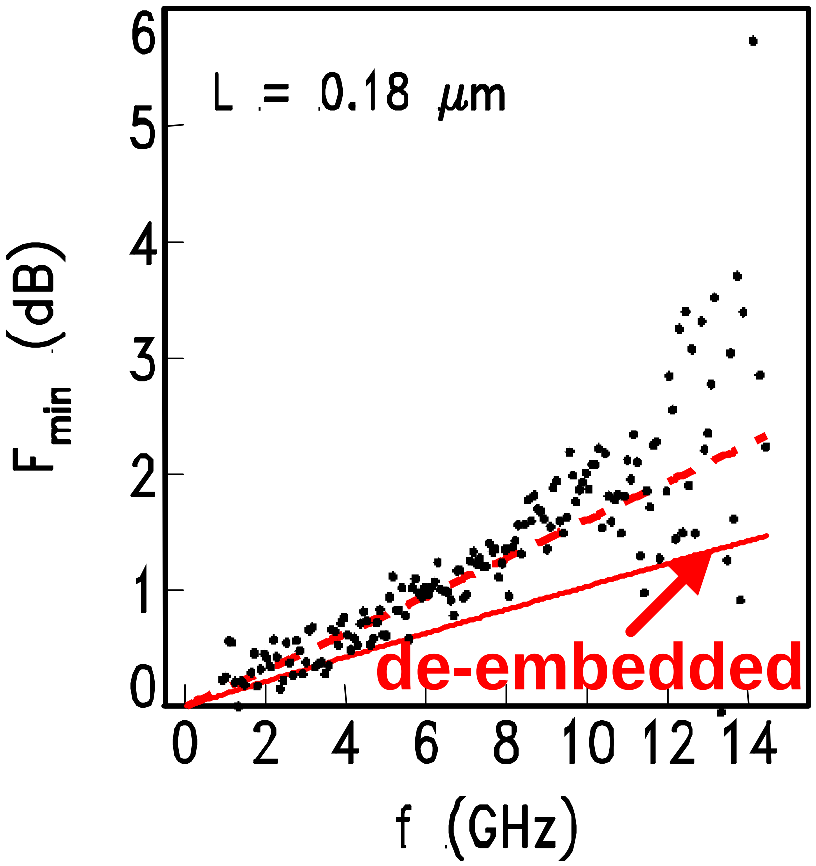
Maximum gain

Examples & Applications : RF-CMOS Model (III)

0.18μm CMOS, NMOS, V_{DS}=1.8V NQS-Model, 5 segments



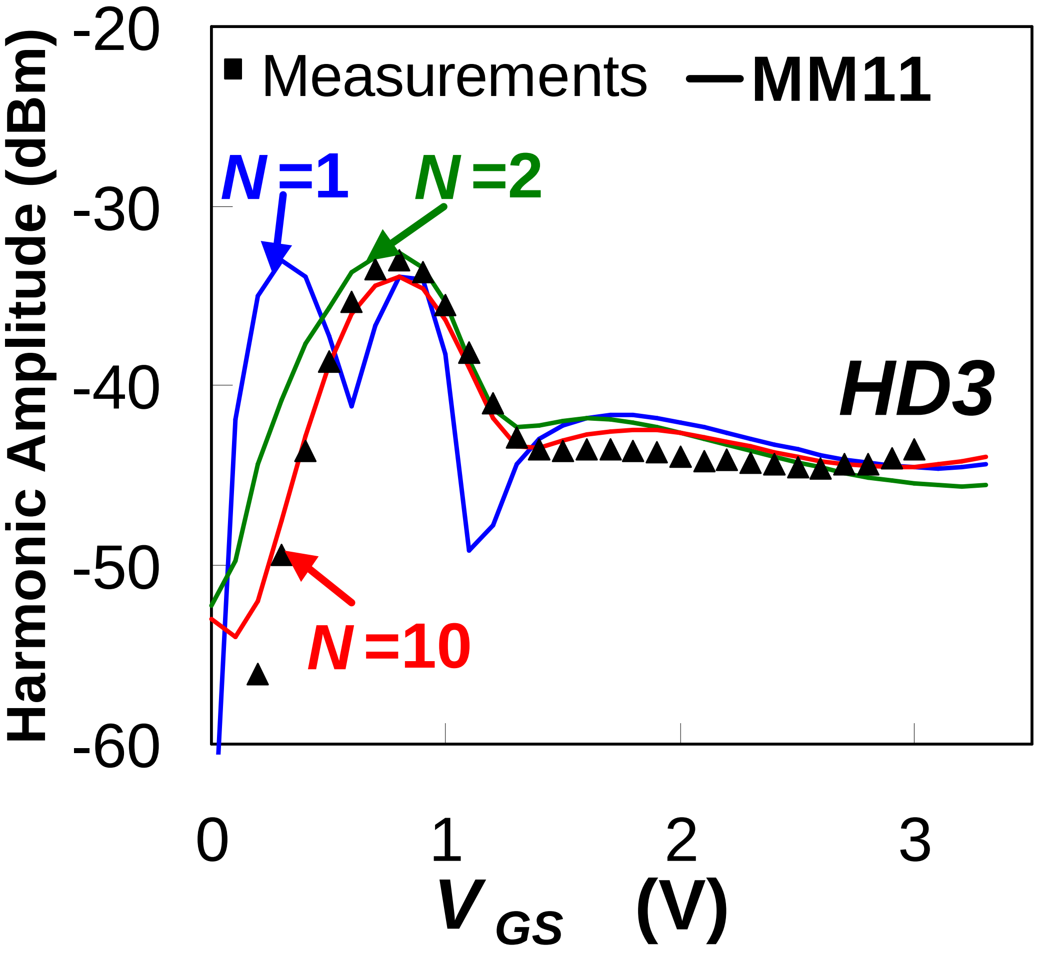
50Ω Noise Figure



Minimum Noise Figure

Examples & Applications : RF-CMOS Model (IV)

NMOS, W/L=160/2µm, *f*=1GHz, V_{DS}=3.3 V, P_{IN}=0dBm



NQS-Model with *N* segments

3rd-order distortion

Conclusions

- MOS Model 11 is a symmetrical, ψ_s-based model including accurate description of transconductance, conductance and gate leakage.
- Charge model: accurate description of accumulation, gate depletion, QM-effects and overlap capacitances
- Noise model: accurate description of 1/*f* noise and thermal noise
- Parameters determined from *I*-*V* and *C*-*V*-measurement
- Model implementation has been finished, first tests on circuits have been performed
- On the Internet (March 2001): http://www.semiconductors.philips.com/Philips_Models