

RF modelling of MOSFETs

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- RF measurements & simulations
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 - common gate configuration
 - cascade configuration
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introduction

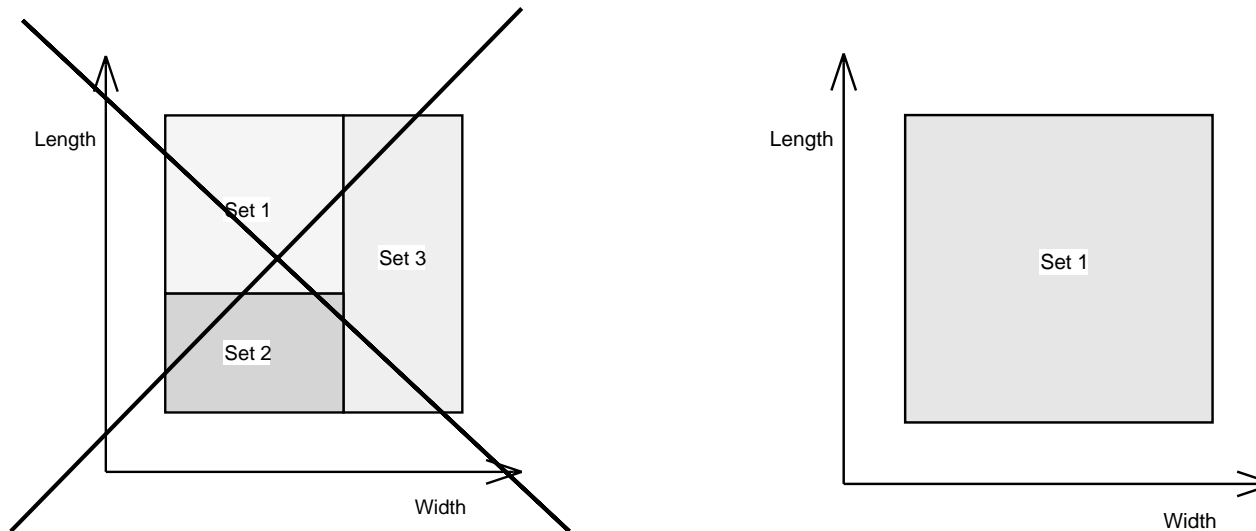
- RF circuit design in mainstream CMOS IC-process
 - foundries supply compact model parameters for IC-processes
 - most compact MOS models are suited for digital applications only
 - few public domain analog compact MOS models
 - BSIM3v3 from UC Berkeley (September 1995)
 - MOS MODEL 9 from Philips (December 1993 in public domain)
 - little literature on high-frequency verification of compact MOS models
- ⇒ ● MOS MODEL 9 verification on basic RF circuits

MOS MODEL 9

- physical basis \Rightarrow minimum number of parameters/phenomenon
 - body-effect for implanted substrate
 - mobility reduction due to transversal field: gate & substrate
 - velocity saturation
 - subthreshold region
 - drain-induced barrier-lowering
 - static feedback
 - channel length modulation
 - avalanche multiplication
 - substrate current
- geometry scaling rules
- temperature scaling rules
- charge model

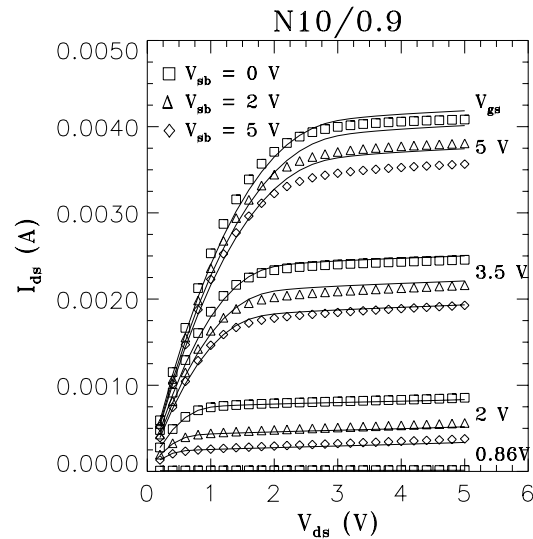
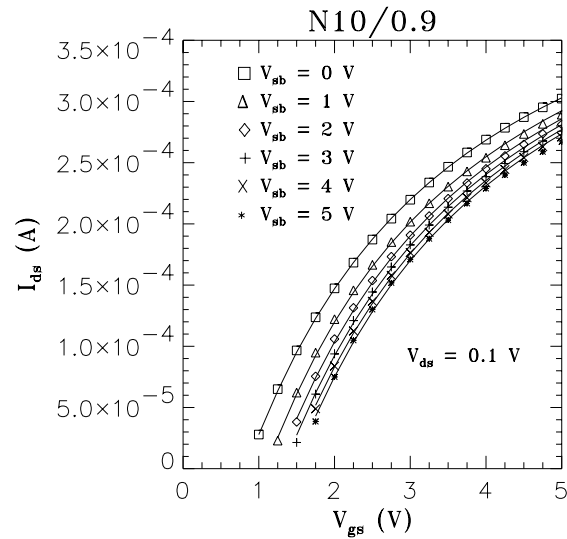
MOS MODEL 9

- 18 parameters for a specific geometry
- 2 parameters for the charge model
- 46 parameters for geometry scaling

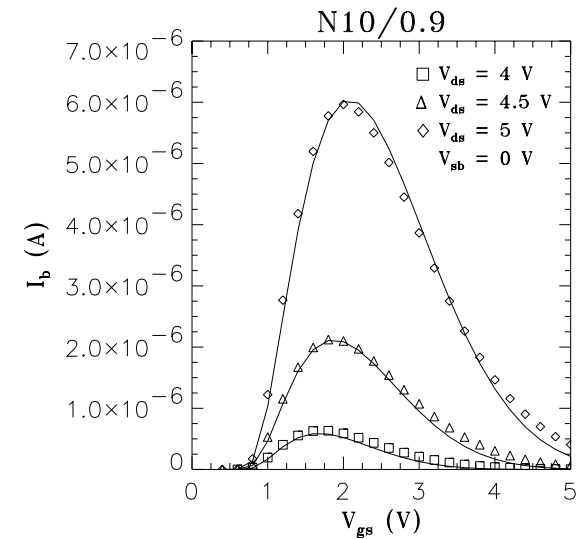
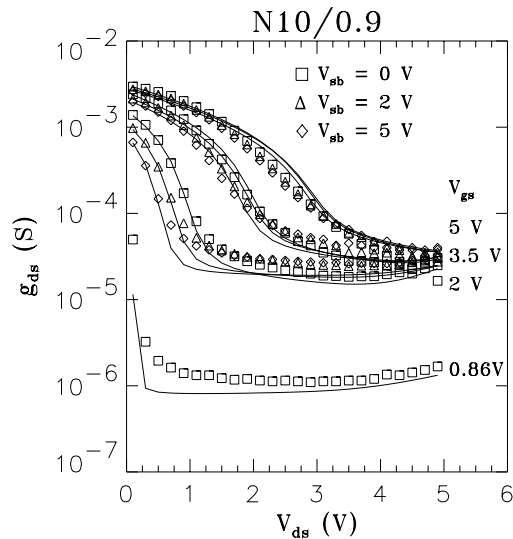
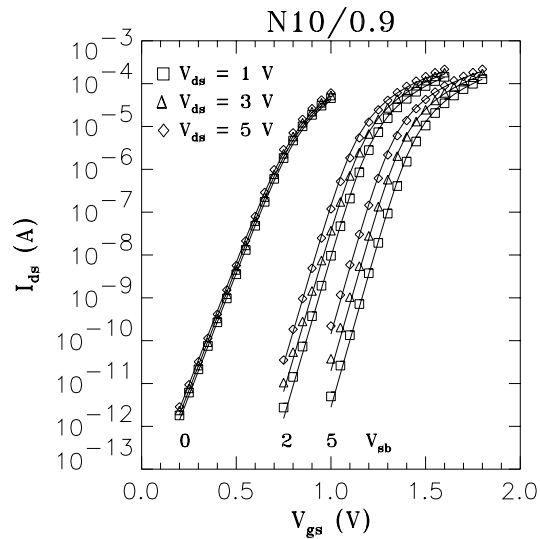


- 10 parameters for temperature scaling

MOS MODEL 9

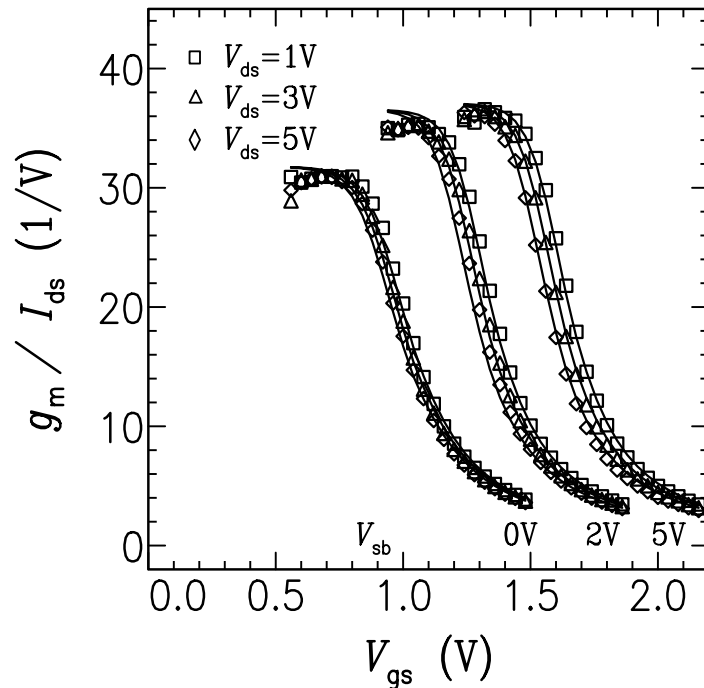


- linear region
- subthreshold region
- saturation region
- output conductance
- substrate current

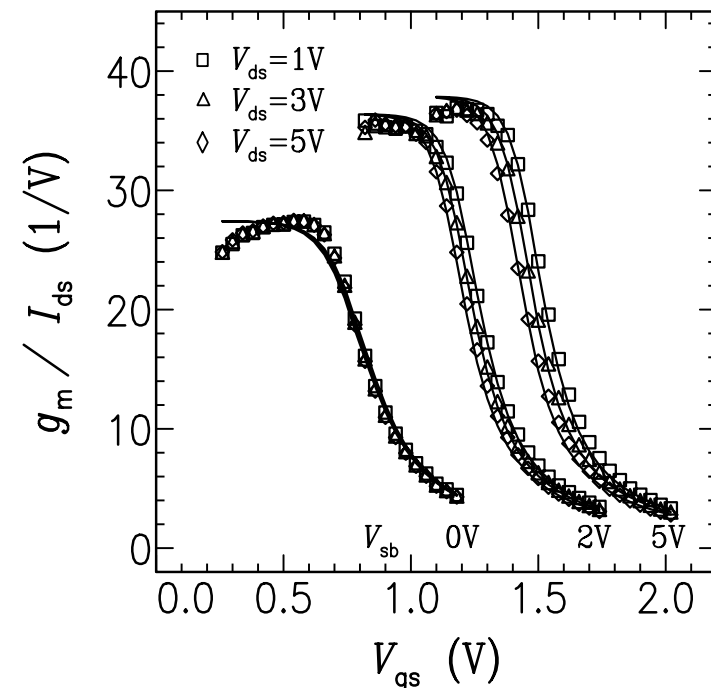


MOS MODEL 9

- complies with most benchmark tests for analog models



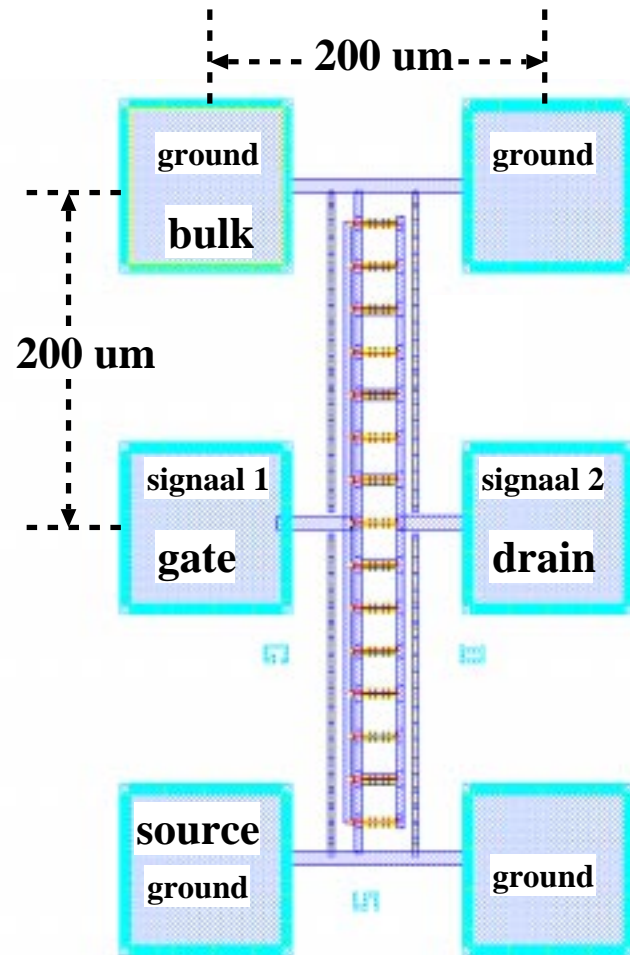
non-implanted substrate



implanted substrate

- MOS MODEL 9 is a quasi-static model

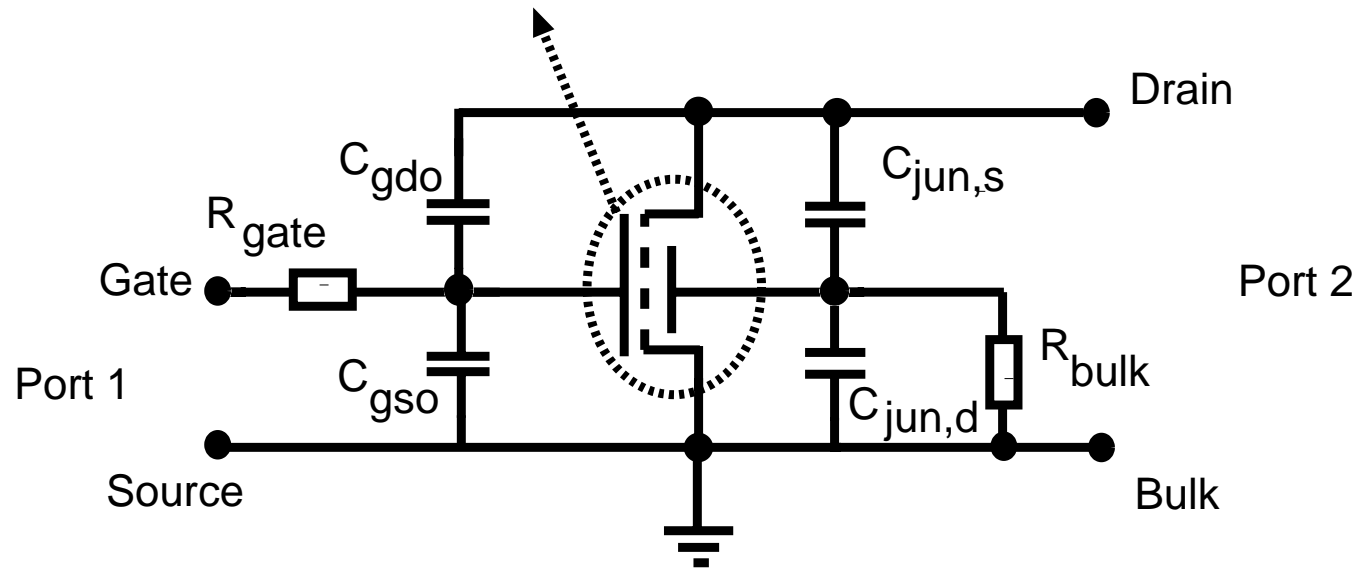
RF measurements



- two-port S-parameter measurements
- HP8510B network analyzer
- on wafer
- air coplanar high-frequency probes
in ground-signal-ground configuration
- special MOS structures
in common source-bulk configuration
- S- to Y-parameter conversion
- de-embedding procedure for parasitics

RF simulations

intrinsic device: MOS model 9 : DC-parameters + oxide capacitance

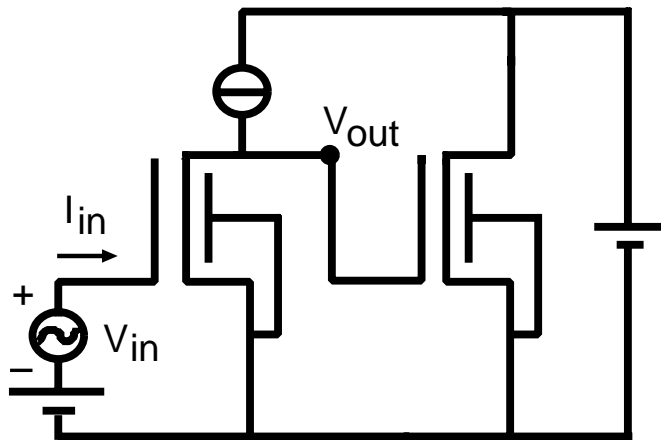
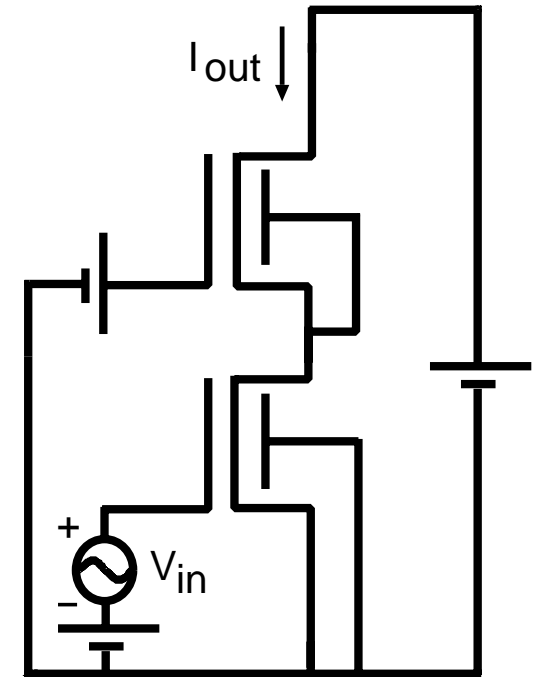
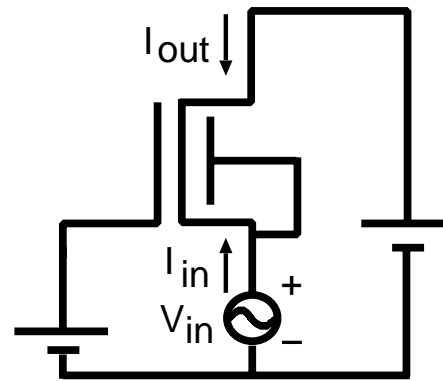
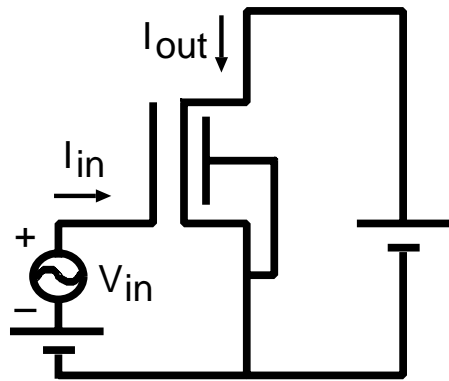


extrinsic elements: resistances: R_{gate} ; R_{bulk}

capacitances: overlap : C_{gd0} ; C_{gs0}

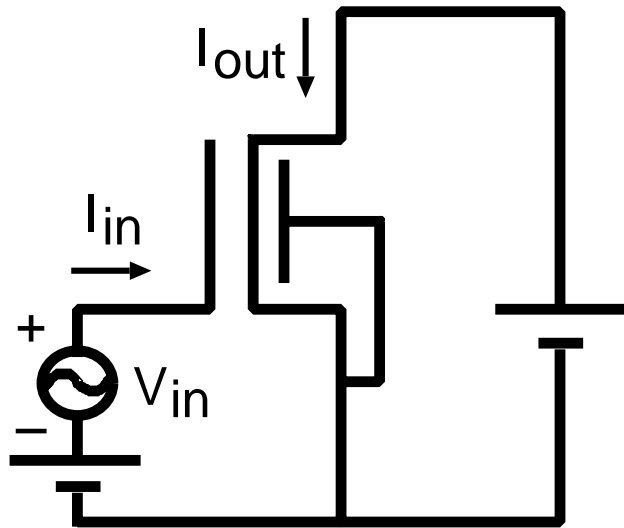
junction : $C_{jun,d}$; $C_{jun,s}$

basic RF circuits



- common source-bulk
- common gate
- cascode
- cascode

common source-bulk configuration



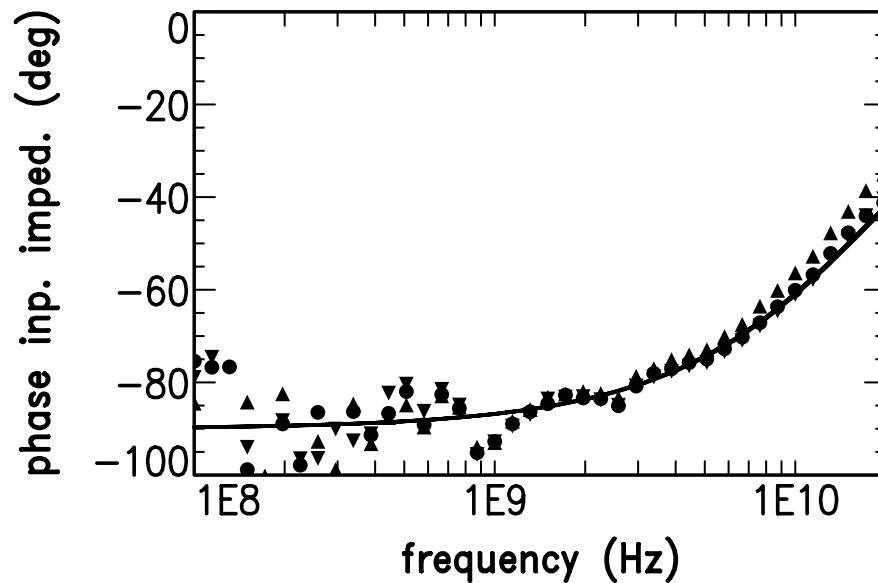
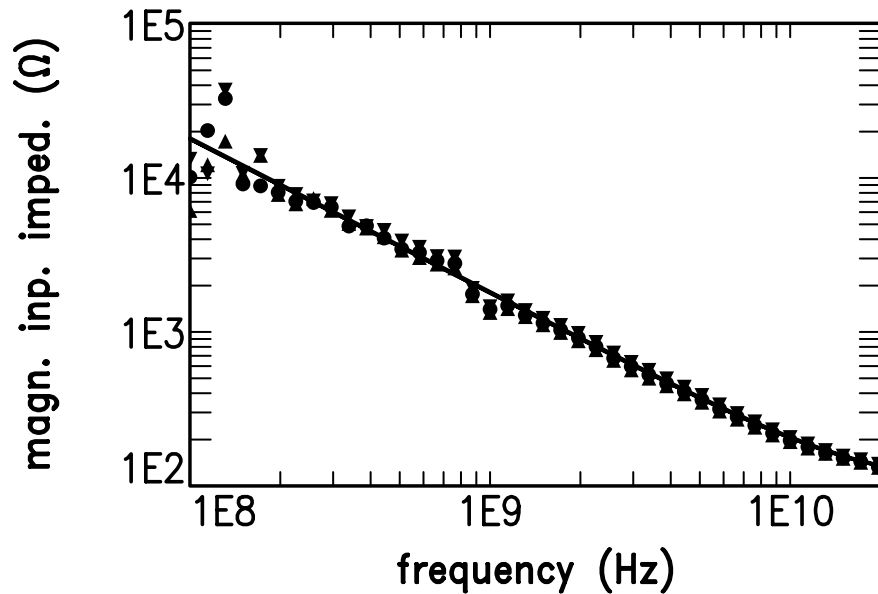
- voltage driven
- drain ac short-circuited

- input impedance $Z_{in} = \frac{v_{in}}{i_{in}}$

- current gain $\frac{i_{out}}{i_{in}}$

- transconductance $\frac{i_{out}}{v_{in}}$

common SB configuration: input impedance

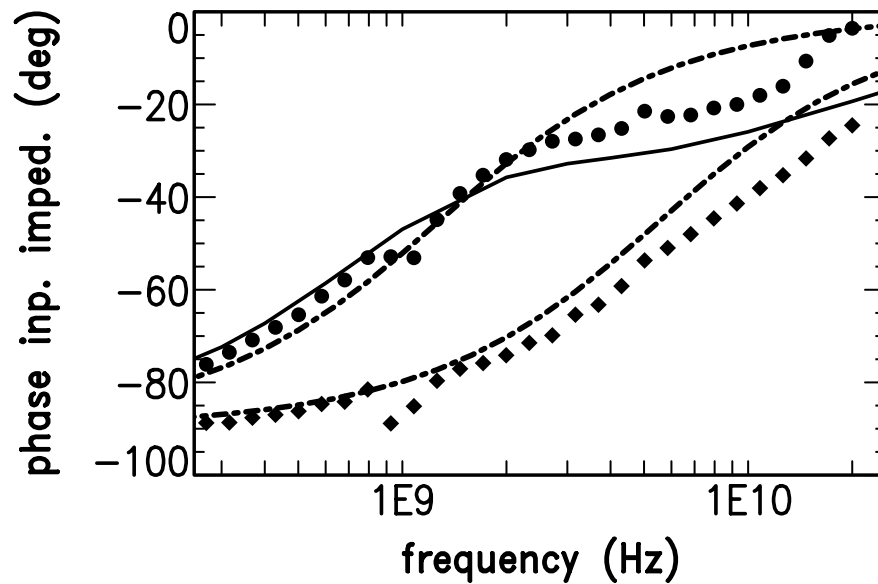
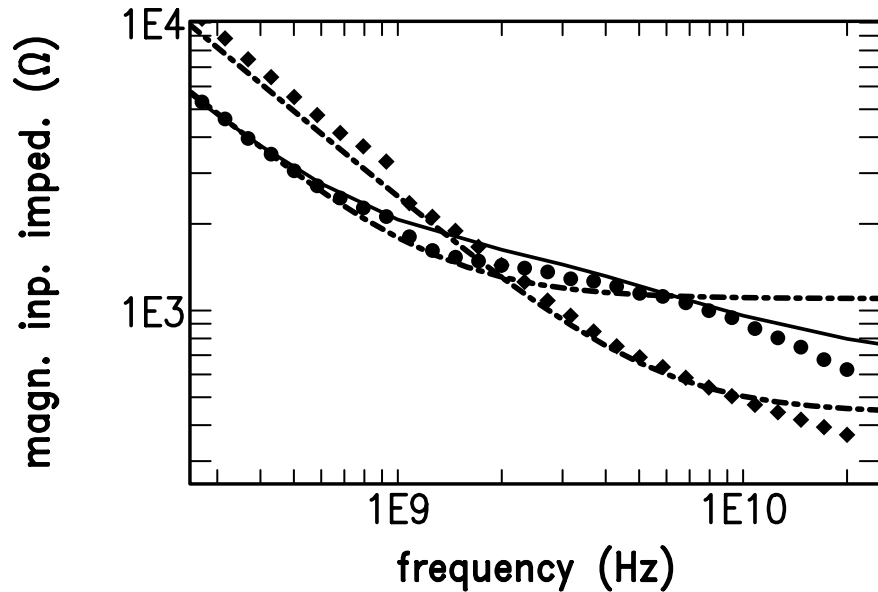


- N-channel 60/0.5 with $V_{T0} = 0.6V$
- salicidated 0.5 micron CMOS ($V_{dd} = 3.3V$)

- $V_{ds} = 2.0V$; $V_{gs} = 0.9, 1.2$ and $1.5V$

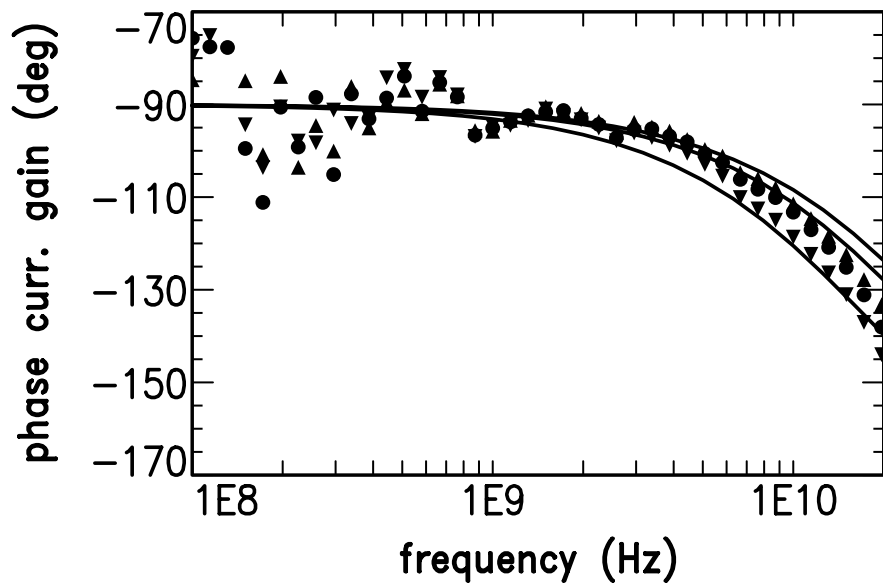
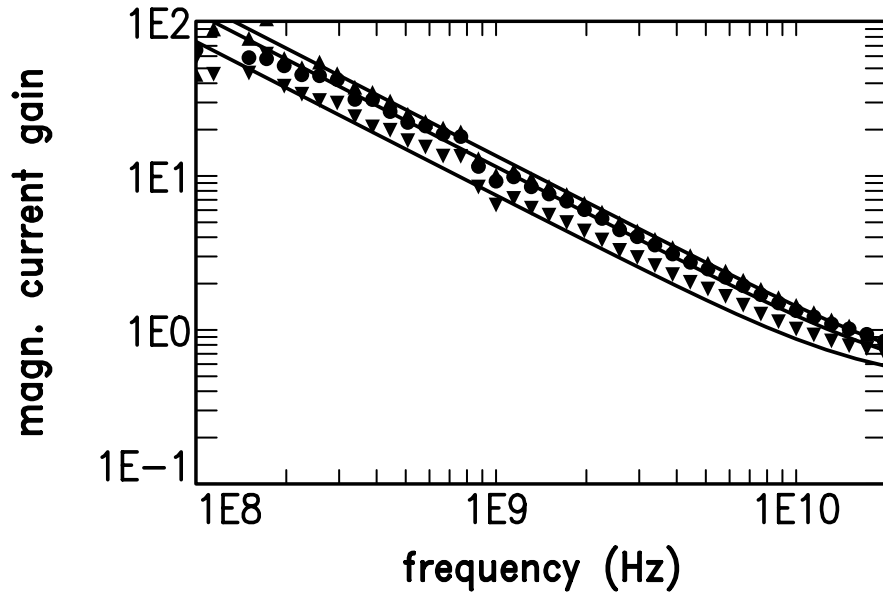
- $$Z_{in} = \frac{v_{in}}{i_{in}} \approx \frac{1 + j\omega R_g C_{gg}^{eff}}{j\omega C_{gg}^{eff}}$$

common SB configuration: inp. impedance & gate resistance



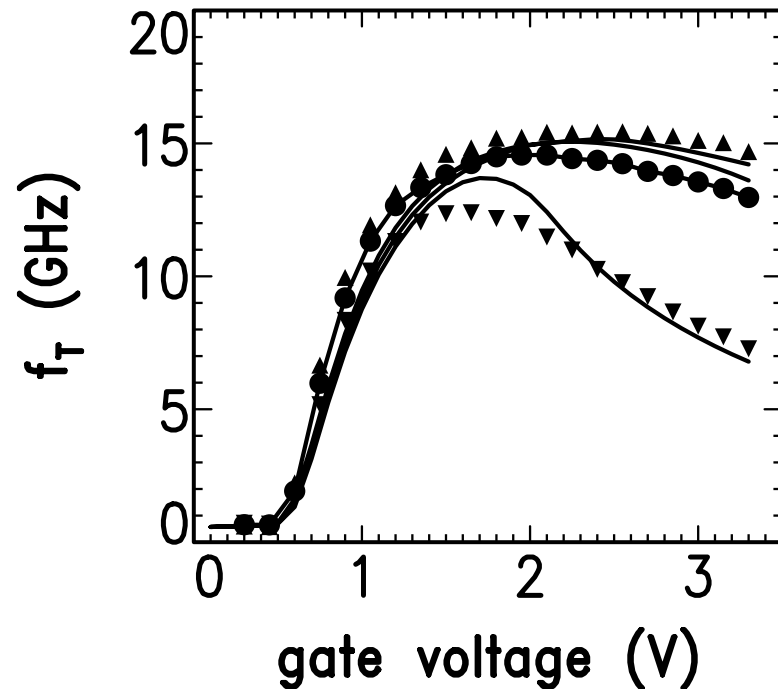
- N-ch. 100/1 and 40/1
- 1 micron CMOS ($V_{dd} = 5 V$)
- $V_{ds} = 5.0 V$; $V_{gs} = 2.0 V$
- $Z_{in} \approx \frac{1}{j\omega C_{gg}^{eff}} + R_g$
- 5 “distributed” parallel segments

common SB configuration: current gain



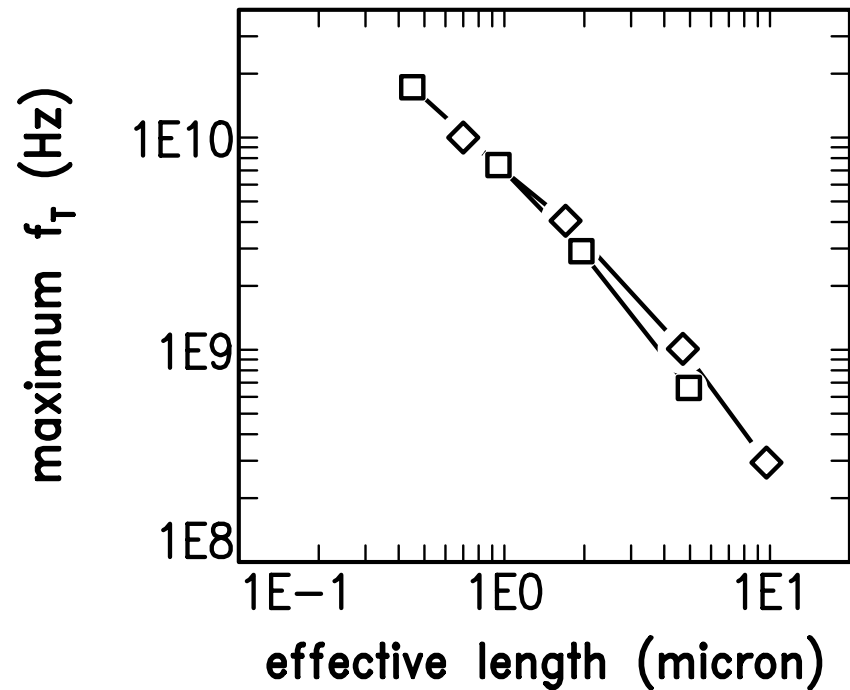
- N-channel 60/0.5 with $V_{TO} = 0.6V$
- salicidated 0.5 micron CMOS ($V_{dd} = 3.3V$)
- $V_{ds} = 2.0V$; $V_{gs} = 0.9, 1.2$ and $1.5V$
- $\frac{i_{out}}{i_{in}} \approx \frac{g_m}{j\omega C_{gg}^{eff}} \left(1 - j\omega \frac{C_{dg}^{eff}}{g_m} \right)$
- $f_T \approx \frac{g_m}{2\pi C_{gg}^{eff}}$

common SB configuration: f_T vs. gate voltage



- N-channel 60/0.5 with $V_{T0} = 0.6V$
- salicidated 0.5 micron CMOS ($V_{dd} = 3.3V$)
- $V_{ds} = 1.0, 2.0$ and $3.3V$
- $\frac{i_{out}}{i_{in}} \approx \frac{g_m}{j\omega C_{gg}^{eff}} \left(1 - j\omega \frac{C_{dg}^{eff}}{g_m} \right)$
- $f_T \approx \frac{g_m}{2\pi C_{gg}^{eff}}$

common SB configuration: maximum f_T vs. length



- N-channels

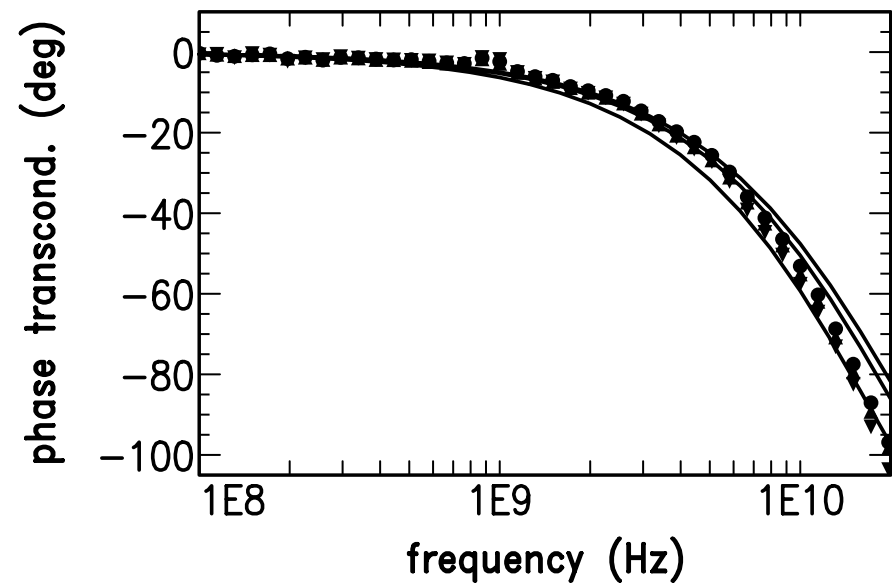
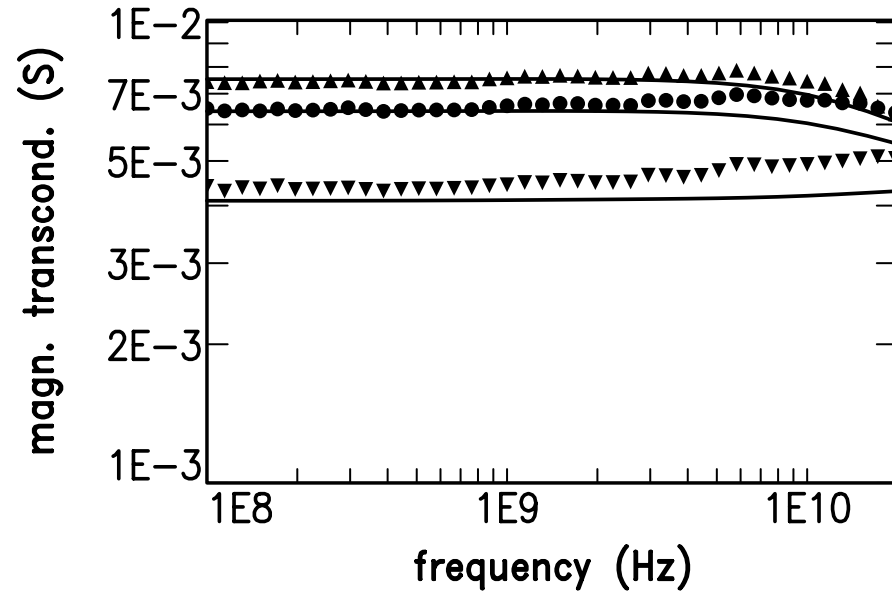
◇ 1 micron CMOS; $V_{dd} = 5.0 V$

□ 0.5 micron CMOS; $V_{dd} = 3.3 V$

- $f_T \approx \frac{g_m}{2\pi C_{gg}^{eff}} \propto \frac{1}{L_{eff}^2}$

- quasi-static model is valid for $f < f_T$

common SB configuration: transconductance

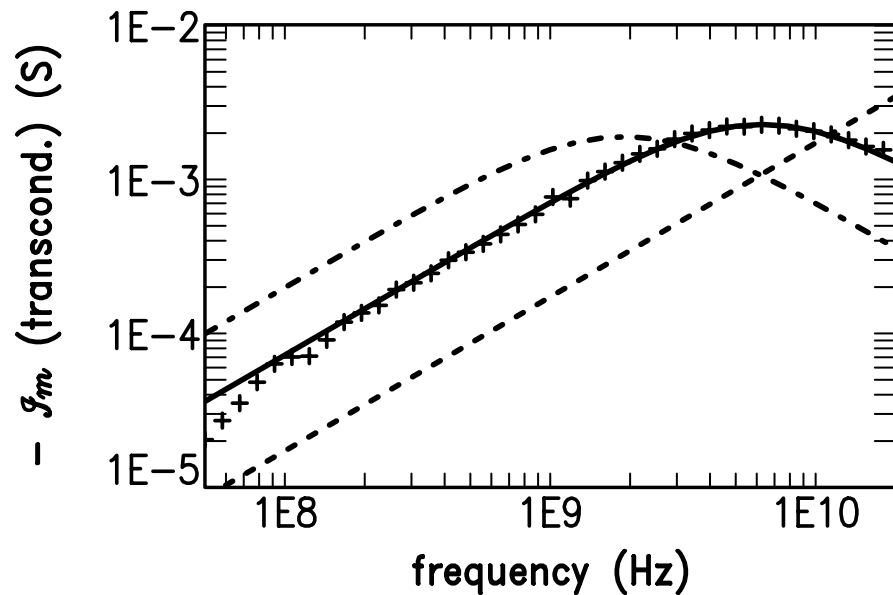
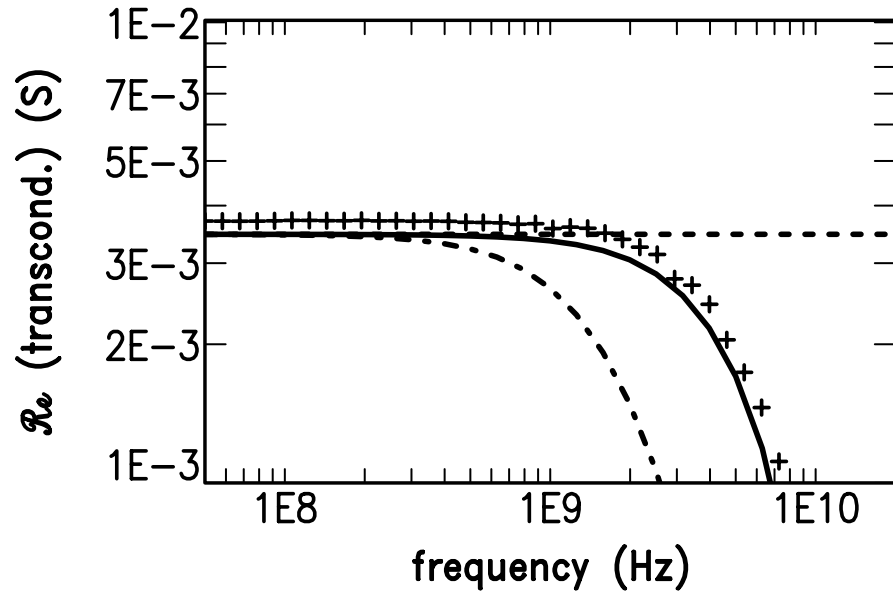


- N-channel 60/0.5 with $V_{T0} = 0.6V$
- salicidated 0.5 micron CMOS ($V_{dd} = 3.3V$)

- $V_{ds} = 2.0V$; $V_{gs} = 0.9, 1.2$ and $1.5V$

- $$\frac{i_{out}}{v_{in}} \approx \frac{g_m \left(1 - j\omega \frac{C_{dg}^{eff}}{g_m} \right)}{1 + j\omega R_g C_{gg}^{eff}}$$

common SB conf.: transconductance & gate resistance



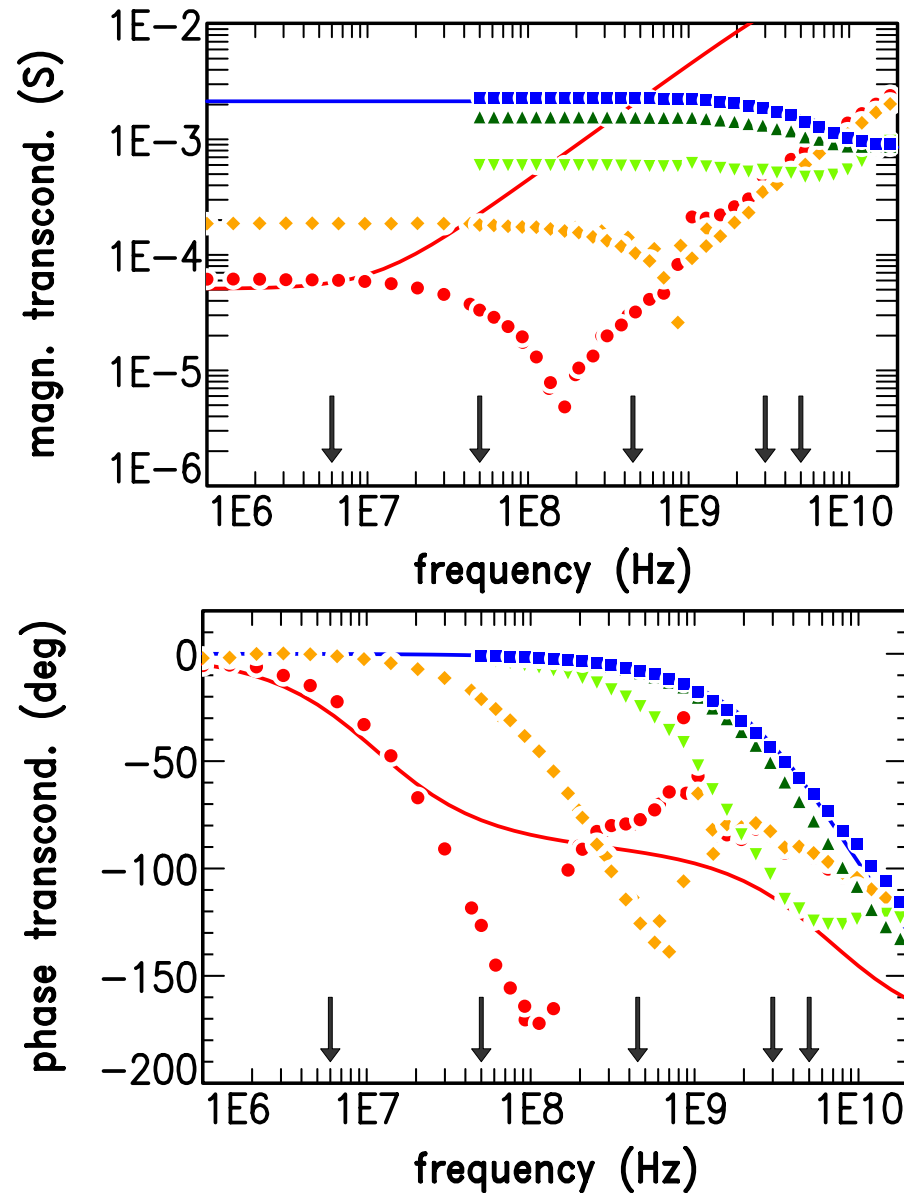
- N-channel 40/1
- 1 micron CMOS ($V_{dd} = 5 V$)
- $V_{ds} = 4.0 V$; $V_{gs} = 4.0 V$

- $\frac{i_{out}}{v_{in}} \approx$

$$\frac{g_m - \omega^2 R_g C_{dg}^{eff} C_{gg}^{eff} - j\omega (g_m R_g C_{gg}^{eff} + C_{dg}^{eff})}{1 + (\omega R_g C_{gg}^{eff})^2}$$

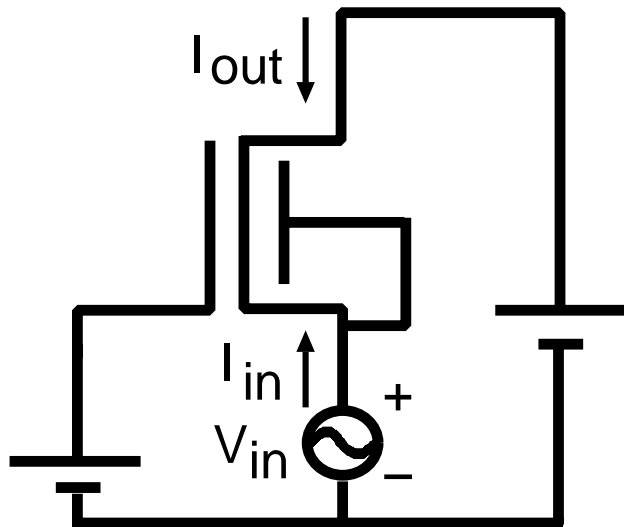
- $R_g = 0$, $\frac{W}{3L} \rho_{\square, poly}$ and $\frac{W}{L} \rho_{\square, poly}$

common SB configuration: transconductance vs. length



- P-ch. 30/30, 30/10, 30/3, 30/1, 30/0.6
- 0.7 micron CMOS ($V_{dd} = 5 V$)
- $V_{ds} = 4.0 V$; $V_{gs} = 4.0 V$
- $f_T \approx \frac{g_m}{2\pi C_{gg}^{eff}}$
- non-quasi static effects for $f > f_T$

common gate configuration



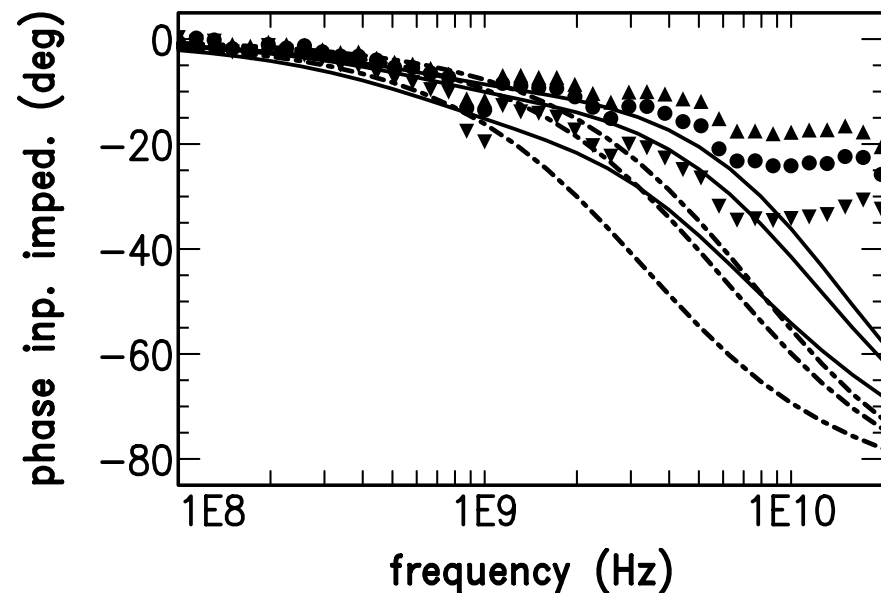
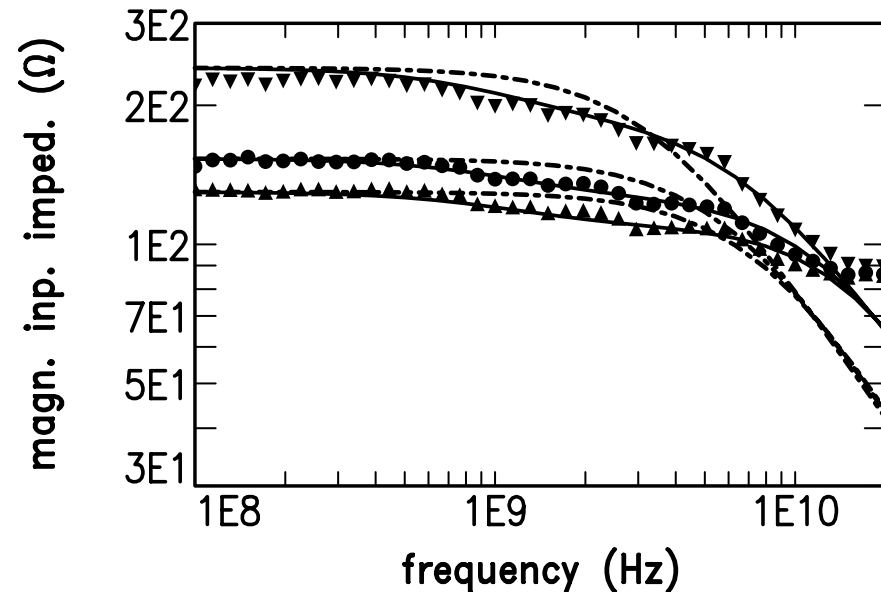
- voltage driven
- drain ac short-circuited

- input impedance $Z_{in} = \frac{v_{in}}{i_{in}}$

- current gain $\frac{i_{out}}{i_{in}}$

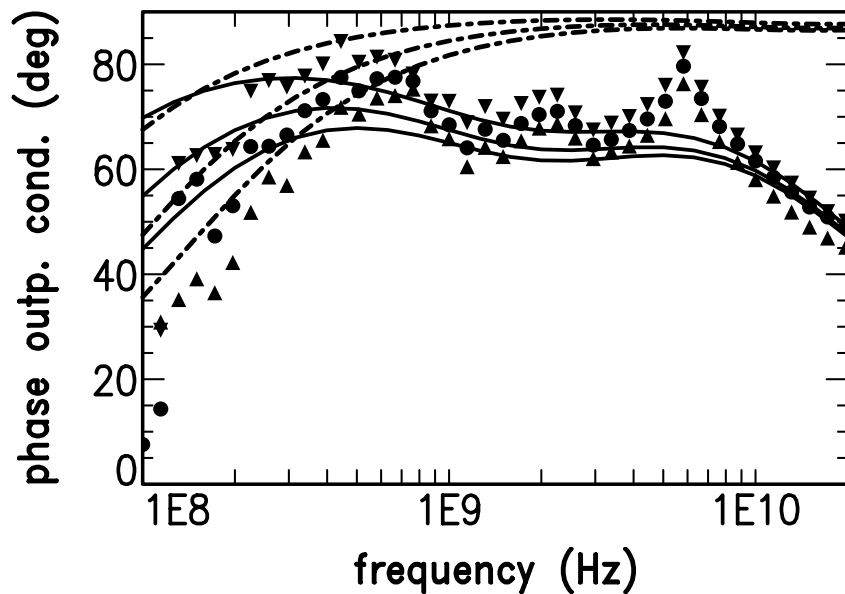
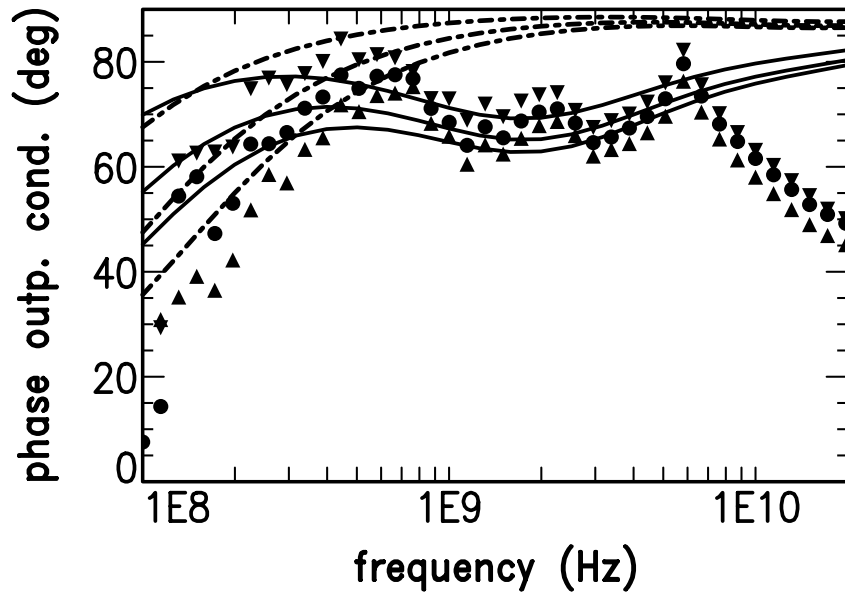
- transconductance $\frac{i_{out}}{v_{in}}$

common gate configuration: input impedance



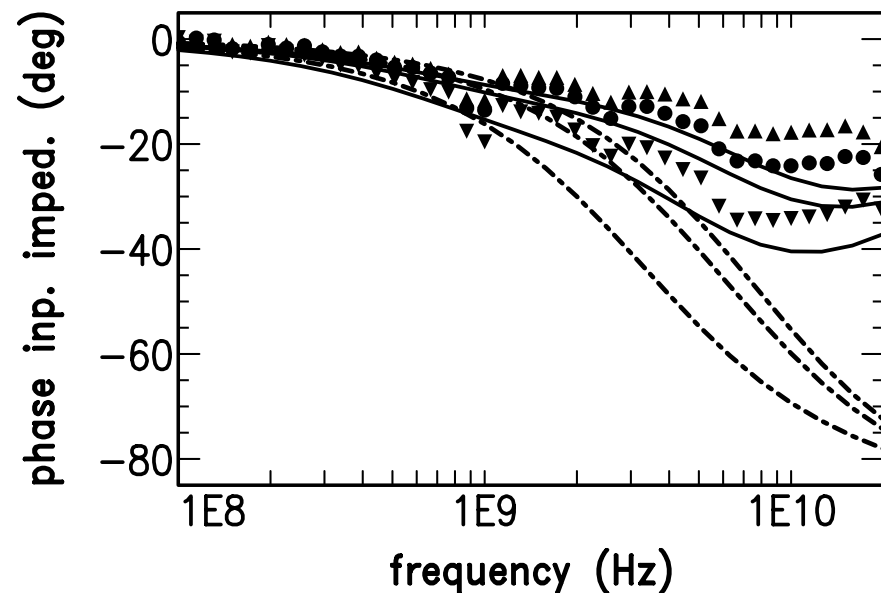
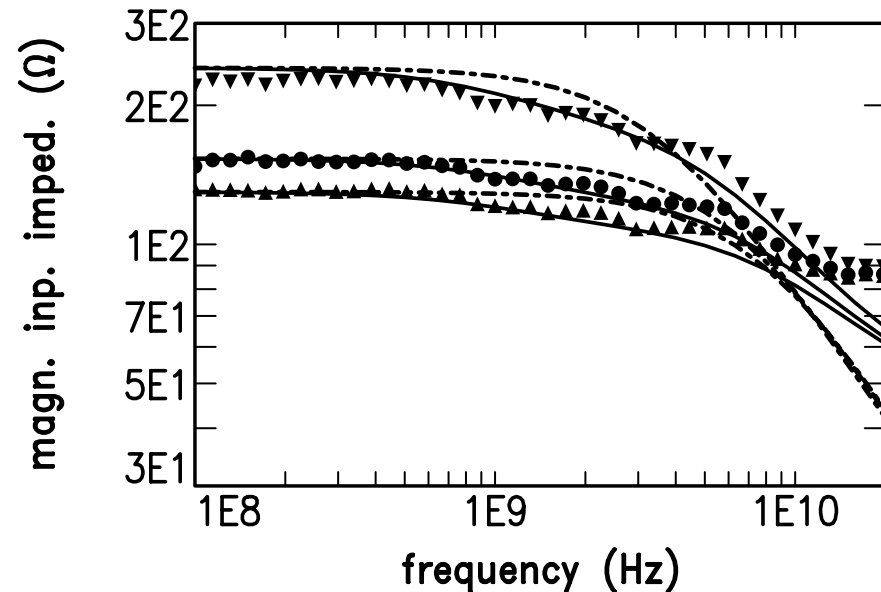
- N-channel 60/0.5 with $V_{TO} = 0.6V$
- salicidated 0.5 micron CMOS ($V_{dd} = 3.3V$)
- $V_{ds} = 2.0V$; $V_{gs} = 0.9, 1.2$ and $1.5V$
- $Z_{in} \approx (g_m + g_{ds})^{-1} \left(1 + j\omega \frac{C_{ss}^{eff}}{g_m + g_{ds}} \right)^{-1}$
- with and without bulk resistance

common gate configuration: output conductance



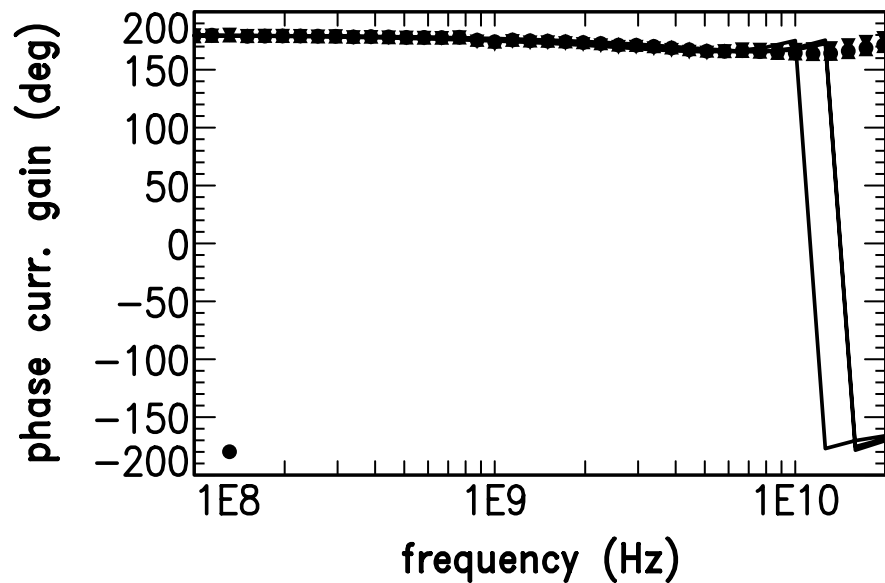
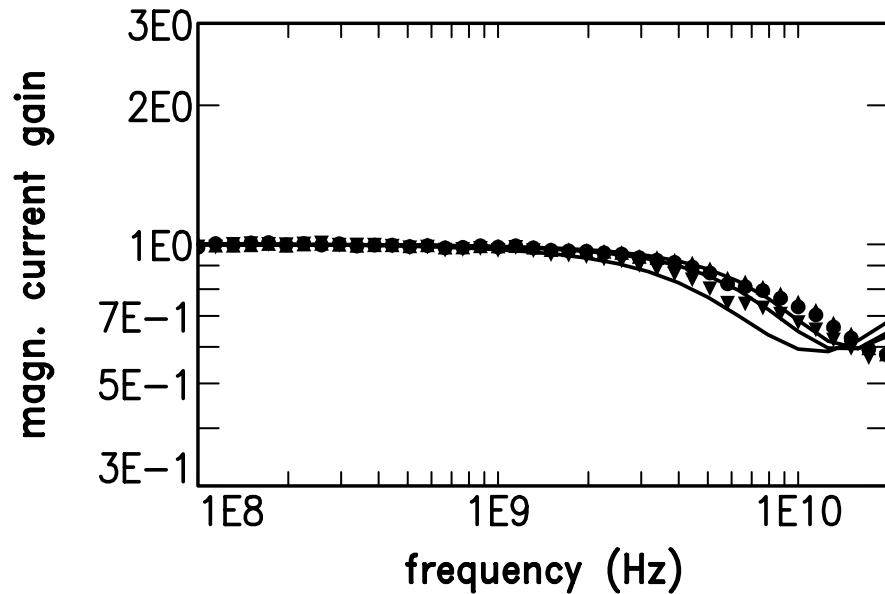
- N-channel 60/0.5 with $V_{T0} = 0.6V$
- salicidated 0.5 micron CMOS ($V_{dd} = 3.3V$)
- $V_{ds} = 2.0V$; $V_{gs} = 0.9, 1.2$ and $1.5V$
- bulk resistance
 - zero
 - lumped
 - “distributed”

common gate configuration: input impedance



- N-channel 60/0.5 with $V_{T0} = 0.6V$
- salicidated 0.5 micron CMOS ($V_{dd} = 3.3V$)
- $V_{ds} = 2.0V$; $V_{gs} = 0.9, 1.2$ and $1.5V$
- $Z_{in} \approx (g_m + g_{ds})^{-1} \left(1 + j\omega \frac{C_{ss}^{eff}}{g_m + g_{ds}} \right)^{-1}$
- bulk resistance: zero and “distributed”

common gate configuration: current gain

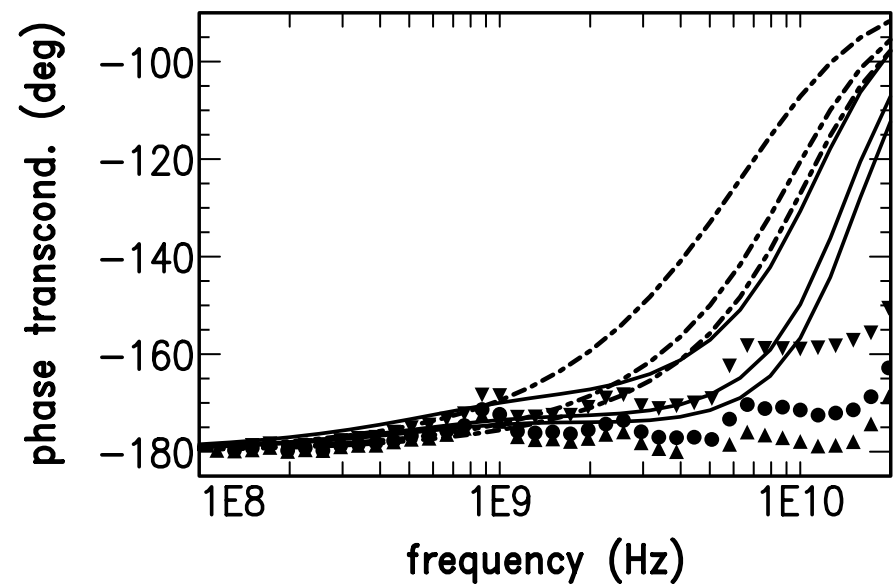
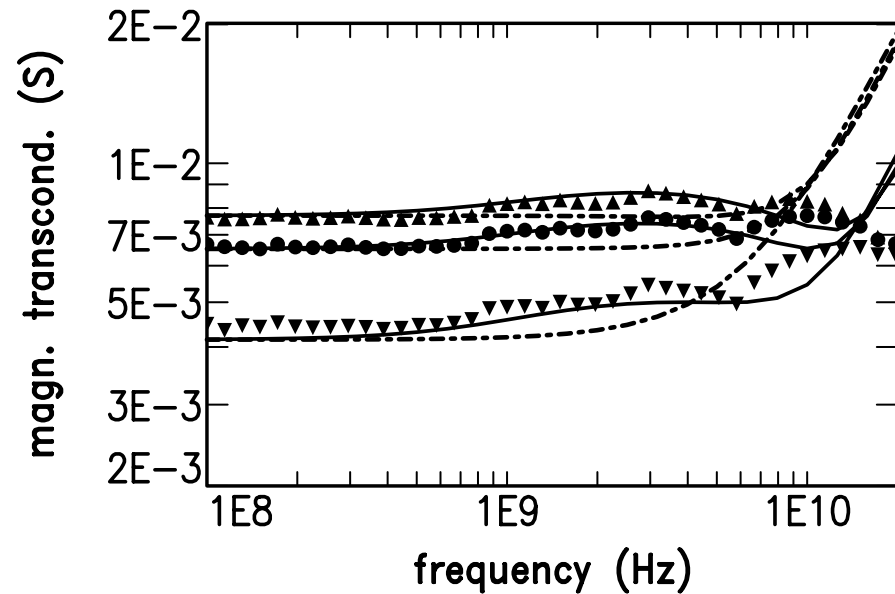


- N-channel 60/0.5 with $V_{T0} = 0.6V$
- salicidated 0.5 micron CMOS ($V_{dd} = 3.3V$)

- $V_{ds} = 2.0V$; $V_{gs} = 0.9, 1.2$ and $1.5V$

- $$\frac{i_{out}}{i_{in}} \approx - \left(1 + j\omega \frac{C_{ds}^{eff}}{g_m + g_{ds}} \right) \times \left(1 + j\omega \frac{C_{ss}^{eff}}{g_m + g_{ds}} \right)^{-1}$$

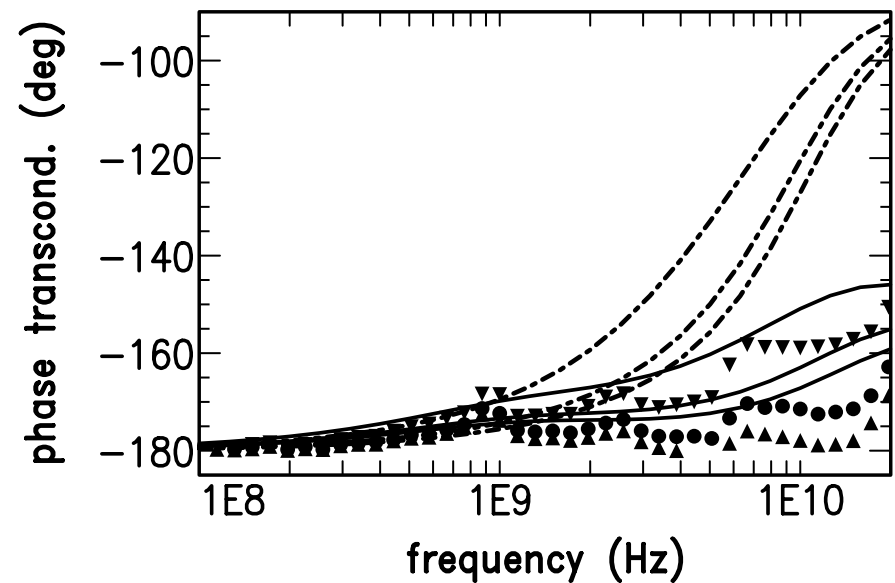
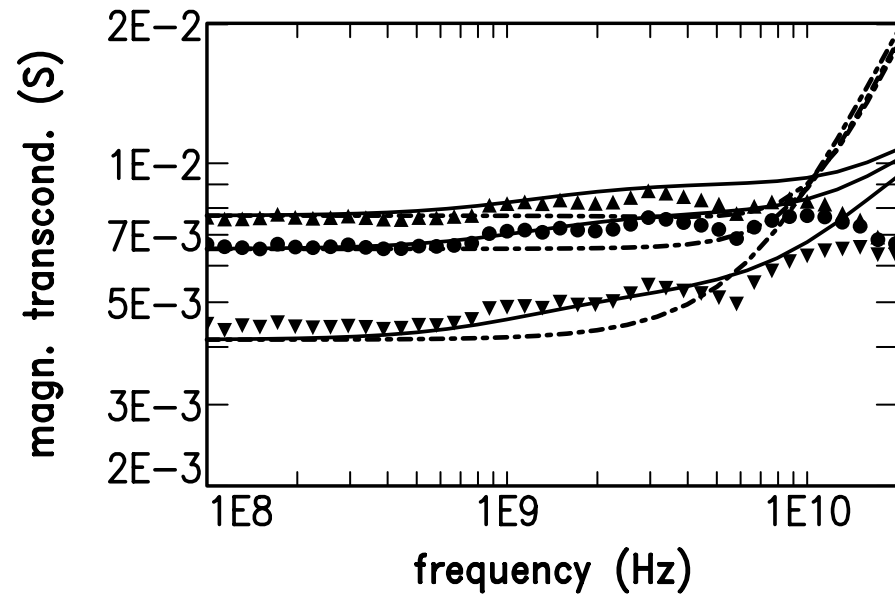
common gate configuration: transconductance



- N-channel 60/0.5 with $V_{TO} = 0.6V$
- salicidated 0.5 micron CMOS ($V_{dd} = 3.3V$)
- $V_{ds} = 2.0V$; $V_{gs} = 0.9, 1.2$ and $1.5V$
- $\frac{i_{out}}{v_{in}} \approx$

$$-(g_m + g_{ds}) \left(1 + j\omega \frac{C_{ds}^{eff}}{g_m + g_{ds}} \right)$$
- with and without bulk resistance

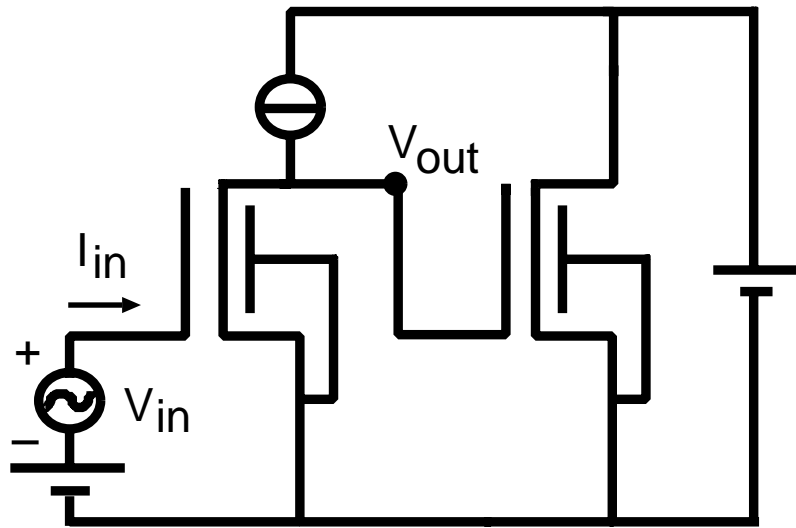
common gate configuration: transconductance



- N-channel 60/0.5 with $V_{TO} = 0.6V$
- salicidated 0.5 micron CMOS ($V_{dd} = 3.3V$)
- $V_{ds} = 2.0V$; $V_{gs} = 0.9, 1.2$ and $1.5V$
- $\frac{i_{out}}{v_{in}} \approx$

$$-(g_m + g_{ds}) \left(1 + j\omega \frac{C_{ds}^{eff}}{g_m + g_{ds}} \right)$$
- bulk resistance: zero and “distributed”

cascade configuration

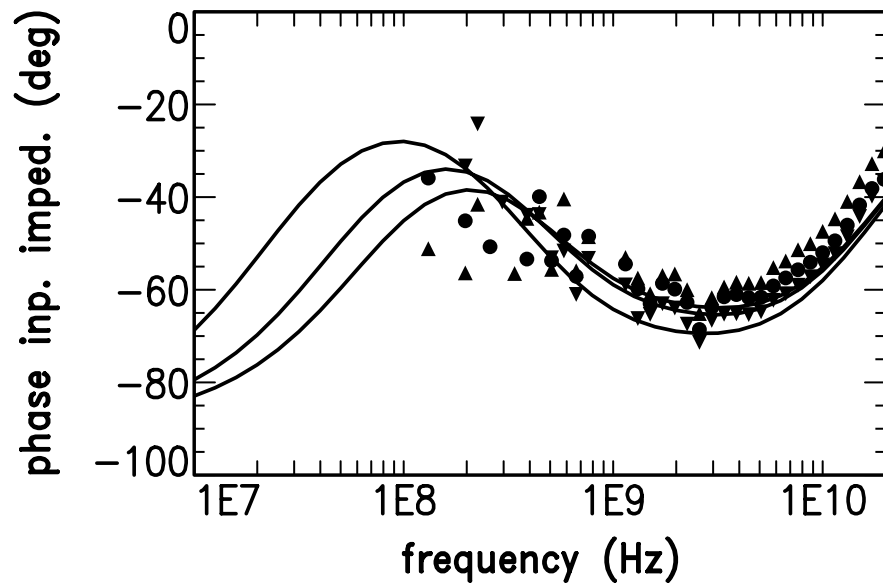
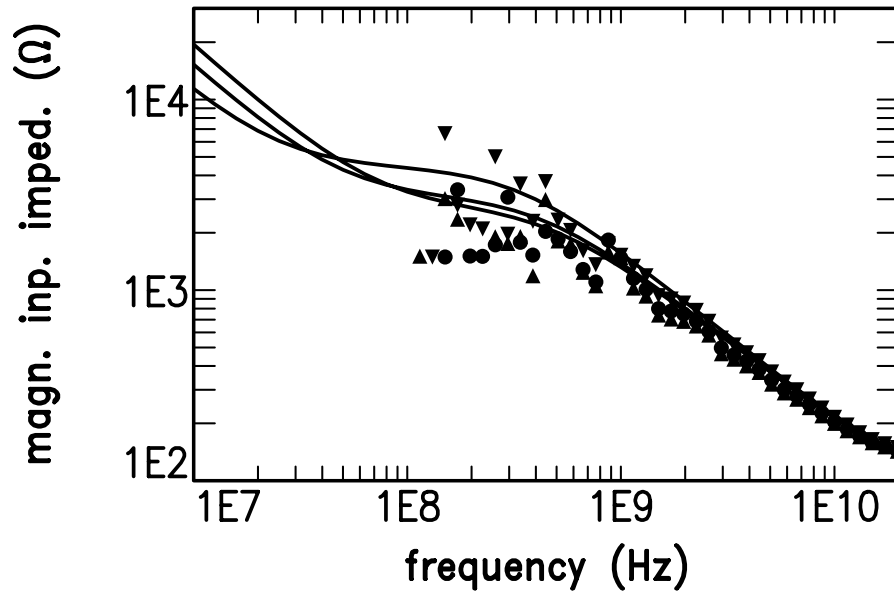


- voltage driven
- drain ac short-circuited

- input impedance $Z_{in} = \frac{v_{in}}{i_{in}}$

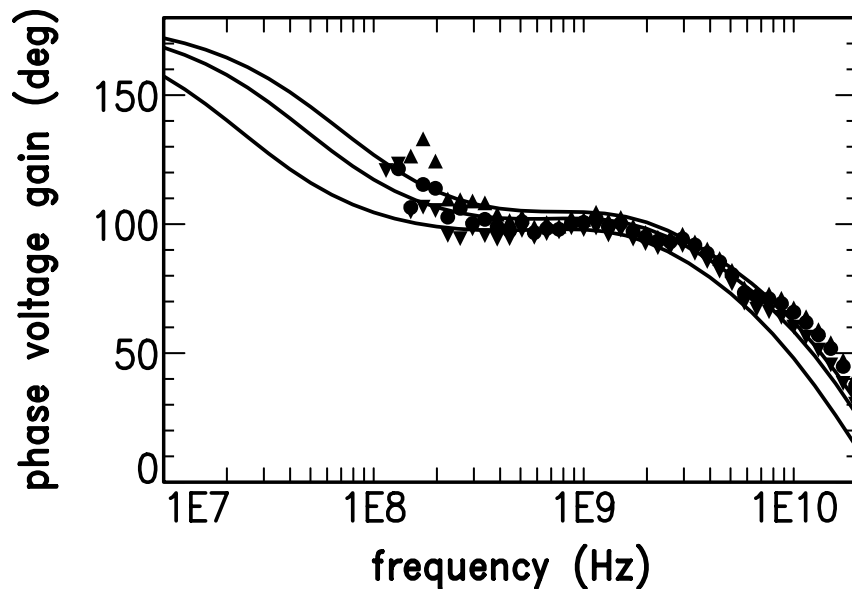
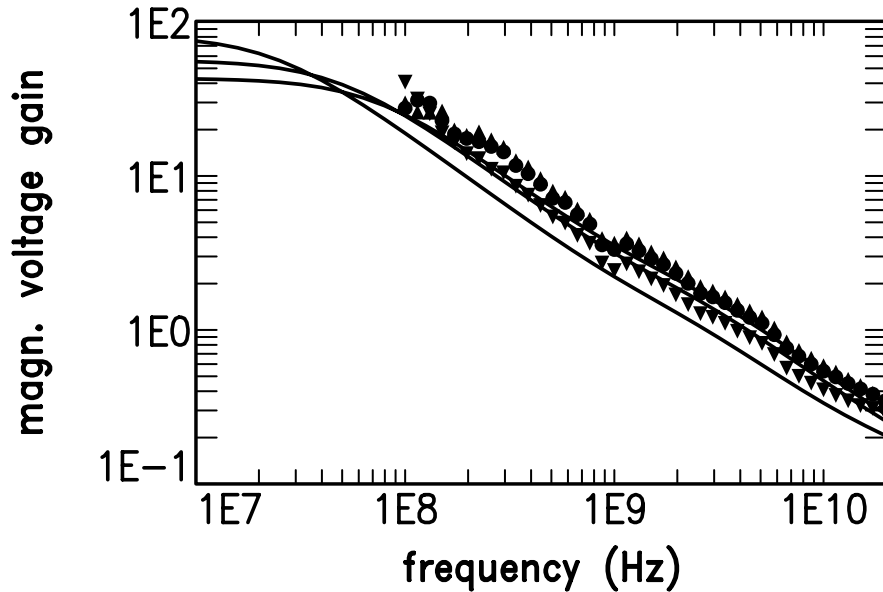
- voltage gain $\frac{v_{out}}{v_{in}}$

cascade configuration: input impedance



- N-channel 60/0.5 with $V_{TO} = 0.6V$
- salicidated 0.5 micron CMOS ($V_{dd} = 3.3V$)
- $V_{ds} = 2.0V$; $V_{gs} = 0.9, 1.2$ and $1.5V$

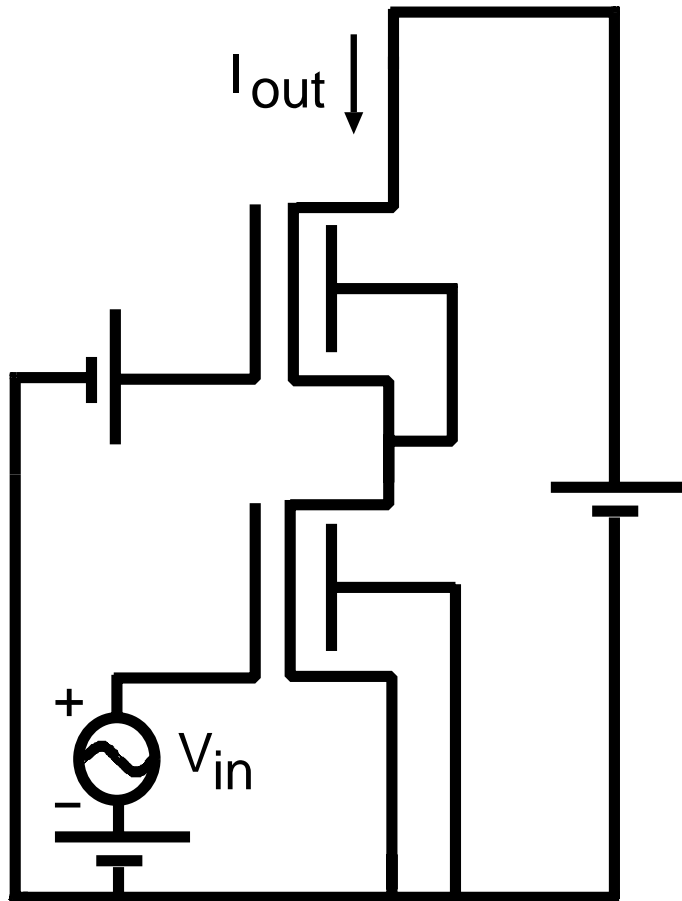
cascade configuration: voltage gain



- N-channel 60/0.5 with $V_{T0} = 0.6V$
- salicidated 0.5 micron CMOS ($V_{dd} = 3.3V$)
- $V_{ds} = 2.0V$; $V_{gs} = 0.9, 1.2$ and $1.5V$

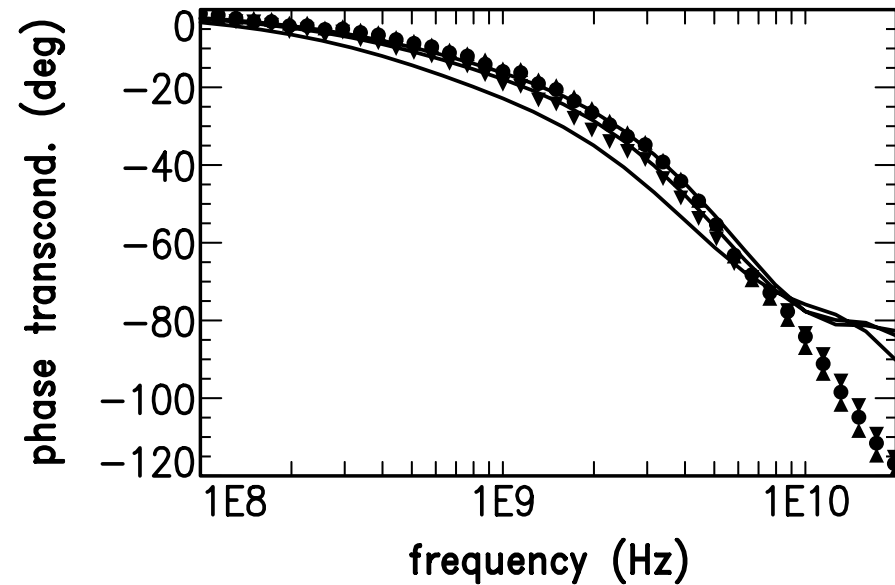
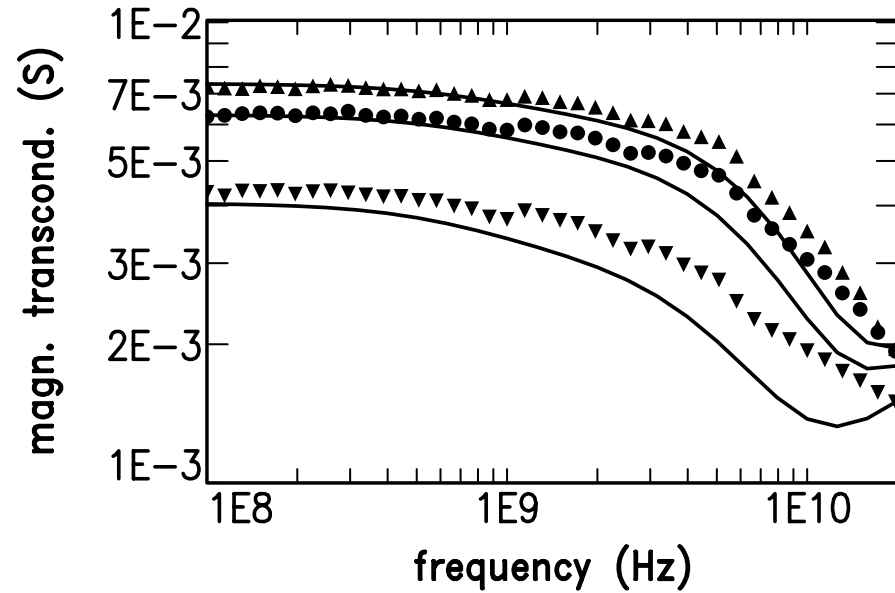
$$\bullet \frac{v_{out}}{v_{in}} \approx - \frac{g_m}{g_{ds}} \left(1 - j\omega \frac{C_{dg}^{eff}}{g_m} \right) \times \left(1 + j\omega \frac{C_{gg}^{eff} + C_{dd}^{eff}}{g_{ds}} \right)^{-1}$$

cascode configuration



- voltage driven
- drain ac short-circuited
- transconductance $\frac{i_{out}}{v_{in}}$

cascode configuration: transconductance



- N-channel 60/0.5 with $V_{TO} = 0.6V$
- salicidated 0.5 micron CMOS ($V_{dd} = 3.3V$)
- $V_{ds} = 2.0V$; $V_{gs} = 0.9, 1.2$ and $1.5V$

summary & conclusions

- MOS MODEL 9
- comparison measurements & simulations
 - MOSFET in common source-bulk configuration
 - MOSFET in common gate configuration
 - cascade configuration
 - cascode configuration
- effect of gate and bulk resistance
- MOS MODEL 9 gives accurate description for $f < f_T$