

Impact of Process Scaling on 1/f Noise in Advanced CMOS Technologies

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Abstract

The influence of the gate-oxide thickness, the substrate dope, and the gate bias on the input-referred spectral 1/f noise density $S_{V_{gate}}$ has been experimentally investigated. It is shown that the dependence on the oxide thickness and the gate bias can be described by the model of Hung, and that $S_{V_{gate}}$ can be predicted for future technologies. Discrepancies with the ITRS roadmap are discussed.

Introduction

Low-frequency (or 1/f) noise is very important for analog and RF applications in advanced CMOS technologies. Knowledge about the impact of process scaling on 1/f noise is therefore desirable. In Fig. 1 the 1997 NTRS roadmap and the 1999 ITRS roadmap data for the input-referred spectral noise density $S_{V_{gate}}$ is plotted versus technology generation. Large differences in $S_{V_{gate}}$ are observed. It is not clear how process scaling affects 1/f noise. Although different technologies have been compared [5], a systematic study of the impact of individual process scaling parameters on 1/f noise has never been reported. In this paper such a study is presented for the first time, both for NMOS and PMOS devices. The most important parameters acting on the 1/f noise, i.e. the gate-oxide thickness t_{ox} and the substrate doping N_A , were varied *independently*. The model of Hung [6] is used to interpret the data and to predict trends in $S_{V_{gate}}$ with technology scaling according to the ITRS roadmap.

Device fabrication and characterization

NMOS and PMOS transistors (with $W \times L = 10 \times 4 \mu\text{m}^2$, where W and L are the transistor width and length, respectively) were manufactured with physical t_{ox} of 2, 3.6, 5, 7.5, 10 and 20 nm, and N_A variants of $5 \cdot 10^{16} \text{cm}^{-3}$ and $5 \cdot 10^{17} \text{cm}^{-3}$. From every variant, 3 to 4 nominally identical samples (with minimal DC parameter variation) were selected for 1/f noise measurements. Noise measurements were all performed in saturation and as a function of the effective gate bias V_{gt} ($=V_{gs} - V_t$ where V_t is the threshold voltage). They were carried out with a BTA 9812A standard noise probe. Fig. 2 shows typical drain current noise spectra. We present all our further measurements in terms of $S_{V_{gate}}$ which is defined as: $S_{V_{gate}} = S_I / (g_m)^2$, with g_m the transconductance. Average $S_{V_{gate}}$ values at 100 Hz and standard deviations based on sample-to-sample spread were determined.

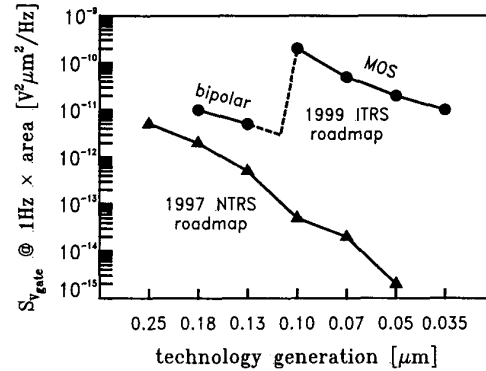


Figure 1: The 1997 NTRS [1] roadmap and the 1999 ITRS roadmap [2] for the 1/f noise spectral density $S_{V_{gate}}$ of a RF transistor. Note that $S_{V_{gate}}$ is normalized to an active device area of $1 \mu\text{m}^2$ and that $S_{V_{gate}} \propto (W \cdot L)^{-1}$ [3,4]. The 1997 roadmap does not mention the transistor type explicitly. The 1999 roadmap assumes a bipolar device through 110 nm and a MOS device for later generations. The effective gate bias V_{gt} however, is not mentioned.

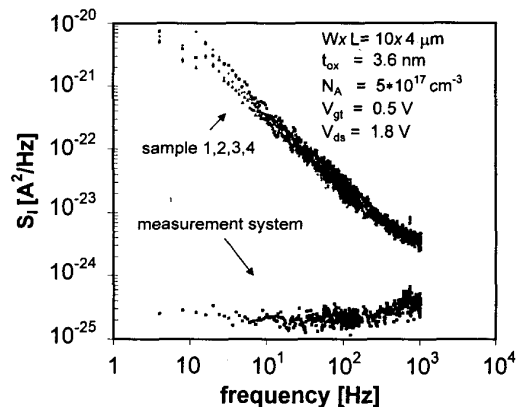


Figure 2: Drain current noise spectral density S_I versus frequency for 4 PMOS samples with identical thickness t_{ox} , dope concentration N_A and identical bias conditions. The sample to sample spread is at most a factor of 2, consistent with literature [4].

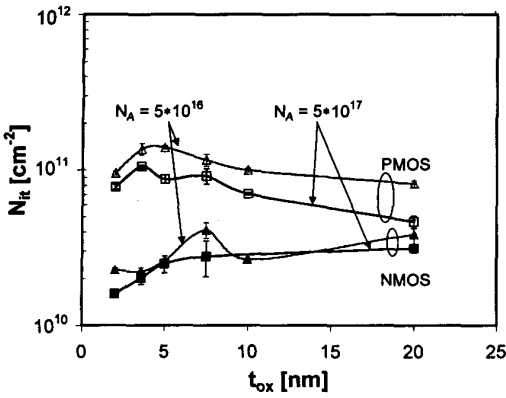


Figure 3: Interface state density N_{it} measured by means of charge pumping as a function of the gate-oxide thickness t_{ox} for NMOS and PMOS transistors at two different substrate dope

The number of interface states N_{it} , measured by charge pumping, is depicted in Fig. 3. For fixed N_A , the variation in N_{it} with t_{ox} is limited, both for N- and PMOS. This indicates similar oxide trap density near the interface for the different gate-oxides [7].

Experimental observations

In Fig. 4, Sv_{gate} is plotted versus t_{ox} for NMOS devices, for two values of N_A and V_{gt} . Data points show a power dependence on t_{ox} and the powers p are indicated. In Fig. 5 the same is done for PMOS devices. In Fig. 6 the values for p are plotted versus V_{gt} , both for N- and PMOS. According to Figs. 4 and 5, Sv_{gate} decreases with decreasing t_{ox} . Fig. 6 shows that Sv_{gate} of NMOS depends stronger on t_{ox} than that of PMOS. In Figs. 7(a-d) Sv_{gate} is plotted versus V_{gt} . For large t_{ox} , Sv_{gate} of PMOS shows a stronger dependence on V_{gt} than Sv_{gate} of NMOS. For small t_{ox} both NMOS and PMOS show a strong V_{gt} dependence. The substrate dope concentration N_A affects Sv_{gate} as well. With a 10 \times increase of N_A , Sv_{gate} enlarges with a factor 3 ± 1.5 (dependent on t_{ox} and V_{gt}). Moreover, with increasing N_A the dependence of Sv_{gate} on t_{ox} becomes stronger (Fig. 6).

Interpretation

The experimental observations are interpreted using the 1/f noise model by Hung *et al.* [6], which is implemented a.o. in BSIM3 and MOS Model 9. The model attributes the 1/f noise to trapping/detrapping of charge carriers in the gate oxide, which causes both the number of carriers in the inversion layer as well as their mobility to fluctuate in a correlated fashion. Previously, we have shown that this model describes

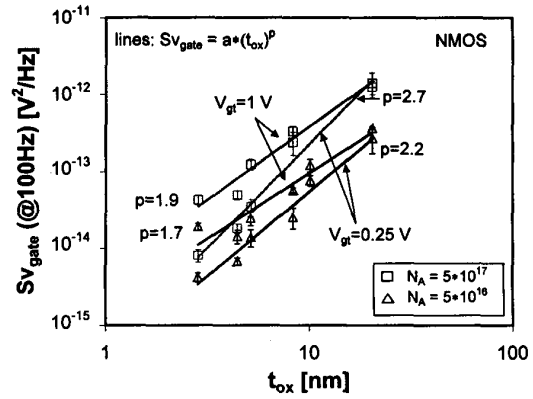


Figure 4: Sv_{gate} versus t_{ox} , for NMOS devices, for two values of N_A and V_{gt} . The error bars represent the measured sample-to-sample spread.

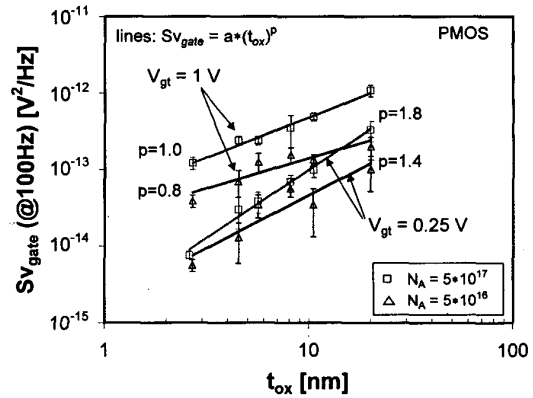


Figure 5: Sv_{gate} versus t_{ox} , for PMOS devices, for two values of N_A and V_{gt} . The error bars represent the measured sample-to-sample spread.

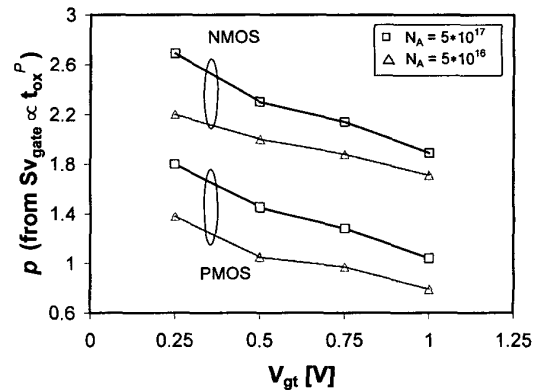


Figure 6: The powers p , determined according to the method of Figs. 4 and 5, for N- and PMOS devices.

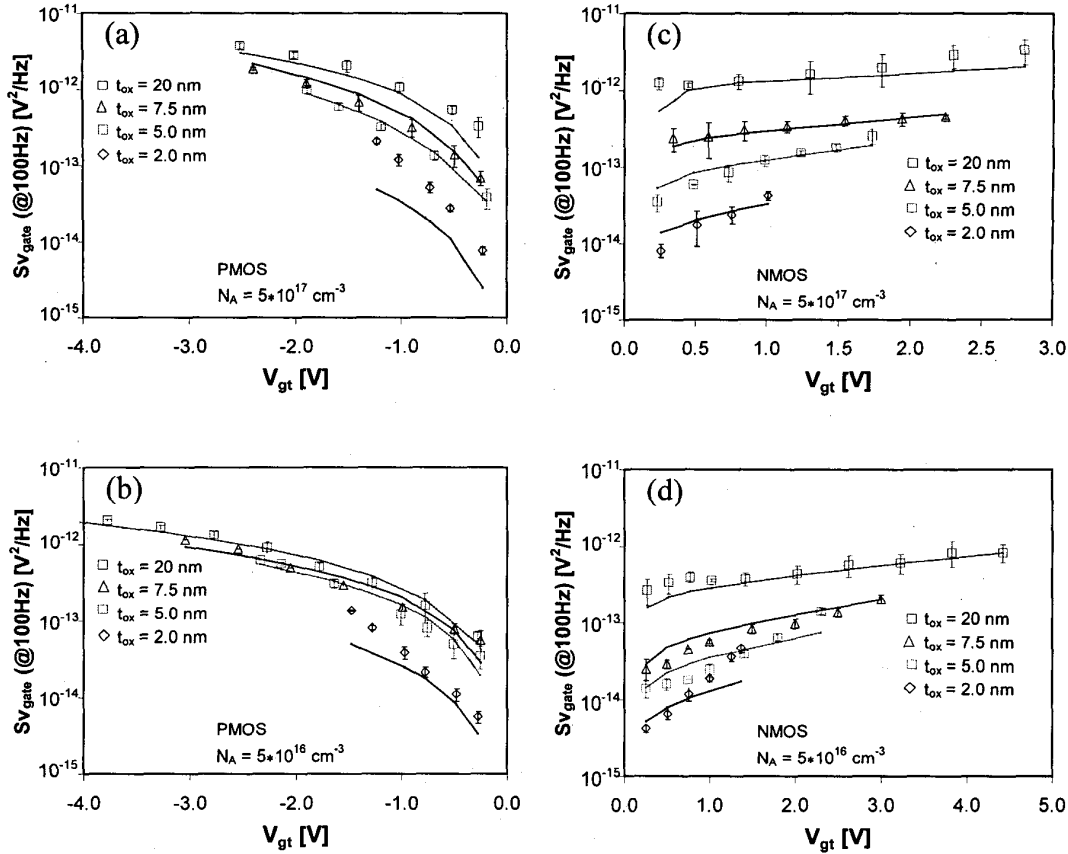


Figure 7: Symbols represent measured Sv_{gate} data as a function V_{gt} for $10 \times 4 \mu\text{m}^2$ devices with different gate-oxide thickness t_{ox} . (a) PMOS with high substrate dope concentration N_A . (b) PMOS with low N_A . (c) NMOS with high N_A and (d) NMOS with low N_A . The error bars represent the measured sample to sample spread. For clarity, not all t_{ox} variants are plotted. The lines represent fits using Hung's model [6], see text.

the bias dependence and the geometry scaling of the $1/f$ noise correctly [3]. To extract physical parameters from the model, we reduced the number of adjustable noise parameters to 2, following Ref. [8]. The first parameter is $N_{ot} \cdot d_{ox}$, the product of the density of oxide traps N_{ot} and the penetration depth of the electron wave function in the oxide d_{ox} . The second is the scattering parameter α_S , causing the mobility fluctuations. Using these parameters, both the V_{gt} - and the t_{ox} dependence can be described. This is shown in Figs. 7(a-d). In each figure, the 4 solid lines were fitted to the data using a single set of two noise parameters. N_{ot} is assumed to be proportional to the measured number of interface traps [7]. In the model the larger V_{gt} dependence of PMOS devices is attributed to the mobility fluctuation effect. The mobility fluctuation term in Sv_{gate} follows a slower t_{ox} scaling (t_{ox}^{-1}) than the number fluctuation term (t_{ox}^{-2}). This agrees with the observation that in

case of PMOS, Sv_{gate} scales slower with t_{ox} than in case of NMOS (Fig. 6). For both highly doped and lightly doped NMOS, we find $\alpha_S \approx 10^{-15} \text{ V}\cdot\text{s}$, in agreement with literature [6]; d_{ox} is found to be a factor of 4 larger for the highly doped case. Since in PMOS the contribution of mobility fluctuations to the noise is dominant, the separation between $N_{ot} \cdot d_{ox}$ and α_S is difficult. We could determine, however, that α_S is at least an order of magnitude higher for PMOS than for NMOS, and that d_{ox} is an order of magnitude smaller.

Technology scaling

Once the capability of Hung's model to describe our experimental data has been established, this model is used to predict Sv_{gate} in future technologies. Noise parameters extracted for

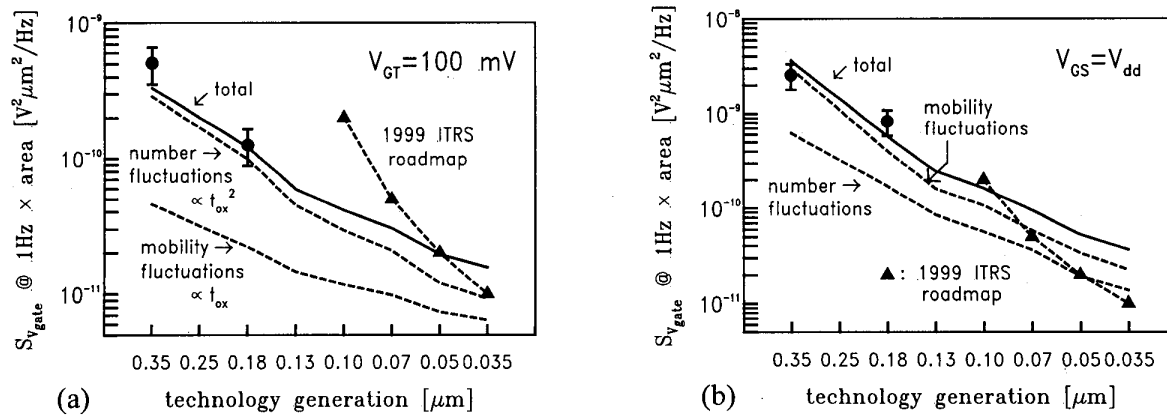


Figure 8: Solid curve: predicted $S_{v_{gate}}$ as a function of technology generation for NMOS at (a) $V_{gt}=100$ mV and (b) $V_{gs}=V_{dd}$. The contributions of the number fluctuation term and the mobility fluctuation term to $S_{v_{gate}}$ are separately depicted. For comparison the 1999 roadmap data is added. Circles: experimental results of existing generations.

the highly doped NMOS, were combined with compact model parameters for various technologies according to the ITRS roadmap. The changeover to nitrided oxides, taking place around $0.13 \mu\text{m}$, is not taken into account. Although nitridation tends to raise $1/f$ noise, process techniques to cancel out this increase have been demonstrated [9]. Since $S_{v_{gate}}$ depends on V_{gt} , two values for $S_{v_{gate}}$ were calculated. One just above threshold ($V_{gt}=0.1\text{V}$, Fig. 8 (a)), and the other at maximum bias ($V_{gs}=V_{dd}$, Fig. 8 (b)). For verification the predicted curves for $S_{v_{gate}}$ are compared with experimentally determined $S_{v_{gate}}$ values of two existing technologies (0.35 and $0.18 \mu\text{m}$). A good agreement is found. Comparing our prediction with the $1/f$ noise data in the 1999 ITRS roadmap, the roadmap numbers turn out to be reasonable, though a bit pessimistic at low gate drives. The trend on the other hand, is a bit too optimistic. In Fig. 8(a), our curve scales roughly with $(t_{ox})^2$ and changes slowly into a t_{ox} scaling for future generations. This can be understood by considering the separate contributions of the mobility - and the number fluctuation terms. $S_{v_{gate}}$ is dominated by the number fluctuation term, though a growing part comes from mobility fluctuations. Making $V_{gs}=V_{dd}$ leads to an opposite situation: at $0.35 \mu\text{m}$ the mobility fluctuation term prevails, but for more modern generations the number fluctuation term becomes significant. The steep slope of the mobility fluctuation curve in Fig. 8 (b) is due to the dependence of this curve on both t_{ox} and V_{gs} . Since $V_{gs}=V_{dd}$, V_{gs} changes with generation.

Conclusion

The influence of the parameters t_{ox} , N_A and V_{gt} on $S_{v_{gate}}$ has been investigated experimentally for the first time. The de-

pendence on t_{ox} and V_{gt} can be described by the model of Hung. Using this model, $S_{v_{gate}}$ can be predicted for future technologies. At low V_{gt} , $S_{v_{gate}}$ scales with $(t_{ox})^2$ down to the $0.13 \mu\text{m}$ technology. However, on the longer term, $S_{v_{gate}}$ will scale with t_{ox} , which deviates from roadmap data.

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