The JESD204A interface – The key to broadband wireless system miniaturization

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0.0 Introduction - New and transformative high-speed data converter interface

The new JEDEC JESD204A high speed serial data converter interface offers many system design and system cost advantages; see http://www.jedec.org/standards-documents/results/JESD204A. NXP Semiconductors estimates that early adopters of this SerDes-based interface are realizing a 25 % to 40 % Total Cost of Ownership (TCO) savings, which quickly pays for the NRE (such as expert-level specification competence, implementing the system change, testing the new system design, etc.) associated with moving to this plug and play point-to-point unidirectional interconnect. One of the relatively under-appreciated performance advantages of JESD204A is lower Electro-Magnetic Interference (EMI) and Radio Frequency Interference (RFI). Lower EMI and RFI allow the miniaturization of broadband wireless infrastructure subsystem, specifically radio transceiver boards, to an extent not possible with traditional LVDS parallel interfaces.

1.0 Emergent base radio transceiver station design imperatives

As base station radio designers demand increasingly smaller transceiver subsystems to save system cost and power, EMI/RFI isolation becomes more challenging to maintain, and mixed-signal RF crosstalk more difficult to manage. This is due to the high speed ADCs and DACs, RF mixers, RF demodulators, digitally-controlled VGAs and RF Low-Noise Amplifiers (LNAs) that are being forced to co-exist together in a shrinking PCB footprint, either as packaged ICs or bare dice in Multi-Chip Modules (MCMs). It should be self-evident that electromagnetic isolation is more difficult to achieve in tighter physical spaces as EMI follows the inverse square law in terms of field strength versus distance.

S-parameter simulations demonstrate that the low-voltage CML switching used in the JESD204A interface specification has significantly lower EMI/RFI radiation than the legacy LVDS parallel interface. The JESD204A interface also has a higher bandwidth pipe, offering a maximum 312.5 MB/s payload per differential lane pair versus a maximum 1 Gbps LVDS pair (JESD204A uses 8B/10B coding, hence the encoding overhead factor).

The physical layer defined in the JESD204A specification has low voltage swing, differential, and suitable for low voltage supply IC technologies. The PHY specification is aligned with the OIF (Optical Internetworking Forum) SxI-5 and TFI-5 implementation agreements and corresponds to what is known generally in the industry as "CML". Compliant transmitters and receivers achieve a Bit Error Rate (BER) of less than 1E−12 over a reach of up to 20 cm. JESD204A uses 8B/10B coding to enable so-called “clock data recovery”; the differential serial bit stream is encoded with sufficient logic state transitions to allow the bit clock to be recovered from the data stream itself. This avoids the need for a separate bit clock signal, simplifying the hardware interface. These

signalling characteristics also make JESD204A friendly to fibre optical transport for extended reach applications in base station radio transceivers and other industrial applications where EMI/RFI immunity is desired.

Of course, the JESD204A interface's fatter pipe means fewer wires are needed to carry the equivalent bandwidth compared to the wider parallel LVDS interface it replaces and significantly reduces the digital interface pin count. For example, a dual-channel 14-bit ADC typically requires 28 pins for the data interface (LVDS Dual Data Rate) plus 2 pins for clock, or roughly 30 pins. Not included in this total are the many grounds and VDD pins required to minimize supply switching bounce. Conversely, JESD204A does not require separate pins for clocks, just a differential SYNC signal from receiver to transmitter. As an example, for a dual-channel 16-bit 250 Msps ADC, four lanes or 8 pins are sufficient or 10 pins including the differential SYNC signal. This is an interconnect reduction of 66 % at minimum.

2.0 JESD204A – FPGA pin count reduction and channel capacity expansion

There is a corresponding pin count reduction on the transceiver board FPGA. The Xilinx Virtex 5 and Virtex 6 family FPGAs support the NXP Semiconductors' JESD204A ADCs and DACs optimally; indeed, NXP Semiconductors used Virtex 5 family FPGAs to create the world's first JESD204A interoperability test platform, and uses the same FPGA to demonstrate Multi-Device Synchronization (MDS), a feature which ensures precisely phase-coherent outputs on up to sixteen DAC data streams. The Virtex RocketIO, GTX and GTH SerDes-based transceivers are OIF CEI (Common Electrical I/O) compliant, and perfectly suited to JESD204A and the JESD204B specification expected in 2011.

The pin count reduction associated with JESD204A ADCs and DACs means that the same Xilinx Virtex family FPGA can support more transceiver channels on one radio PCB. This is an especially compelling advantage as end-market demands from cellular voice and data service providers shift toward LTE and Multiple Input Multiple Output (MIMO) to achieve higher spectral efficiency (bits/Hz). Wireless service providers are also expected to increasingly demand small form factor microcell and picocell base transceiver stations, to avoid the high CAPEX and OPEX associated with macrocell towers. JESD204A is well-aligned to the need for smaller BTS implementations. Xilinx FPGAs are fully interoperable with NXP Semiconductors' JESD204A high speed converters as announced by the two companies in February 2010; see http://www.nxp.com/news/content/file_1678.html.

Fewer signaling pins means that more pins can be devoted to power and ground for switching robustness and EMI/RFI isolation. Fewer pins also mean smaller functional subsystems, without compromising or sacrificing mixed-signal isolation to yield minimal crosstalk.

3.0 Unique system enhancements from JESD204A

Another unique feature of JESD204A contributes to overall system performance. An optional pseudo-random scrambling mode, implemented as a shift-register feedback scheme based on a simple polynomial, functions in the ADC Tx to decorrelate the output digital bit stream from any periodicity in the input analog waveform. This also helps to attenuate or eliminate periodic cross-talkers arising from board-level EMI/RFI.

Sophisticated symbol-based protocols, using embedded state machines with no system software overhead, including signal lane alignment, eliminate signal skew concerns and permit easy implementation of quadrature (phase-coherent I/Q) sampling.

Xilinx offers several JESD204A resources to radio transceiver system designers on their website:

http://www.xilinx.com/support/documentation/application_notes/xapp876.pdf

http://www.xilinx.com/publications/prod_mktg/wireless_brochure.pdf

NXP Semiconductors' JESD204A resources can be found at:

http://www.nxp.com/campaigns/fasttrackyourdesign/index.php?ecmp=610&utm_source=NXP_marketing_dcc&utm_campaign=data_converters&utm_medium=email_ext_dcc&utm_region=WW

4.0 Conclusion – Exciting backwards-compatible future path

As base station designers drive relentlessly toward lower capital and operating expense goals, the JESD204A high speed data converter interface becomes more and more attractive. The coming JESD204B version, expected to bring backwards-compatible bandwidth and deterministic delay specification enhancements in 2011, will make this new interface even more compelling to wireless infrastructure developers. By 2012, all new base station transceiver designs are anticipated to adopt this exciting new interconnect standard.

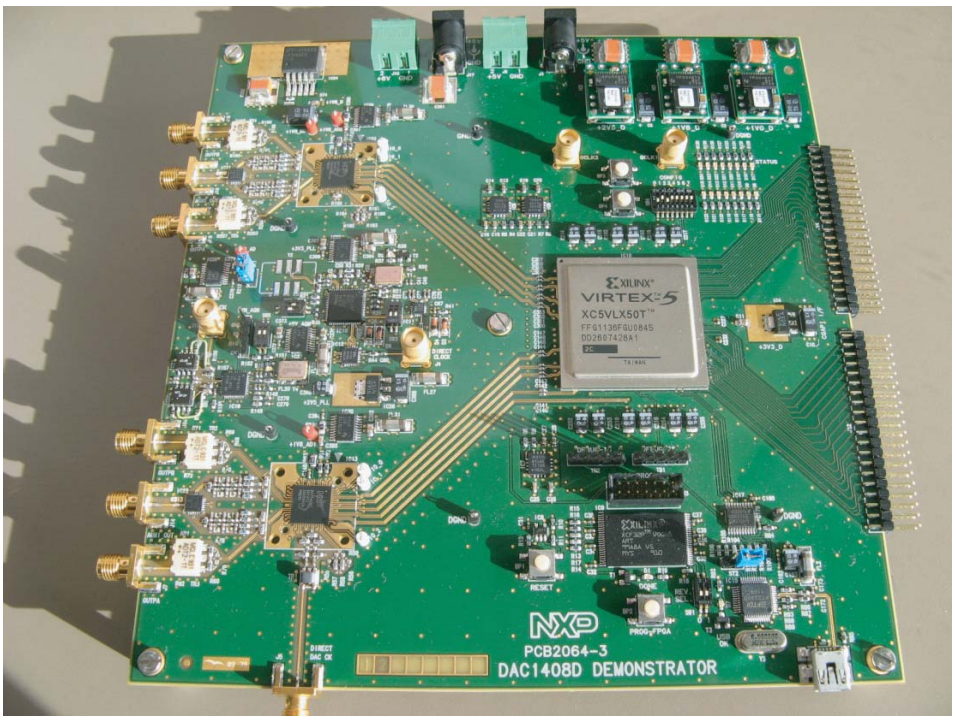

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Fig 1. The NXP Semiconductors DAC1408D MDS demonstration board using the Xilinx Virtex-5 family FPGA

Table 2. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
BTS	Base Transceiver Station
CAPEX	CAPital EXpenditure
CML	Current Mode Logic
DAC	Digital-to-Analog Converter
FPGA	Field-Programmable Gate Array
IC	Integrated Circuit
LTE	Long-Term Evolution
LVDS	Low-Voltage Differential Signaling
NRE	Non-Recurring Engineering
OPEX	OPErating EXpenditure
PCB	Printed-Circuit Board
PHY	PHYsical layer protocol
SerDes	Serializer Deserializer
VDD	positive IC voltage supply
VGA	Variable Gain Amplifier

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