Business and Commercial Implications of NXP Semiconductors' New JEDEC JESD204A High-Speed Data Converters

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June 2009

0.0 Introduction

In early June 2009, NXP Semiconductors announced a commitment to providing high-speed data converters compliant to the JEDEC JESD204A interface standard. A demonstration of the first JESD204A digital-to-analog converter (DAC) was conducted at the International Microwave Symposium (www.ims2009.org) in Boston on June 8th, 2009. The JEDEC JESD204A specification (see www.jedec.org/download/search/JESD204A.pdf), to which NXP Semiconductors was a primary contributor, is a new industry standard for the high-speed serial interconnection of data converters and logic devices. JESD204A standard (2008) extends the older JESD204 standard (2006) with the key concept of multiple synchronous serial data lanes, with embedded protocols which monitor and maintain time-aligned data lanes. This new standard offers compelling business and commercial merits which system design managers and equipment technology planners should carefully consider. This whitepaper explores those business and commercial merits in moderate detail.

By way of context, the NXP JESD204A compliant ADCs offer input sampling rates up to 125 MSPS, and the NXP JESD204A compliant DACs offer output update rates up to 650 MSPS. Both the ADC models and the DAC models offer typical Spurious-Free Dynamic Range (SFDR) specifications of 90 dBc. Select NXP JESD204A ADC and DAC family members are currently sampling, along with demo boards for system performance evaluation by prospective lead customers. See http://www.nxp.com/#/homepage/cb=[t=p,p=/50935/53500]|pp=[t=pfp,i=53500] for more information.

These new JESD204A data converters are targeted to macrocell basestation, medical imaging, high-speed instrumentation, video processing and broadcast, military and industrial data acquisition applications. Indeed, the combination of outstanding dynamic performance plus the advanced feature set enabled by the low-overhead JEDEC JESD204A digital interface presents a compelling new design-in option for high-speed data acquisition engineers across the electronics industry. JESD204A is supported by Xilinx's Spartan and Virtex product families with GTP and GTX transceivers, by Lattice's ECP2M and EPC3 product families, and by Altera's Arria and Stratix product families with GX transceivers.

1.0 JEDEC JESD204A Serialization – A Brief Overview

In April 2008, the JEDEC Solid State Technology Association JC-16 Committee on Interface Technology published the JESD204A specification, which is a significant revision to the JESD204 specification, published in 2006.

The key enhancement offered by JESD204A is the support beyond single lane links, to multiple time-aligned (synchronized) lanes per link. This enhancement enables the use of much higher bandwidth data converters, as well as multiple synchronized data converter channels. Specifically, the JESD204 specification, with only one lane defined at 3.125 Gbps, limits a single-channel 16-bit data converter

to (3.125 Gbps/20) = 156.25 MSPS and limits a dual-channel 16-bit data converter to 78.125 MSPS. [The division by 20 is a consequence of the 8B/10B data encoding mentioned below.]

JESD204A allows a single-channel data converter to multiplex its digital I/O across multiple lanes. For example, a 16-bit single-channel ADC multiplexing its output across four lanes has the potential to support a maximum sampling rate of ((3.125 Gbps/20) * 4) = 625 MSPS.

The use of a high-speed serial interface brings the important benefit of semiconductor package I/O pin reduction. For example, using conventional parallel LVDS I/O, a high-speed dual-channel 14-bit ADC requires (2 * 14) = 28 interconnect wires. By comparison, a JESD204A compliant high-speed dual-channel 14-bit ADC defines two differential data lanes, each consuming two interconnect wires, each with (3.125 Gbps/10) = 312.5 MB/sec of raw link bandwidth, plus a differential SYNC signal, for a total of six interconnect wires, an apples-to-apples pin count reduction of roughly 80%. Note that this pin count reduction occurs at both the data converter and the logic device (typically an FPGA). **This pin count reduction leads to several important commercial benefits**. The printed circuit board (PCB) is both easier to route (**labor cost savings**), potentially smaller (**Bill of Materials [BOM] cost savings**), and typically will require fewer routing layers (**more BOM cost savings**).

Following typical open systems models, the JESD204A specification includes an electrical PHY layer protocol, a transport layer protocol, and a data link layer protocol, and as noted above, adds an important new capability to the existing JESD204 specification: the ability to support multiple time-aligned lanes in a single data link protocol structure. JESD204A also allows a single ASIC (including DSPs and microcontrollers) or FPGA to support multiple (or "multipoint") links, as shown in Figure 1.

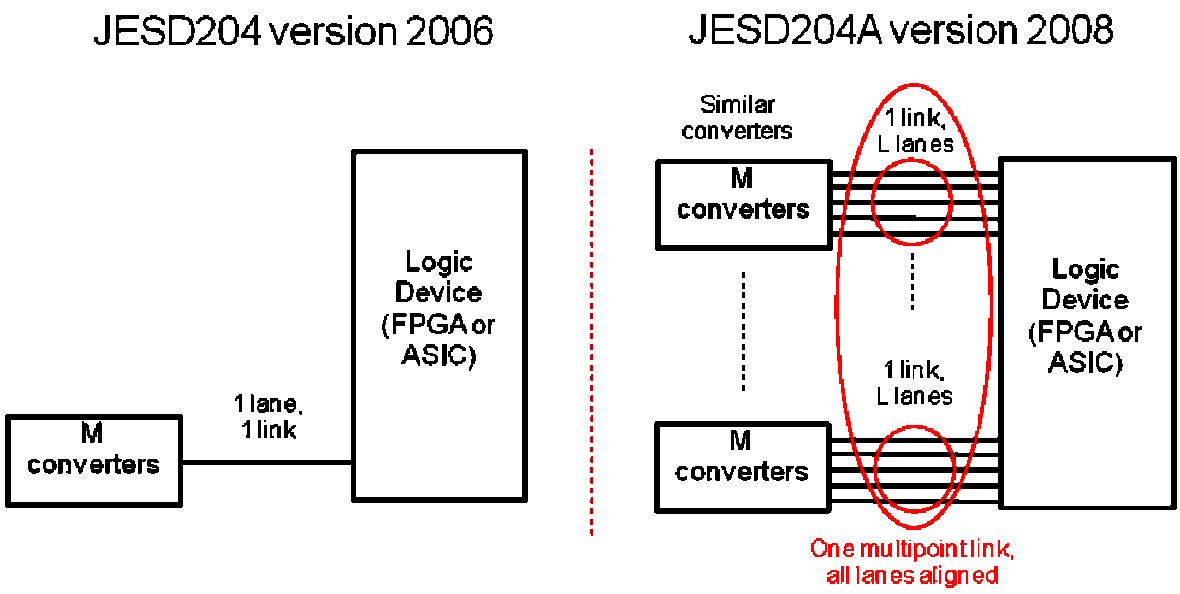

Figure 1 – JESD204 (2006) versus JESD204A (2008)

Again by way of context, time-aligned synchronization of two or more ADC channels or DAC channels is a requirement in many data acquisition systems, particularly in modern communications systems. For example, many wireless communications systems such as GSM/GPRS/EDGE/UMTS cell phone systems rely on quadrature sampling techniques to reduce the minimum Nyquist sampling frequency and thus the bandwidth of the data processed by the downstream digital baseband

processor, with the goal of reducing power, PCB area and BOM cost. In multi-carrier communications systems, such as those based on OFDM (including multi-carrier GSM/EDGE, 3GPP Long Term Evolution [LTE], IEEE 802.11 WiFi, and IEEE 802.16 WiMAX) fundamentally rely on quadrature sampling and on the preservation of precise phase information in the transmitter and receiver. OFDM systems must preserve phase coherency at the sample level for the digital signal processing algorithms to be valid. In the past, communication system engineers had to use awkward and potentially troublesome proprietary synchronization techniques at the board-level to guarantee quadrature sample synchronization. The JEDEC JESD204A specification is intended to address this commonly found technical requirement, and foster interoperability among data converters and logic devices such as FPGAs.

2.0 JEDEC JESD204A – Ease of Use and System Cost Reduction

JESD204A defines a serializer-deserializer (SERDES) based differential serial protocol which is unidirectional and point-to-point, operating with self-clocked 8B/10B coded data at rates from 312.5 Mbps to 3.125 Gbps. **This physical layer definition leads to additional commercial benefits.** First, the self-clocked protocol, referred to as Clock Data Recovery (CDR), means that there is no dedicated high frequency clock signal for the data. This makes EMI/RFI management easier, and the associated regulatory certification process easier (**development cost savings, faster end-product qualification**). The broad data rate definition, which spans a full order of magnitude of bandwidth, also has commercial implications. A single PCB design, using pin-compatible data converters and FPGA with different speed grades, enables design scalability not possible with conventional data converter interfaces (**development cost savings**).

JESD204A transmitter devices (ADCs or FPGAs/ASICs) and receiver devices (DACs or FPGAs/ASICs) on the same FR-4 printed circuit board are guaranteed to operate up to 3.125 Gbps on copper traces at least 20 cm in length with full signal integrity if the physical layer implementation is complaint to the JESD204A specification. **The JESD204A signalling is very robust, leading to yet more commercial advantages.** Compared to conventional parallel data converter interfaces, signal skew management is much more straightforward (**development cost reduction**). The 20 cm signal run (NXP has demonstrated 30 cm signal runs with full eye pattern compliance) means that the data converter and the FPGA/logic device can be flexibly placed on the PCB, enabling more innovative system packaging and form factor compliance (**development cost savings**).

The 8B/10B encoding has the dual merits of utilizing a computed “running disparity” to maintain DC balance (zero DC offset) in the electrical signal (allowing the signal to be high-pass optically, capacitively or inductively coupled) and the ability to detect single-bit errors at the receiver. **More cost savings accrue from this technical nuance.** DC balanced data signal(s) are easy to transmit and process, putting fewer constraints on downstream logic devices or processors (**development and BOM cost savings).**

The electrical signalling defined by JESD204A is low-swing / low-voltage and differential. It complies with what is widely known as CML (Current Mode Logic), used in the DVI and HDMI standards for digital audio and video transmission. JESD204A compliant transmitters and receivers must achieve a Bit Error Rate (BER) of less than 10^{-12}. This very low bit error rate is a statement of system robustness and reliability. It is well known that most electrical subsystem failures are due to interconnect faults (opens or shorts). The low bit error rate of JESD204A combined with the reduced number of interconnect wires enables significantly higher system reliability (**RMA and equipment repair cost reduction**).

Figures 2 and 3 show typical ADC and DAC subsystems based on two of the new NXP JEDEC JESD204A data converters.

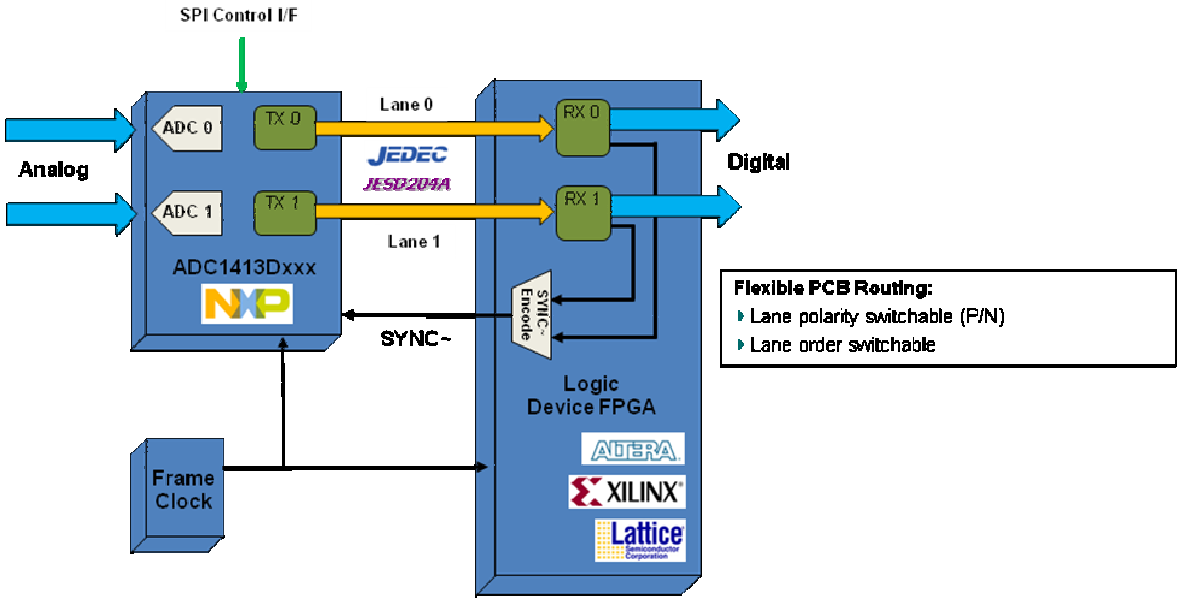

Figure 2 – NXP ADC1413Dxxx: Two ADCs over Two Lanes

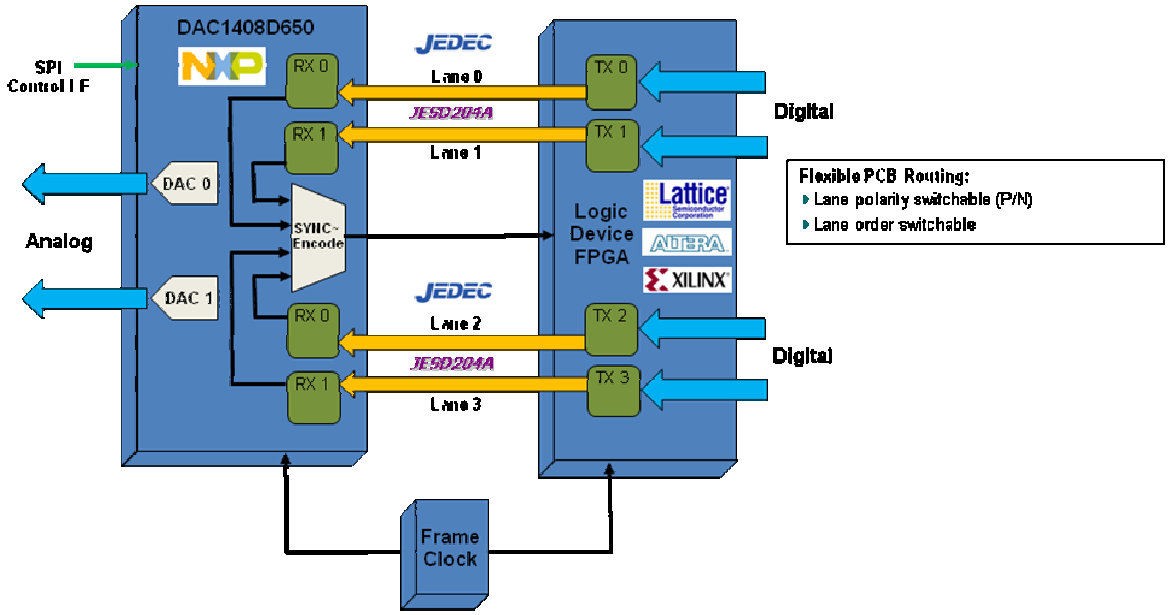

Figure 3 – NXP DAC1408D650: Two DACs over Four Lanes

JESD204A allows for link power-down, for power savings when the application is inactive or in standby / idle mode. Link resynchronization is required when transitioning back to full operating mode. There is no provision for power-down in conventional parallel data converter interconnect

schemes. This is very attractive to OEMs developing systems with many data converters (**energy savings and total cost of ownership savings**).

JESD204A also includes optional data scrambling prior to 8B/10B encoding, to de-correlate repeated data patterns and help to avoid related spurious tones induced in the analog domain. Data scrambling can help avoid unwanted spectral tones/spurs that can otherwise occur with high-speed serial transmission. **Spurious tones in the analog domain can otherwise be time and cost intensive to identify and eliminate (development cost savings).**

The JESD204A specification includes a protocol definition for test modes and test samples. The transmitter transmits test sample sequences, and the receiver verifies the test sample sequence. NXP's compliant data converters include Pseudo Random Bit Sequence (PRBS) generators at several stages in the JESD204A interface blocks. For examples, the transmit block includes three PRBS generators: one prior to frame assembly; one prior to scrambling and 8B/10B encoding; and one prior to the serializer. **The PRBS generators are useful to the system engineer to facilitate testing of the serial interface and verifying the system bit error rate (development cost savings).**

3.0 8B/10B Encoding – A Quick Look

8B/10B encoding schemes date from the 1970s, and was patented by IBM in 1984 (that patent has now expired). It is used broadly in intra-board (chip-to-chip) and inter-board (backplane) serial communication protocols including PCI Express, serial ATA, gigabit Ethernet, XAUI and Serial RapidIO. Use of a well-established coding scheme reduces engineering risk (**development cost savings**). 8B/10B coding allows for the definition of in-band control symbols. Several of these control symbols are reserved for synchronization and alignment protocols, a provision impossible in conventional uncoded data converter interconnect architectures.

Among others, the JESD204A specification defines the essential user data synchronization protocol sequence. At system reset (or subsequently, should user data synchronization be lost), the receivers assert the SYNC signal, causing control symbols to be sent from the transmitters (ADCs or FPGA/ASIC). Once four valid control symbols are received, the receivers de-assert the SYNC signal. The transmitters then send valid 10B user data symbols at the beginning of the next data frame.

In JESD204A, the lane alignment protocol occurs immediately after the user data symbol synchronization protocol described above. In this protocol sequence, a control symbol signals the receiver that lane alignment is underway.

The synchronization/alignment schemes defined by JESD204A are quite clever. For example, in the frame alignment monitoring protocol, 8B/10B user data symbols are themselves used as periodic frame alignment symbols (a technique called character replacement), enabling frame alignment without data loss. Again, there is no comparable feature in conventional data converter interconnects; these synchronization and alignment schemes are totally transparent to the system developer and lend additional system reliability and robustness (**development and repair cost savings**).

4.0 JESD204A Scalability and Performance

It is straight forward to calculate the number of JESD204A links required to support an ADC or DAC, based on the converter resolution and the desired sampling rate.

For a first example, consider a single-channel 12-bit non-oversampled ADC (NXP ADC1213S125) with one over-range bit per sample. After the 8B/10B encoder, each data byte expands to 10 bits. With the link frequency at 3.125 Gbps, simple math shows that the maximum sample frequency is (3.125

Gbps / 20 bits per dual samples) = 156.25 MSPS per link. Thus one link is needed to support the maximum sample rate of 125 MSPS of this high-speed ADC.

For a second example, consider a dual-channel 14-bit non-oversampling DAC (NXP DAC1408D650); note that this DAC includes four JESD204A receivers. With the link frequency at 3.125 Gbps, the maximum sample frequency is (3.125 Gbps / 40 bits per dual samples) = 78.125 MSPS per link. Four links support 312.5 MSPS maximum.

NXP has found that the JEDEC JESD204A interface has little or no impact on analog performance. For example, the NXP ADC1413Dxxx achieves better than 85 dBc of SFDR performance typically, while consuming 1140 mW typically.

JESD204A's assured scalability and analog domain performance means easier and less costly system development.

5.0 Conclusion

The new JEDEC JESD204A data converter interface definition has numerous system-level commercial merits:

- Simplified PCB layout and routing, with the potential for PCB cost reduction (fewer signal layers, smaller PCB form factor)
- Data converter and FPGA or ASIC pin count reduction, with the potential for BOM cost reduction
- EMI/RFI radiation reduction, with the potential for easier device compliance test approval
- Reduced signal skew management, with the potential for reduced engineering development cost
- No PCB redesign for data converter resolution changes (10 to 16-bit), only FPGA logic reconfiguration / recoding, with the potential for reduced engineering development cost and faster end-product qualification.
- Single bit error detection, by virtue of the 8B/10B coding scheme, with the potential for increased system reliability
- Four or more time-aligned and phase coherent data converter channels for system designs such as LTE MIMO basestations, with the potential for simplified system design and reduced engineering development cost
- Guaranteed interoperability with Altera, Lattice and Xilinx FPGAs, with each vendor offering compliant IP for their latest cost-effective programmable logic products
- Periodic frame alignment monitoring with the potential to maintain frame alignment without data loss for system reliability and robustness
- Optional data and control symbol scrambling to produce data independence across the JESD204A link, with the potential to reduce non-harmonic spurs in the data converter analog domain

NXP Semiconductors is proud to offer the industry the first data converters featuring the JESD204A high-speed serial interface. NXP plans to offer several compliant ADCs and DACs in 2009, as follows:

- ADC1213Sxxx single channel, JEDEC interface, 12-bit ADC, 80/105/125 MSPS
- ADC1413Sxxx single channel, JEDEC interface, 14-bit ADC, 80/105/125 MSPS
- ADC1213Dxxx dual channel, JEDEC interface, 12-bit ADC, 65/80/105/125 MSPS
- ADC1413Dxxx dual channel, JEDEC interface, 14-bit ADC, 65/80/105/125 MSPS
- DAC1408D650 dual channel, JEDEC interface, 14-bit DAC, 650 MSPS

For more information on these products, please visit http://www.nxp.com/#/homepage/cb=[t=p,p=/50935/53500]|pp=[t=pfp,i=53500], and contact your local NXP sales office to request literature, data converter samples, demo boards and application engineering assistance.