S32N55 Vehicle Super-Integration Processor
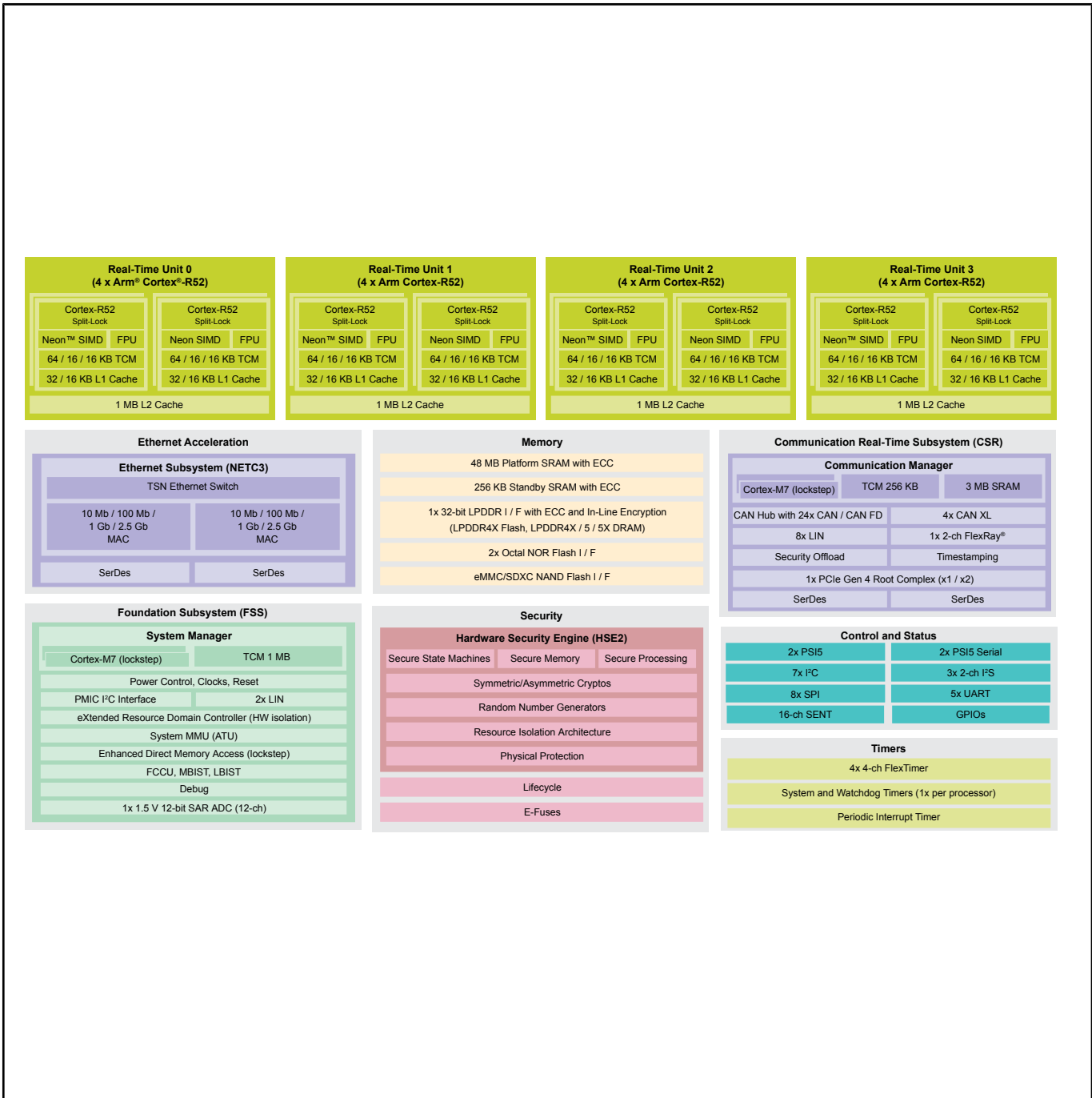
S32N55

Preproduction

This page contains information on a preproduction product. Specifications and information herein are subject to change without notice. For additional information contact support or your sales representative.

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The S32N55 real-time super-integration processor accelerates the development of central vehicle controller applications in software-defined vehicle (SDV) architectures. It safely consolidates real-time vehicle control, management and services into a single system-on-chip solution.

The S32N55 processor combines high-performance real-time processing, a firewalled hardware security engine, an integrated multiport TSN Ethernet switch, extensive automotive communication interfaces and hardware isolation and virtualization for safe and secure integration of real-time vehicle functions.

S32N55 Product Features Block Diagram

Real-Time Unit 0
(4 x Arm® Cortex®-R52)

Cortex-R52 Split-Lock	Cortex-R52 Split-Lock
Neon™ SIMD / FPU	Neon SIMD / FPU
64 / 16 / 16 KB TCM	64 / 16 / 16 KB TCM
32 / 16 KB L1 Cache	32 / 16 KB L1 Cache

1 MB L2 Cache

Real-Time Unit 1
(4 x Arm Cortex-R52)

Cortex-R52 Split-Lock	Cortex-R52 Split-Lock
Neon™ SIMD / FPU	Neon SIMD / FPU
64 / 16 / 16 KB TCM	64 / 16 / 16 KB TCM
32 / 16 KB L1 Cache	32 / 16 KB L1 Cache

1 MB L2 Cache

Real-Time Unit 2
(4 x Arm Cortex-R52)

Cortex-R52 Split-Lock	Cortex-R52 Split-Lock
Neon™ SIMD / FPU	Neon SIMD / FPU
64 / 16 / 16 KB TCM	64 / 16 / 16 KB TCM
32 / 16 KB L1 Cache	32 / 16 KB L1 Cache

1 MB L2 Cache

Real-Time Unit 3
(4 x Arm Cortex-R52)

Cortex-R52 Split-Lock	Cortex-R52 Split-Lock
Neon™ SIMD / FPU	Neon SIMD / FPU
64 / 16 / 16 KB TCM	64 / 16 / 16 KB TCM
32 / 16 KB L1 Cache	32 / 16 KB L1 Cache

1 MB L2 Cache

Ethernet Acceleration

Ethernet Subsystem (NETC3)

TSN Ethernet Switch

10 Mb / 100 Mb / 1 Gb / 2.5 Gb MAC	10 Mb / 100 Mb / 1 Gb / 2.5 Gb MAC
SerDes	SerDes

Memory

- 48 MB Platform SRAM with ECC
- 256 KB Standby SRAM with ECC
- 1x 32-bit LPDDR I / F with ECC and In-Line Encryption (LPDDR4X Flash, LPDDR4X / 5 / 5X DRAM)
- 2x Octal NOR Flash I / F
- eMMC/SDXC NAND Flash I / F

Communication Real-Time Subsystem (CSR)

Communication Manager

Cortex-M7 (lockstep)	TCM 256 KB	3 MB SRAM
CAN Hub with 24x CAN / CAN FD		4x CAN XL
8x LIN		1x 2-ch FlexRay®
Security Offload		Timestamping
1x PCIe Gen 4 Root Complex (x1 / x2)		
SerDes		SerDes

Foundation Subsystem (FSS)

System Manager

Cortex-M7 (lockstep)	TCM 1 MB

- Power Control, Clocks, Reset
- PMIC I²C Interface / 2x LIN
- eXtended Resource Domain Controller (HW isolation)
- System MMU (ATU)
- Enhanced Direct Memory Access (lockstep)
- FCCU, MBIST, LBIST
- Debug
- 1x 1.5 V 12-bit SAR ADC (12-ch)

Security

Hardware Security Engine (HSE2)

Secure State Machines	Secure Memory	Secure Processing

- Symmetric/Asymmetric Cryptos
- Random Number Generators
- Resource Isolation Architecture
- Physical Protection
- Lifecycle
- E-Fuses

Control and Status

2x PSI5	2x PSI5 Serial
7x I²C	3x 2-ch I²S
8x SPI	5x UART
16-ch SENT	GPIOs

Timers

- 4x 4-ch FlexTimer
- System and Watchdog Timers (1x per processor)
- Periodic Interrupt Timer

View additional information for S32N55 Vehicle Super-Integration Processor.

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